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2.5MHz, Synchronous Boost Regulator with Bypass Mode

General Description

The RT4805B allows systems to take advantage of new battery chemistries that can supply significant energy when the battery voltage is lower than the required voltage for system power ICs. By combining built-in power transistors, synchronous rectification, and low supply current; this IC provides a compact solution for systems using advanced Li-Ion battery chemistries.

The RT4805B is a boost regulator designed to provide a minimum output voltage from a single-cell Li-Ion battery, even when the battery voltage is below system minimum. In boost mode, output voltage regulation is guaranteed to a maximum load current of 2A. Quiescent current in Shutdown Mode is less than 1μA, which maximizes battery life. The regulator transitions smoothly between Bypass and normal Boost Mode. The device can be forced into Bypass Mode to reduce quiescent current.

The RT4805B is available in the WL-CSP-16B 1.67x1.67 (BSC) package.

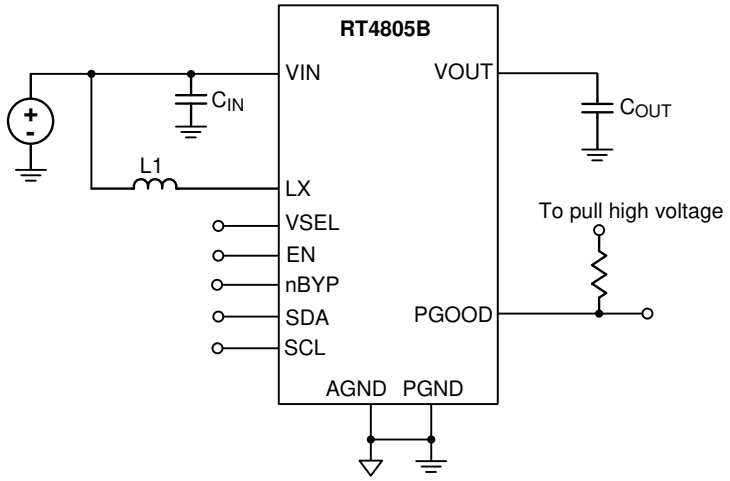
Features

- **4 Few External Components : 0.47μH Inductor and 0603 Case Size Input and Output Capacitors**
- **Input Voltage Range : 1.8V to 5V**
- **Output Range from 2.85V to 4.4V**
  - **VSEL = L 3.15V**
  - **VSEL = H 3.6V**
- **Maximum Continuous Load Current : 2A at V_{IN} > 2.65V Boosting V_{OUT} to 3.35V**
- **Up to 96% Efficient**
- **True Bypass Operation when V_{IN} > Target V_{OUT}**
- **Internal Synchronous Rectifier**
- **True Load Disconnect when Shut Down**
- **Forced Bypass Mode**
- **V_{SEL} Control to Optimize Target V_{OUT}**
- **Short-Circuit Protection**
- **I^2C Controlled Interface**
- **Ultra Low Operating Quiescent Current**
- **Small WL-CSP 16B Package**

Applications

- Single-Cell Li-Ion, LiFePO4 Smart-Phones or Tablet
- 2.5G/3G/4G Mini-Module Data Cards

Simplified Application Circuit



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Ordering Information

RT4805B □
└Package Type
WSC : WL-CSP-16B 1.67x1.67 (BSC)

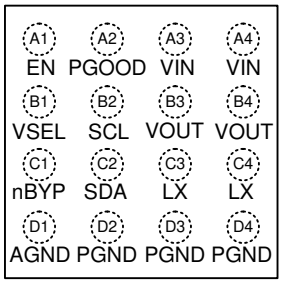
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

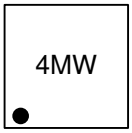
Pin Configuration

(TOP VIEW)



WL-CSP-16B 1.67x1.67 (BSC)

Marking Information



4M : Product Code
W : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	EN	Enable. When this pin is HIGH, the circuit is enabled.
A2	PGOOD	Power good. It is a open-drain output. PGOOD pin pulls low automatically if the overload or OTP event occurs.
A3, A4	VIN	Input voltage. Connect to Li-Ion battery input power source.
B1	VSEL	Output voltage select. When boost is running, this pin can be used to select output voltage
B2	SCL	Serial interface clock. (Pull down if I^2C is non-used).
B3, B4	VOUT	Output voltage. Place C_{OUT} as close as possible to the device.
C1	nBYP	Bypass. This pin can be used to activate forced bypass mode. When this pin is LOW, the bypass switches are turned on and the IC is otherwise inactive.
C2	SDA	Serial interface date line. (Pull down if I^2C is non-used).
C3, C4	LX	Switching node. Connect to inductor.
D1	AGND	Analog ground. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin.
D2, D3, D4	PGND	Power ground. This is the power return for the IC. The C_{OUT} bypass capacitor should be returned with the shortest path possible to these pins.

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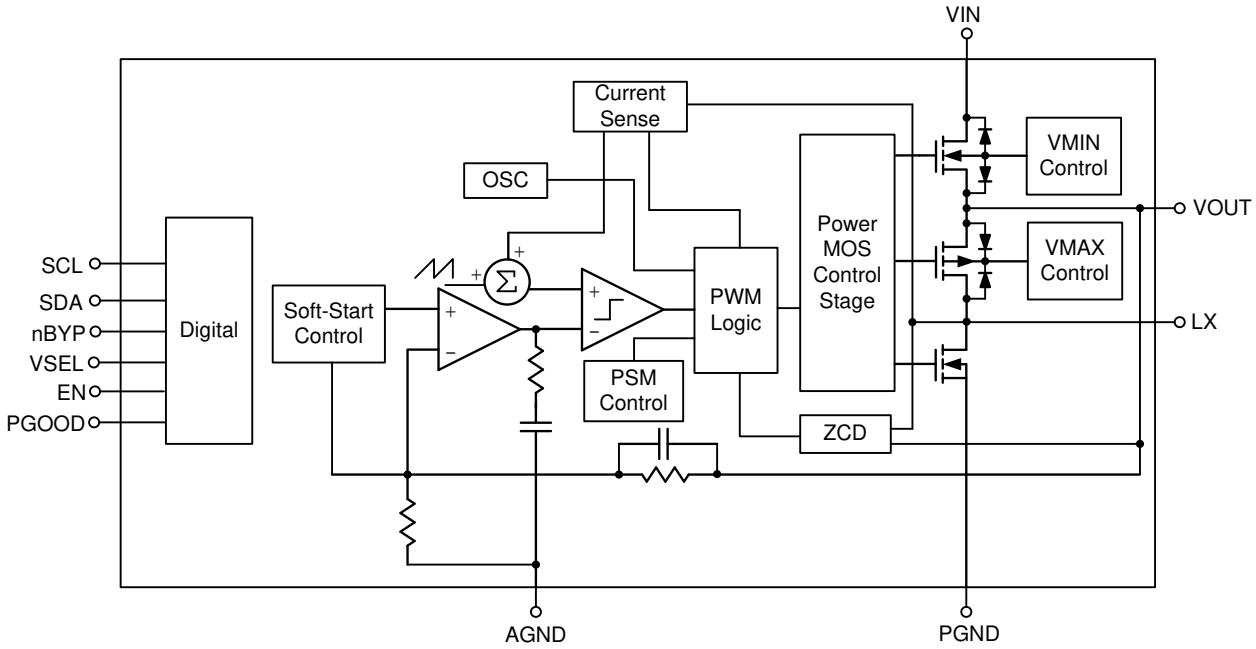
Functional Block Diagram



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Operation

The RT4805B combined built-in power transistors, synchronous rectification, and low supply current, it provides a compact solution for system using advanced Li-Ion battery chemistries.

In boost mode, output voltage regulation is guaranteed to a maximum load current of 2A. Quiescent current in Shutdown mode is less than 1μA, which maximizes battery life.

Mode		Depiction	Condition
LIN	LIN 1	Linear startup 1	$V_{IN} > V_{OUT}$
	LIN 2	Linear startup 2	$V_{IN} > V_{OUT}$
Soft-Start		Boost soft-start	$V_{OUT} < V_{OUT(MIN)}$
Boost		Boost mode	$V_{OUT} = V_{OUT(MIN)}$
Bypass		Bypass mode	$V_{IN} > V_{OUT(MIN)}$

LIN State

When V_{IN} is rising, it enters the LIN State. There are two parts for the LIN state. It provides maximum current for 1A to charge the C_{OUT} in LIN1, and the other one is for 2A in LIN2. By the way, the EN is pulled high and V_{IN} > UVLO.

As the figure shown, if the timeout is over the specification, it will enter the Fault mode.

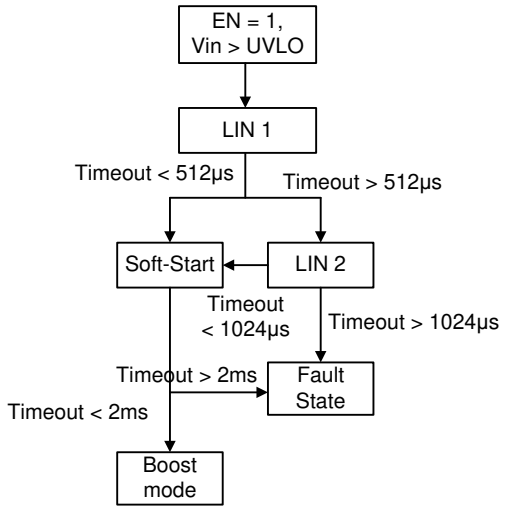

Figure 1. The RT4805B State Chart

Startup and Shutdown State

When V_{IN} is rising and through the LIN state, it will enter the Startup state. If EN is pulled low, any function is turned-off in shutdown mode.

Soft-Start State

It starts to switch in Soft-start state. After the LIN state, output voltage is rising with the internal reference voltage.

There is a point, it will go to fault condition, if the large output capacitor is used and the timeout is over 2ms after the soft-start state.

Fault State

As the Figure 1 shown, it will enter to the Fault state as below,

- The timeout of LIN2 is over the 1024μs.
- It is over the 2ms when the state changed from Soft-start state to Boost mode.

It will be the high impedance between the input and output when the fault is triggered. A restart will be start after 1ms.

Boost Mode

There are two normal operation modes, one is the Boost mode, and the other one is Bypass mode. In the Boost mode, it provides the power to load by internal synchronous switches after the soft-start state.

Bypass Mode

In Bypass mode, output voltage will increase with VIN when input voltage is rising after the soft-start state.

Bypass Mode Operation

In automatic mode, it transits from Boost mode to Bypass mode. As the Figure 2 shown, there are three MOSFET (Q1 to Q3). The Q1 & Q2 is for Boost mode, it is used by Q3 for Bypass mode. V_{OUT} will be followed the V_{IN} when V_{IN} is higher than the target output voltage. As the Figure 3 shown, it is transited by bypass MOSFET (Q3). V_{OUT} followed the V_{IN}.

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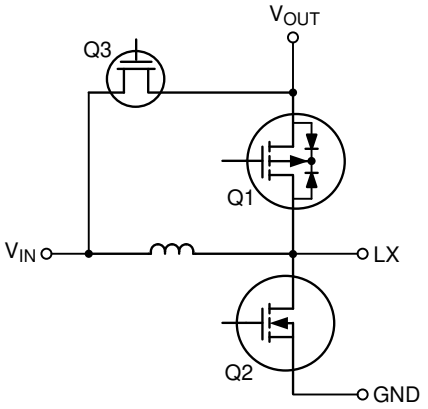

Figure 2. Boost Converter With Bypass Mode

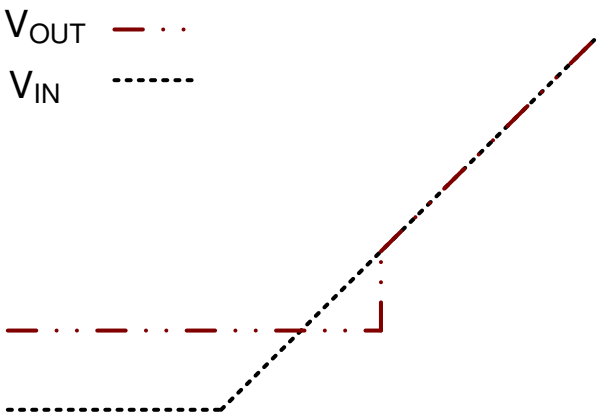

Figure 3. The RT4805B Mode Changed

Force Pass-Through Mode

When EN pulled high and nBYP pulled low. The device is active in the Force pass-through mode. It supplies current is approximately 15μA typ. From the battery, the device is short circuit protected by a current limit of 4000mA.

VSEL

It is concerned the minimum output voltage at the heavy load condition. There are two output voltage levels (3.15V & 3.6V) in Boost mode and Bypass mode. It can be selected by VSET, so it must not be floating.

PGOOD (Power Good)

Power good is a open-drain output. If it is 0, it stands for fault occurred. The power good provide the information to show the state of the system,

- PGOOD pin show high when the sequence of soft-start is completed.
- Any fault cause PGOOD to be pulled low.
- PGOOD low when PMOS current limit has triggered for OR the die the temperature exceeds 120°C. PGOOD is re-asserted when the device cools below to 100°C.

OCP

The converter senses the current signal when the high-side P-MOSFET turns on. As a result, the OCP is cycle by-cycle current limitation. If the OCP occurs, the converter holds off the next on pulse until inductor current drops below the OCP limit.

OTP

The converter has an over-temperature protection. When the junction temperature is higher than the thermal shutdown rising threshold, the system will be latched and the output voltage will no longer be regulated until the junction temperature drops under the falling threshold.

EN & nBYP

It is used to select mode. As the table 1 shown, there are four device states.

If the EN pull low, and nBYP pull high/low, the RT4805B is forced in shut-down mode and the quiescent is less than 1μA. It works in force pass-through mode, if the EN set high and nBYP set low. When EN and nBYP both pull high, the RT4805B is normal operation and enter automatic mode. There should be a delay time (> 60μS) from EN pull high to nBYP pull high to guarantee normal automatic mode operation.

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Table 1

EN input	nBYP input	Device State
0	0/1	The device is in shut down mode, and features a shutdown current down to ca. 1μA typ.
1	0	The device is active in forced pass-through mode. The device supply current is approximately 15μA typ. from the battery. The device is short circuit protected by a current limit of ca. 4000mA.
1	1	The device is active in auto mode (dc-dc boost, pass-through mode) The device supply current is approximately 55μA typ. from the battery

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Absolute Maximum Ratings (Note 1)

- VIN, VOUT to AGND ---------- –0.2V to 6V
- EN, VSEL, PGOOD, nBYP to AGND ---------- –0.2V to 6V
- LX ---------- (PGND – 0.2V) to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-16B 1.67x1.67 (BSC) ---------- 2.09W
- Package Thermal Resistance (Note 2)
  WL-CSP-16B 1.67x1.67 (BSC), θ_{JA} ---------- 47.7°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  CDM (Charge Device Model) ---------- 1kV

Recommended Operating Conditions (Note 4)

- Input Voltage Range ---------- 1.8V to 5V
- Output Voltage Range ---------- 2.85V to 4.4V
- Ambient Temperature Range ---------- –40°C to 85°C
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{IN} = 3V, V_{OUT} = 3.4V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
VIN Operation Range	V_{IN}		1.8	--	5	V
VIN Quiescent Current	I_Q	Auto bypass mode, V_{IN} = 3.8V	--	35	70	μA
VIN Quiescent Current	I_Q	Boost mode, I_{LOAD} = 0mA, switching, V_{IN} = 3V	--	55	100	μA
VIN Quiescent Current	I_Q	Force bypass without LIQ, V_{IN} = 3.6V	--	15	25	μA
VIN Shutdown Current	I_{SHDN}	EN = 0V, V_{IN} = 3.6V	--	--	1	μA
VOUT to VIN Reverse Leakage	I_{LK}	V_{OUT} = 5V, EN = nBYP = H, V_{IN} < V_{OUT}	--	0.2	1	μA
VOUT Leakage Current	I_{LK_OUT}	V_{OUT} = 0V, EN = 0V, V_{IN} = 4.2V	--	0.1	1	μA
Under-Voltage Lock Out	V_{UVLO}	V_{IN} rising	--	1.6	1.8	V
Under-Voltage Lock Out Hysteresis	V_{UVLO_HYS}		--	200	--	mV
PGOOD Low	V_{PGOOD}	I_{PGOOD} = 5mA	--	--	0.4	V
PGOOD Leakage Current	I_{PGOOD_LK}	V_{PGOOD} = 5V	--	--	1	μA
Logic Level High EN, VSEL, nBYP, SCL, SDA	V_{IH}		1.2	--	--	V

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Logic Level Low EN, VSEL, nBYP, SCL, SDA	V_{IL}		--	--	0.4	V
Output Voltage Accuracy	V_{REG}	$V_{OUT} - V_{IN} > 100mV$, PWM	–2	--	2	%
Minimum On Time	t_{ON}	V_{IN} = 3V, V_{OUT} = 3.5V, I_{LOAD} > 1000mA	--	80	--	ns
Maximum Duty Cycle	D_{MAX}		40	--	--	%
Switching Frequency	f_{SW}	V_{IN} = 2.65V, V_{OUT} = 3.5V, I_{LOAD} = 1000mA	2	2.5	3	MHz
Boost Valley Current Limit	I_{CL}	V_{IN} = 2.9V	3.5	4	4.5	A
Soft-Start Input Current Limit	I_{SS_PK}	LIN1	--	1000	--	mA
Soft-Start Input Current Limit	I_{SS_PK}	LIN2	--	2000	--	mA
Pass Through Mode Current Limit	I_{BPCL}	V_{IN} = 3.2V	--	4	--	A
N-Channel Boost Switch $R_{DS(ON)}$	R_{DSN}	V_{IN} = 3.2V, V_{OUT} = 3.5V	--	60	95	mΩ
P-Channel Boost Switch $R_{DS(ON)}$	R_{DSP}	V_{IN} = 3.2V, V_{OUT} = 3.5V	--	40	80	mΩ
N-Channel Bypass Switch $R_{DS(ON)}$	R_{DSP_BYP}	V_{IN} = 3.2V, V_{OUT} = 3.5V	--	40	60	mΩ
Hot Die Trigger Threshold	T_{HD}		--	100	--	°C
Hot Die Release Threshold	T_{HDR}		--	90	--	°C
Over-Temperature Protection	T_{OTP}		--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C
FAULT Restart Time	t_{RST}		--	1	--	ms

Note 1. Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard.

Note 3. Devices are ESD sensitive. Handling precaution recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

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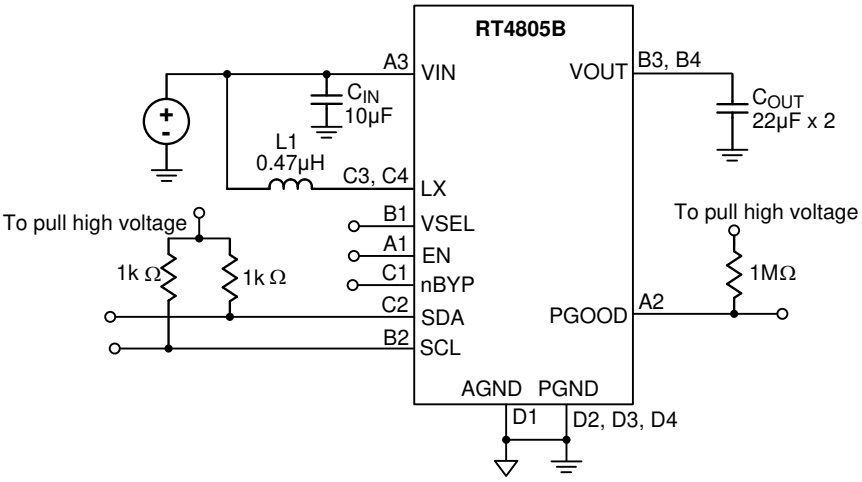
Typical Application Circuit



BOM of Test Board

Reference	Description	Manufacturer	Package	Parameter	Typ	Unit
C_{IN}	10µF/16V/X5R	Taiyo : EMK212ABJ106KG	0805	C	10	µF
C_{OUT}	22µF/10V/X5R	Taiyo : LMK212BBJ226MG	0805	C	22	µF
L1	0.47µH, ±20%	TOKO : DFE2520F-R47M	2520	L	0.47	µH
				DCR (Series R)	29	mΩ

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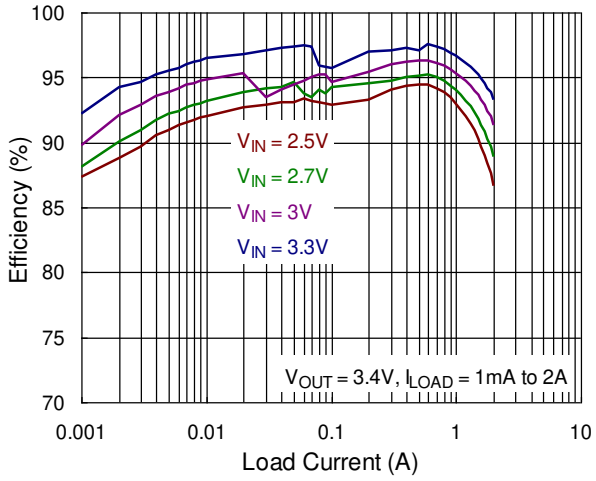
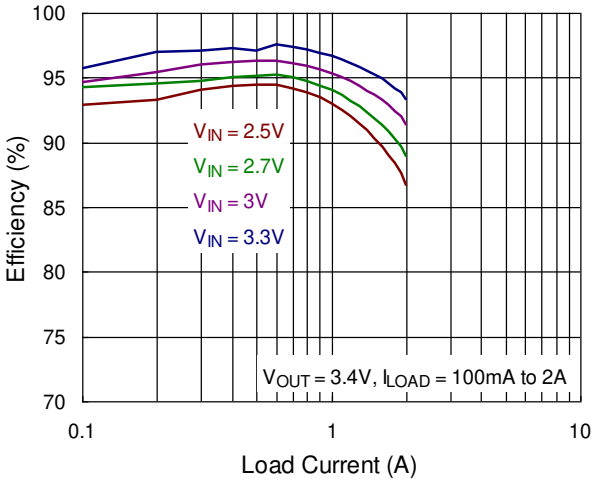
Typical Operating Characteristics

Efficiency vs. Load Current



Efficiency vs. Load Current



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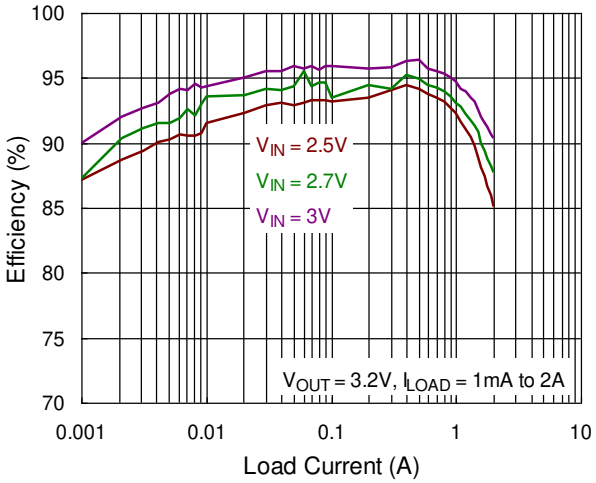
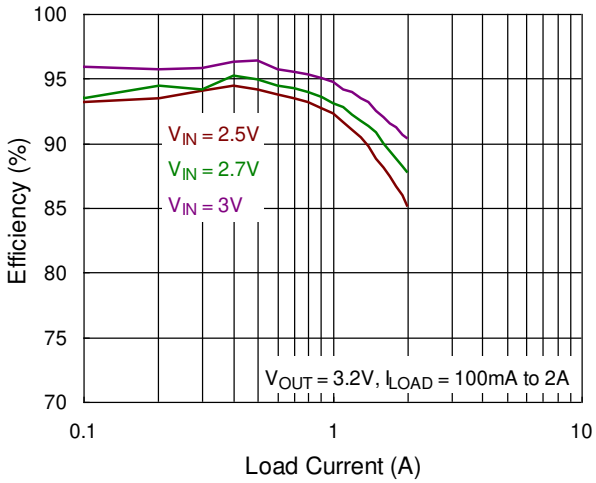
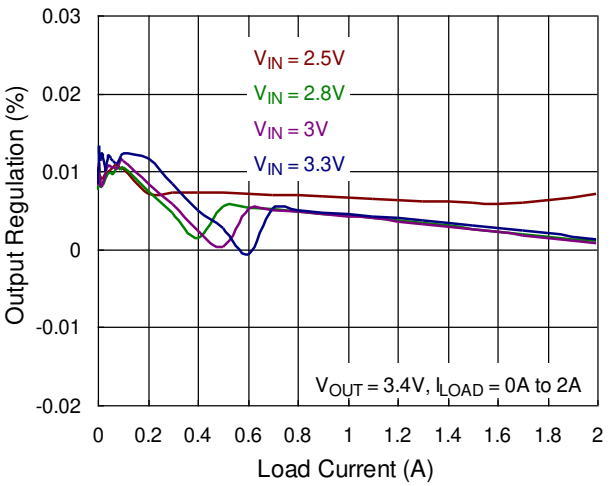


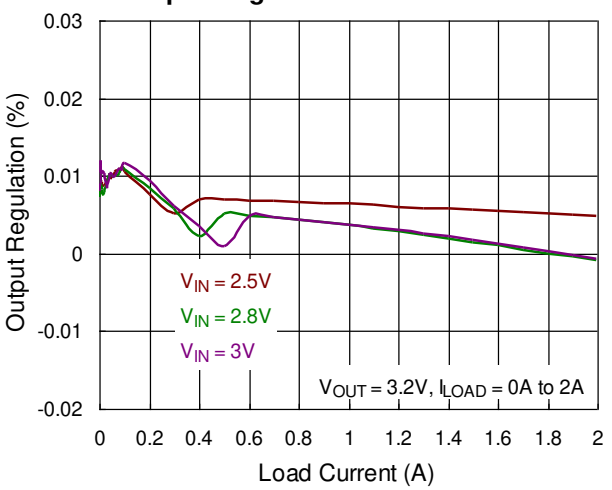
Efficiency vs. Load Current



Output Regulation vs. Load Current



Output Regulation vs. Load Current



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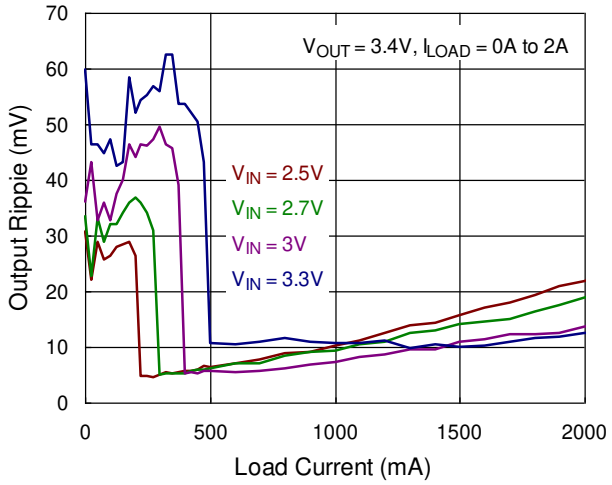
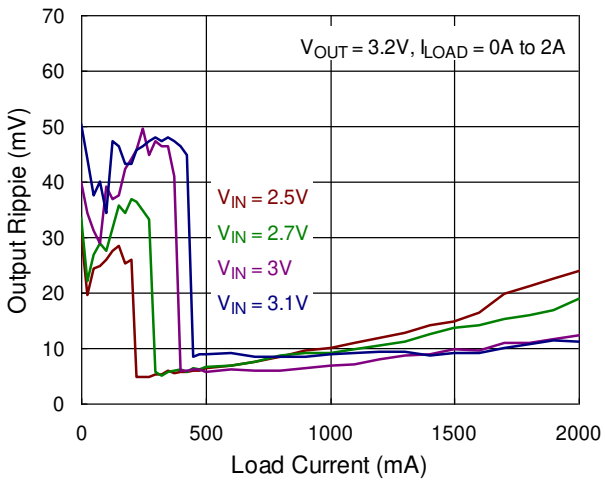
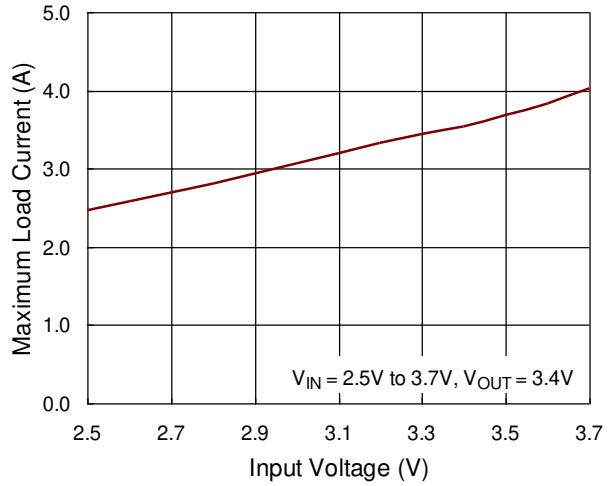
Output Ripple vs. Load Current



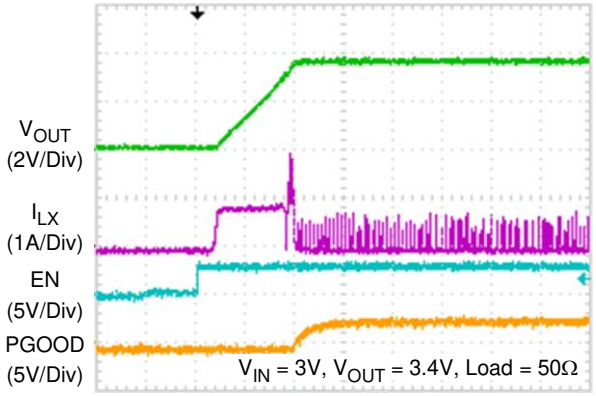
Output Ripple vs. Load Current



Maximum Load Current vs. Input Voltage

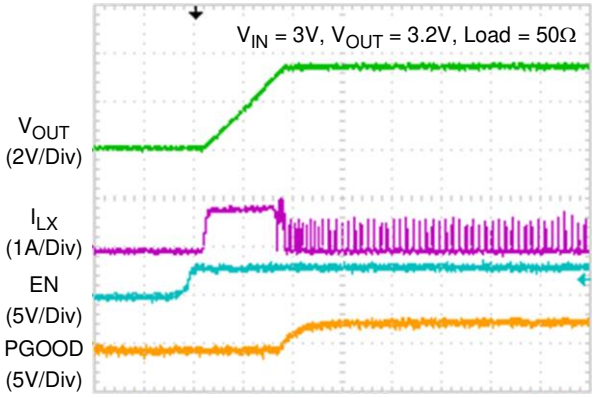


Startup



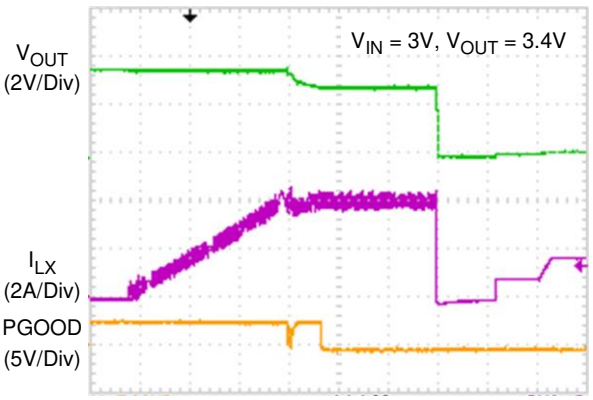
Time (100μs/Div)

Startup



Time (100μs/Div)

Overload Protection



Time (1ms/Div)

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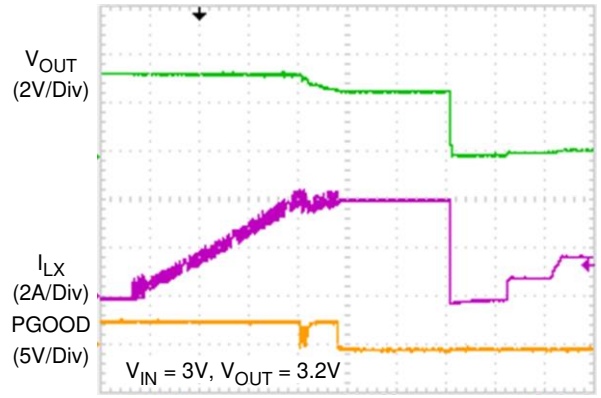
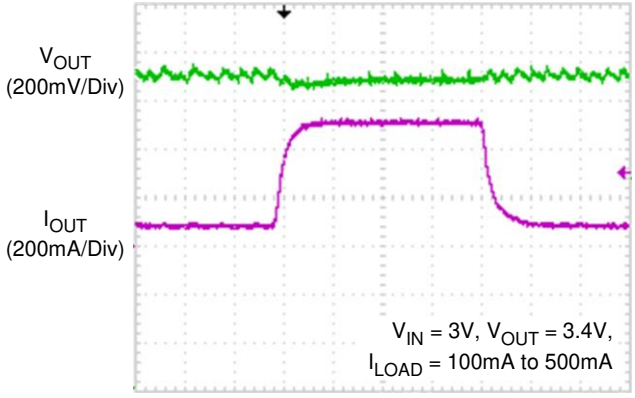
Overload Protection



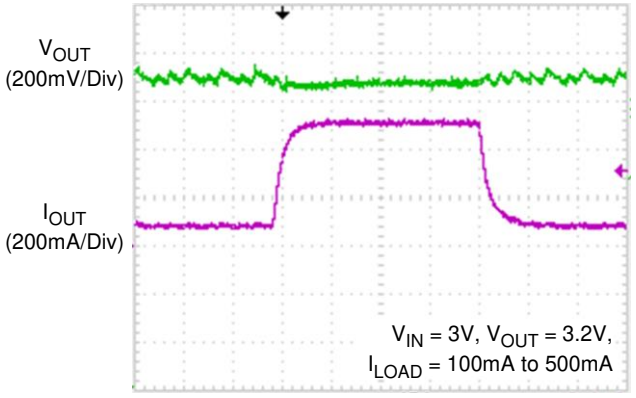
Time (1ms/Div)

Load Transient



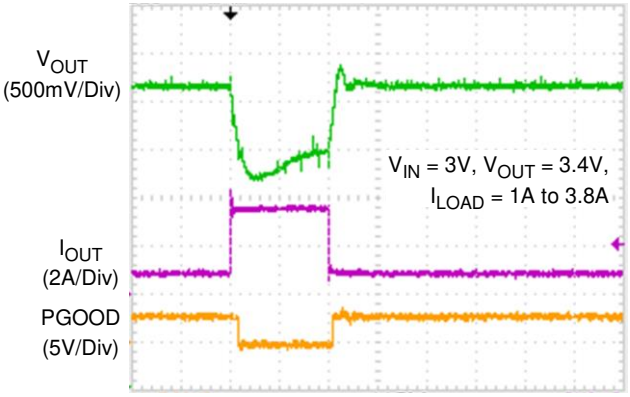
Time (25µs/Div)

Load Transient



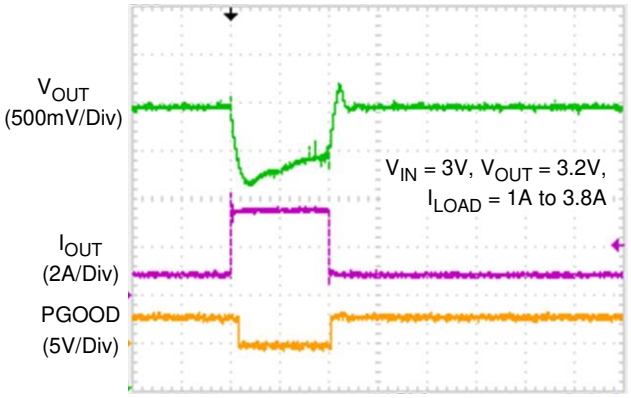
Time (25µs/Div)

Transient Overload



Time (50µs/Div)

Transient Overload



Time (50µs/Div)

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Application Information

Enable

The device can be enabled or disabled by the EN pin. When the EN pin is higher than the threshold of logic-high, the device starts operating with soft-start. Once the EN pin is set at low, the device will be shut down. In shutdown mode, the converter stops switching, internal control circuitry is turned off, and the load is disconnected from the input. This also means that the output voltage can drop below the input voltage during shutdown.

Soft-Start State

After the successful completion of the LIN state (V_{OUT} ≥ V_{IN} – 300mV).

During Soft-Start state, V_{OUT} is ramped up by Boost internal loop. If V_{OUT} fails to reach target value during the Soft-Start period for more than 2ms, a fault condition is declared.

Output Voltage Setting

User can select the output voltage level by VSEL and I2C. If the VSEL pulled low, the default is 3.15V, and if it pulled high, the default is 3.6V.

The output voltage range is from 2.85V to 4.4V.

Power Save Mode

PSM is the way to improve efficiency at light load.

When the output voltage is lower than a set threshold voltage, the converter will operate in PSM.

It raises the output voltage with several pulses until the loop exits PSM.

Under-Voltage Lockout

The under-voltage lockout circuit prevents the device from operating incorrectly at low input voltages. It prevents the converter from turning on the power switches under undefined conditions and prevents the battery from deep discharge. VIN voltage must be greater than 1.7V to enable the converter. During operation, if VIN voltage drops below 1.6V, the converter is disabled until the supply exceeds the UVLO rising threshold. The RT4805B automatically restarts if the input voltage recovers to the input voltage UVLO high level.

Thermal Shutdown

The device has a built-in temperature sensor which monitors the internal junction temperature. If the temperature exceeds the threshold, the device stops operating. As soon as the IC temperature has decreased below the threshold with a hysteresis, it starts operating again. The built-in hysteresis is designed to avoid unstable operation at IC temperatures near the over-temperature threshold.

Inductor Selection

The recommended nominal inductance value is 1.5μH.

It is recommended to use inductor with dc saturation current ≥ 3500mA

Input Capacitor Selection

At least a 10μF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit for LX. And at least a 1μF ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

Output Capacitor Selection

At least 22μF x 2 capacitors is recommended to improve V_{OUT} ripple.

Output voltage ripple is inversely proportional to C_{OUT}.

Output capacitor is selected according to output ripple which is calculated as :

$$V_{RIPPLE(P-P)} = t_{ON} \times \frac{I_{LOAD}}{C_{OUT}}$$

and

$$t_{ON} = t_{SW} \times D = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

therefore :

$$C_{OUT} = t_{SW} \times \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \frac{I_{LOAD}}{V_{RIPPLE(P-P)}}$$

and

$$t_{SW} = \frac{1}{f_{SW}}$$

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The maximum V_{RIPPLE} occurs when V_{IN} is at minimum and I_{LOAD} is at maximum.

Output Discharge Function

With the EN pin set to low, the VOUT pin is internally connected to GND by an internal discharge N-MOSFET switch.

This feature prevents residual charge voltages on capacitor connected to VOUT pins, which may impact proper power up of the system.

Current Limit

The RT4805B employs a valley-current limit detection scheme to sense inductor current during the off-time. When the loading current is increased such that the loading is above the valley current limit threshold, the off-time is increased until the current is decreased to valley-current threshold. Next on-time begins after current is decreased to valley-current threshold. On-time is decided by (V_{OUT} – V_{IN}) / V_{OUT} ratio. The output voltage decreases when further loading current increase. As the following figure shown, the current limit function is implemented by the scheme.

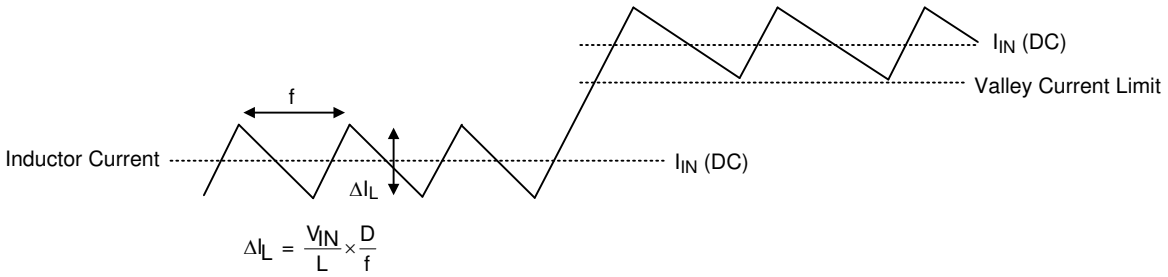

Figure 4. Inductor Currents In Current Limit Operation

Protection

The RT4805B features some protections, such as OCP, OVP, UVP and OTP. As the table shown, it is described the protection actions.

Protection Type	Threshold Refer to Electrical Spec.	Protection Method	Shut Down Delay Time	Reset Method
OCP	IL > 4A	Turn on UG until IL < 4A	2ms	After FAULT 1ms
OVP	VIN > 6V	Turn off UG, LG, BYP_MOS	No delay	VIN < 5.7V
UVP	VIN <1.6V	Turn off UG, LG, BYP_MOS	No delay	VIN>1.7V
OTP	TEMP > 160°C	Turn off UG, LG, BYP_MOS	No delay	OTP Hysteresis = 20°C

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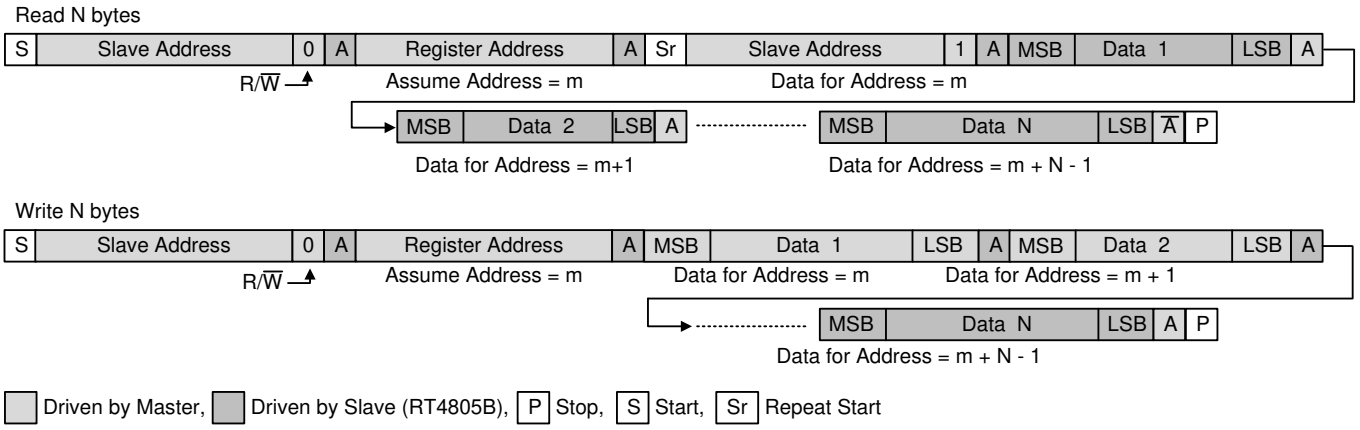
Register Table Lists [Slave address = 1110101 (0x75)]

Name	Address	Description
CONFIG	0x01	MODE control & Spread modulation control
VOUTFLOOR	0x02	Output voltage selection
VOUTROOF	0x03	Output voltage selection
ILIMSET	0x04	Set current limit & Soft-start current limit
STATUS	0x05	Read IC status

I²C Interface

The RT4805B I²C slave address is 1110101 (7bits). The I²C interface supports fast mode (bit rate up to 400kb/s). The write or read bit stream (N ≥ 1) is shown below :



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Offset 0x01		CONFIG						
Bits	7	6	5	4	3	2	1	0
Name	RESET	ENABLE<1>	ENABLE<0>	RESERVED	PG Config.	SSFM	MODE_CTRL<1>	MODE_CTRL<0>
Reset	0	0	0	0	1	0	0	1
Type	RW	RW	RW	RW	RW	RW	RW	RW
Offset 0x02		**VOUTFLOOR**						
Bits	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	RESERVED	VSEL<4>	VSEL<3>	VSEL<2>	VSEL<1>	VSEL<0>
Reset	0	0	0	0	0	1	1	0
Type	RW	RW	RW	RW	RW	RW	RW	RW
Offset 0x03		**VOUTROOF**						
Bits	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	RESERVED	VSEL<4>	VSEL<3>	VSEL<2>	VSEL<1>	VSEL<0>
Reset	0	0	0	0	1	1	1	1
Type	RW	RW	RW	RW	RW	RW	RW	RW
Offset 0x04		**ILIMSET**						
Bits	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	ILIM_OFF	SOFT_START	ILIM<3>	ILIM<2>	ILIM<1>	ILIM<0>
Reset	0	0	0	1	1	1	0	1
Type	RW	RW	RW	RW	RW	RW	RW	RW
Offset 0x05		**STATUS**						
Bits	7	6	5	4	3	2	1	0
Name	TSD	HOTDIE	DCDCMODE	OPMODE	ILIMPT	ILIMBST	FAULT	PGOOD
Reset	0	0	0	0	0	0	0	0
Type	RO	RO	RO	RO	RO	RO	RO	RO

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Name		Function	Addr	
CONFIG		MODE control & Spread modulation control	0x01	
Bit	Mode	Name	Reset	Description
7	R/W	RESET	0	0 : Disable ID detection function 1 : Enable ID detection function
[6 : 5]	R/W	ENABLE[1 : 0]	0	00 : Device operation follows hardware control signal (refer to table 1) 01 : Device operation in auto transition mode (boost/bypass) regardless of the nBYP control signal (EN = 1) 10 : Device is forced in pass-through mode regardless of the nBYP control signal (EN = 1) 11 : Device is in shutdown mode. The output voltage is reduced to a minimum value (V_{IN} – V_{OUT} ≤ 3.6V) regardless of the nBYP control signal (EN = 1)
4	R/W	Reserved	0	
3	R/W	PG Config.	1	0 : PG pin = H, it is not allowed. PG pin = L, it is shut down. 1 : PG pin is for power good indication.
2	R/W	SSFM	0	0 : Spread spectrum modulation is disabled. 1 : Spread spectrum modulation is enabled in PWM mode.
[1 : 0]	R/W	MODE_CTRL[1 : 0]	01	00 : Not allowed. 01 : PFM with automatic transition into PWM operation. 10 : Forced PWM operation. 11 : PFM with automatic transition into PWM operation (VSEL = L), forced PWM operation (VSEL = H).
Name		**Function**	**Addr**	
VOUTFLOOR		Output Voltage Selection	0x02	
Bit	Mode	Name	Reset	Description
[7 : 5]	R/W	Reserved	000	
[4 : 0]	R/W	VOUT[4 : 0]	00110	00000 : V_{OUT} = 2.85V 00001 : V_{OUT} = 2.9V 00010 : V_{OUT} = 2.95V 00011 : V_{OUT} = 3V 00100 : V_{OUT} = 3.05V … 00110 : V_{OUT} = 3.15V (default) … 11111 : V_{OUT} = 4.4V

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Name		Function	Addr	
VOUTROOF		Output Voltage Selection	0x03	
Bit	Mode	Name	Reset	Description
[7 : 5]	R/W	Reserved	000	
[4 : 0]	R/W	VOUT[4 : 0]	01111	00000 : V_{OUT} = 2.85V 00001 : V_{OUT} = 2.9V 00010 : V_{OUT} = 2.95V 00011 : V_{OUT} = 3V 00100 : V_{OUT} = 3.05V … 01111 : V_{OUT} = 3.6V (default) … 11111 : V_{OUT} = 4.4V
Name		**Function**	**Addr**	
ILIMSET		Set current limit & Softstart current limit	0x04	
Bit	Mode	Name	Reset	Description
[7 : 6]	R/W	Reserved	00	
5	R/W	ILIM_OFF	0	0 : Current limit enabled 1 : Current limit disabled
4	R/W	Soft-Start	1	0 : Boost soft-start current is limited per ILIM bit settings 1 : Boost soft-start current is limited to ca. 1250mA inductor valley current
[3 : 0]	R/W	ILIM[3 : 0]	1101	1000 : 1500mA 1001 : 2000mA 1010 : 2500mA 1011 : 3000mA 1100 : 3500mA 1101 : 4000mA (default) 1110 : 4500mA 1111 : 5000mA

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Name		Function	Addr	
STATUS		Read IC status	0x05	
Bit	Mode	Name	Reset	Description
7	R	TSD	0	0 : Normal operation. 1 : Thermal shutdown tripped. The flag is reset after readout.
6	R	HOTDIE	0	0 : T_J < 115°C. 1 : T_J > 115°C.
5	R	DCDCMODE	0	0 : Device operates in PFM mode. 1 : Device operates in PWM mode.
4	R	OPMODE	0	0 : Device operates in pass-through mode. 1 : Device operates in dc-dc mode.
3	R	ILIMPT	0	0 : Normal operation. 1 : Indicates that the bypass FET current limit has triggered. This flag is reset after readout.
2	R	ILIMBST	0	0 : Normal operation. 1 : Indicates that the average input current limit has triggered for 1.5ms in dc-dc boost mode. This flag is reset after readout.
1	R	FAULT	0	0 : Normal operation. 1 : Indicates that a fault condition has occurred. This flag is reset after readout.
0	R	PGOOD	0	0 : Indicates the output voltage is out of regulation. 1 : Indicates the output voltage is within its nominal range. This bit is set if the converter is forced in pass-through mode.

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Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WL-CSP-16B 1.67x1.67 (BSC) package, the thermal resistance, θ_{JA}, is 47.7°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C − 25°C) / (47.7°C/W) = 2.09W for a WL-CSP-16B 1.67x1.67 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 32 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

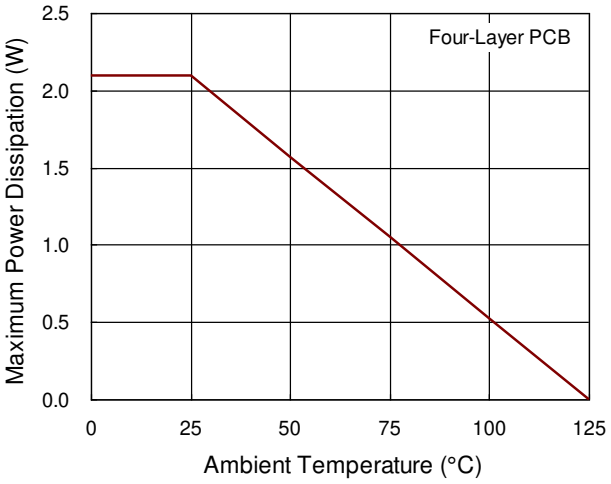

Figure 5. Derating Curve of Maximum Power Dissipation

Layout Consideration

The PCB layout is an important step to maintain the high performance of the RT4805B.

Both the high current and the fast switching nodes demand full attention to the PCB layout to save the robustness of the RT4805B through the PCB layout. Improper layout might show the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RT4805B, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- For thermal consider, it needed to maximize the pure area for the power stage area besides the LX.

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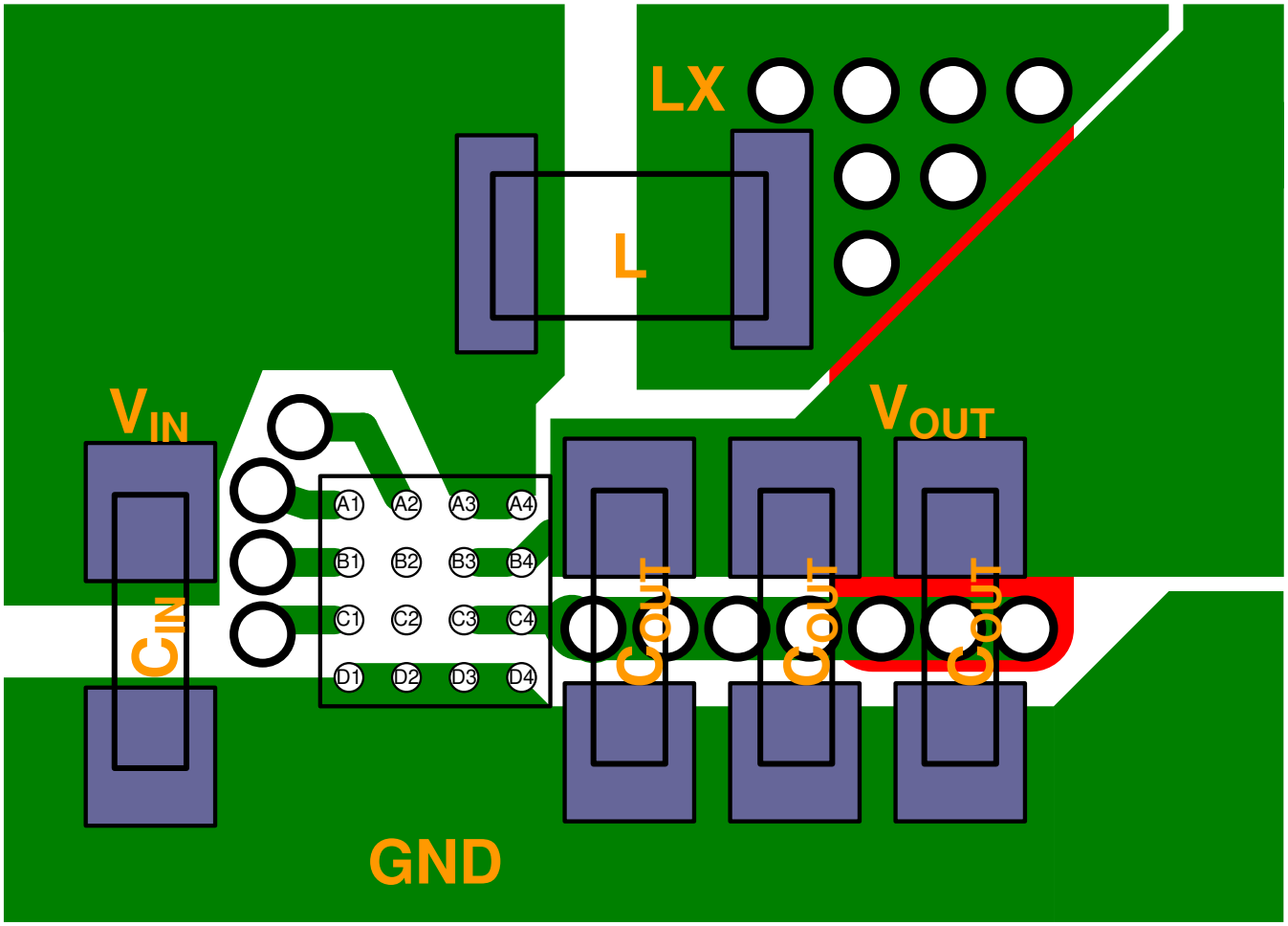

Figure 6. PCB Layout Guide

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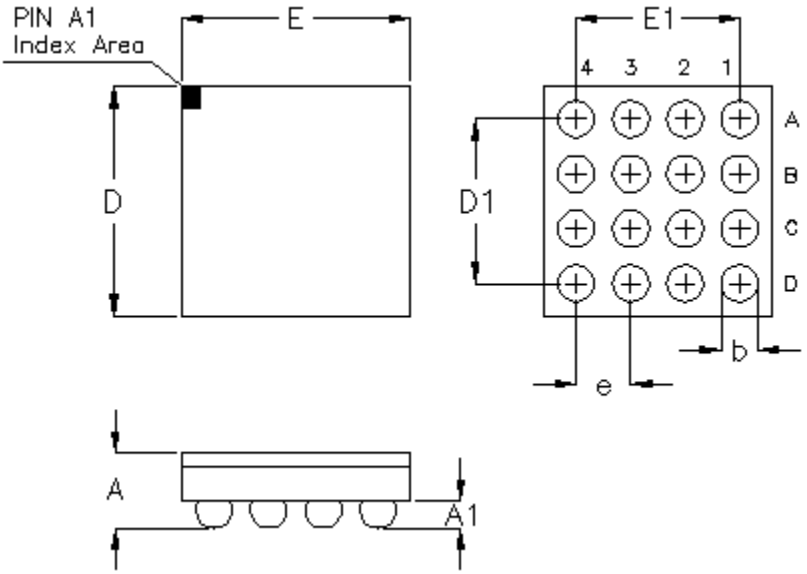
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.620	1.720	0.064	0.068
D1	1.200		0.047	
E	1.620	1.720	0.064	0.068
E1	1.200		0.047	
e	0.400		0.016	

WL-CSP-16B 1.67x1.67 (BSC)

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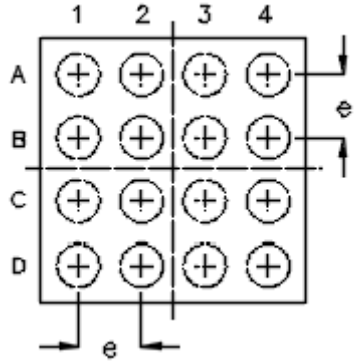
Footprint Information



Package	Number of Pin	Type	Footprint Dimension (mm)			Tolerance
			e	A	B	
WL-CSP1.67*1.67-16(BSC)	16	NSMD	0.400	0.240	0.340	±0.025
		SMD		0.270	0.240	

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