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Integrated PMIC with 4-Channel Synchronous Buck Converters, 8 LDOs, and MTP Non-Volatile Memory for Industrial and Automotive Applications

General Description

The RT5028A is a highly-integrated low-power high-performance analog SOC with PMIC in one single chip designed for Industrial/Automotive applications.

The RT5028A includes four synchronous step-down DC-DC converters and eight LDOs for system power.

The RT5028A also embeds one EEPROM (MTP) for setting sequence and timing etc.

Additionally, the RT5028A PMIC also includes one IRQ report.

Ordering Information

RT5028A □□

- Package Type
  QW : WQFN-56L 7x7 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

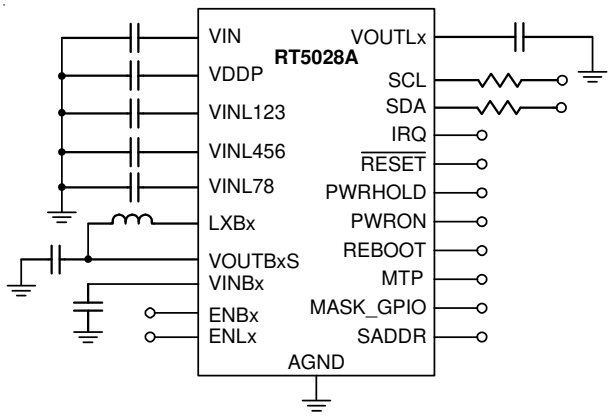
Features

- **Input Voltage Operating Range is 3.3V to 5.5V**
- **Step-Down Regulator : V_{IN} Range is 3.3V to 5.5V**
  - **Max Current 2.4A/2A/1.6A/2A**
  - **Programmable Frequency from 500kHz to 2MHz**
  - **I²C Programmable Output Level**
  - **I²C Programmable Operation Mode (Force PWM or Auto PSM/PWM)**
  - **I²C Programmable Output Discharge Mode (Discharge or Flatting)**
- **Linear Regulators : V_{IN} Range is 2.5V to 5.5V**
  - **Max Current 0.3A**
  - **I²C Programmable Output Level**
- **Embedded 32Bytes MTP for Factory Tuning**
  - **External MTP Pin for Write Protection**
- **Sequence can be Controlled by I²C or each EN pins Defined by MASK_GPIO Pin**
- **OT/UVP/VIN LV/POWRON Press Time Interrupt (IRQ)**
  - **I²C Control Interface : Support Fast Mode up to 400kb/s**
- **Available in AEC-Q100 Grade 3 Qualified**
- **RoHS Compliant and Halogen Free**

Applications

- Industrial/Automotive

Simplified Application Circuit



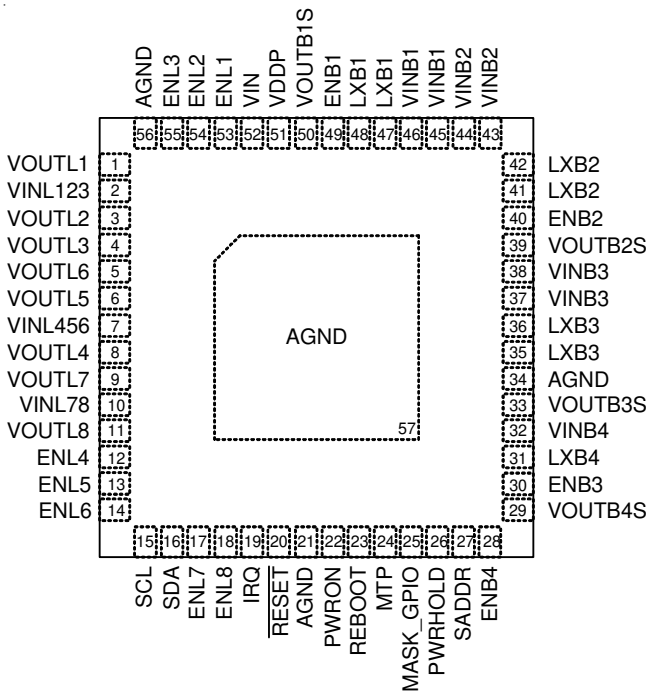
Marking Information

RT5028AGQW : Product Number

YMDNN : Date Code

Pin Configuration

(TOP VIEW)



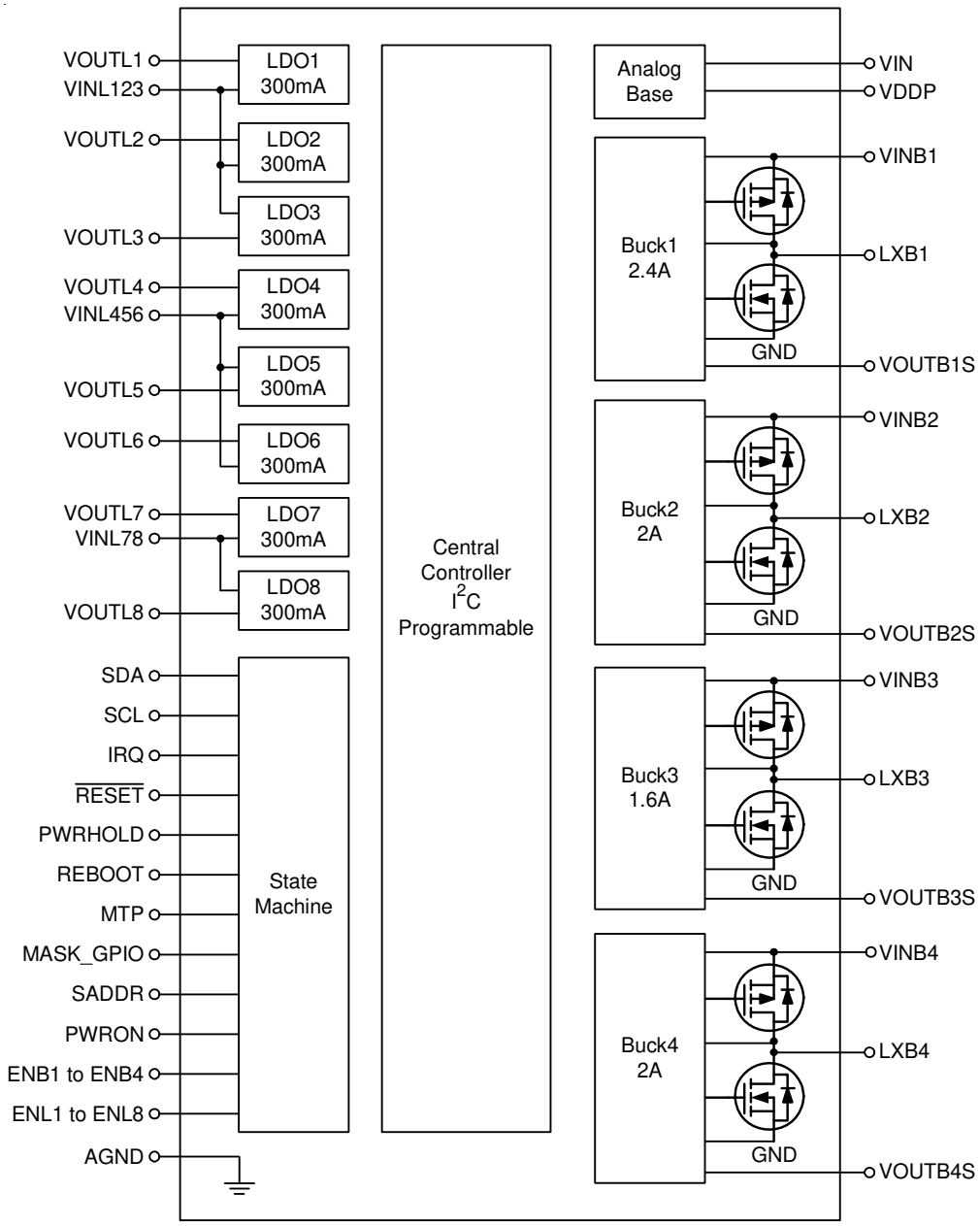
WQFN-56L 7x7

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VOUTL1	Output voltage regulation node for LDO1.
2	VINL123	Input power for LDO1, LDO2 and LDO3.
3	VOUTL2	Output voltage regulation node for LDO2.
4	VOUTL3	Output voltage regulation node for LDO3.
5	VOUTL6	Output voltage regulation node for LDO6.
6	VOUTL5	Output voltage regulation node for LDO5.
7	VINL456	Input power for LDO4, LDO5 and LDO6.
8	VOUTL4	Output voltage regulation node for LDO4.
9	VOUTL7	Output voltage regulation node for LDO7.
10	VINL78	Input power for LDO7 and LDO8.
11	VOUTL8	Output voltage regulation node for LDO8.
12	ENL4	Enable control input for LDO4.
13	ENL5	Enable control input for LDO5.
14	ENL6	Enable control input for LDO6.
15	SCL	Clock input for I^2C. Open-drain output.

Pin No.	Pin Name	Pin Function
16	SDA	Data input for I^2C. Open-drain output.
17	ENL7	Enable control input for LDO7.
18	ENL8	Enable control input for LDO8.
19	IRQ	Open-drain IRQ output node.
20	$\overline{\text{RESET}}$	Reset output.
21, 34, 56, 57 (Exposed Pad)	AGND	Analog ground. The exposed pad must be soldered to a large PCB and connected to AGND for maximum power dissipation.
22	PWRON	Manual power on.
23	REBOOT	System power reboot.
24	MTP	MTP write protection pin. Logic low is inhibited and logic high is permit to write.
25	MASK_GPIO	Select I^2C or EN pin for Bucks and LDOs. Connect a 100kΩ pull-low resistor. As MASK_GPIO is high, ignore all EN pins. As MASK_GPIO is low, EN pins and I^2C both can control. EN pins priority is higher than I^2C.
26	PWRHOLD	Power hold input.
27	SADDR	I^2C slave address.
28	ENB4	Enable control input for Buck4.
29	VOUTB4S	Output voltage regulation node for Buck4.
30	ENB3	Enable control input for Buck3.
31	LXB4	Internal switch node to output inductor connection for Buck4.
32	VINB4	Input power for Buck4.
33	VOUTB3S	Output Voltage regulation node for Buck3.
35, 36	LXB3	Internal switch node to output inductor connection for Buck3.
37, 38	VINB3	Input power for Buck3.
39	VOUTB2S	Output voltage regulation node for Buck2.
40	ENB2	Enable control input for Buck2.
41, 42	LXB2	Internal switch node to output inductor connection for Buck2.
43, 44	VINB2	Input power for Buck2.
45, 46	VINB1	Input power for Buck1.
47, 48	LXB1	Internal switch node to output inductor connection for Buck1.
49	ENB1	Enable control input for Buck1.
50	VOUTB1S	Output voltage regulation node for Buck1
51	VDDP	Internal bias regulator voltage. External load on this pin is not allowed.
52	VIN	Input power for analog base.
53	ENL1	Enable control input for LDO1.
54	ENL2	Enable control input for LDO2.
55	ENL3	Enable control input for LDO3.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Analog Base Input Voltage, VIN ---------- –0.3V to 6V
- PMIC Input Voltage, VINL123/456/78, VINB1/2/3/4 ---------- –0.3V to 6V
- PMIC Output Voltage, VOUTLx, VOUTBxS, LXBx ---------- –0.3V to 6V
- PMIC related Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-56L 7x7 ---------- 3.7W
- Package Thermal Resistance (Note 2)
  WQFN-56L 7x7, θ_{JA} ---------- 27°C/W
  WQFN-56L 7x7, θ_{JC} ---------- 7°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(**Note 5**)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
AMR for VIN			--	--	6	V
Operation Voltage of VIN		As f_{SW} > 1MHz, 3.3V ≤ V_{IN} ≤ 5.5V. If f_{SW} ≤ 1MHz, V_{IN} ≥ 4V.	3.3	--	5.5	V
PMIC						
Quiescent Current	I_{IN}	V_{IN} = 5V, LDOs, Bucks are ON with no load. Bucks operate in auto mode (Reg0x06 = FFh)	500	700	950	μA
		V_{IN} = 5V, SCL = SDA = 0V, LDO and Bucks are OFF, Disable PMIC (Reg0x15[7] = 1)	5	30	60	
Warning for Die Temperature	OTW	Temperature 1	--	100	--	°C
		Temperature 2	--	125	--	
Over-Temperature Protection	OTP		--	165	--	°C
OTP and Warning Hysteresis			--	10	--	°C
Input Pull-Low 100kΩ Resistor	R_{Low}	V_{IN} = 5V, temperature = –40°C to 85°C	70	115	160	kΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Buck1 to Buck4						
Input Voltage	V_{INB}		3.3	--	5.5	V
Consumption Current	I_{VINB}	AUTO mode I_{OUT} = 0mA, each buck	10	30	50	μA
Output Voltage Accuracy	V_{OUTAcc}	3.1V < V_{IN} < 5.5V, 1mA < I_{OUT} < I_{MAX}, −40 < T_A < 85°C	−3	--	3	%
Switching Frequency	f_{SW}	I^2C programmable	0.43	--	2	MHz
Switching Frequency Accuracy		1MHz < f_{SW}	−10	--	10	%
		f_{SW} ≤ 1MHz	−20	--	20	
Peak Current Limit	OCP	Buck1	3.1	4.4	5.8	A
		Buck2	2.8	4	5.2	
		Buck3	2.6	3.7	4.8	
		Buck4	2.8	4.1	5.3	
Under-Voltage Protection	UVP	VOUTB1S to VOUTB4S < 0.66 x (V_{OUT} Target)	56	66	76	%
Maximum Output Current	I_{MAX}	Buck1	2.4	--	--	A
		Buck2	2	--	--	
		Buck3	1.6	--	--	
		Buck4	2.0	--	--	
High-Side On-Resistance	R_{pon}	V_{IN} = 3.7V	50	150	250	mΩ
Low-Side On-Resistance	R_{non}	V_{IN} = 3.7V	40	110	160	mΩ
LDO1 to LDO8						
Input Voltage for VINL123/456/78	V_{INL}		2.5	--	5.5	V
Output Voltage LDO123/78	V_{OUTL}	3.1V ≤ V_{IN} ≤ 5.5V, 50μA ≤ I_{OUT} ≤ I_{MAX} −40 < T_A < 85°C	−3	--	3	%
Output Voltage LDO456	V_{OUTL}	3.1V ≤ V_{IN} ≤ 5.5V, 50μA ≤ I_{OUT} ≤ I_{MAX} −40 < T_A < 85°C	−3	--	3	%
Output Current	I_{OUT}		300	--	--	mA
Output Short Current	Isht		330	450	600	mA
Voltage Difference	V_{IN} − V_{OUT}	V_{IN} > 3.1V; V_{IN} = V_{SET}, I_{OUT} = I_{OUTMAX}	0.05	0.1	0.3	V
		V_{IN} > 2.5V; V_{IN} = V_{SET}, I_{OUT} = I_{OUTMAX}	0.05	0.11	0.5	
Supply Current	I_{SS}	I_{OUT} = 0mA	10	50	75	μA
Shutdown Current	I_{OFF}		0	1	2	μA

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Control Input Pin Electrical Characteristics							
Voltage Output Low		V_{OL}		--	--	0.4	V
Input Voltage	High-Level	V_{IH}		1.5	--	--	V
	Low-Level	V_{IL}		--	--	0.4	
$\overline{\text{RESET}}$ Pin Electrical Characteristics							
Output Low Voltage $\overline{\text{RESET}}$			Isink = 1mA, V_{IN} = 3.3V to 5.5V	--	--	0.2	V
Output High Leakage $\overline{\text{RESET}}$			T_A = 25°C, V_{IN} = 3.3V to 5.5V	−1	0	1	μA
			T_A = 85°C, V_{IN} = 3.3V to 5.5V	--	0.1	--	

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

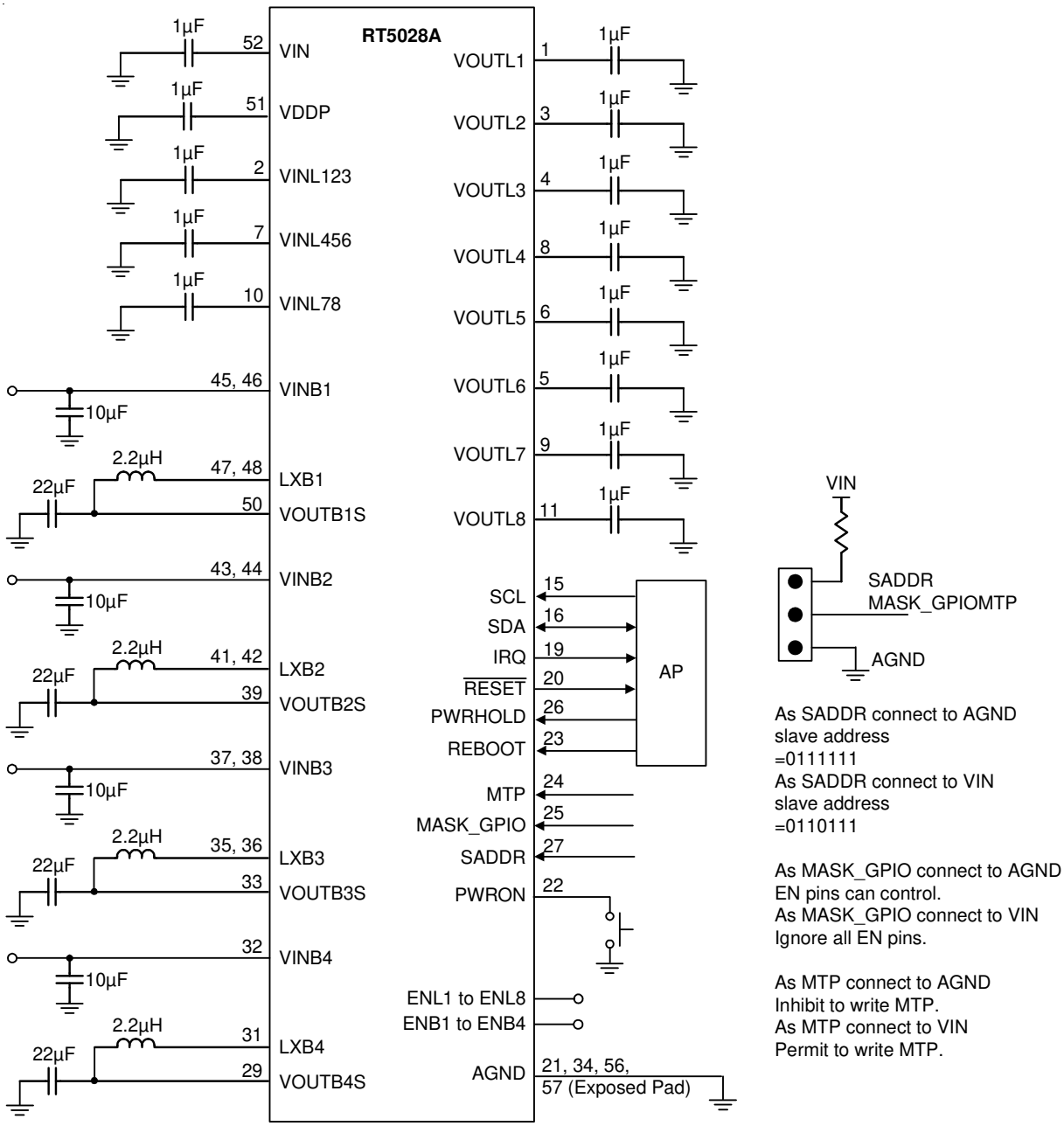
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. Limits apply to the recommended operating temperature range of −40°C to 85°C, unless otherwise noted. Minimum and maximum limits are verified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_A = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply : V_{IN} = 3.3V to 5.5V.

Typical Application Circuit

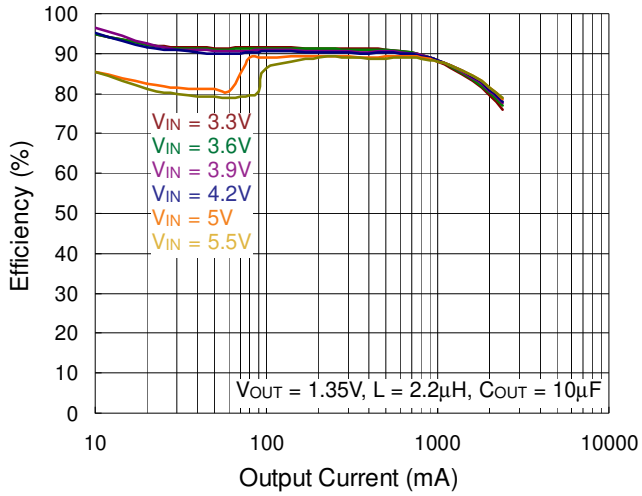


Suggested Components for Typical Application Circuit

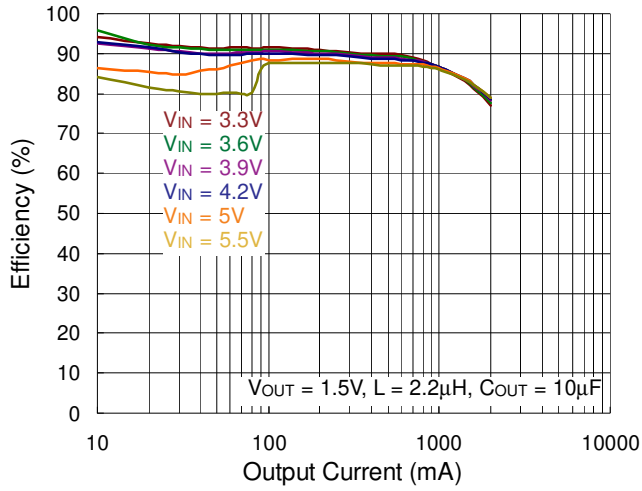
Description	P/N	Manufacturer
Inductor for Buck-2.2µH	LQH43PB2R2M26L	Murata
C_{IN} for Buck-10µF	C1206X7R1E516DT	Murata
C_{OUT} for Buck-22µF	C1206X7R22E416DT	Murata
C_{IN}/C_{OUT} for LDO-1µF	C0603X7R1E216DT	Murata

Typical Operating Characteristics

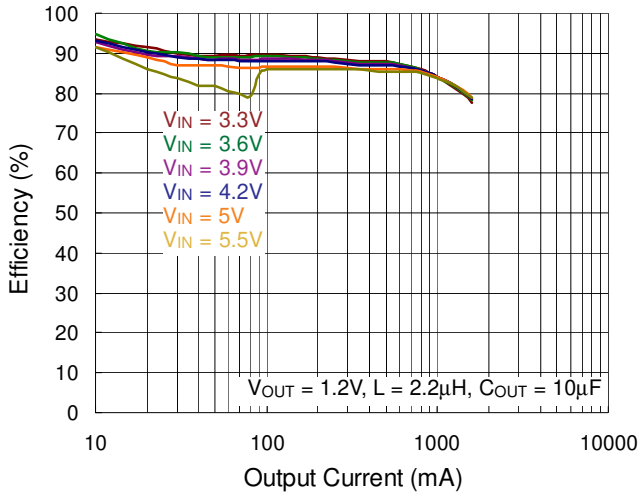
CH1 Buck Efficiency vs. Output Current



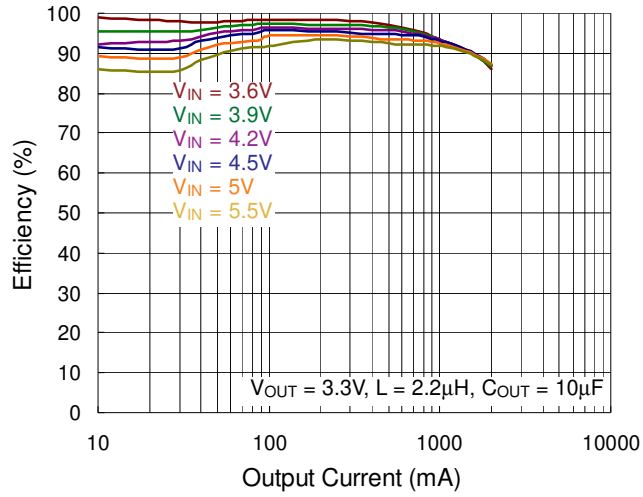
CH2 Buck Efficiency vs. Output Current



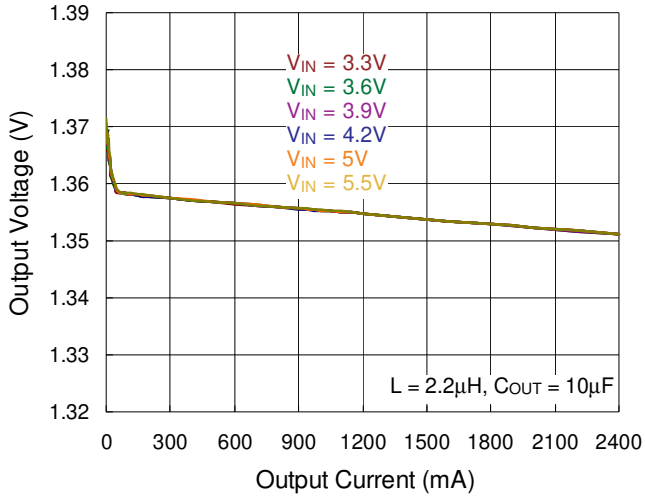
CH3 Buck Efficiency vs. Output Current



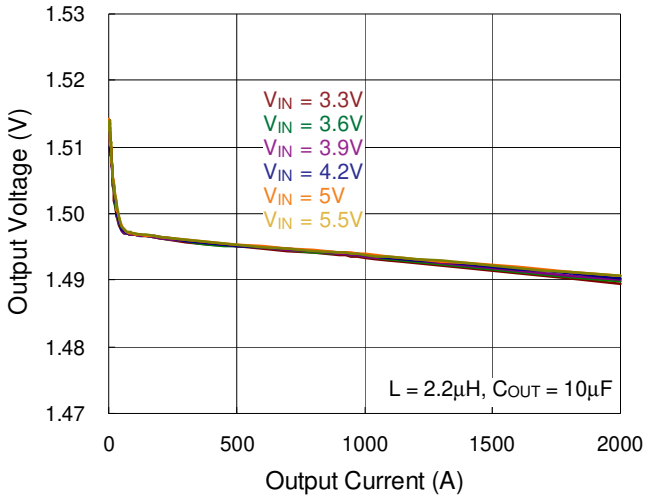
CH4 Buck Efficiency vs. Output Current



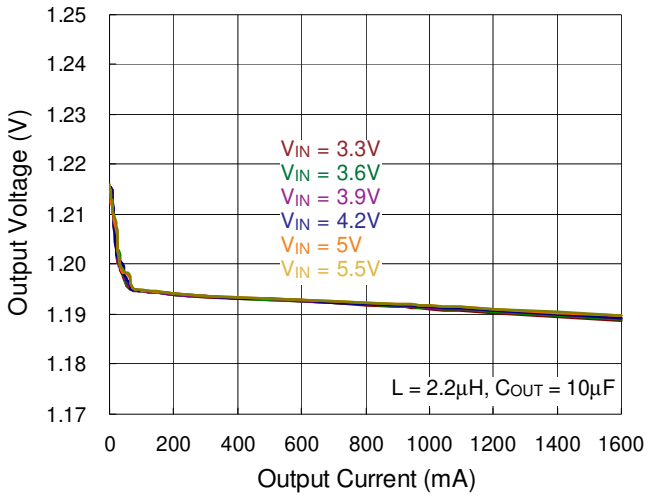
CH1 Buck Output Voltage vs. Output Current



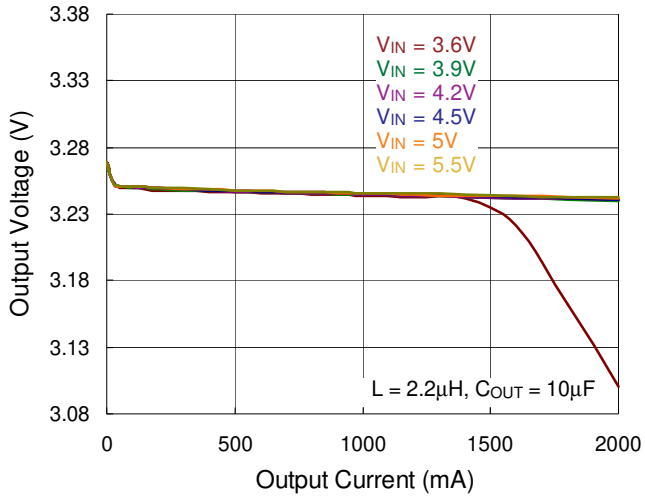
CH2 Buck Output Voltage vs. Output Current



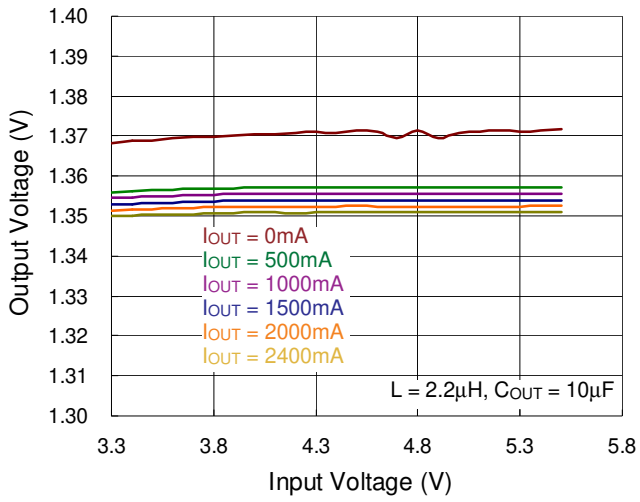
CH3 Buck Output Voltage vs. Output Current



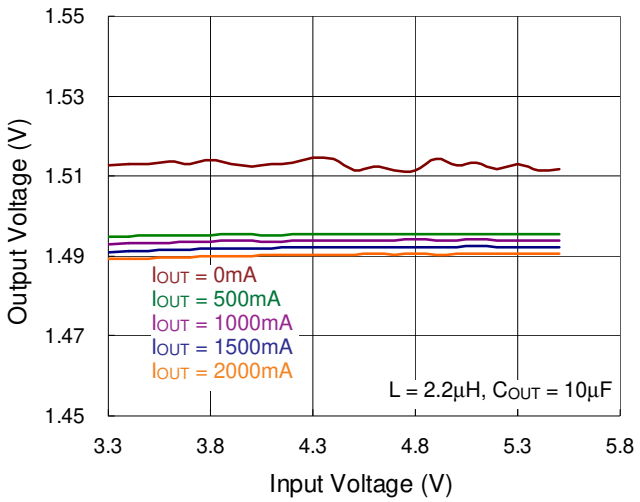
CH4 Buck Output Voltage vs. Output Current



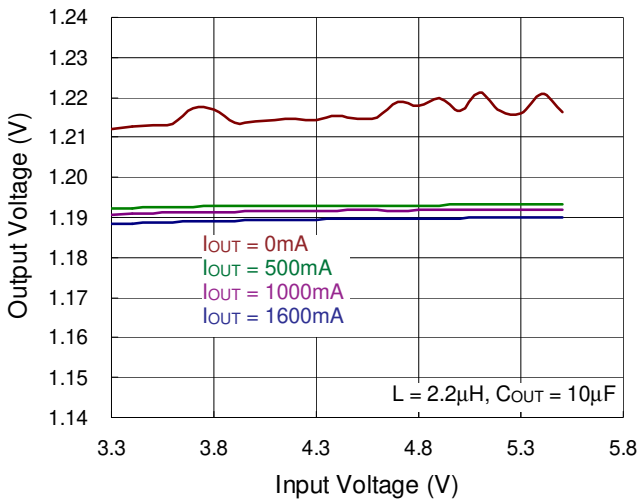
CH1 Buck Output Voltage vs. Input Voltage



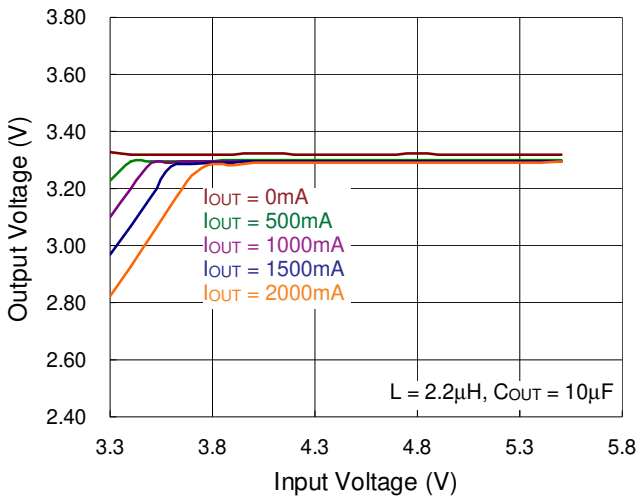
CH2 Buck Output Voltage vs. Input Voltage



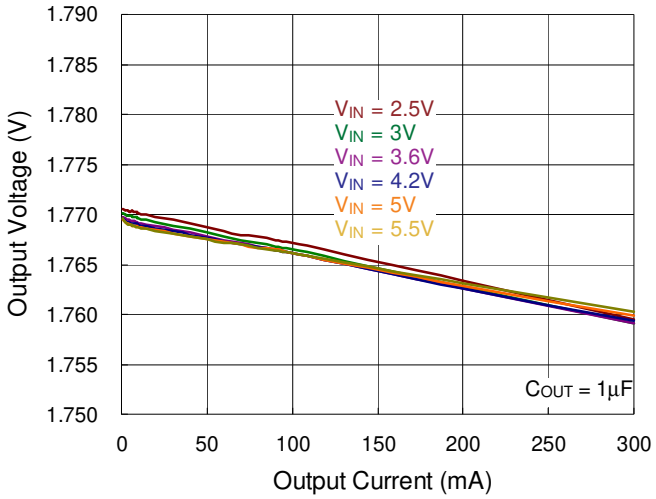
CH3 Buck Output Voltage vs. Input Voltage



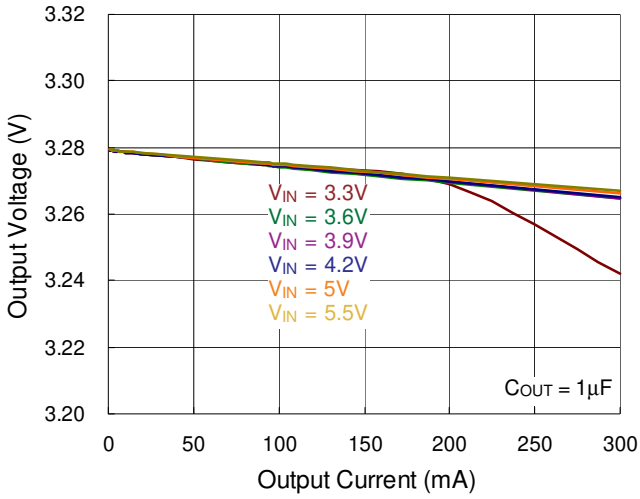
CH4 Buck Output Voltage vs. Input Voltage



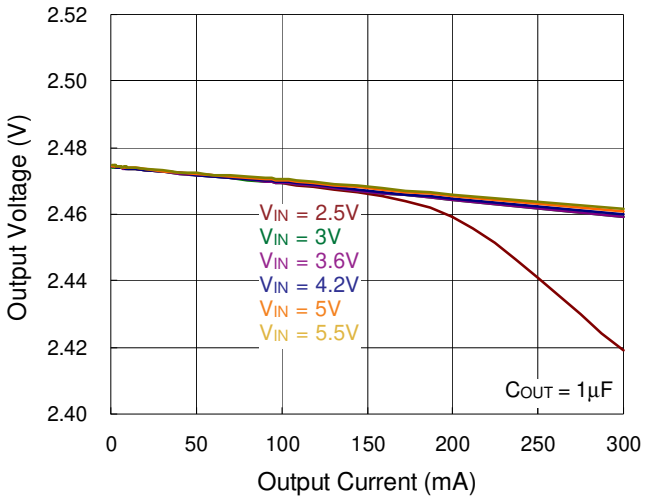
LDO2 Output Voltage vs. Output Current



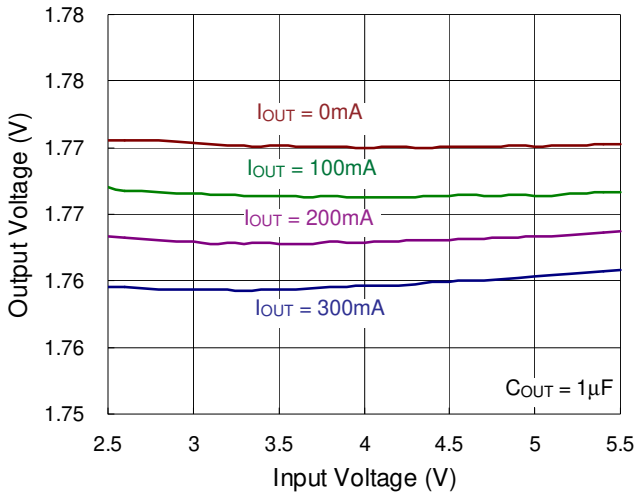
LDO5 Output Voltage vs. Output Current



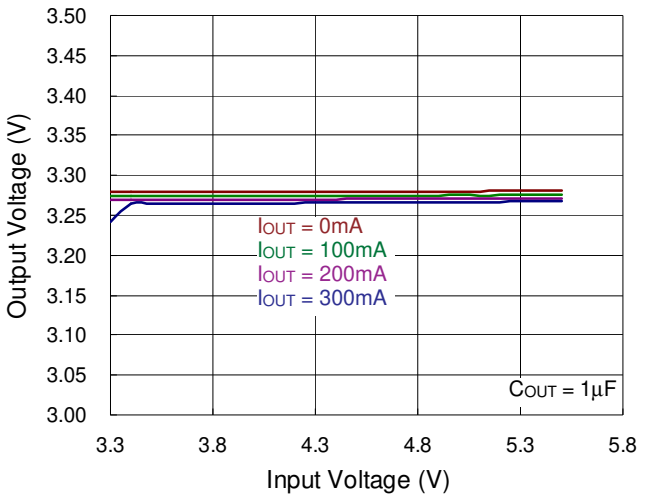
LDO7 Output Voltage vs. Output Current



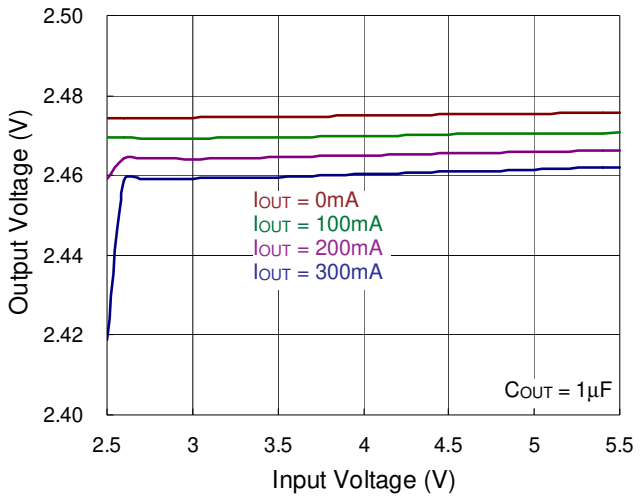
LDO2 Output Voltage vs. Input Voltage



LDO5 Output Voltage vs. Input Voltage



LDO7 Output Voltage vs. Input Voltage



Application Information

The RT5028A is a highly-integrated solution for automotive system including PMIC and memory system. The RT5028A application mechanism and I²C compatible interface are introduced in later sections. The system's slave address is 0110111 (As SADDR = high) or 0111111 (As SADDR = low).

PMIC - Power management system provides 8 low dropout linear regulator and 4 high efficiency synchronous step-down DC-DC converters. Power-On and Power-Off sequences are control by PWRON and $\overline{\text{RESET}}$ input pins.

Detail time sequence control is described in Power ON/OFF diagram. The I²C interface can program individual regulator output voltage as well as on/off control and voltage setting.

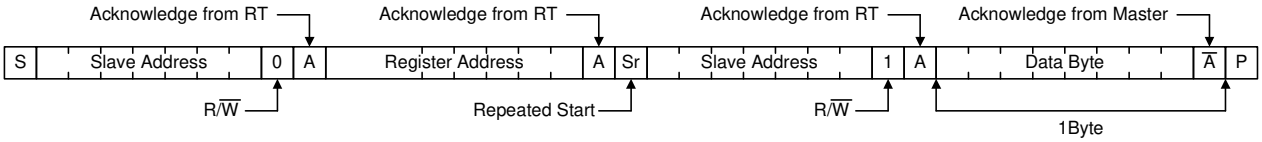
I²C Interface Timing Diagram

The RT5028A acts as an I²C -bus slave. The I²C-bus master configures the settings for all function blocks by sending command bytes to the RT5028A via the 2-wire I²C-bus. The I²C timing diagrams are list in the following.

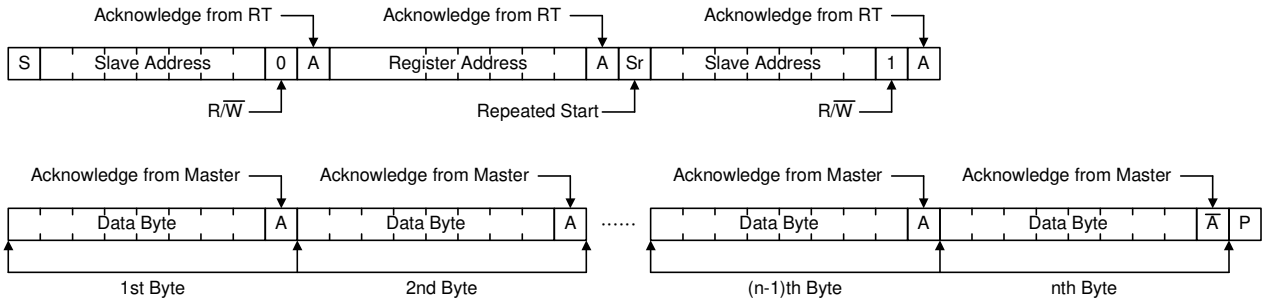
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
I²C Interface Electrical Characteristics						
SDA, SCLK Input High Level Threshold			0.7 x VDDP	--	--	V
SDA, SCLK Input Low Level Threshold			--	--	0.3 x VDDP	V
SCLK Clock Rate	f_{SCL}		--	--	400	kHz
Hold Time (Repeated) START Condition. After this period, the first clock pulse is generated	$t_{HD;STA}$		0.6	--	--	µs
LOW Period of the SCL Clock	t_{LOW}		1.3	--	--	µs
HIGH Period of the SCL Clock	t_{HIGH}		0.6	--	--	µs
Set-Up Time for a Repeated START Condition	$t_{SU;STA}$		0.6	--	--	µs
Data Hold Time	$t_{HD;DAT}$		0	--	0.9	µs
Data Set-Up Time	$t_{SU;DAT}$		100	--	--	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		0.6	--	--	µs
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3	--	--	µs
Rise Time of Both SDA and SCL Signals	t_R		20	--	300	ns
Fall Time of Both SDA and SCL Signals	t_F		20	--	300	ns
SDA and SCL Output Low Sink Current	I_{OL}	SDA or SCL voltage = 0.4V	2	--	--	mA

Read Function

Reading One Indexed Byte of Data from RT (With 1-Byte)

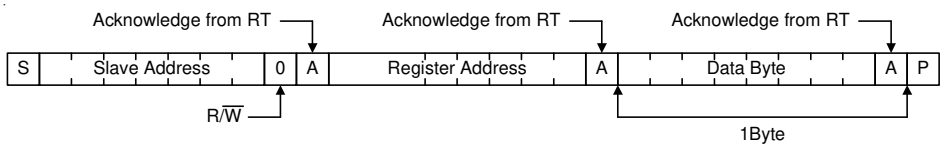


Reading n Indexed Words of Data from RT (With N-Byte)

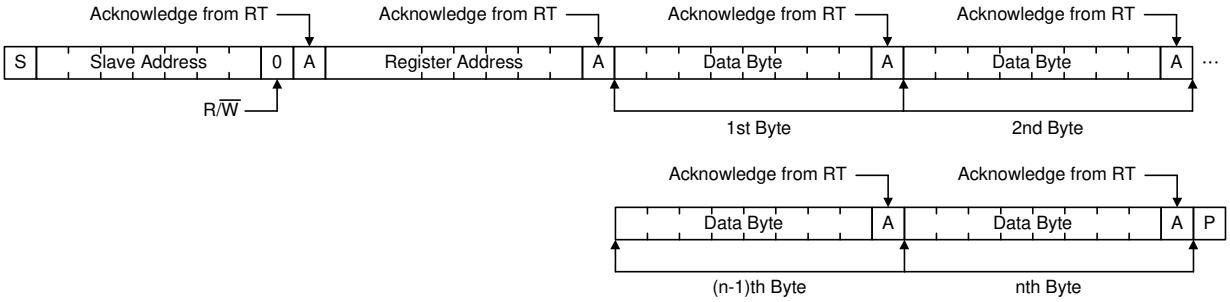


Write Function

Writing One Byte of Data to RT (With 1-Byte)



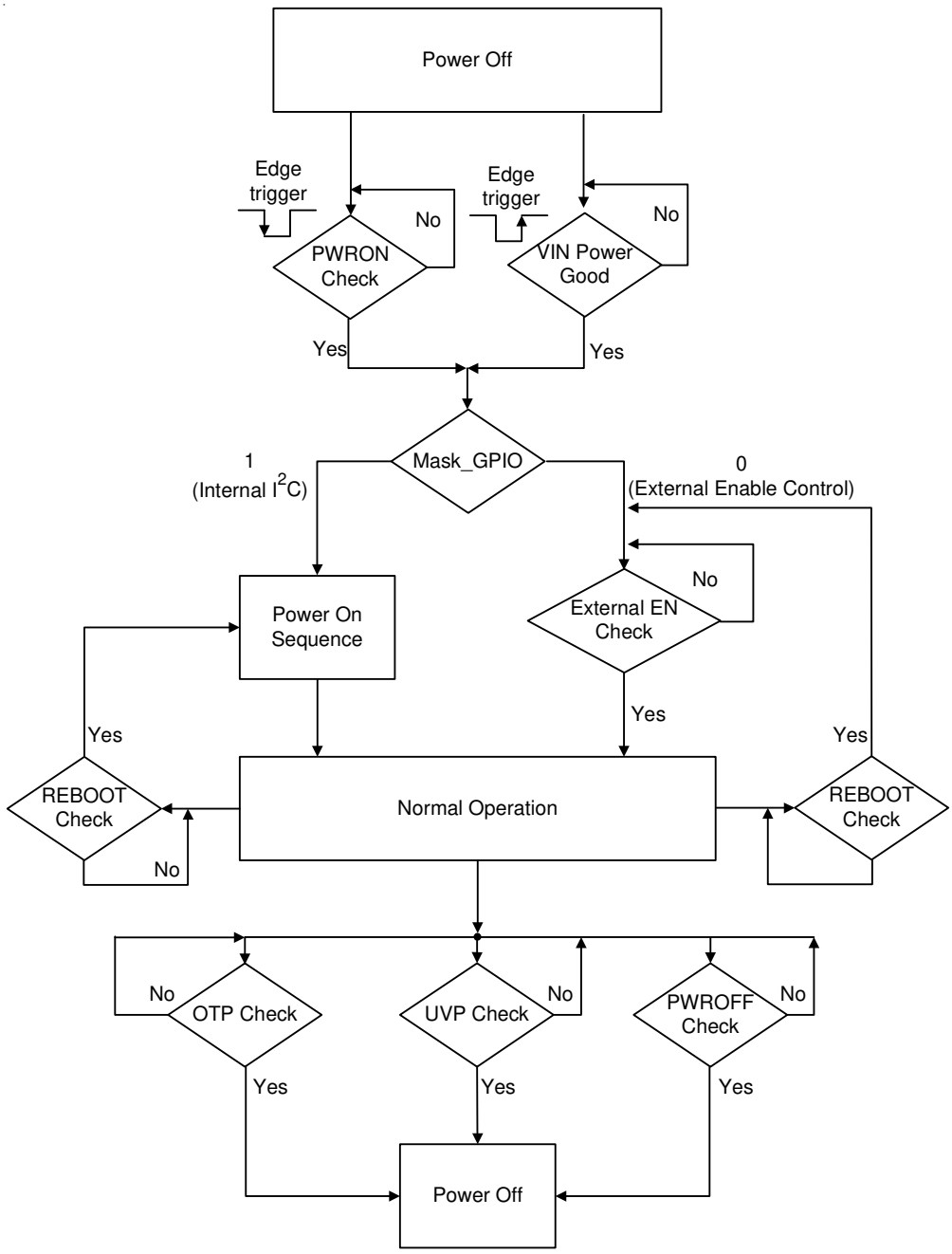
Writing n Bytes of Data to RT (With N-Byte)



PMIC

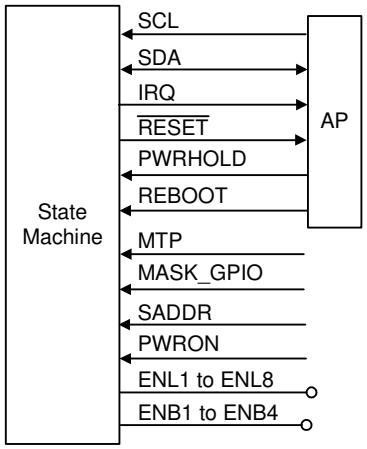
Power Channels Control Methodology

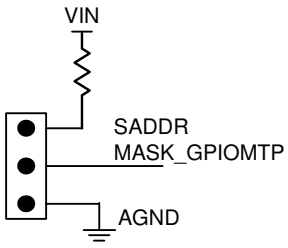
When VIN power Good or PWRON event occurs, the PMIC will follow the power on sequence to turn on channels. During normal operation, users can use the REBOOT pin to restart PMIC again. Another PWROFF event, OTP or UVP occurs, PMIC will execute the power off. In the RT5028A PMIC, the UVP event will be set out when the Buck1 to Buck4s' output voltage is lower than 1/2 x (V_{OUT}).



PMIC - POWER ON/OFF Setting

The circuit setting for communication between RT5028A and AP is showed as below.





As SADDR connect to AGND
slave address
=0111111
As SADDR connect to VIN
slave address
=0110111

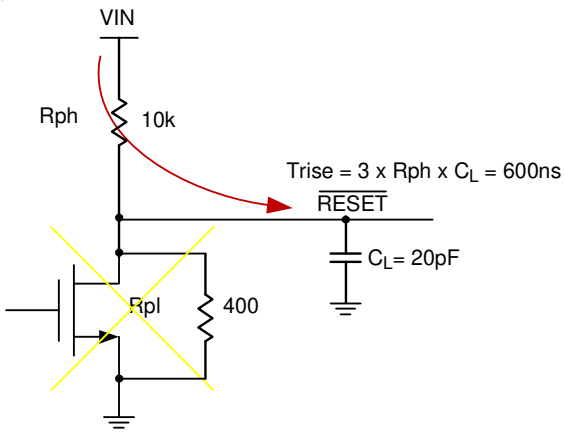
As MASK_GPIO connect to AGND
EN pins can control.
As MASK_GPIO connect to VIN
Ignore all EN pins.

As MTP connect to AGND
Inhibit to write MTP.
As MTP connect to VIN
Permit to write MTP.

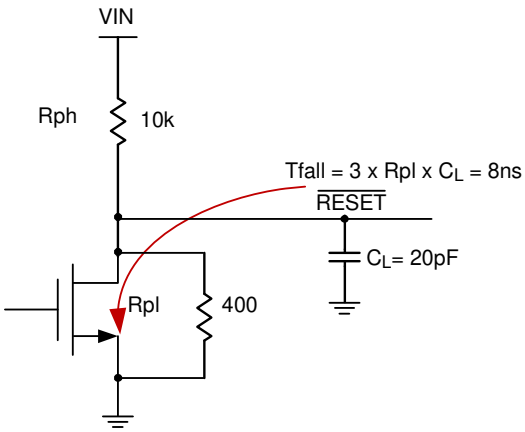
$\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ comparator features an open drain output. The $\overline{\text{RESET}}$ pin pull high to input voltage with 10kΩ which slew rate define as follow.

$\overline{\text{RESET}}$ Rising Slew Rate



$\overline{\text{RESET}}$ Falling Slew Rate



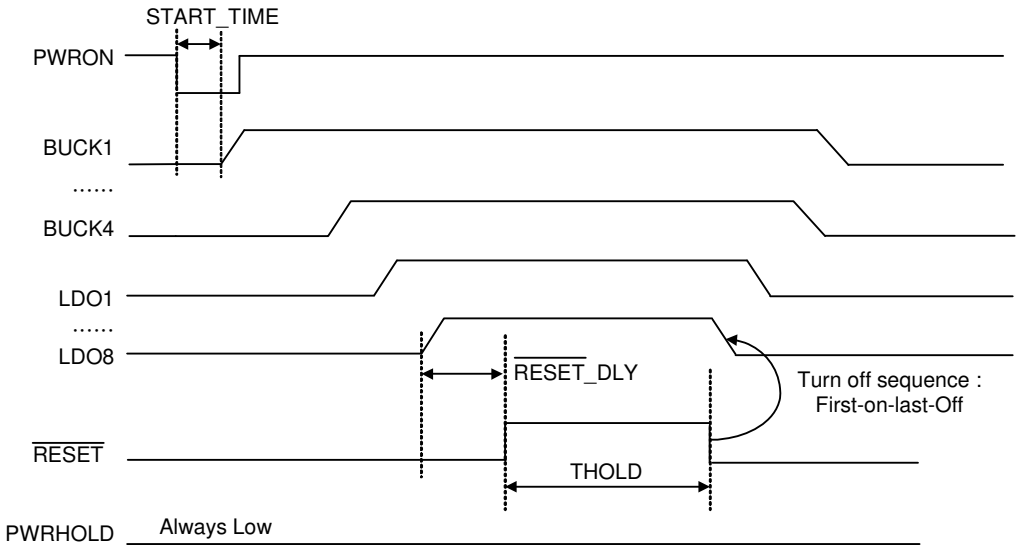
GPIO Pin Pull-Up/Down Defined

Pin No.	Pin Name	GPIO Pin Pull-Up/Down Defined	Resistor
12	ENL4	Internal 100kΩ pull low resistor	Internal
13	ENL5	Internal 100kΩ pull low resistor	Internal
14	ENL6	Internal 100kΩ pull low resistor	Internal
15	SCL	Open drain, need to connect 10kΩ pull up	External
16	SDA	Open drain, need to connect 10kΩ pull up	External
17	ENL7	Internal 100kΩ pull low resistor	Internal
18	ENL8	Internal 100kΩ pull low resistor	Internal
22	PWRON	Internal 100kΩ pull up resistor	Internal
23	REBOOT	Internal 100kΩ pull low resistor	Internal
24	MTP	Internal 100kΩ pull low resistor	Internal
26	PWRHOLD	Internal 100kΩ pull low resistor	Internal
27	SADDR	Internal 100kΩ pull low resistor	Internal
28	ENB4	Internal 100kΩ pull low resistor	Internal
30	ENB3	Internal 100kΩ pull low resistor	Internal
40	ENB2	Internal 100kΩ pull low resistor	Internal
49	ENB1	Internal 100kΩ pull low resistor	Internal
53	ENL1	Internal 100kΩ pull low resistor	Internal
54	ENL2	Internal 100kΩ pull low resistor	Internal
55	ENL3	Internal 100kΩ pull low resistor	Internal

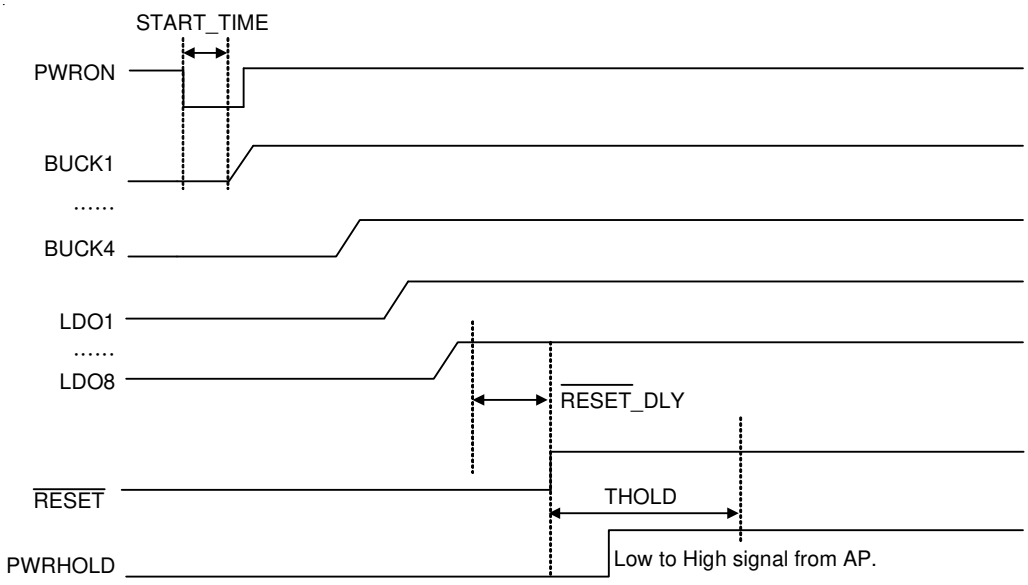
Power Hold Function

When the "PWRHOLD" signal does not come during THOLD time, the RT5028A will do shutdown sequence.

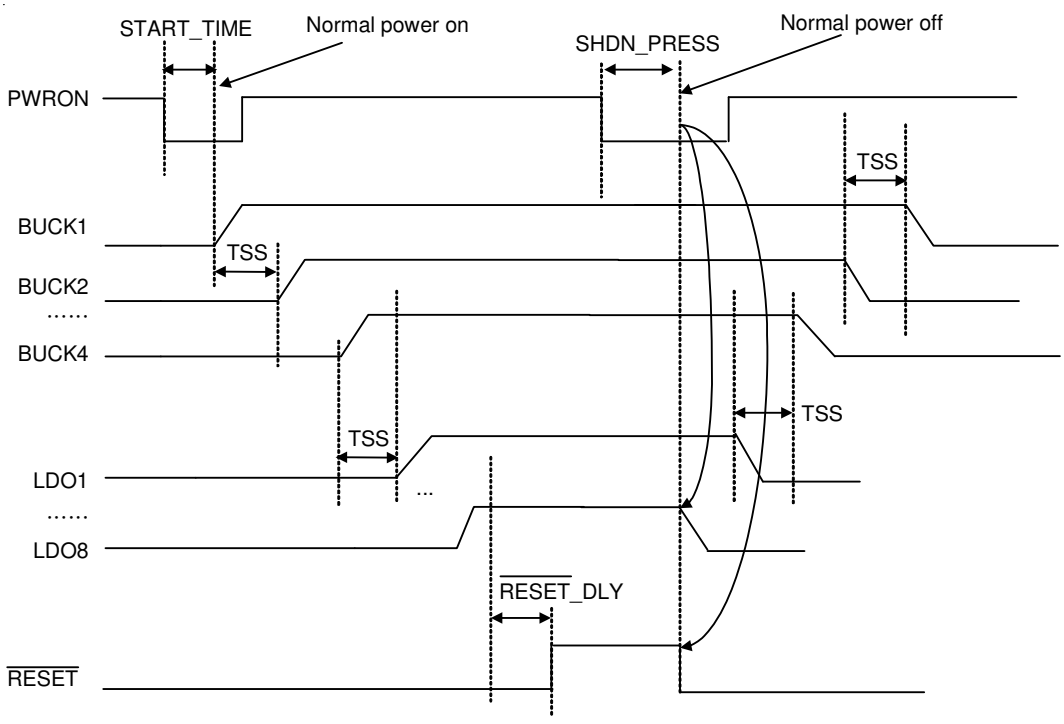
If users want to disable power hold function, set "DisTHOLD" bit in I^2C register 10 bit[0] to disable this function. In the timing diagram below, the "THOLD" and "$\overline{\text{RESET}}$_DLY" can be set by MTP program.



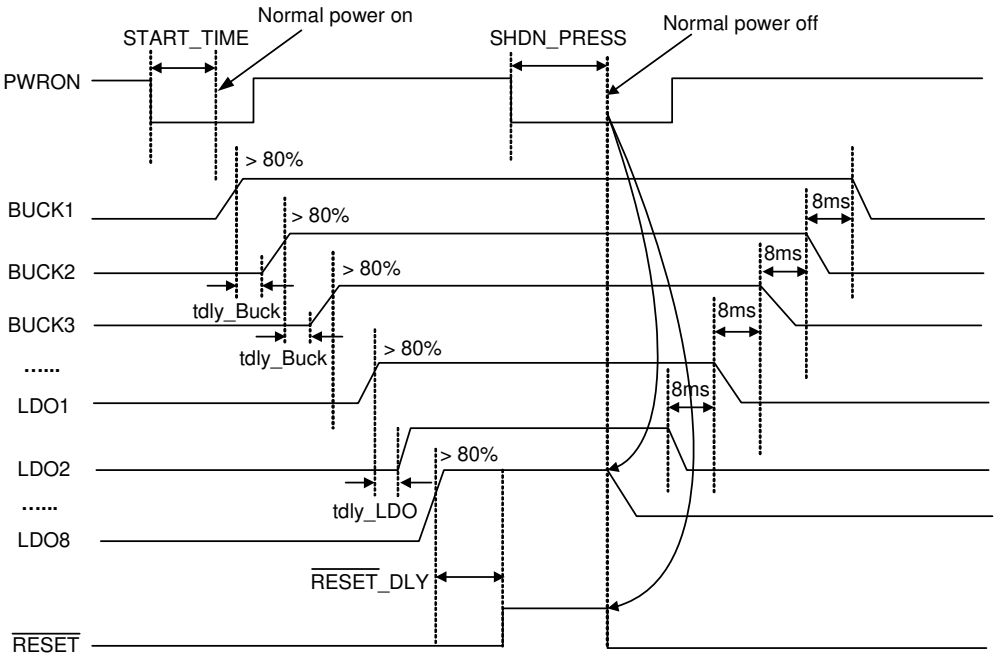
When AP sends the " PWRHOLD" signal during THOLD time, the RT5028A will keep power-on.



Timing Based ON/OFF Sequence (PWRON_NORMOFF_EN, Reg0x15[0] = 1)

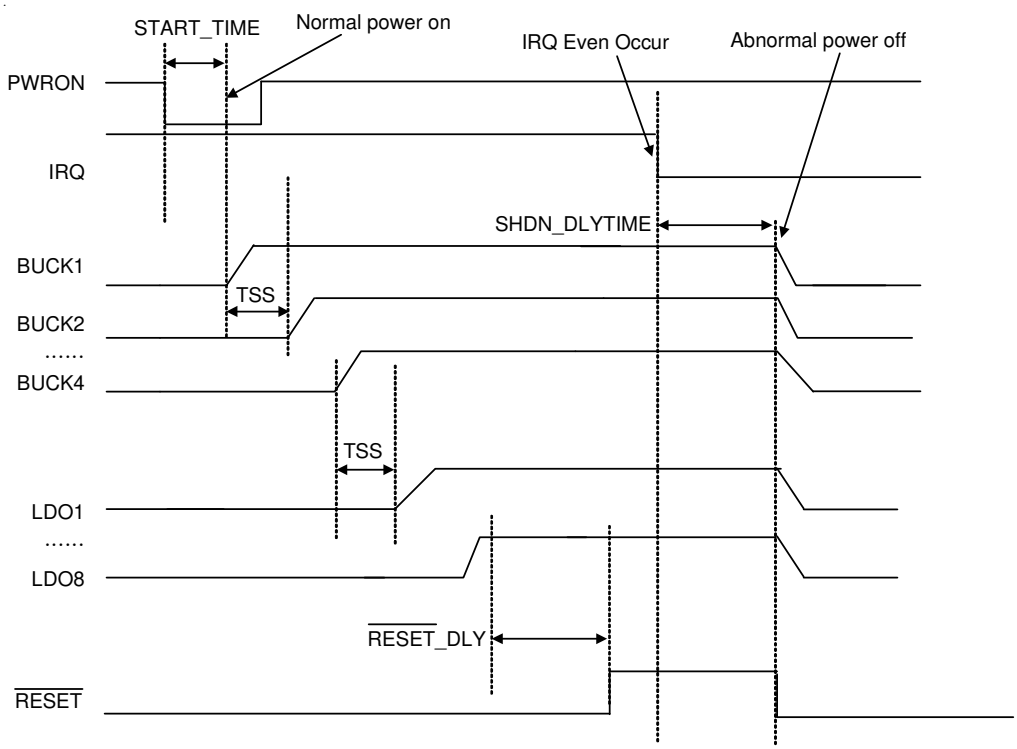


Level Based ON/OFF Sequence (PWRON_NORMOFF_EN, Reg0x15[0] = 1)

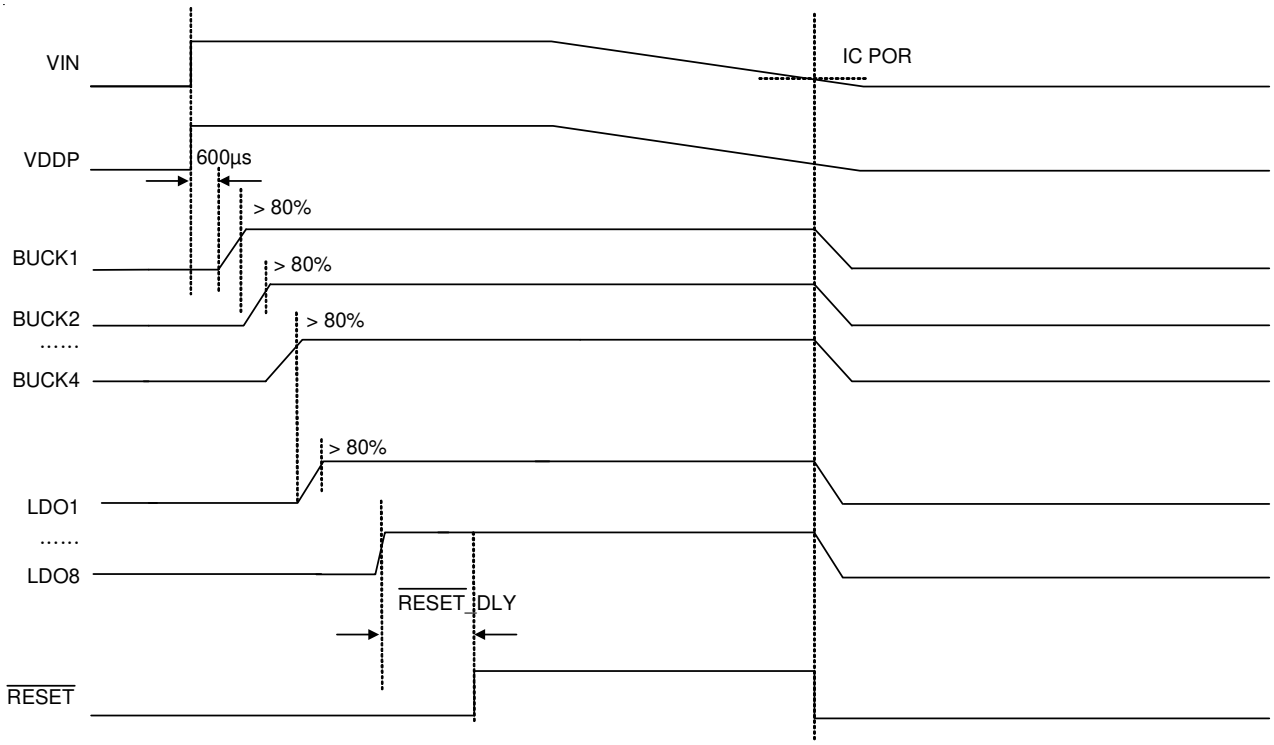


Note.
Sequence : BUCK1→BUCK2→BUCK3→BUCK4→LDO1→LDO2→LDO3→LDO4→LDO5→LDO6→LDO7→LDO8
tdly_Buck : 192 x (1/fsw) + 40μs ±35%
tdly_LDO : 110μs ±20% (If previous one channel is Buck, additional delay time 32 x (1/fsw) need to be added to tdly_LDO.)

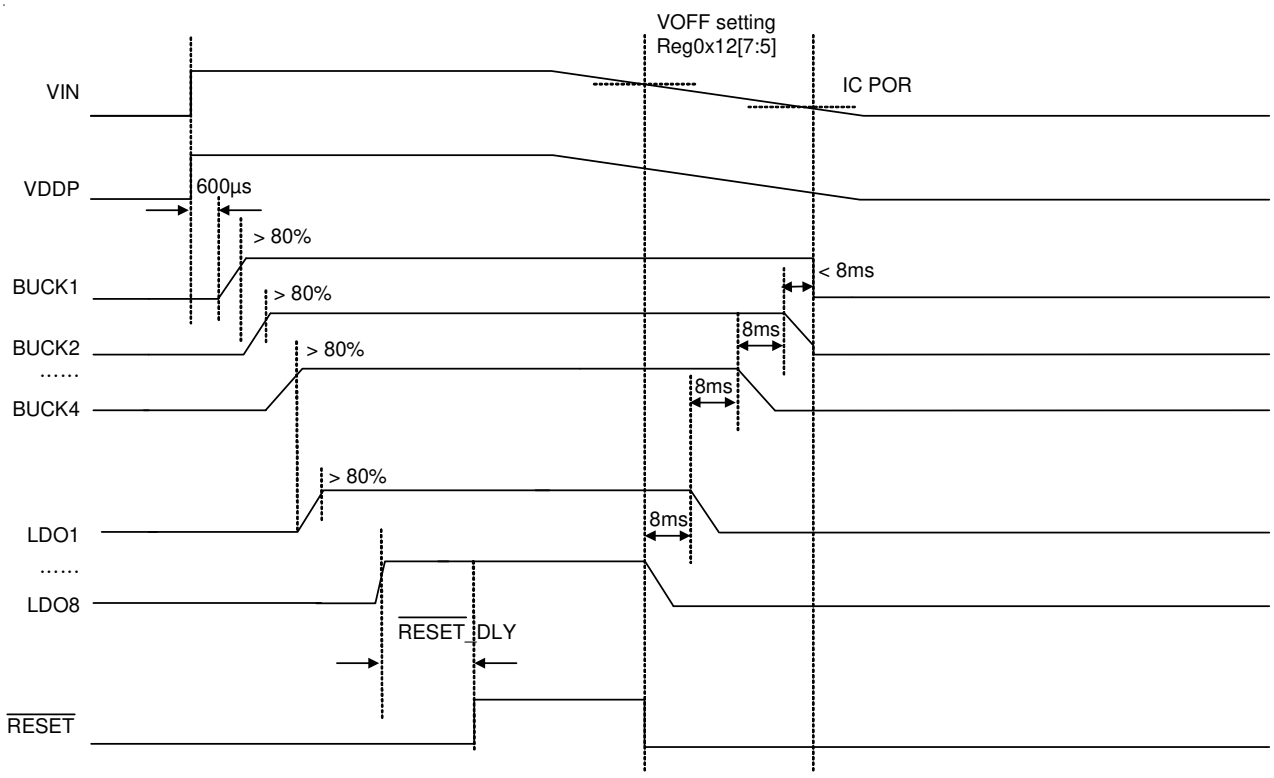
Abnormal OFF (OTP, Buck 1/2/3/4 UVP)



Based ON/OFF Sequence by VIN (VINLV_ENSHDN, Reg0x16[1] = 0)



(VINLV_ENSHDN, Reg0x16[1] = 1; VINLV_SEQ_EN, Reg0x16[0] = 1)



PMU On/Off Sequence Setting

In the RT5028A, users can set the power on/off sequence and output voltage by I^2C register 0x01 to 0x04 for Buck output voltage, 0x07 to 0x0E for LDO output voltage and 0x2C to 0X32 for startup sequence setting.

In the table below, users must set one by one (continues number) and missing code is not allowed.

If users miss sequence code, the RT5028A will wait for next channel and the IC will be hold in waiting status.

	Output Voltage Setting	Startup Sequence Setting	Startup Enable Method (Soft-Start Control)
Buck1	Buck1Output[5:0]	Buck1_Seq[3:0]	[10]
	[000000]	[0001]	
Buck2	Buck2Output[5:0]	Buck2_Seq[3:0]	
	[101100]	[0010]	
Buck3	Buck3Output[5:0]	Buck3_Seq[3:0]	
	[000000]	[0011]	
Buck4	Buck4Output[5:0]	Buck4_Seq[3:0]	
	[101100]	[0100]	
LDO1	LDO1OUT[6:0]	LDO1_Seq[3:0]	
	[0000000]	[0101]	
LDO2	LDO2OUT[6:0]	LDO2_Seq[3:0]	
	[0101000]	[0110]	
LDO3	LDO3OUT[6:0]	LDO3_Seq[3:0]	
	[0000000]	[0111]	
LDO4	LDO4OUT[6:0]	LDO4_Seq[3:0]	
	[0101000]	[1000]	
LDO5	LDO5OUT[6:0]	LDO5_Seq[3:0]	
	[0000000]	[1001]	
LDO6	LDO6OUT[6:0]	LDO6_Seq[3:0]	
	[0101000]	[1010]	
LDO7	LDO7OUT[6:0]	LDO7_Seq[3:0]	
	[0000000]	[1011]	
LDO8	LDO8OUT[6:0]	LDO8_Seq[3:0]	
	[0101000]	[1100]	

Note :

* Output Voltage Setting: fill relative binary code to set the output voltage.
* Startup Sequence Setting :

  “0000” denotes no operation (disable).

  “0001” denotes first-startup.

  “1100 to 1111” denotes last-startup.

  If same number, it means startup at the same time.

*Startup Enable Method :

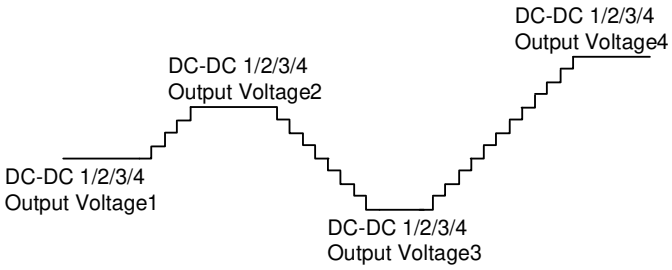
  [01] to [11] : each startup enable interval time (1ms, 4ms, 8ms).

  [00] : start end voltage (the output voltage's 80%)

Synchronous Step-Down DC-DC Converter

Four current mode synchronous step-down DC-DC converters operate with internal power MOSFETs and compensation network. These channels supply the power core chip of portable system. They can be operated at 100% maximum duty cycle to extend battery operating voltage range. When the input voltage is close to the output voltage, the converter enters low dropout mode with low output ripple. The operating frequency range of step-down converter is 0.5MHz to 2MHz.

Four step-down converters have RAMP control function as the following diagram.

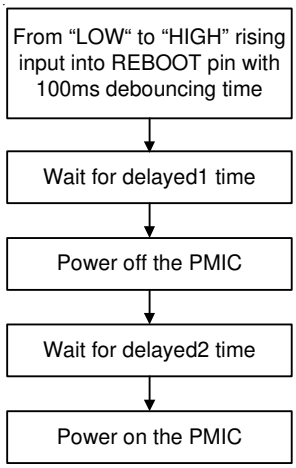


REBOOT Function

As the REBOOT pin is set from low to high, the REBOOT function will be active. The REBOOT's FSM is shown as below. It concludes 100ms de-bouncing time and delay1/ delay2 power off delay time.

Table 1. REBOOT Input Control Setting

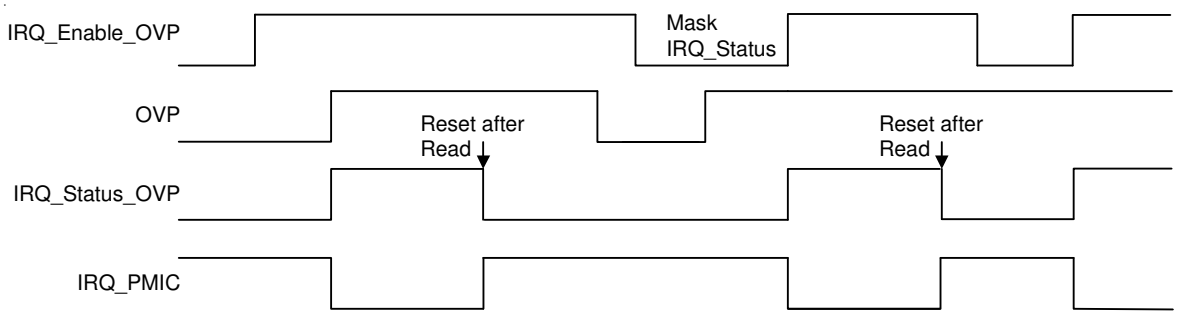
	Description	Default
delayed2	00 : 100ms 10 : 1s 01 : 500ms 11 : 2s	Option
delayed1		Option
Action	delayed1 power-off then delayed2 power-on PMIC	



IRQ Table

We summarize all IRQ items in the register table. All IRQ_status registers are implemented as reset after read. If IRQ_enable bit is Low, the IRQ_status bit will not update status. IRQ_enable will mask IRQ_status to trigger IRQ_PMIC Low, so the system can decide which interrupt is necessary.

Waveform - (when the other IRQ_status are low)



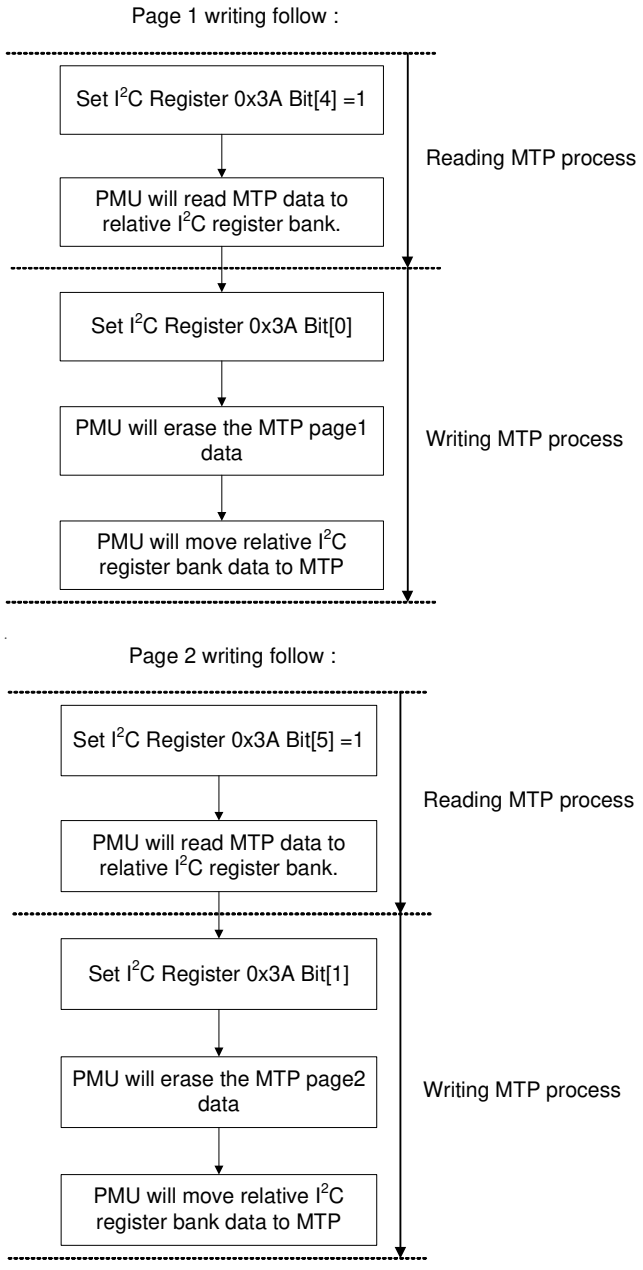
Waveform - (when the other IRQ_status are low)

* OTW125/OTW100 means the 125°C/100°C pre-warming over temperature. It only change IRQ status bits and don't trigger IRQ pin.

EEPROM (MTP) Control Flow

The RT5028A embeds 32 bytes MTP memory, and it allows users to save some I²C register bank data to MTP. When the I²C register 0x3A Bit[0]/Bit[1] is wrote to "1", the MTP Page1/Page2 will execute erase process firstly.

Because the erase process will be done in every writing time, the MTP data will be missed. So it would be best for users to read data from MTP to I²C first before executing writing process.



Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WQFN-56L 7x7 package, the thermal resistance, θ_{JA}, is 27°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (27°C/W) = 3.7W for WQFN-56L 7x7 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

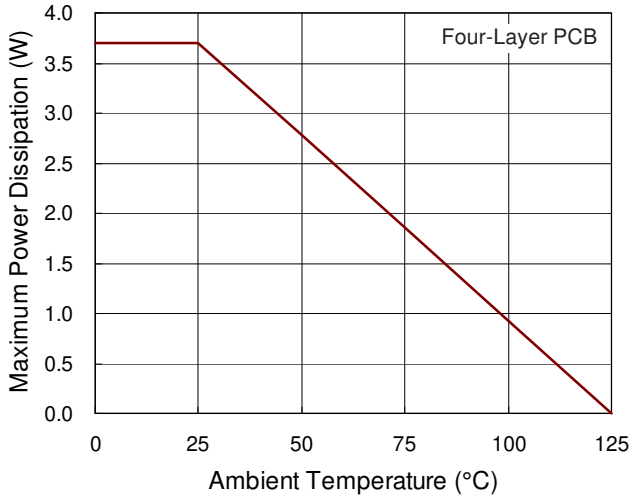


Figure 1. Derating Curve of Maximum Power Dissipation

Layout Consideration

For the best performance of the RT5028A, the following PCB layout guidelines must be strictly followed.

- Place the input and output capacitors as close as possible to the input and output pins respectively for good filtering.
- Keep the main power traces as wide and short as possible.
- The switching node area connected to LX and inductor should be minimized for lower EMI.
- Connect the GND and Exposed Pad to a strong ground plane for maximum thermal dissipation and noise protection.
- Directly connect the output capacitors to the feedback network of each channel to avoid bouncing caused by parasitic resistance and inductance from the PCB trace.

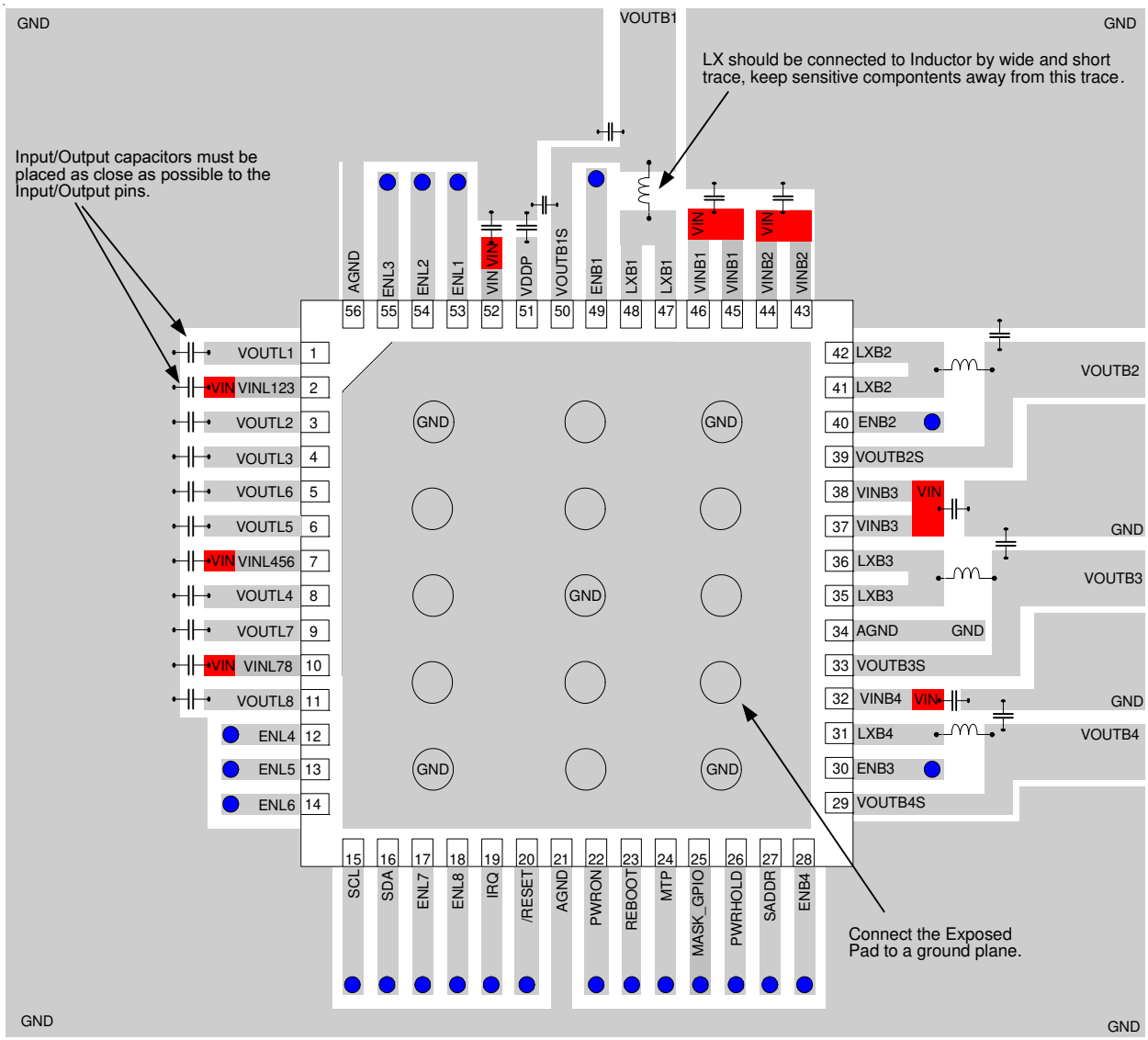


Figure 2. PCB Layout Guide

Table 2. I²C Register Table

Detail Description				
Address	00	Device ID		
Bit	Name	Description	Read/Write	Reset Value
[7:4]	VENDOR_ID	Vendor Identification : Richtek : 1000b	R	1000
[3:0]	CHIP_REV	Chip Revision	R	0001
Address	01	BUCKcontrol1		
Bit	Name	Description	R/W	Reset Value
[7:2]	Buck1Output[5:0]	Buck1 output voltage regulation 000000 : 0.7V, 25mV per step 000001 : 0.725V … 101100 : 1.8V … 111111 : 1.8V	R/W	Option
[1:0]	Buck1VRC	VRC setting 00 : 25mV/10μs, 01 : 50mV/10μs, 10 : 100mV/10μs, 11 : 200mV/10μs	R/W	Option
Address	02	BUCKcontrol2		
Bit	Name	Description	R/W	Reset Value
[7:2]	Buck2Output[5:0]	Buck2 output voltage regulation 000000 : 0.7V, 25mV per step 000001 : 0.725V … 101100 : 1.8V … 111111 : 1.8V	R/W	Option
[1:0]	Buck2VRC	VRC setting 00 : 25mV/10μs, 01 : 50mV/10μs, 10 : 100mV/10μs, 11 : 200mV/10μs	R/W	Option
Address	03	BUCKcontrol3		
Bit	Name	Description	R/W	Reset Value
[7:2]	Buck3Output[5:0]	Buck3 output voltage regulation 000000 : 0.7V, 50mV per step 000001 : 0.75V … 111010 : 3.6V … 111111 : 3.6V	R/W	Option
[1:0]	Buck3VRC	VRC setting 00 : 50mV/10μs, 01 : 100mV/10μs, 10 : 200mV/10μs, 11 : 400mV/10μs	R/W	Option

Address	04	BUCKcontrol4		
Bit	Name	Description	R/W	Reset Value
[7:2]	Buck4Output[5:0]	Buck4 output voltage regulation 000000 : 0.7V, 50mV per step 000001 : 0.75V … 111010 : 3.6V … 111111 : 3.6V	R/W	Option
[1:0]	Buck4VRC	VRC setting 00 : 50mV/10μs, 01 : 100mV/10μs, 10 : 200mV/10μs, 11 : 400mV/10μs	R/W	Option
Address	05	VRC Control		
Bit	Name	Description	R/W	Reset Value
7	Buck1VRC_EN	Buck1 VRC 0 : disable - voltage ramps up to target voltage with one time 1 : enable - voltage ramps up to target voltage with slope control	R/W	Option
6	Buck2VRC_EN	Buck2 VRC 0 - disable - voltage ramps up to target voltage with one time 1 - enable - voltage ramps up to target voltage with slope control	R/W	Option
5	Buck3VRC_EN	Buck3 VRC 0 : disable - voltage ramps up to target voltage with one time 1 : enable - voltage ramps up to target voltage with slope control	R/W	Option
4	Buck4VRC_EN	Buck4 VRC 0 : disable - voltage ramps up to target voltage with one time 1 : enable - voltage ramps up to target voltage with slope control	R/W	Option
[3:0]	Reserved		R/W	0000
Address	06	BUCK Mode		
Bit	Name	Description	R/W	Reset Value
7	Buck1mode	Buck1 mode 0 : Force PWM 1 : Auto Mode (PSM/PWM)	R/W	Option
6	Buck2mode	Buck2 mode 0 : Force PWM 1 : Auto Mode (PSM/PWM)	R/W	Option
5	Buck3mode	Buck3 mode 0 : Force PWM 1 : Auto Mode (PSM/PWM)	R/W	Option