Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Dual Single-Phase PWM Controller for CPU Core/GFX Power Supply

General Description

The RT8167A is a dual single-phase synchronous Buck PWM controller with integrated gate drivers, compliant with Intel VR12/IMVP7 specification. A serial VID (SVID) interface is built-in in the RT8167A to communicate with Intel VR12/IMVP7 compliant CPU. The integrated differential remote output voltage sensing function and built-in high accuracy DAC achieve accurate output voltage regulation.

The RT8167A supports VR12/ IMVP7 compatible power management states and VID on-the-fly function. The RT8167A operates in two power management states including DEM in PS2 and Forced-CCM in PS1/PS0. Richtek's proprietary G-NAVP™ (Green Native AVP) makes AVP (Active Voltage Positioning) design easier and more robust. By utilizing the G-NAVP™ topology, DEM and CCM efficiency can be improved.

The RT8167A integrates high accuracy ADC for platform setting functions, such as no-load offset or over current level. Individual VR ready output signals are provided for both CORE VR and GFX VR. The IC also features complete fault protection functions, including over voltage, under voltage, negative voltage, over current and under voltage lockout. The RT8167A is available in a WQFN-48L 6x6 small foot print package.

Marking Information

RT8167AGQW : Product Number

YMDNN : Date Code

Features

- **G-NAVP™ (Green Native Active Voltage Positioning) Topology**
- **Dual Output Controller with Two Built-in Gate Drivers**
- **Serial VID Interface**
- **0.5% DAC Accuracy**
- **Differential Remote Output Voltage Sensing**
- **Built-in ADC for Platform Programming**
- **Diode Emulation Mode (DEM) at Light Load Condition**
- **Droop Enable/Disable**
- **Fast Transient Response**
- **VR12/IMVP7 Compatible Power Management States**
- **VR Ready Indicator**
- **Thermal Throttling Indicator**
- **Current Monitor Output**
- **Switching Frequency up to 1MHz per Phase**
- **Protection : OVP, UVP, NVP, OCP, UVLO**
- **Small 48-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- VR12 / IMVP7 Intel CPU Core Supply
- AVP Step-down Converter
- Notebook/ Netbook/ Desktop Computer CPU Core Supply

Ordering Information

RT8167A□□

- Package Type
  QW : WQFN-48L 6x6 (W-Type)
  (Exposed Pad-Option 1)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

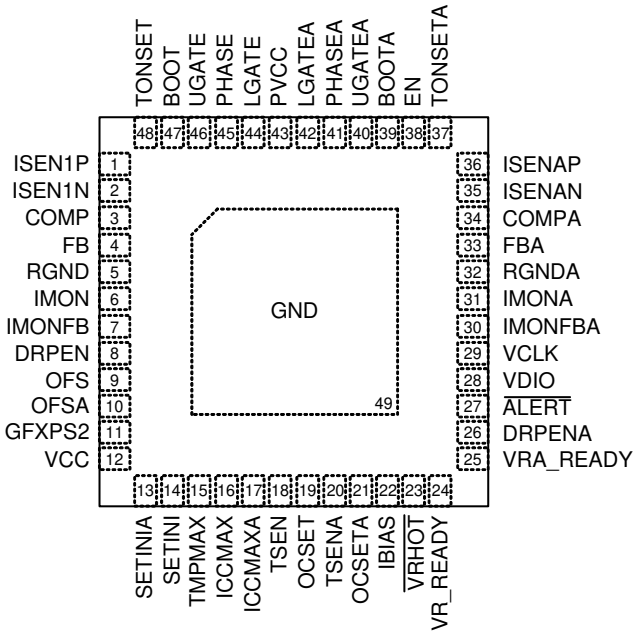
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)



WQFN-48L 6x6

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	ISEN1P	Positive Current Sense Input of CORE VR
2	ISEN1N	Negative Current Sense Input of CORE VR
3	COMP	CORE VR Compensation. This pin is the output node of the error amplifier.
4	FB	CORE VR Feedback. This is the negative input node of the error amplifier.
5	RGND	Return Ground for CORE VR. This pin is the negative input for differential remote voltage sensing.
6	IMON	Current Monitor Output of CORE VR. The output voltage V_{IMON} of this pin is proportional to the output current. For digital output current reporting, detailed V_{IMON} is generated by built-in ADC.
7	IMONFB	This pin is used to externally set the current monitor output gain of CORE VR. Connect this pin with one resistor R_{IMONFB} to CORE VCC_SENSE while IMON pin is connected to ground with another resistor, R_{IMON}. The current monitor output gain can be set by the ratio of these two resistors.
8	DRPEN	Droop Enable Mode Setting of CORE VR. An internal 80μA current source is connected to the DRPEN pin and flows out of this pin for 10μs. Connect this pin to V_{CC} to enable droop function. Connect this pin to GND to disable droop function.
9	OFS	Output Voltage No-Load Offset Setting of CORE VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage V_{OFS} for offset setting. Connect this pin to GND for no offset setting.
10	OFSA	Output Voltage No-Load Offset Setting of GFX VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage V_{OFSA} for offset setting. Connect this pin to GND for no offset setting.

Pin No.	Pin Name	Pin Function
11	GFXPS2	Forced DEM Enable Setting of GFX VR. Connect to V_{CC} for forced-DEM setting and connect to GND for following SVID power state command.
12	VCC	5V Power Supply Input of Controller. Bypass this pin to GND with a 1μF or greater ceramic capacitor.
13	SETINIA	Initial Startup Voltage V_{INI_GFX} Setting of GFX VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage $V_{SETINIA}$ for GFX VR initial startup voltage V_{INI_GFX} setting. Connect this pin to GND for 0V V_{INI_GFX} setting.
14	SETINI	Initial Startup Voltage V_{INI_CORE} Setting of CORE VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage V_{SETINI} for CORE VR initial startup voltage V_{INI_CORE} setting. Connect this pin to GND for 0V V_{INI_CORE} setting.
15	TMPMAX	Maximum Temperature Setting of CORE VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage V_{TMPMAX} for TMPMAX setting.
16	ICCMAX	Maximum Current Setting of CORE VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage V_{ICCMAX} for ICCMAX setting.
17	ICCMAXA	Maximum Current Setting of GFX VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage $V_{ICCMAXA}$ for ICCMAXA setting.
18	TSEN	Thermal Monitor Sense Pin of CORE VR.
19	OCSET	Over Current Protection Setting of CORE VR. Connect to a resistive voltage divider from V_{CC} to GND to set the pin voltage V_{OCSET} from 0 to 3.3V for CORE VR over current protection threshold.
20	TSENA	Thermal Monitor Sense Pin of GFX VR.
21	OCSETA	Over Current Protection Setting of GFX VR. Connect to a resistive voltage divider from V_{CC} to GND to adjust the pin voltage V_{OCSETA} from 0 to 3.3V for GFX VR over current protection threshold.
22	IBIAS	Internal bias current setting. Connect a 53.6kΩ resistor from IBIAS pin to GND.
23	$\overline{\text{VRHOT}}$	Thermal Monitor Output (Active Low). Connect a pull high resistor from $\overline{\text{VRHOT}}$ pin to 1.05V.
24	VR_READY	Voltage Ready Indicator of CORE VR. Connect a pull high resistor from VR_READY pin to 1.05V.
25	VRA_READY	Voltage Ready Indicator GFX VR. Connect a pull high resistor from VRA_READY pin to 1.05V.
26	DRPENA	Droop Enable Mode Setting of GFX VR. An internal 80μA current source is connected to DRPENA pin and flows out of this pin for 10μs. Connect this pin to V_{CC} to enable droop function. Connect this pin to GND to disable droop function.
27	$\overline{\text{ALERT}}$	SVID Alert Pin (Active Low). Connect a 75Ω resistor from $\overline{\text{ALERT}}$ pin to 1.05V.
28	VDIO	Controller and CPU Data Transmission Interface. Connecting a 64.9Ω resistor between VDIO pin to 1.05V.
29	VCLK	Synchronous Clock from the CPU. Connect a 64.9Ω resistor from VCLK pin to 1.05V.
30	IMONFBA	This pin is used to externally set the current monitor output gain of GFX VR. Connect this pin with one resistor $R_{IMONFBA}$ to GFX VCC_SENSE while IMON pin is connected to ground with another resistor R_{IMONA}. The current monitor output gain can be set by the ratio of these two resistors.
31	IMONA	Current Monitor Output of GFX VR. The output voltage VIMONA of this pin is proportional to the output current. For digital output current reporting, detailed VIMONA is generated by built-in ADC.

Pin No.	Pin Name	Pin Function
32	RGNDA	Return Ground for GFX VR. This pin is the negative input for differential remote voltage sensing.
33	FBA	GFX VR Feedback. This is the negative input node of the error amplifier.
34	COMPA	GFX VR Compensation. This pin is the output node of the error amplifier.
35	ISENAN	Negative Current Sense Input of GFX VR.
36	ISENAP	Positive Current Sense Input of GFX VR.
37	TONSETA	On-Time Setting of GFX VR. Connect this pin to VIN with one resistor.
38	EN	Chip Enable (Active High).
39	BOOTA	Bootstrap Flying Capacitor Connection for GFX VR. This pin powers the high side MOSFET drivers. Connect this pin to PHASEA with an external ceramic capacitor.
40	UGATEA	High Side MOSFET Floating Gate Driver Output for GFX VR. Connect this pin to the gate of high side MOSFET.
41	PHASEA	Switching Node Connection for GFX VR. PHASEA is also the zero cross detect input for GFX VR. Connect this pin to the high side MOSFET sources together with the low side MOSFET drains and the inductor.
42	LGATEA	Synchronous-Rectifier Gate Driver Output of GFX VR. Connect this pin to the gate of low side MOSFET.
43	PVCC	5V Power Supply of Driver. Bypass this pin to GND with a 1μF or greater ceramic capacitor.
44	LGATE	Synchronous-Rectifier Gate Driver Output of CORE VR. Connect this pin to the gate of low side MOSFET.
45	PHASE	Switching Node Connection for CORE VR. PHASE is the internal lower supply rail for the UGATE. PHASE is also the zero cross detect input for CORE VR. Connect this pin to the high side MOSFET sources together with the low side MOSFET drains and the inductor.
46	UGATE	High Side MOSFET Floating Gate Driver Output for CORE VR. Connect this pin to the gate of high side MOSFET.
47	BOOT	Bootstrap Flying Capacitor Connection for CORE VR. This pin powers the high side MOSFET drivers. Connect this pin to PHASE with an external ceramic capacitor.
48	TONSET	On-Time Setting of CORE VR. Connect this pin to VIN with one resistor.
49 (Exposed pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Typical Application Circuit

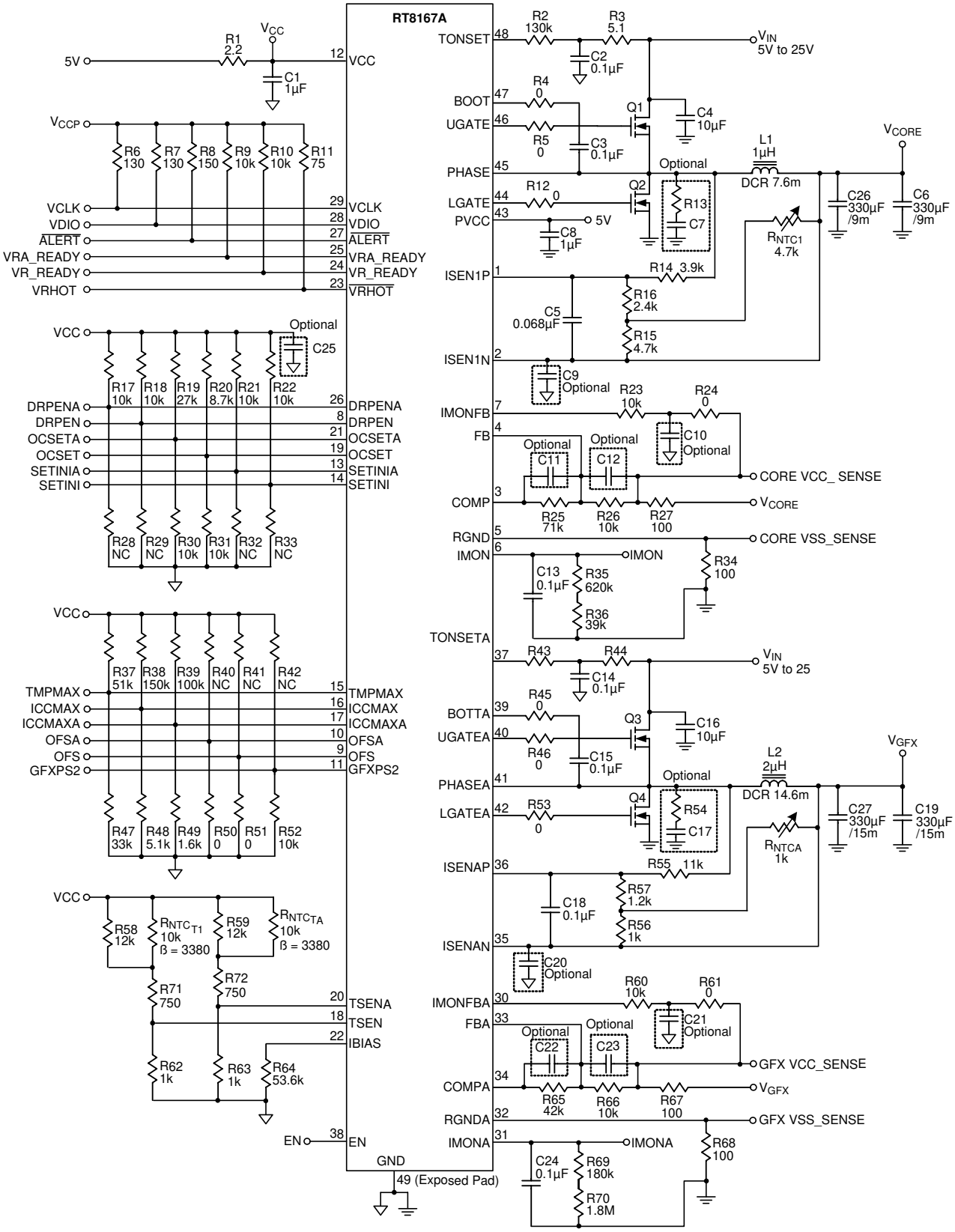


Figure 1. Dual Output Application Circuit

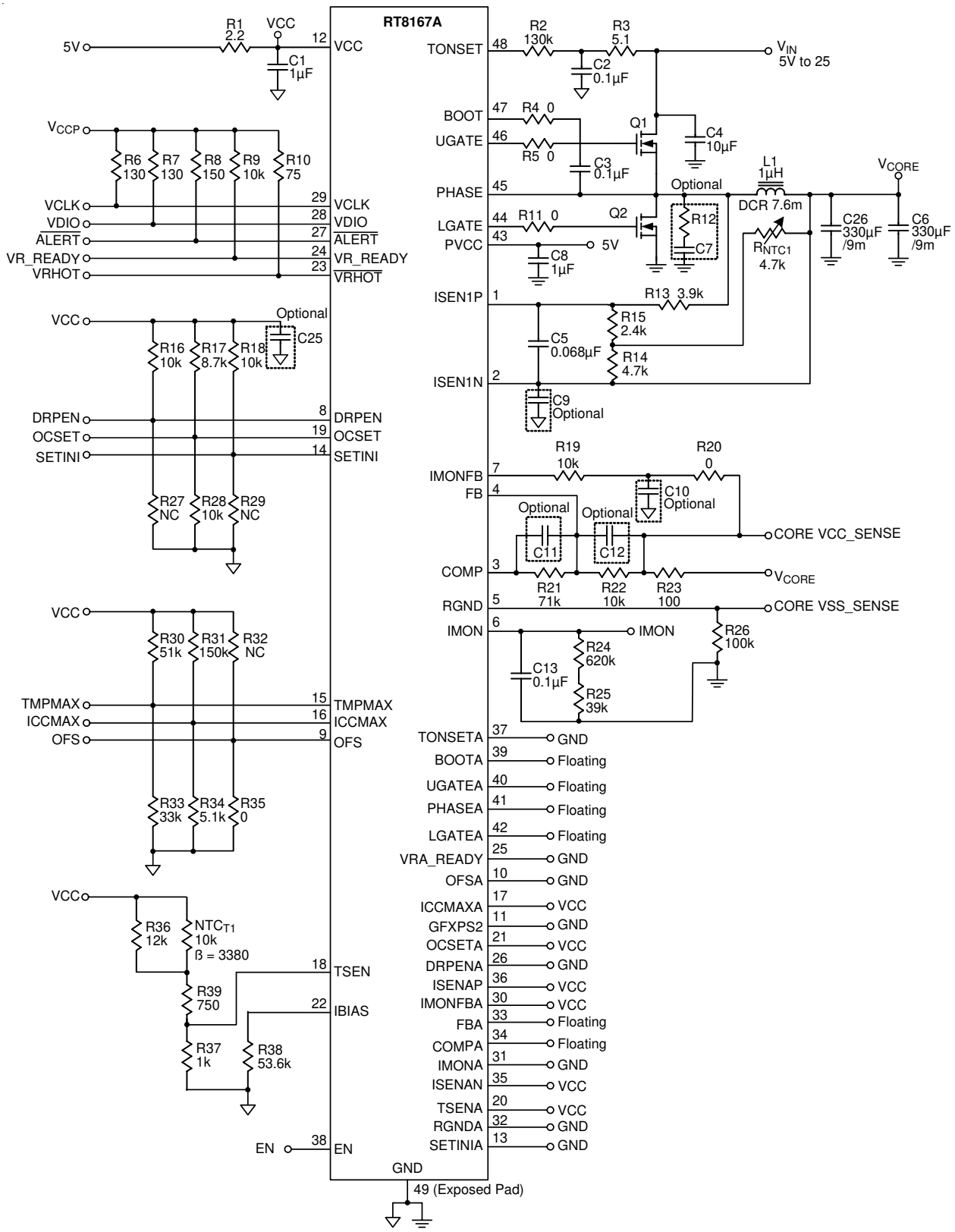


Figure 2. Single Output Application Circuit

Function Block Diagram

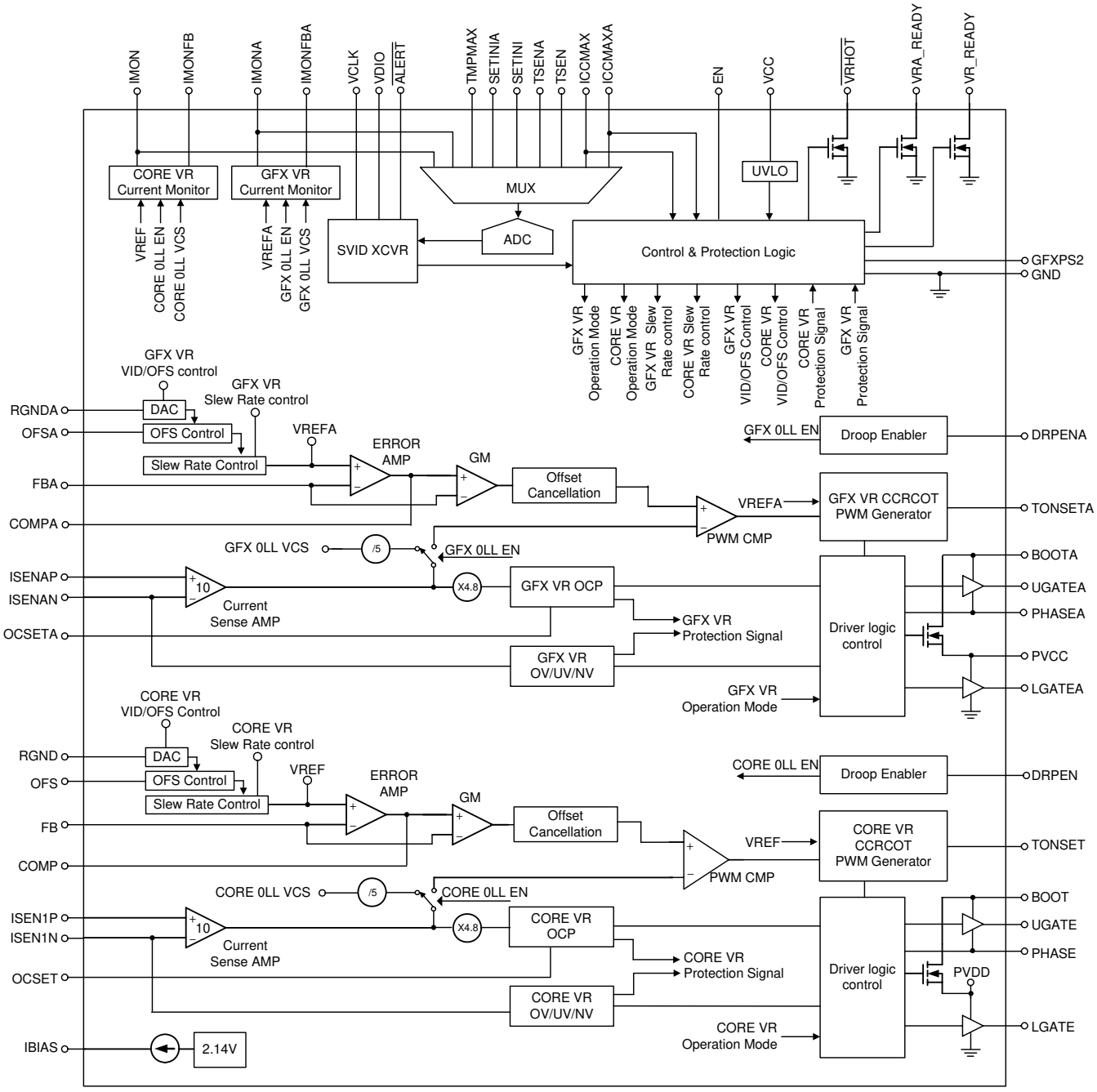


Table 1. IMVP7/VR12 Compliant VID Table

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	VDAC Voltage
0	0	0	0	0	0	0	0	0	0	0.000
0	0	0	0	0	0	0	1	0	1	0.250
0	0	0	0	0	0	1	0	0	2	0.255
0	0	0	0	0	0	1	1	0	3	0.260
0	0	0	0	0	1	0	0	0	4	0.265
0	0	0	0	0	1	0	1	0	5	0.270
0	0	0	0	0	1	1	0	0	6	0.275
0	0	0	0	0	1	1	1	0	7	0.280
0	0	0	0	1	0	0	0	0	8	0.285
0	0	0	0	1	0	0	1	0	9	0.290
0	0	0	0	1	0	1	0	0	A	0.295
0	0	0	0	1	0	1	1	0	B	0.300
0	0	0	0	1	1	0	0	0	C	0.305
0	0	0	0	1	1	0	1	0	D	0.310
0	0	0	0	1	1	1	0	0	E	0.315
0	0	0	0	1	1	1	1	0	F	0.320
0	0	0	1	0	0	0	0	1	0	0.325
0	0	0	1	0	0	0	1	1	1	0.330
0	0	0	1	0	0	1	0	1	2	0.335
0	0	0	1	0	0	1	1	1	3	0.340
0	0	0	1	0	1	0	0	1	4	0.345
0	0	0	1	0	1	0	1	1	5	0.350
0	0	0	1	0	1	1	0	1	6	0.355
0	0	0	1	0	1	1	1	1	7	0.360
0	0	0	1	1	0	0	0	1	8	0.365
0	0	0	1	1	0	0	1	1	9	0.370
0	0	0	1	1	0	1	0	1	A	0.375
0	0	0	1	1	0	1	1	1	B	0.380
0	0	0	1	1	1	0	0	1	C	0.385
0	0	0	1	1	1	0	1	1	D	0.390
0	0	0	1	1	1	1	0	1	E	0.395
0	0	0	1	1	1	1	1	1	F	0.400
0	0	1	0	0	0	0	0	2	0	0.405
0	0	1	0	0	0	0	1	2	1	0.410
0	0	1	0	0	0	1	0	2	2	0.415

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
0	0	1	0	0	0	1	1	2	3	0.420
0	0	1	0	0	1	0	0	2	4	0.425
0	0	1	0	0	1	0	1	2	5	0.430
0	0	1	0	0	1	1	0	2	6	0.435
0	0	1	0	0	1	1	1	2	7	0.440
0	0	1	0	1	0	0	0	2	8	0.445
0	0	1	0	1	0	0	1	2	9	0.450
0	0	1	0	1	0	1	0	2	A	0.455
0	0	1	0	1	0	1	1	2	B	0.460
0	0	1	0	1	1	0	0	2	C	0.465
0	0	1	0	1	1	0	1	2	D	0.470
0	0	1	0	1	1	1	0	2	E	0.475
0	0	1	0	1	1	1	1	2	F	0.480
0	0	1	1	0	0	0	0	3	0	0.485
0	0	1	1	0	0	0	1	3	1	0.490
0	0	1	1	0	0	1	0	3	2	0.495
0	0	1	1	0	0	1	1	3	3	0.500
0	0	1	1	0	1	0	0	3	4	0.505
0	0	1	1	0	1	0	1	3	5	0.510
0	0	1	1	0	1	1	0	3	6	0.515
0	0	1	1	0	1	1	1	3	7	0.520
0	0	1	1	1	0	0	0	3	8	0.525
0	0	1	1	1	0	0	1	3	9	0.530
0	0	1	1	1	0	1	0	3	A	0.535
0	0	1	1	1	0	1	1	3	B	0.540
0	0	1	1	1	1	0	0	3	C	0.545
0	0	1	1	1	1	0	1	3	D	0.550
0	0	1	1	1	1	1	0	3	E	0.555
0	0	1	1	1	1	1	1	3	F	0.560
0	1	0	0	0	0	0	0	4	0	0.565
0	1	0	0	0	0	0	1	4	1	0.570
0	1	0	0	0	0	1	0	4	2	0.575
0	1	0	0	0	0	1	1	4	3	0.580
0	1	0	0	0	1	0	0	4	4	0.585
0	1	0	0	0	1	0	1	4	5	0.590

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
0	1	0	0	0	1	1	0	4	6	0.595
0	1	0	0	0	1	1	1	4	7	0.600
0	1	0	0	1	0	0	0	4	8	0.605
0	1	0	0	1	0	0	1	4	9	0.610
0	1	0	0	1	0	1	0	4	A	0.615
0	1	0	0	1	0	1	1	4	B	0.620
0	1	0	0	1	1	0	0	4	C	0.625
0	1	0	0	1	1	0	1	4	D	0.630
0	1	0	0	1	1	1	0	4	E	0.635
0	1	0	0	1	1	1	1	4	F	0.640
0	1	0	1	0	0	0	0	5	0	0.645
0	1	0	1	0	0	0	1	5	1	0.650
0	1	0	1	0	0	1	0	5	2	0.655
0	1	0	1	0	0	1	1	5	3	0.660
0	1	0	1	0	1	0	0	5	4	0.665
0	1	0	1	0	1	0	1	5	5	0.670
0	1	0	1	0	1	1	0	5	6	0.675
0	1	0	1	0	1	1	1	5	7	0.680
0	1	0	1	1	0	0	0	5	8	0.685
0	1	0	1	1	0	0	1	5	9	0.690
0	1	0	1	1	0	1	0	5	A	0.695
0	1	0	1	1	0	1	1	5	B	0.700
0	1	0	1	1	1	0	0	5	C	0.705
0	1	0	1	1	1	0	1	5	D	0.710
0	1	0	1	1	1	1	0	5	E	0.715
0	1	0	1	1	1	1	1	5	F	0.720
0	1	1	0	0	0	0	0	6	0	0.725
0	1	1	0	0	0	0	1	6	1	0.730
0	1	1	0	0	0	1	0	6	2	0.735
0	1	1	0	0	0	1	1	6	3	0.740
0	1	1	0	0	1	0	0	6	4	0.745
0	1	1	0	0	1	0	1	6	5	0.750
0	1	1	0	0	1	1	0	6	6	0.755
0	1	1	0	0	1	1	1	6	7	0.760
0	1	1	0	1	0	0	0	6	8	0.765
0	1	1	0	1	0	0	1	6	9	0.770

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
0	1	1	0	1	0	1	0	6	A	0.775
0	1	1	0	1	0	1	1	6	B	0.780
0	1	1	0	1	1	0	0	6	C	0.785
0	1	1	0	1	1	0	1	6	D	0.790
0	1	1	0	1	1	1	0	6	E	0.795
0	1	1	0	1	1	1	1	6	F	0.800
0	1	1	1	0	0	0	0	7	0	0.805
0	1	1	1	0	0	0	1	7	1	0.810
0	1	1	1	0	0	1	0	7	2	0.815
0	1	1	1	0	0	1	1	7	3	0.820
0	1	1	1	0	1	0	0	7	4	0.825
0	1	1	1	0	1	0	1	7	5	0.830
0	1	1	1	0	1	1	0	7	6	0.835
0	1	1	1	0	1	1	1	7	7	0.840
0	1	1	1	1	0	0	0	7	8	0.845
0	1	1	1	1	0	0	1	7	9	0.850
0	1	1	1	1	0	1	0	7	A	0.855
0	1	1	1	1	0	1	1	7	B	0.860
0	1	1	1	1	1	0	0	7	C	0.865
0	1	1	1	1	1	0	1	7	D	0.870
0	1	1	1	1	1	1	0	7	E	0.875
0	1	1	1	1	1	1	1	7	F	0.880
1	0	0	0	0	0	0	0	8	0	0.885
1	0	0	0	0	0	0	1	8	1	0.890
1	0	0	0	0	0	1	0	8	2	0.895
1	0	0	0	0	0	1	1	8	3	0.900
1	0	0	0	0	1	0	0	8	4	0.905
1	0	0	0	0	1	0	1	8	5	0.910
1	0	0	0	0	1	1	0	8	6	0.915
1	0	0	0	0	1	1	1	8	7	0.920
1	0	0	0	1	0	0	0	8	8	0.925
1	0	0	0	1	0	0	1	8	9	0.930
1	0	0	0	1	0	1	0	8	A	0.935
1	0	0	0	1	0	1	1	8	B	0.940
1	0	0	0	1	1	0	0	8	C	0.945
1	0	0	0	1	1	0	1	8	D	0.950

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
1	0	0	0	1	1	1	0	8	E	0.955
1	0	0	0	1	1	1	1	8	F	0.960
1	0	0	1	0	0	0	0	9	0	0.965
1	0	0	1	0	0	0	1	9	1	0.970
1	0	0	1	0	0	1	0	9	2	0.975
1	0	0	1	0	0	1	1	9	3	0.980
1	0	0	1	0	1	0	0	9	4	0.985
1	0	0	1	0	1	0	1	9	5	0.990
1	0	0	1	0	1	1	0	9	6	0.995
1	0	0	1	0	1	1	1	9	7	1.000
1	0	0	1	1	0	0	0	9	8	1.005
1	0	0	1	1	0	0	1	9	9	1.010
1	0	0	1	1	0	1	0	9	A	1.015
1	0	0	1	1	0	1	1	9	B	1.020
1	0	0	1	1	1	0	0	9	C	1.025
1	0	0	1	1	1	0	1	9	D	1.030
1	0	0	1	1	1	1	0	9	E	1.035
1	0	0	1	1	1	1	1	9	F	1.040
1	0	1	0	0	0	0	0	A	0	1.045
1	0	1	0	0	0	0	1	A	1	1.050
1	0	1	0	0	0	1	0	A	2	1.055
1	0	1	0	0	0	1	1	A	3	1.060
1	0	1	0	0	1	0	0	A	4	1.065
1	0	1	0	0	1	0	1	A	5	1.070
1	0	1	0	0	1	1	0	A	6	1.075
1	0	1	0	0	1	1	1	A	7	1.080
1	0	1	0	1	0	0	0	A	8	1.085
1	0	1	0	1	0	0	1	A	9	1.090
1	0	1	0	1	0	1	0	A	A	1.095
1	0	1	0	1	0	1	1	A	B	1.100
1	0	1	0	1	1	0	0	A	C	1.105
1	0	1	0	1	1	0	1	A	D	1.110
1	0	1	0	1	1	1	0	A	E	1.115
1	0	1	0	1	1	1	1	A	F	1.120
1	0	1	1	0	0	0	0	B	0	1.125
1	0	1	1	0	0	0	1	B	1	1.130

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
1	0	1	1	0	0	1	0	B	2	1.135
1	0	1	1	0	0	1	1	B	3	1.140
1	0	1	1	0	1	0	0	B	4	1.145
1	0	1	1	0	1	0	1	B	5	1.150
1	0	1	1	0	1	1	0	B	6	1.155
1	0	1	1	0	1	1	1	B	7	1.160
1	0	1	1	1	0	0	0	B	8	1.165
1	0	1	1	1	0	0	1	B	9	1.170
1	0	1	1	1	0	1	0	B	A	1.175
1	0	1	1	1	0	1	1	B	B	1.180
1	0	1	1	1	1	0	0	B	C	1.185
1	0	1	1	1	1	0	1	B	D	1.190
1	0	1	1	1	1	1	0	B	E	1.195
1	0	1	1	1	1	1	1	B	F	1.200
1	1	0	0	0	0	0	0	C	0	1.205
1	1	0	0	0	0	0	1	C	1	1.210
1	1	0	0	0	0	1	0	C	2	1.215
1	1	0	0	0	0	1	1	C	3	1.220
1	1	0	0	0	1	0	0	C	4	1.225
1	1	0	0	0	1	0	1	C	5	1.230
1	1	0	0	0	1	1	0	C	6	1.235
1	1	0	0	0	1	1	1	C	7	1.240
1	1	0	0	1	0	0	0	C	8	1.245
1	1	0	0	1	0	0	1	C	9	1.250
1	1	0	0	1	0	1	0	C	A	1.255
1	1	0	0	1	0	1	1	C	B	1.260
1	1	0	0	1	1	0	0	C	C	1.265
1	1	0	0	1	1	0	1	C	D	1.270
1	1	0	0	1	1	1	0	C	E	1.275
1	1	0	0	1	1	1	1	C	F	1.280
1	1	0	1	0	0	0	0	D	0	1.285
1	1	0	1	0	0	0	1	D	1	1.290
1	1	0	1	0	0	1	0	D	2	1.295
1	1	0	1	0	0	1	1	D	3	1.300
1	1	0	1	0	1	0	0	D	4	1.305
1	1	0	1	0	1	0	1	D	5	1.310

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
1	1	0	1	0	1	1	0	D	6	1.315
1	1	0	1	0	1	1	1	D	7	1.320
1	1	0	1	1	0	0	0	D	8	1.325
1	1	0	1	1	0	0	1	D	9	1.330
1	1	0	1	1	0	1	0	D	A	1.335
1	1	0	1	1	0	1	1	D	B	1.340
1	1	0	1	1	1	0	0	D	C	1.345
1	1	0	1	1	1	0	1	D	D	1.350
1	1	0	1	1	1	1	0	D	E	1.355
1	1	0	1	1	1	1	1	D	F	1.360
1	1	1	0	0	0	0	0	E	0	1.365
1	1	1	0	0	0	0	1	E	1	1.370
1	1	1	0	0	0	1	0	E	2	1.375
1	1	1	0	0	0	1	1	E	3	1.380
1	1	1	0	0	1	0	0	E	4	1.385
1	1	1	0	0	1	0	1	E	5	1.390
1	1	1	0	0	1	1	0	E	6	1.395
1	1	1	0	0	1	1	1	E	7	1.400
1	1	1	0	1	0	0	0	E	8	1.405
1	1	1	0	1	0	0	1	E	9	1.410
1	1	1	0	1	0	1	0	E	A	1.415
1	1	1	0	1	0	1	1	E	B	1.420
1	1	1	0	1	1	0	0	E	C	1.425
1	1	1	0	1	1	0	1	E	D	1.430
1	1	1	0	1	1	1	0	E	E	1.435
1	1	1	0	1	1	1	1	E	F	1.440
1	1	1	1	0	0	0	0	F	0	1.445
1	1	1	1	0	0	0	1	F	1	1.450
1	1	1	1	0	0	1	0	F	2	1.455
1	1	1	1	0	0	1	1	F	3	1.460
1	1	1	1	0	1	0	0	F	4	1.465
1	1	1	1	0	1	0	1	F	5	1.470
1	1	1	1	0	1	1	0	F	6	1.475
1	1	1	1	0	1	1	1	F	7	1.480
1	1	1	1	1	0	0	0	F	8	1.485

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
1	1	1	1	1	0	0	1	F	9	1.490
1	1	1	1	1	0	1	0	F	A	1.495
1	1	1	1	1	0	1	1	F	B	1.500
1	1	1	1	1	1	0	0	F	C	1.505
1	1	1	1	1	1	0	1	F	D	1.510
1	1	1	1	1	1	1	0	F	E	1.515
1	1	1	1	1	1	1	1	F	F	1.520

Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6.5V
- PVCC to GND ---------- –0.3V to 6.5V
- RGNDx to GND ---------- –0.3V to 0.3V
- TONSETx to GND ---------- –0.3V to 28V
- Others ---------- –0.3V to (VCC + 0.3V)
- BOOTx to PHASEx ---------- –0.3V to 6.5V
- PHASEx to GND
  - DC ---------- –0.3V to 28V
  - <20ns ---------- –8V to 32V
- UGATEx to PHASEx
  - DC ---------- –0.3V to (BOOTx – PHASEx)
  - <20ns ---------- –5V to 7.5V
- LGATEx to GND
  - DC ---------- –0.3V to (PVCC – 0.3V)
  - <20ns ---------- –2.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN–48L 6x6 ---------- 2.857W
- Package Thermal Resistance (Note 2)
  - WQFN–48L 6x6, θ_{JA} ---------- 35°C/W
  - WQFN–48L 6x6, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage of Controller, V_{CC} ---------- 4.5V to 5.5V
- Supply Voltage of Gate Driver, V_{PVCC} ---------- 4.5V to 5.5V
- Battery Input Voltage, V_{IN} ---------- 5V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Input Voltage Range	V_{CC}/V_{PVCC}	V_{EN} = 1.05V, Not Switching	4.5	5	5.5	V
	V_{IN}	Battery Input Voltage	5	--	25	V
Supply Current (V_{CC} + PVCC)	I_{VCC} + I_{PVCC}	V_{EN} = 1.05V, Not Switching	--	12	20	mA
Supply Current (TONSETx)	$I_{TONSETx}$	V_{FB} =1V, V_{IN} = 12V, R_{TON} = 100kΩ	--	110	--	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current (PVCC + V_{CC})	I_{VCC_SHDN} + I_{PVCC_SHDN}	V_{EN} = 0V	--	--	5	μA
Shutdown Current (TONSETx)	$I_{TONSETx\_SHDN}$	V_{EN} = 0V	--	--	5	μA
TON Setting						
TONSETx Voltage	$V_{TONSETx}$	I_{RTON} = 80μA, V_{FBx} = 1V	0.95	1.075	1.2	0V
On-Time	t_{ON}	I_{RTON} = 80μA, V_{FBx} = 1V	315	350	385	ns
TONSETx Input Current Range	I_{RTON}	V_{FBx} = 1.1V	25	--	280	μA
Minimum Off-Time	T_{OFF_MIN}		--	350	--	ns
Droop Enable / Disable						
DRPENx Internal Current Source	I_{DRPENx}	EN goes high within 10μs	--	80	--	μA
Droop Enable Threshold	V_{DRPENx}	Detect V_{DRPENx}, EN goes high within 10μs	4.5	--	--	V
Droop Disable Threshold	V_{DRPENx}	Detect V_{DRPENx}, EN goes high within 10μs	--	--	2	
GFX VR Forced DEM						
GFXPS2x Enable Threshold	V_{GFXPS}		4.3	--	--	V
GFXPS2x Disable Threshold	V_{GFXPS}		--	--	0.7	V
References and System Output Voltage						
DAC Accuracy (PS0/PS1)	V_{FBx}	VID_{SVID} Setting = 1.000V~1.520V OFS_{SVID} Setting = 0V	–0.5	0	0.5	%VID
		VID_{SVID} Setting = 0.800V~1.000V OFS_{SVID} Setting = 0V	–5	0	5	mV
		VID_{SVID} Setting = 0.500V~0.800V OFS_{SVID} Setting = 0V	–8	0	8	
		VID_{SVID} Setting = 0.250V~0.500V OFS_{SVID} Setting = 0V	–8	0	8	
		VID_{SVID} Setting = 1.100V OFS_{SVID} Setting = –0.640V~0.635V	–10	0	10	
SETINIx Voltage	$V_{SETINIx}$	V_{INI_CORE} = 0V, V_{INI_GFX} = 0V	0	0.3125	0.5125	V
		V_{INI_CORE} = 0.9V, V_{INI_GFX} = 0.9V	0.7375	0.9375	1.1375	
		V_{INI_CORE} = 1V, V_{INI_GFX} = 1V	1.3625	1.5625	1.7625	
		V_{INI_CORE} = 1.1V, V_{INI_GFX} = 1.1V	2.6125	--	5	
External OFSx Voltage	V_{OFSx}	Offset = 100mV	68	72	--	$\%V_{CC}$
		Offset = 50mV	52	56	60	
		Offset = –50mV	36	40	44	
		Offset = –100mV	20	24	28	
		No Offset Voltage	0	8	12	
Impedance of OFSx Pin	R_{OFSx}		1	--	--	MΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
IBIAS Pin Voltage	V_{IBIAS}	R_{IBIAS} = 53.6kΩ	2.09	2.14	2.19	V
Dynamic VID Slew Rate	SR_{DVID}	SetVID Slow	2.5	3.125	3.75	mV/μs
		SetVID Fast	10	12.5	15	
Error Amplifier						
DC Gain	A_{DC}	R_L = 47kΩ (Note5)	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF (Note5)	--	10	--	MHz
Slew Rate	SR_{COMP}	C_{LOAD} = 10pF (Gain = –4, R_{LOAD_COMP} = 47kΩ, V_{COMPx} = 0.5V to 3V)	--	5	--	V/μs
Output Voltage Range	V_{COMP}	R_L = 47kΩ	0.5	--	3.6	V
MAX Source/Sink Current	I_{COMP}	V_{COMP} = 2V	--	250	--	μA
Impedance of FBx	R_{FBx}		1	--	--	MΩ
Current Sense Amplifier						
Input Offset Voltage	V_{OFS_CSA}		–1	--	1	mV
Impedance of Neg. Input	R_{ISENxN}		1	--	--	MΩ
Impedance of Pos. Input	R_{ISENxP}		1	--	--	MΩ
Current Sense Differential Input Range	V_{CSDIx}	V_{FBx} = 1.1V, $V_{CSDIx} = V_{ISENxP} - V_{ISENxN}$	–50	--	100	mV
Current Sense DC Gain (Loop)	A_I	V_{FBx} = 1.1V, –30mV < V_{CSDIx} < 50mV	--	10	--	V/V
V_{ISEN} Linearity	V_{ISEN_ACC}	V_{DAC} = 1.1V –30mV < V_{ISEN_IN} < 50mV	–1	--	1	%
Digital Current Monitor						
Current Monitor Output Voltage (Droop Enabled)	V_{IMONx_ENLL}	V_{FBx} = 1V, V_{ISENxN} = 0.9V, $V_{RIMONFBx}$ = 10k, R_{IMONx} = 160k	--	1.6	--	V
Current Monitor Output Voltage (Droop Disabled)	V_{IMONx_DISLL}	$V_{CSDIx} = V_{ISENxP} - V_{ISENxN}$ = 100mV V_{FBx} = 1V, $V_{RIMONFBx}$ = 10k, R_{IMONx} = 80k	--	1.6	--	V
IMON Voltage Range	V_{IMON}		0	--	3.3	V
Digital IMON LSB		3.3V / 255 = 12.94mV	--	12.94	--	mV
Digital Code of IMON	C_{DIMON}	V_{IMONx} = 388.3mV, DIOUT [7 : 0] = 30	27	30	33	Decimal
		V_{IMONx} = 776.5mV, DIOUT [7 : 0] = 60	57	60	63	Decimal
		V_{IMONx} = 1164.7mV, DIOUT [7 : 0] = 90	87	90	93	Decimal
Update Period of Digital Current Monitor	t_{IMON}		--	1600	--	μs
Gate Driver						
Upper Driver Source	R_{UGATEx_sr}	$V_{BOOTx} - V_{PHASEx}$ = 5V $V_{BOOTx} - V_{UGATEx}$ = 0.1V	--	1	--	Ω
Upper Driver Sink	R_{UGATEx_sk}	V_{UGATEx} = 0.1V	--	1	--	Ω
Lower Driver Source	R_{LGATEx_sr}	PVCC = 5V, PVCC – V_{LGATEx} = 0.1V	--	1	--	Ω
Lower Driver Sink	R_{LGATEx_sk}	V_{LGATEx} = 0.1V	--	0.5	--	Ω
Internal Boot Charging Switch On-Resistance	R_{BOOTx}	PVCC to BOOTx	--	30	--	Ω

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Zero Current Detection Threshold		V_{ZCD_TH}	V_{ZCD_TH} = GND − V_{PHASEx}	--	10	--	mV
Protection							
Under Voltage Lock-out Threshold		V_{UVLO}	VCC Falling edge	4.04	4.24	--	V
Under Voltage Lock-out Hysteresis		ΔV_{UVLO}		--	100	--	mV
Over Voltage Protection Threshold		V_{OVP}	Respect to $VOUT\_MAX_{SVID}$, with 1μs filter time	100	150	200	mV
Under Voltage Protection Threshold		V_{UVP}	V_{UVP} = V_{ISENxN} − V_{REFx}, 0.8V < V_{REFx} <1.52V, with 3μs filter time	−350	−300	−250	mV
Negative Voltage Protection Threshold		V_{NVP}	V_{NVP} = V_{ISENxN} − GND	−100	−50	--	mV
Current Sense Gain for Over Current Protection		A_{OC}	V_{OCSET} = 2.4V V_{ISENxP} − V_{ISENxN} = 50mV	--	48	--	V/V
Logic Inputs							
EN Input Threshold Voltage	Logic-High	V_{IH}	With respect to 1V, 70%	0.7	--	--	V
	Logic-Low	V_{IL}	With respect to 1V, 30%	--	--	0.3	V
Leakage Current of EN				−1	--	1	μA
VCLK,VDIO Input Threshold Voltage		V_{IH}	With respect to Intel Spec.	0.65	--	--	V
		V_{IL}	With respect to Intel Spec.	--	--	0.45	V
Leakage Current of VCLK, VDIO		I_{LEAK_IN}		−1	--	1	μA
$\overline{ALERT}$							
$\overline{ALERT}$ Low Voltage		$V_{\overline{ALERT}}$	$I_{\overline{ALERT}\_SINK}$ = 4mA	--	--	0.4	V
VR Ready							
VRx_READY Low Voltage		V_{VRx_READY}	$I_{VRx\_READY\_SINK}$ = 4mA	--	--	0.4	V
VRx_READY Delay		t_{VRx_READY}	V_{ISENxN} = V_{BOOT} to V_{VRx_READY} high	70	100	160	μs
Thermal Throttling							
$\overline{VRHOT}$ Output Voltage		$V_{\overline{VRHOT}}$	$I_{\overline{VRHOT}\_SINK}$ = 40mA	--	0.4	--	V
High Impedance Output							
$\overline{ALERT}$, VRx_READY, $\overline{VRHOT}$		I_{LEAK_OUT}		−1	--	1	μA
Temperature Zone							
TSEN Threshold for Tmp_Zone [7] transition		V_{TSENx}	100°C	--	1.8725	--	V
TSEN Threshold for Tmp_Zone [6] transition			97°C	--	1.8175	--	V
TSEN Threshold for Tmp_Zone [5] transition			94°C	--	1.7625	--	V
TSEN Threshold for Tmp_Zone [4] transition			91°C	--	1.7075	--	V
TSEN Threshold for Tmp_Zone [3] transition			88°C	--	1.6525	--	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TSEN Threshold for Tmp_Zone [2] transition	V_{TSENx}	85°C	--	1.5975	--	V
TSEN Threshold for Tmp_Zone [1] transition		82°C	--	1.5425	--	V
TSEN Threshold for Tmp_Zone [0] transition		75°C	--	1.4875	--	V
Update Period	t_{TSEN}		--	1600	--	μs
ADC						
Latency	t_{LAT}		--	--	400	μs
Digital Code of ICCMAX	$C_{ICCMAX1}$	V_{ICCMAX} = 0.637V	29	32	35	decimal
	$C_{ICCMAX2}$	V_{ICCMAX} = 1.2642V	61	64	67	decimal
	$C_{ICCMAX3}$	V_{ICCMAX} = 2.5186V	125	128	131	decimal
Digital Code of ICCMAXA	$C_{ICCMAXA1}$	$V_{ICCMAXA}$ = 0.1666V	5	8	11	decimal
	$C_{ICCMAXA2}$	$V_{ICCMAXA}$ = 0.3234V	13	16	19	decimal
	$C_{ICCMAXA3}$	$V_{ICCMAXA}$ = 0.637V	29	32	35	decimal
Digital Code of TMPMAX	$C_{TMPMAX1}$	V_{TMPMAX} = 1.6758V	82	85	88	decimal
	$C_{TMPMAX2}$	V_{TMPMAX} = 1.9698V	97	100	103	decimal
	$C_{TMPMAX3}$	V_{TMPMAX} = 2.4598V	122	125	128	decimal

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

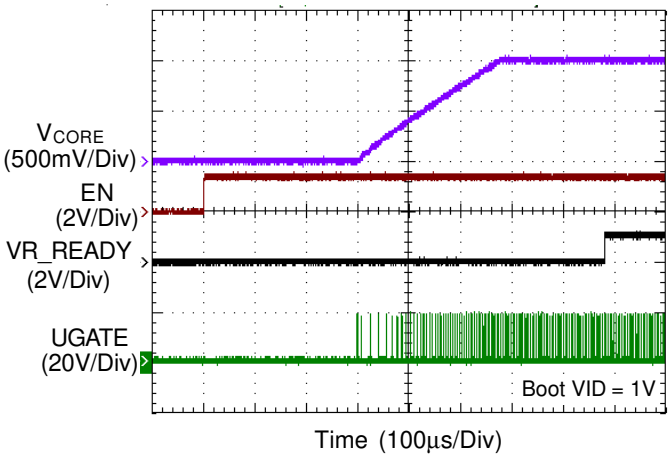
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

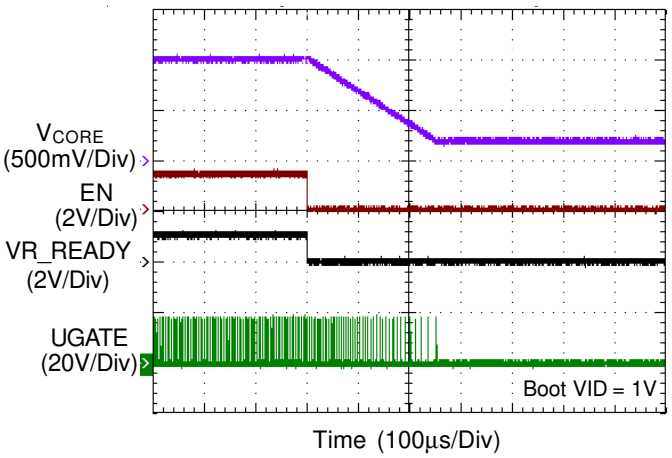
Note 5. Guaranteed by design.

Typical Operating Characteristics

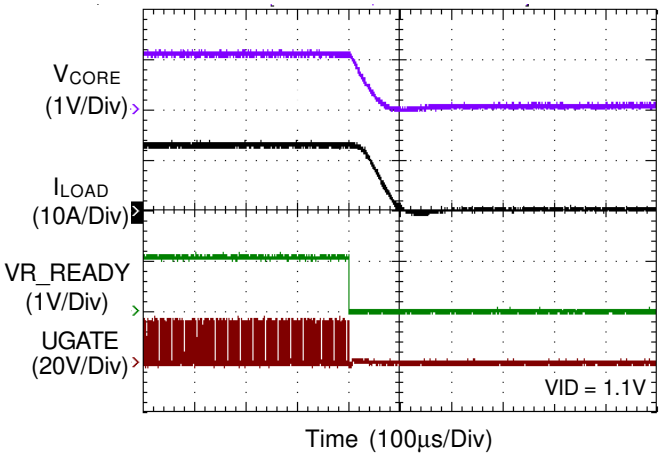
CORE VR Power On from EN



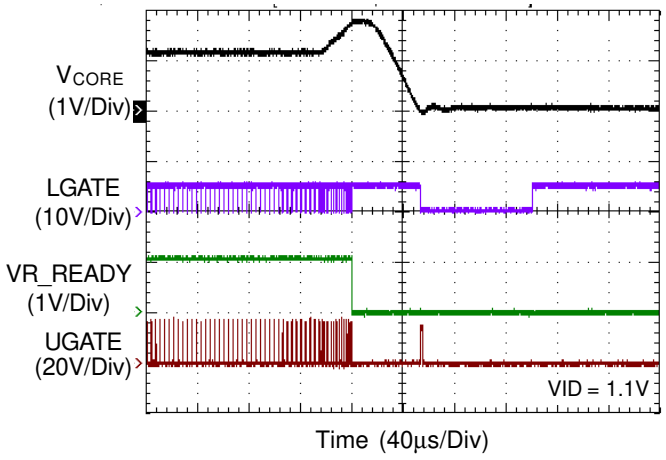
CORE VR Power Off from EN



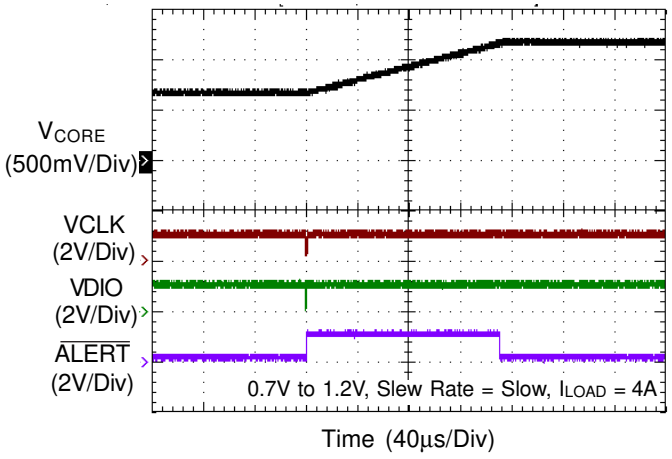
CORE VR OCP



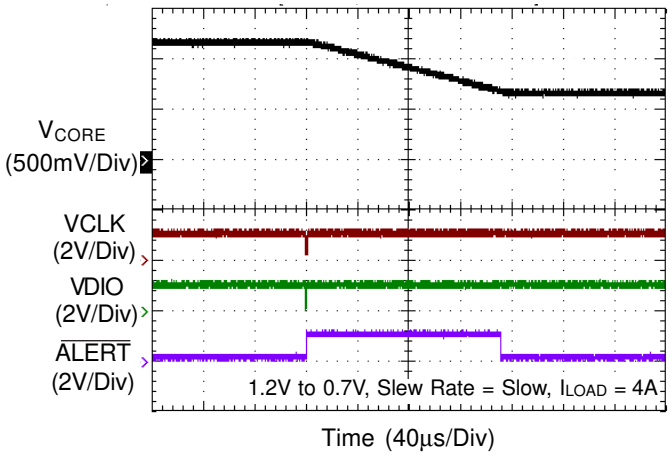
CORE VR OVP and NVP



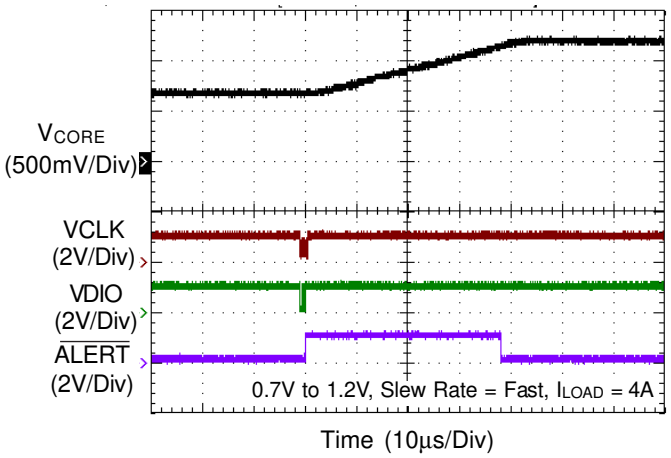
CORE VR Dynamic VID Up



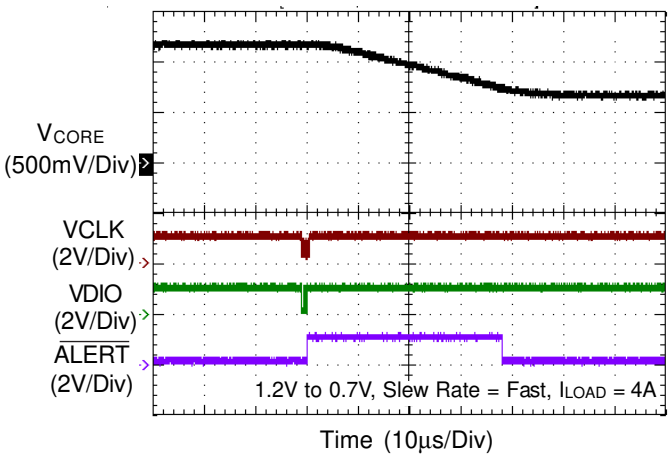
CORE VR Dynamic VID Down



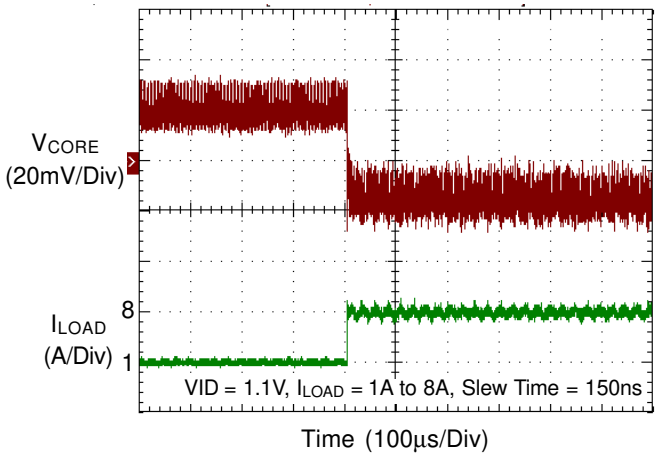
CORE VR Dynamic VID Up



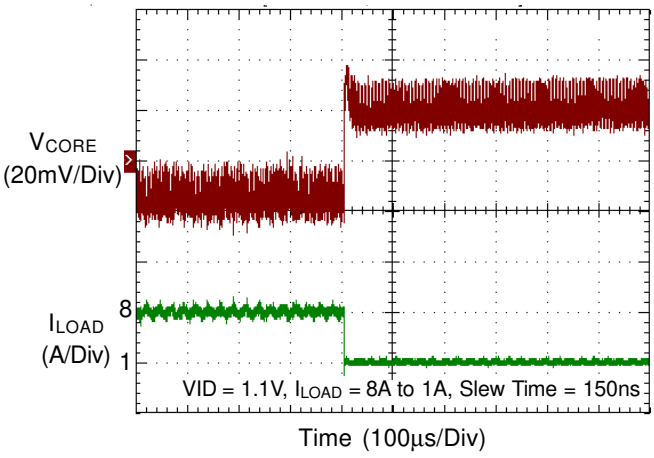
CORE VR Dynamic VID Down



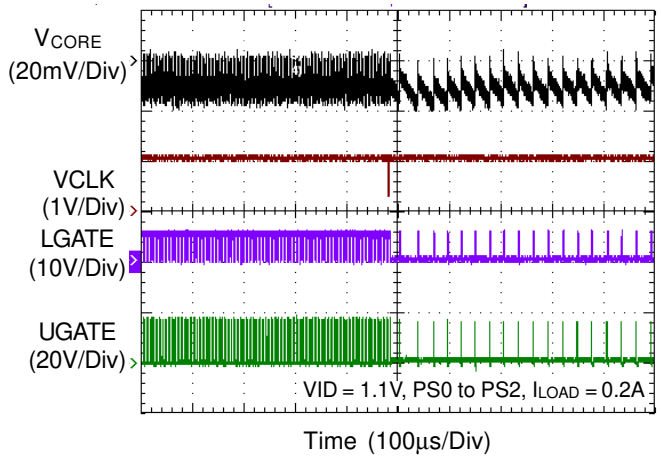
CORE VR Load Transient



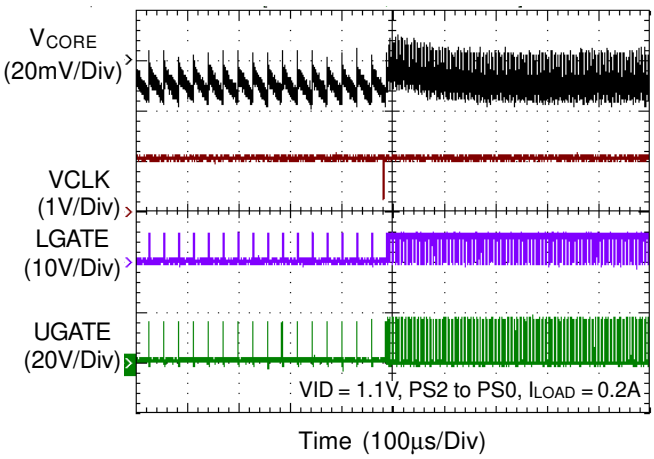
CORE VR Load Transient



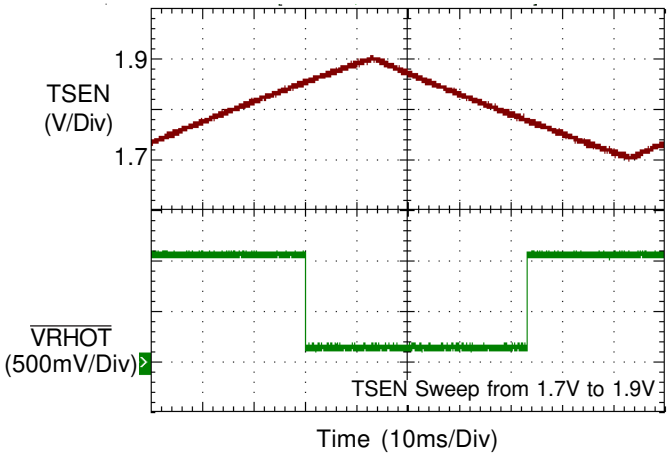
CORE VR Mode Transition



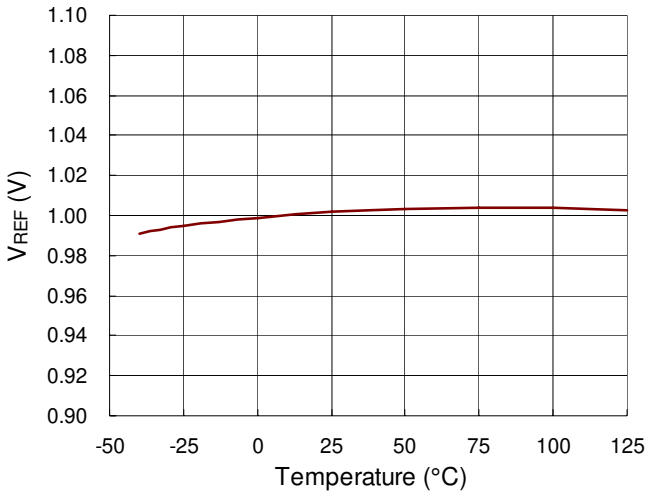
CORE VR Mode Transition



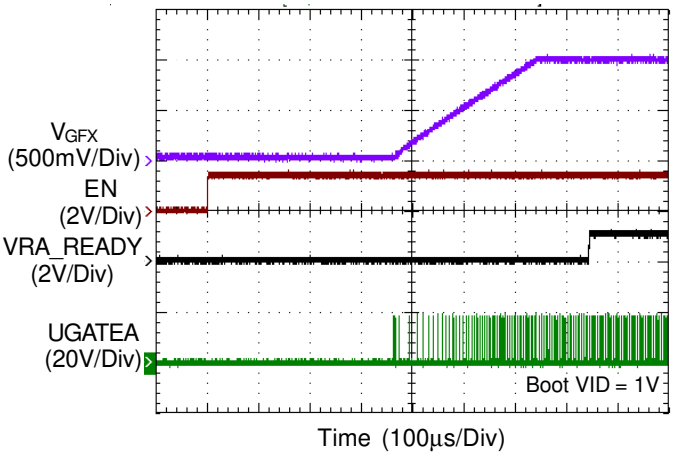
CORE VR Thermal Monitoring



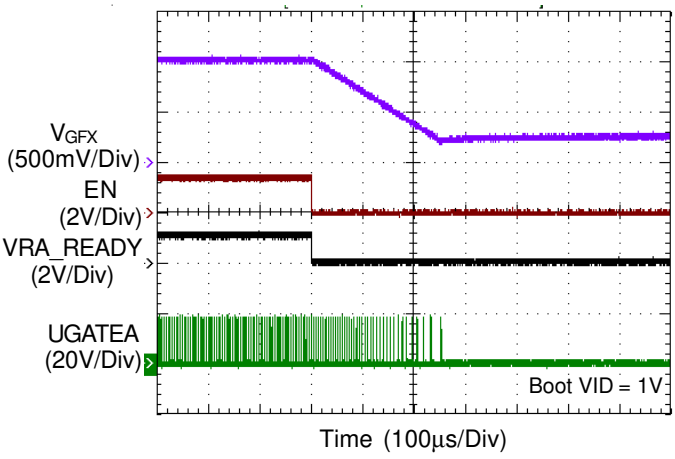
CORE VR V_{REF} vs. Temperature



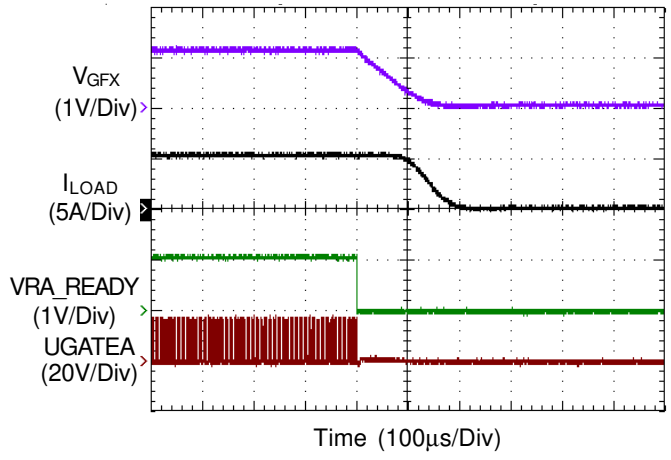
GFX VR Power On from EN



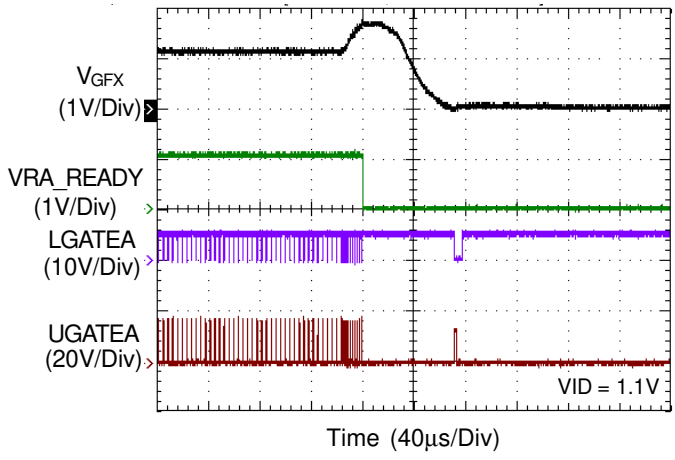
GFX VR Power Off from EN



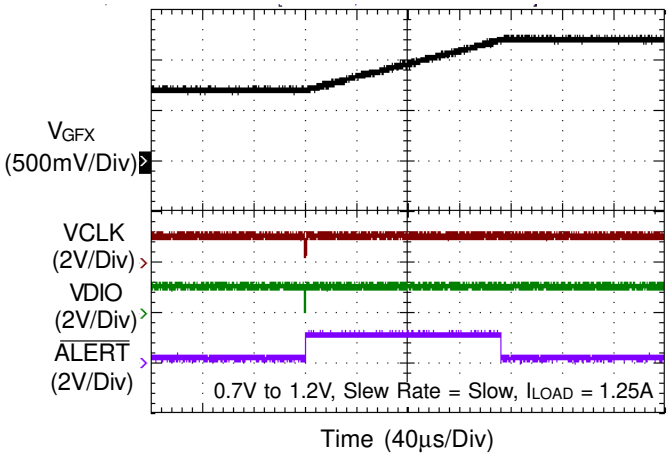
GFX VR OCP



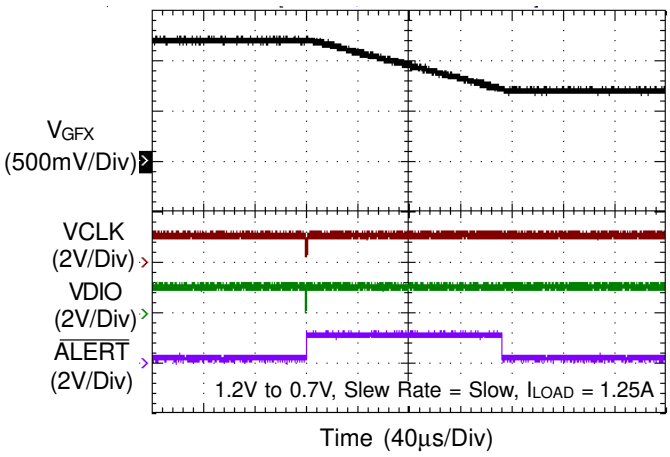
GFX VR OVP and NVP



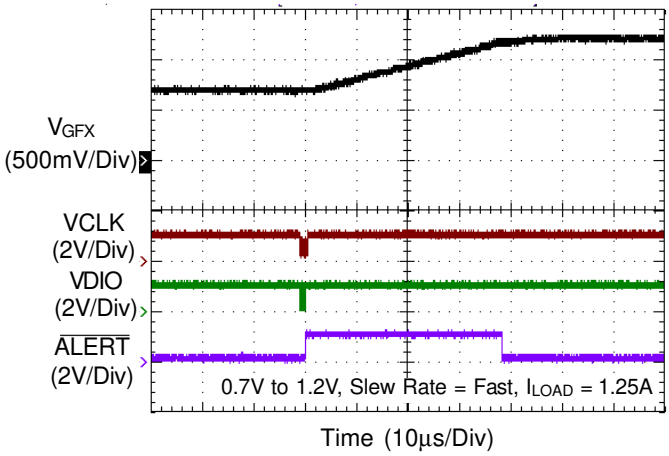
GFX VR Dynamic VID



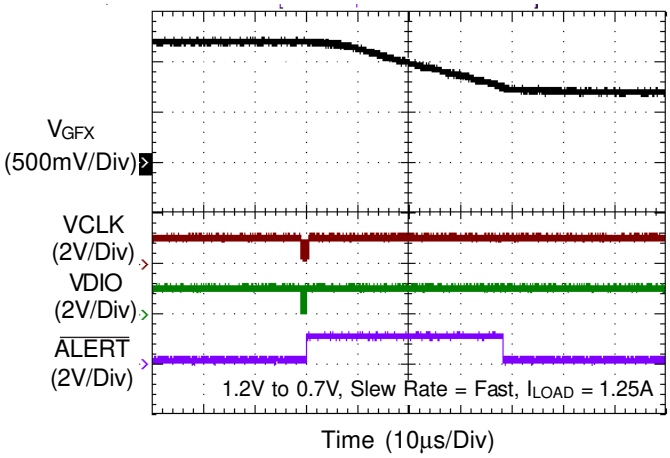
GFX VR Dynamic VID



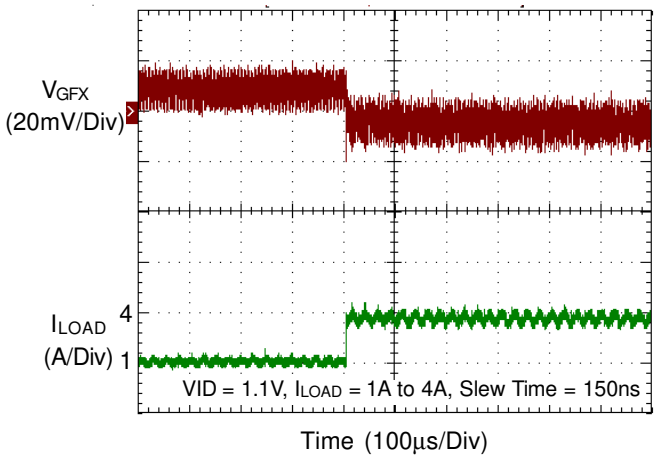
GFX VR Dynamic VID



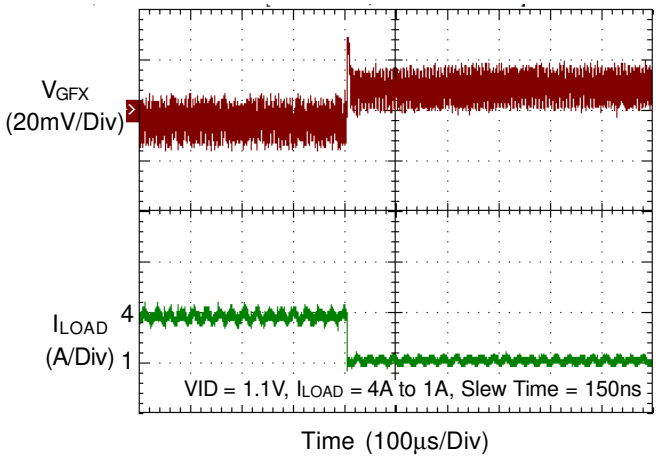
GFX VR Dynamic VID



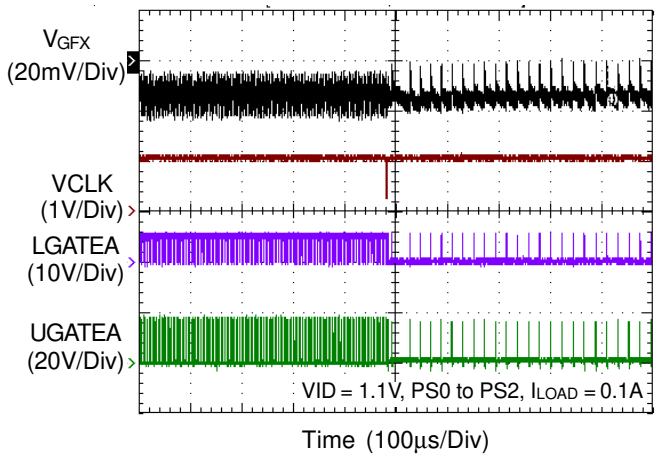
GFX VR Load Transient



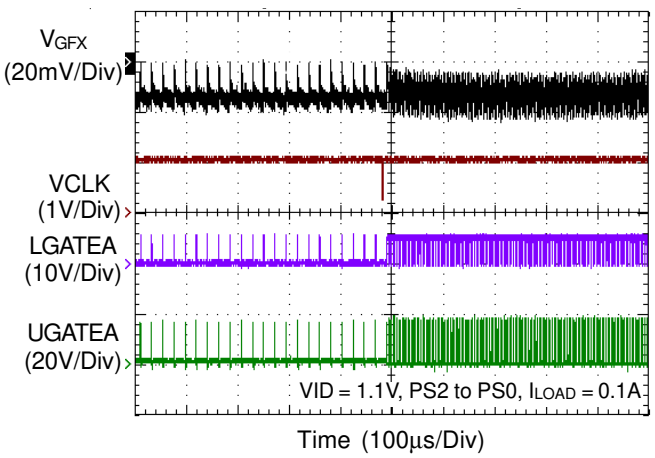
GFX VR Load Transient



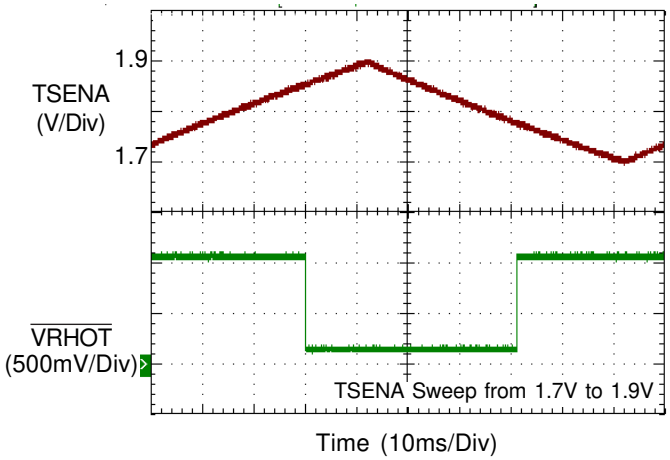
GFX VR Mode Transition



GFX VR Mode Transition



GFX VR Thermal Monitoring



GFX VR V_{REF} vs. Temperature