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Dual Single-Phase PWM Controller for CPU and GPU Core Power Supply

General Description

The RT8168B is a dual single-phase PWM controller with integrated MOSFET drivers, compliant with Intel IMVP7 Pulse Width Modulation Specification to support both CPU core and GPU core power. This part adopts G-NAVP™ (Green-Native AVP), which is a Richtek proprietary topology derived from finite DC gain compensator in constant on-time control mode. G-NAVP™ makes this part an easy setting PWM controller to meet all Intel AVP (Active Voltage Positioning) mobile CPU/GPU requirements. The RT8168B uses SVID interface to control an 8-bit DAC for output voltage programming. The built-in high accuracy DAC converts the received VID code into a voltage value ranging from 0V to 1.52V with 5mV step voltage. The system accuracy of the controller can reach 0.8%. The RT8168B operates in continuous conduction mode or diode emulation mode, according to the SVID command. The maximum efficiency can reach up to 90% in different operating modes according to different load conditions. The droop function (load line) can be easily programmed by setting the DC gain of the error amplifier. With proper compensation, the load transient response can achieve optimized AVP performance.

The output voltage transition slew rate is set via the SVID interface. The RT8168B supports both DCR and sense resistor current sensing. The RT8168B provides VR_READY and thermal throttling output signals for IMVP7 CPU and GPU core. This part also features complete fault protection functions including over voltage, under voltage, negative voltage, over current and thermal shutdown.

The RT8168B is available in a WQFN-40L 5x5 small footprint package.

Features

- **Dual Single-Phase PWM Controller for CPU Core and GPU Core Power**
- **IMVP7 Compatible Power Management States**
- **Serial VID Interface**
- **G-NAVP™ Topology**
- **AVP for CPU VR Only**
- **0.5% DAC Accuracy**
- **0.8% System Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-in ADC for Platform Programming**
  - **SETINI/SETINIA for CPU/GPU Core VR Initial Startup Voltage**
  - **TMPMAX to Set Platform Maximum Temperature**
  - **ICCMAX/ICCMAXA for CPU/GPU Core VR Maximum Current**
- **Power Good Indicator : VR_READY/VRA_READY for CPU/GPU Core Power**
- **Thermal Throttling Indicator : $\overline{\text{VRHOT}}$**
- **Diode Emulation Mode at Light Load Condition**
- **Fast Line/Load Transient Response**
- **Switching Frequency up to 1MHz per Phase**
- **OVP, UVP, NVP, OTP, UVLO, OCP**
- **Small 40-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Applications

- IMVP7 Intel CPU/GPU Core Power Supply
- Laptop Computers
- AVP Step-Down Converter

Ordering Information

RT8168B□□

- Package Type
  QW : WQFN-40L 5x5 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

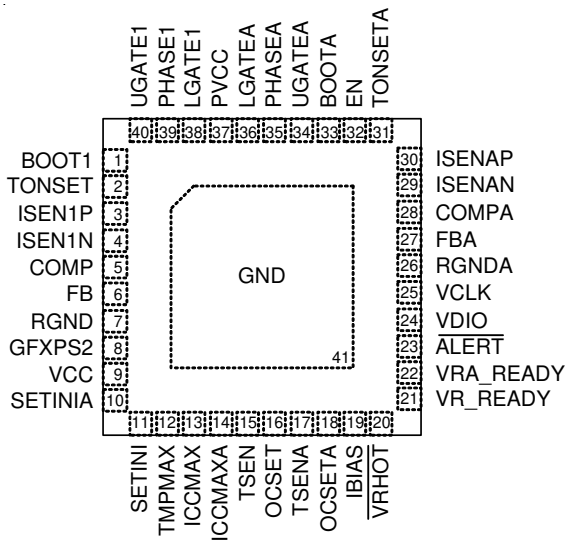
Marking Information

RT8168BGQW : Product Number

YMDNN : Date Code

Pin Configurations

(TOP VIEW)



WQFN-40L 5x5

Typical Application Circuit

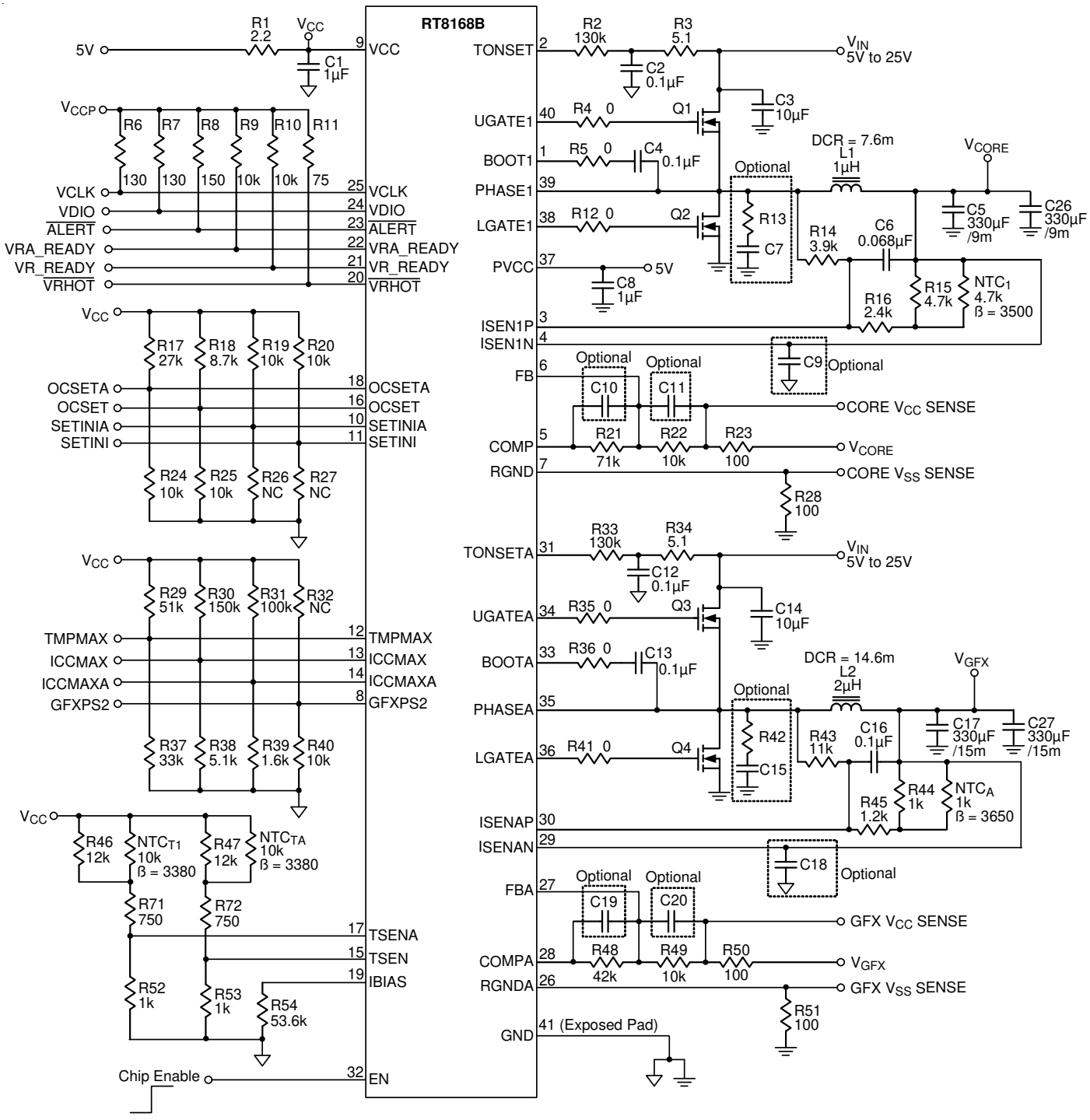


Table 1. IMVP7/VR12 Compliant VID Table

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	VDAC Voltage
0	0	0	0	0	0	0	0	0	0	0.000
0	0	0	0	0	0	0	1	0	1	0.250
0	0	0	0	0	0	1	0	0	2	0.255
0	0	0	0	0	0	1	1	0	3	0.260
0	0	0	0	0	1	0	0	0	4	0.265
0	0	0	0	0	1	0	1	0	5	0.270
0	0	0	0	0	1	1	0	0	6	0.275
0	0	0	0	0	1	1	1	0	7	0.280
0	0	0	0	1	0	0	0	0	8	0.285
0	0	0	0	1	0	0	1	0	9	0.290
0	0	0	0	1	0	1	0	0	A	0.295
0	0	0	0	1	0	1	1	0	B	0.300
0	0	0	0	1	1	0	0	0	C	0.305
0	0	0	0	1	1	0	1	0	D	0.310
0	0	0	0	1	1	1	0	0	E	0.315
0	0	0	0	1	1	1	1	0	F	0.320
0	0	0	1	0	0	0	0	1	0	0.325
0	0	0	1	0	0	0	1	1	1	0.330
0	0	0	1	0	0	1	0	1	2	0.335
0	0	0	1	0	0	1	1	1	3	0.340
0	0	0	1	0	1	0	0	1	4	0.345
0	0	0	1	0	1	0	1	1	5	0.350
0	0	0	1	0	1	1	0	1	6	0.355
0	0	0	1	0	1	1	1	1	7	0.360
0	0	0	1	1	0	0	0	1	8	0.365
0	0	0	1	1	0	0	1	1	9	0.370
0	0	0	1	1	0	1	0	1	A	0.375
0	0	0	1	1	0	1	1	1	B	0.380
0	0	0	1	1	1	0	0	1	C	0.385
0	0	0	1	1	1	0	1	1	D	0.390
0	0	0	1	1	1	1	0	1	E	0.395
0	0	0	1	1	1	1	1	1	F	0.400
0	0	1	0	0	0	0	0	2	0	0.405
0	0	1	0	0	0	0	1	2	1	0.410
0	0	1	0	0	0	1	0	2	2	0.415

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
0	0	1	0	0	0	1	1	2	3	0.420
0	0	1	0	0	1	0	0	2	4	0.425
0	0	1	0	0	1	0	1	2	5	0.430
0	0	1	0	0	1	1	0	2	6	0.435
0	0	1	0	0	1	1	1	2	7	0.440
0	0	1	0	1	0	0	0	2	8	0.445
0	0	1	0	1	0	0	1	2	9	0.450
0	0	1	0	1	0	1	0	2	A	0.455
0	0	1	0	1	0	1	1	2	B	0.460
0	0	1	0	1	1	0	0	2	C	0.465
0	0	1	0	1	1	0	1	2	D	0.470
0	0	1	0	1	1	1	0	2	E	0.475
0	0	1	0	1	1	1	1	2	F	0.480
0	0	1	1	0	0	0	0	3	0	0.485
0	0	1	1	0	0	0	1	3	1	0.490
0	0	1	1	0	0	1	0	3	2	0.495
0	0	1	1	0	0	1	1	3	3	0.500
0	0	1	1	0	1	0	0	3	4	0.505
0	0	1	1	0	1	0	1	3	5	0.510
0	0	1	1	0	1	1	0	3	6	0.515
0	0	1	1	0	1	1	1	3	7	0.520
0	0	1	1	1	0	0	0	3	8	0.525
0	0	1	1	1	0	0	1	3	9	0.530
0	0	1	1	1	0	1	0	3	A	0.535
0	0	1	1	1	0	1	1	3	B	0.540
0	0	1	1	1	1	0	0	3	C	0.545
0	0	1	1	1	1	0	1	3	D	0.550
0	0	1	1	1	1	1	0	3	E	0.555
0	0	1	1	1	1	1	1	3	F	0.560
0	1	0	0	0	0	0	0	4	0	0.565
0	1	0	0	0	0	0	1	4	1	0.570
0	1	0	0	0	0	1	0	4	2	0.575
0	1	0	0	0	0	1	1	4	3	0.580
0	1	0	0	0	1	0	0	4	4	0.585
0	1	0	0	0	1	0	1	4	5	0.590

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
0	1	0	0	0	1	1	0	4	6	0.595
0	1	0	0	0	1	1	1	4	7	0.600
0	1	0	0	1	0	0	0	4	8	0.605
0	1	0	0	1	0	0	1	4	9	0.610
0	1	0	0	1	0	1	0	4	A	0.615
0	1	0	0	1	0	1	1	4	B	0.620
0	1	0	0	1	1	0	0	4	C	0.625
0	1	0	0	1	1	0	1	4	D	0.630
0	1	0	0	1	1	1	0	4	E	0.635
0	1	0	0	1	1	1	1	4	F	0.640
0	1	0	1	0	0	0	0	5	0	0.645
0	1	0	1	0	0	0	1	5	1	0.650
0	1	0	1	0	0	1	0	5	2	0.655
0	1	0	1	0	0	1	1	5	3	0.660
0	1	0	1	0	1	0	0	5	4	0.665
0	1	0	1	0	1	0	1	5	5	0.670
0	1	0	1	0	1	1	0	5	6	0.675
0	1	0	1	0	1	1	1	5	7	0.680
0	1	0	1	1	0	0	0	5	8	0.685
0	1	0	1	1	0	0	1	5	9	0.690
0	1	0	1	1	0	1	0	5	A	0.695
0	1	0	1	1	0	1	1	5	B	0.700
0	1	0	1	1	1	0	0	5	C	0.705
0	1	0	1	1	1	0	1	5	D	0.710
0	1	0	1	1	1	1	0	5	E	0.715
0	1	0	1	1	1	1	1	5	F	0.720
0	1	1	0	0	0	0	0	6	0	0.725
0	1	1	0	0	0	0	1	6	1	0.730
0	1	1	0	0	0	1	0	6	2	0.735
0	1	1	0	0	0	1	1	6	3	0.740
0	1	1	0	0	1	0	0	6	4	0.745
0	1	1	0	0	1	0	1	6	5	0.750
0	1	1	0	0	1	1	0	6	6	0.755
0	1	1	0	0	1	1	1	6	7	0.760
0	1	1	0	1	0	0	0	6	8	0.765
0	1	1	0	1	0	0	1	6	9	0.770

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
0	1	1	0	1	0	1	0	6	A	0.775
0	1	1	0	1	0	1	1	6	B	0.780
0	1	1	0	1	1	0	0	6	C	0.785
0	1	1	0	1	1	0	1	6	D	0.790
0	1	1	0	1	1	1	0	6	E	0.795
0	1	1	0	1	1	1	1	6	F	0.800
0	1	1	1	0	0	0	0	7	0	0.805
0	1	1	1	0	0	0	1	7	1	0.810
0	1	1	1	0	0	1	0	7	2	0.815
0	1	1	1	0	0	1	1	7	3	0.820
0	1	1	1	0	1	0	0	7	4	0.825
0	1	1	1	0	1	0	1	7	5	0.830
0	1	1	1	0	1	1	0	7	6	0.835
0	1	1	1	0	1	1	1	7	7	0.840
0	1	1	1	1	0	0	0	7	8	0.845
0	1	1	1	1	0	0	1	7	9	0.850
0	1	1	1	1	0	1	0	7	A	0.855
0	1	1	1	1	0	1	1	7	B	0.860
0	1	1	1	1	1	0	0	7	C	0.865
0	1	1	1	1	1	0	1	7	D	0.870
0	1	1	1	1	1	1	0	7	E	0.875
0	1	1	1	1	1	1	1	7	F	0.880
1	0	0	0	0	0	0	0	8	0	0.885
1	0	0	0	0	0	0	1	8	1	0.890
1	0	0	0	0	0	1	0	8	2	0.895
1	0	0	0	0	0	1	1	8	3	0.900
1	0	0	0	0	1	0	0	8	4	0.905
1	0	0	0	0	1	0	1	8	5	0.910
1	0	0	0	0	1	1	0	8	6	0.915
1	0	0	0	0	1	1	1	8	7	0.920
1	0	0	0	1	0	0	0	8	8	0.925
1	0	0	0	1	0	0	1	8	9	0.930
1	0	0	0	1	0	1	0	8	A	0.935
1	0	0	0	1	0	1	1	8	B	0.940
1	0	0	0	1	1	0	0	8	C	0.945
1	0	0	0	1	1	0	1	8	D	0.950

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
1	0	0	0	1	1	1	0	8	E	0.955
1	0	0	0	1	1	1	1	8	F	0.960
1	0	0	1	0	0	0	0	9	0	0.965
1	0	0	1	0	0	0	1	9	1	0.970
1	0	0	1	0	0	1	0	9	2	0.975
1	0	0	1	0	0	1	1	9	3	0.980
1	0	0	1	0	1	0	0	9	4	0.985
1	0	0	1	0	1	0	1	9	5	0.990
1	0	0	1	0	1	1	0	9	6	0.995
1	0	0	1	0	1	1	1	9	7	1.000
1	0	0	1	1	0	0	0	9	8	1.005
1	0	0	1	1	0	0	1	9	9	1.010
1	0	0	1	1	0	1	0	9	A	1.015
1	0	0	1	1	0	1	1	9	B	1.020
1	0	0	1	1	1	0	0	9	C	1.025
1	0	0	1	1	1	0	1	9	D	1.030
1	0	0	1	1	1	1	0	9	E	1.035
1	0	0	1	1	1	1	1	9	F	1.040
1	0	1	0	0	0	0	0	A	0	1.045
1	0	1	0	0	0	0	1	A	1	1.050
1	0	1	0	0	0	1	0	A	2	1.055
1	0	1	0	0	0	1	1	A	3	1.060
1	0	1	0	0	1	0	0	A	4	1.065
1	0	1	0	0	1	0	1	A	5	1.070
1	0	1	0	0	1	1	0	A	6	1.075
1	0	1	0	0	1	1	1	A	7	1.080
1	0	1	0	1	0	0	0	A	8	1.085
1	0	1	0	1	0	0	1	A	9	1.090
1	0	1	0	1	0	1	0	A	A	1.095
1	0	1	0	1	0	1	1	A	B	1.100
1	0	1	0	1	1	0	0	A	C	1.105
1	0	1	0	1	1	0	1	A	D	1.110
1	0	1	0	1	1	1	0	A	E	1.115
1	0	1	0	1	1	1	1	A	F	1.120
1	0	1	1	0	0	0	0	B	0	1.125
1	0	1	1	0	0	0	1	B	1	1.130

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
1	0	1	1	0	0	1	0	B	2	1.135
1	0	1	1	0	0	1	1	B	3	1.140
1	0	1	1	0	1	0	0	B	4	1.145
1	0	1	1	0	1	0	1	B	5	1.150
1	0	1	1	0	1	1	0	B	6	1.155
1	0	1	1	0	1	1	1	B	7	1.160
1	0	1	1	1	0	0	0	B	8	1.165
1	0	1	1	1	0	0	1	B	9	1.170
1	0	1	1	1	0	1	0	B	A	1.175
1	0	1	1	1	0	1	1	B	B	1.180
1	0	1	1	1	1	0	0	B	C	1.185
1	0	1	1	1	1	0	1	B	D	1.190
1	0	1	1	1	1	1	0	B	E	1.195
1	0	1	1	1	1	1	1	B	F	1.200
1	1	0	0	0	0	0	0	C	0	1.205
1	1	0	0	0	0	0	1	C	1	1.210
1	1	0	0	0	0	1	0	C	2	1.215
1	1	0	0	0	0	1	1	C	3	1.220
1	1	0	0	0	1	0	0	C	4	1.225
1	1	0	0	0	1	0	1	C	5	1.230
1	1	0	0	0	1	1	0	C	6	1.235
1	1	0	0	0	1	1	1	C	7	1.240
1	1	0	0	1	0	0	0	C	8	1.245
1	1	0	0	1	0	0	1	C	9	1.250
1	1	0	0	1	0	1	0	C	A	1.255
1	1	0	0	1	0	1	1	C	B	1.260
1	1	0	0	1	1	0	0	C	C	1.265
1	1	0	0	1	1	0	1	C	D	1.270
1	1	0	0	1	1	1	0	C	E	1.275
1	1	0	0	1	1	1	1	C	F	1.280
1	1	0	1	0	0	0	0	D	0	1.285
1	1	0	1	0	0	0	1	D	1	1.290
1	1	0	1	0	0	1	0	D	2	1.295
1	1	0	1	0	0	1	1	D	3	1.300
1	1	0	1	0	1	0	0	D	4	1.305
1	1	0	1	0	1	0	1	D	5	1.310

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
1	1	0	1	0	1	1	0	D	6	1.315
1	1	0	1	0	1	1	1	D	7	1.320
1	1	0	1	1	0	0	0	D	8	1.325
1	1	0	1	1	0	0	1	D	9	1.330
1	1	0	1	1	0	1	0	D	A	1.335
1	1	0	1	1	0	1	1	D	B	1.340
1	1	0	1	1	1	0	0	D	C	1.345
1	1	0	1	1	1	0	1	D	D	1.350
1	1	0	1	1	1	1	0	D	E	1.355
1	1	0	1	1	1	1	1	D	F	1.360
1	1	1	0	0	0	0	0	E	0	1.365
1	1	1	0	0	0	0	1	E	1	1.370
1	1	1	0	0	0	1	0	E	2	1.375
1	1	1	0	0	0	1	1	E	3	1.380
1	1	1	0	0	1	0	0	E	4	1.385
1	1	1	0	0	1	0	1	E	5	1.390
1	1	1	0	0	1	1	0	E	6	1.395
1	1	1	0	0	1	1	1	E	7	1.400
1	1	1	0	1	0	0	0	E	8	1.405
1	1	1	0	1	0	0	1	E	9	1.410
1	1	1	0	1	0	1	0	E	A	1.415
1	1	1	0	1	0	1	1	E	B	1.420
1	1	1	0	1	1	0	0	E	C	1.425
1	1	1	0	1	1	0	1	E	D	1.430
1	1	1	0	1	1	1	0	E	E	1.435
1	1	1	0	1	1	1	1	E	F	1.440
1	1	1	1	0	0	0	0	F	0	1.445
1	1	1	1	0	0	0	1	F	1	1.450
1	1	1	1	0	0	1	0	F	2	1.455
1	1	1	1	0	0	1	1	F	3	1.460
1	1	1	1	0	1	0	0	F	4	1.465
1	1	1	1	0	1	0	1	F	5	1.470
1	1	1	1	0	1	1	0	F	6	1.475
1	1	1	1	0	1	1	1	F	7	1.480
1	1	1	1	1	0	0	0	F	8	1.485

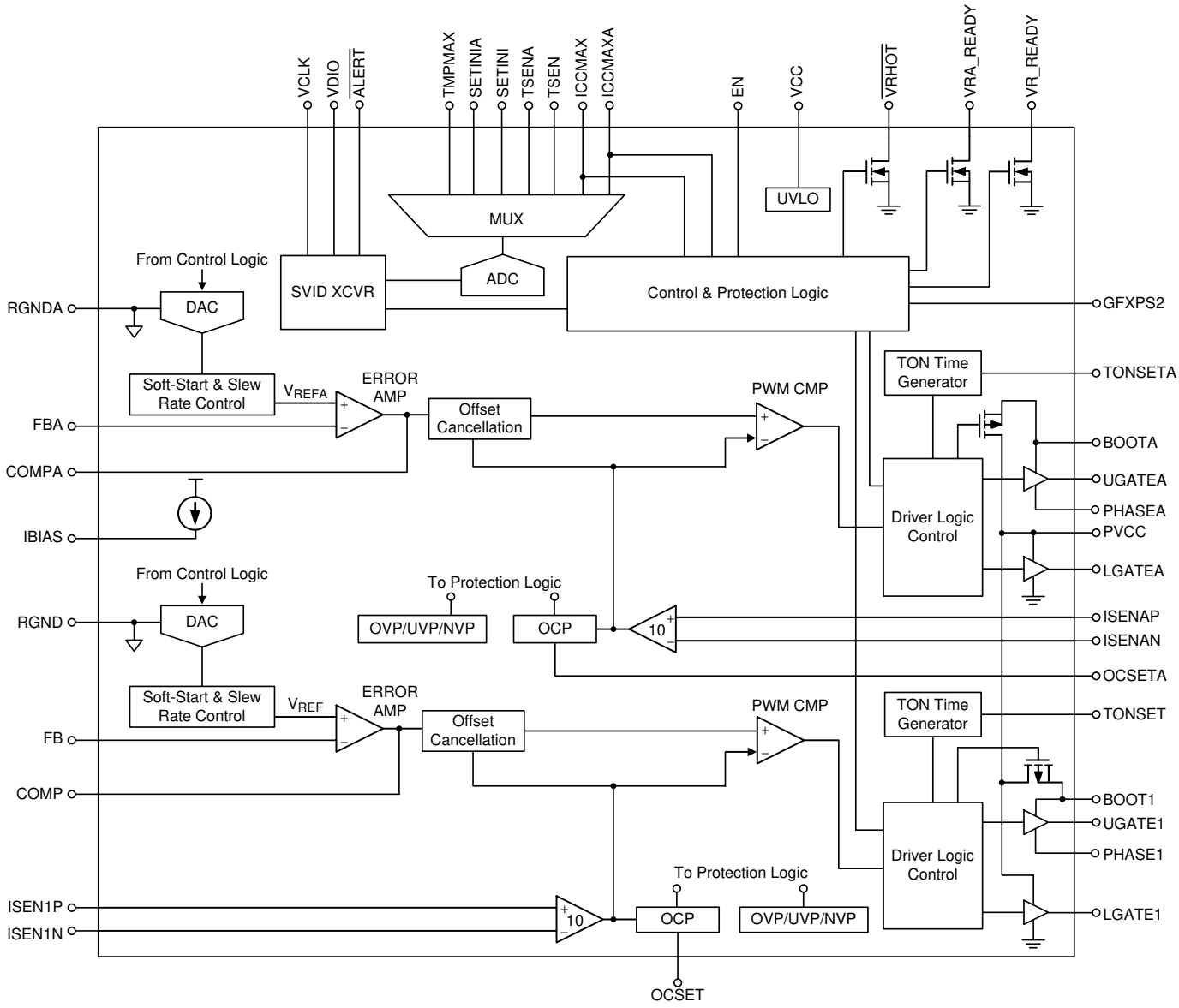
VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	H1	H0	DAC Voltage
1	1	1	1	1	0	0	1	F	9	1.490
1	1	1	1	1	0	1	0	F	A	1.495
1	1	1	1	1	0	1	1	F	B	1.500
1	1	1	1	1	1	0	0	F	C	1.505
1	1	1	1	1	1	0	1	F	D	1.510
1	1	1	1	1	1	1	0	F	E	1.515
1	1	1	1	1	1	1	1	F	F	1.520

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT1	CPU VR Bootstrap Power Pin. This pin powers the high side MOSFET drivers. Connect this pin to the PHASE1 pin with a bootstrap capacitor.
2	TONSET	Single-Phase CPU VR On-Time Setting Pin. Connect this pin to V_{IN} with a resistor to set ripple size in PWM mode.
3	ISEN1P	Positive Current Sense Input Pin of CPU VR.
4	ISEN1N	Negative Current Sense Input Pin of CPU VR.
5	COMP	CPU VR Compensation Pin. This pin is the output of the error amplifier.
6	FB	CPU VR Feedback Pin. This pin is the inverting input node of the error amplifier.
7	RGND	Return Ground for CPU VR. This pin is the inverting input node for differential remote voltage sensing.
8	GFXPS2	Set Pin for GPU VR Operation Mode. Logic-high on this pin will force the GPU VR to enter DCM.
9	VCC	Controller Power Supply Pin. Connect this pin to GND via a ceramic capacitor larger than 1μF.
10	SETINIA	ADC Input for Single-Phase GPU VR VBOOT Voltage Setting.
11	SETINI	ADC Input for Single-Phase CPU VR VBOOT Voltage Setting.
12	TMPMAX	ADC Input for Single-Phase CPU VR Maximum Temperature Setting.
13	ICCMAX	ADC Input for Single-Phase CPU VR Maximum Current Setting.
14	ICCMAXA	ADC Input for Single-Phase GPU VR Maximum Current Setting.
15	TSEN	Thermal Monitor Sense Input Pin for CPU VR.
16	OCSET	Set Pin for Single-Phase CPU VR Over Current Protection Threshold. Connect a resistive voltage divider from VCC to ground, and connect the joint of the voltage divider to the OCSET pin. The voltage, V_{OCSET}, at this pin sets the over current threshold, I_{LIMIT}, for CPU VR.
17	TSENA	Thermal Monitor Sense Input for GPU VR.
18	OCSETA	Set Pin for Single-Phase GPU VR Over Current Protection Threshold. Connect a resistive voltage divider from VCC to ground, and connect the joint of the voltage divider to the OCSETA pin. The voltage, V_{OCSETA}, at this pin sets the over current threshold, I_{LIMIT}, for GPU VR.
19	IBIAS	Internal Bias Current Setting. Connect a 53.6kΩ resistor from this pin to GND to set the internal bias current.
20	$\overline{\text{VRHOT}}$	Thermal Monitor Output Pin (active low).
21	VR_READY	CPU VR Voltage Ready Indicator. This pin has an open drain output.
22	VRA_READY	GPU VR Voltage Ready Indicator. This pin has an open drain output.
23	$\overline{\text{ALERT}}$	Alert Line of SVID Interface (active low). This pin has an open drain output.
24	VDIO	Data Transmission Line of SVID Interface.
25	VCLK	Clock Signal Line of SVID Interface.
26	RGNDA	Return Ground for Single-Phase GPU VR. This pin is the inverting input node for differential remote voltage sensing.
27	FBA	GPU VR Feedback Pin. This pin is the inverting input node of the error amplifier.
28	COMPA	Single-Phase GPU VR Compensation Pin. This pin is the output of the error amplifier.
29	ISENAN	Negative Current Sense Input Pin of Single-Phase GPU VR.
30	ISENAP	Positive Current Sense Input Pin of Single-Phase GPU VR.
31	TONSETA	Single-Phase GPU VR On-Time Setting Pin. Connect this pin to VIN with a resistor to set ripple size in PWM mode.

Pin No.	Pin Name	Pin Function
32	EN	Voltage Regulator Enable Signal Input Pin.
33	BOOTA	GPU VR Bootstrap Power Pin. This pin powers the high side MOSFET drivers. Connect this pin to the PHASEA pin with a bootstrap capacitor.
34	UGATEA	Upper Gate Driver of GPU VR. This pin drives the high side MOSFET of GPU VR.
35	PHASEA	Switch Node of GPU VR. This pin is the return node of the high side MOSFET driver for GPU VR. Connect this pin to the joint of the source of high side MOSFET, drain of the low side MOSFET, and the output inductor.
36	LGATEA	Lower Gate Driver of GPU VR. This pin drives the low side MOSFET of GPU VR.
37	PVCC	MOSFET Driver Power Supply Pin. Connect this pin to GND via a ceramic capacitor larger than 1μF.
38	LGATE1	Lower Gate Driver of CPU VR. This pin drives the low side MOSFET of CPU VR.
39	PHASE1	Switch Node of CPU VR. This pin is the return node of the high side driver for CPU VR. Connect this pin to the joint of the source of high side MOSFET, drain of the low side MOSFET, and the output inductor.
40	UGATE1	Upper Gate Driver of CPU VR. This pin drives the high side MOSFET of CPU VR.
41 (Exposed Pad)	GND	Ground of Low Side MOSFET Driver. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- PVCC, VCC to GND ---------- –0.3V to 6.5V
- RGNDx to GND ---------- –0.3V to 0.3V
- TONSETx to GND ---------- –0.3V to 28V
- Others ---------- –0.3V to (V_{CC} + 0.3V)
- BOOTx to PHASEx ---------- –0.3V to 6.5V
- PHASEx to GND
  - DC ---------- –3V to 28V
  - <20ns ---------- –8V to 32V
- UGATEx to PHASEx
  - DC ---------- –0.3V to (BOOTx – PHASEx)
  - <20ns ---------- –5V to 7.5V
- LGATEx to GND
  - DC ---------- –0.3V to (PVCC + 0.3V)
  - <20ns ---------- –2.5V to 7.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WQFN–40L 5x5 ---------- 2.778W
- Package Thermal Resistance (Note 2)
  - WQFN–40L 5x5, θ_{JA} ---------- 36°C/W
  - WQFN–40L 5x5, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{CC} ---------- 4.5V to 5.5V
- Input Voltage, V_{IN} ---------- 5V to 25V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Input Voltage Range	V_{CC}/V_{PVCC}	V_{EN} = 1.05V, Not Switching	4.5	5	5.5	V
	V_{IN}	Battery Input Voltage	5	--	25	V
Supply Current (V_{CC} + PVCC)	I_{VCC} + I_{PVCC}	V_{EN} = 1.05V, Not Switching	--	12	20	mA
Supply Current (TONSETx)	$I_{TONSETx}$	V_{FB} =1V, V_{IN} = 12V, R_{TON} = 100kΩ	--	110	--	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current (PVCC + V_{CC})	I_{VCC_SHDN} + I_{PVCC_SHDN}	V_{EN} = 0V	--	--	5	μA
Shutdown Current (TONSETx)	$I_{TONSETx\_SHDN}$	V_{EN} = 0V	--	--	5	μA
TON Setting						
TONSETx Voltage	$V_{TONSETx}$	I_{RTON} = 80μA, V_{FBx} = 1V	0.95	1.075	1.2	0V
On-Time	t_{ON}	I_{RTON} = 80μA, V_{FBx} = 1V	315	350	385	ns
TONSETx Input Current Range	I_{RTON}	V_{FBx} = 1.1V	25	--	280	μA
Minimum Off-Time	T_{OFF_MIN}		--	350	--	ns
GFX VR Forced DEM						
GFXPS2x Enable Threshold	V_{GFXPS}		4.3	--	--	V
GFXPS2x Disable Threshold	V_{GFXPS}		--	--	0.7	V
References and System Output Voltage						
DAC Accuracy (PS0/PS1)	V_{FBx}	VID_{SVID} Setting = 1.000V~1.520V OFS_{SVID} Setting = 0V	–0.5	0	0.5	%VID
		VID_{SVID} Setting = 0.800V~1.000V OFS_{SVID} Setting = 0V	–5	0	5	mV
		VID_{SVID} Setting = 0.500V~0.800V OFS_{SVID} Setting = 0V	–8	0	8	
		VID_{SVID} Setting = 0.250V~0.500V OFS_{SVID} Setting = 0V	–8	0	8	
		VID_{SVID} Setting = 1.100V OFS_{SVID} Setting = –0.640V~0.635V	–10	0	10	
SETINIx Voltage	$V_{SETINIx}$	V_{INI_CORE} = 0V, V_{INI_GFX} = 0V	0	0.3125	0.5125	V
		V_{INI_CORE} = 0.9V, V_{INI_GFX} = 0.9V	0.7375	0.9375	1.1375	
		V_{INI_CORE} = 1V, V_{INI_GFX} = 1V	1.3625	1.5625	1.7625	
		V_{INI_CORE} = 1.1V, V_{INI_GFX} = 1.1V	2.6125	--	5	
IBIAS Pin Voltage	V_{IBIAS}	R_{IBIAS} = 53.6kΩ	2.09	2.14	2.19	V
Dynamic VID Slew Rate	SR_{DVID}	SetVID Slow	2.5	3.125	3.75	mV/μs
		SetVID Fast	10	12.5	15	
Error Amplifier						
DC Gain	A_{DC}	R_L = 47kΩ (Note5)	70	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF (Note5)	--	10	--	MHz
Slew Rate	SR_{COMP}	C_{LOAD} = 10pF (Gain = –4, R_{LOAD_COMP} = 47kΩ, V_{COMPx} = 0.5V to 3V)	--	5	--	V/μs
Output Voltage Range	V_{COMP}	R_L = 47kΩ	0.5	--	3.6	V
MAX Source/Sink Current	I_{COMP}	V_{COMP} = 2V	--	250	--	μA
Impedance of FBx	R_{FBx}		1	--	--	MΩ

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Current Sense Amplifier						
Input Offset Voltage	V_{OFS_CSA}		–1	--	1	mV
Impedance of Neg. Input	R_{ISENxN}		1	--	--	MΩ
Impedance of Pos. Input	R_{ISENxP}		1	--	--	MΩ
Current Sense Differential Input Range	V_{CSDIx}	V_{FBx} = 1.1V, $V_{CSDIx} = V_{ISENxP} - V_{ISENxN}$	–50	--	100	mV
Current Sense DC Gain (Loop)	A_I	V_{FBx} = 1.1V, –30mV < V_{CSDIx} < 50mV	--	10	--	V/V
V_{ISEN} Linearity	V_{ISEN_ACC}	V_{DAC} = 1.1V –30mV < V_{ISEN_IN} < 50mV	–1	--	1	%
Gate Driver						
Upper Driver Source	R_{UGATEx_sr}	$V_{BOOTx} - V_{PHASEx}$ = 5V $V_{BOOTx} - V_{UGATEx}$ = 0.1V	--	1	--	Ω
Upper Driver Sink	R_{UGATEx_sk}	V_{UGATEx} = 0.1V	--	1	--	Ω
Lower Driver Source	R_{LGATEx_sr}	PVCC = 5V, PVCC – V_{LGATEx} = 0.1V	--	1	--	Ω
Lower Driver Sink	R_{LGATEx_sk}	V_{LGATEx} = 0.1V	--	0.5	--	Ω
Internal Boot Charging Switch On-Resistance	R_{BOOTx}	PVCC to BOOTx	--	30	--	Ω
Zero Current Detection Threshold	V_{ZCD_TH}	V_{ZCD_TH} = GND – V_{PHASEx}	--	10	--	mV
Protection						
Under Voltage Lock-out Threshold	V_{UVLO}	VCC Falling edge	4.04	4.24	--	V
Under Voltage Lock-out Hysteresis	ΔV_{UVLO}		--	100	--	mV
Over Voltage Protection Threshold	V_{OVP}	Respect to $VOUT\_MAX_{SVID}$, with 1μs filter time	100	150	200	mV
Under Voltage Protection Threshold	V_{UVP}	V_{UVP} = V_{ISENxN} – V_{REFx}, 0.8V < V_{REFx} <1.52V, with 3μs filter time	–350	–300	–250	mV
Negative Voltage Protection Threshold	V_{NVP}	$V_{NVP} = V_{ISENxN}$ – GND	–100	–50	--	mV
Current Sense Gain for Over Current Protection	A_{OC}	V_{OCSET} = 2.4V $V_{ISENxP} - V_{ISENxN}$ = 50mV	--	48	--	V/V
Logic Inputs						
EN Input Threshold Voltage	Logic-High	V_{IH}	With respect to 1V, 70%	0.7	--	--	V
	Logic-Low	V_{IL}	With respect to 1V, 30%	--	--	0.3	
Leakage Current of EN				–1	--	1	μA
VCLK,VDIO Input Threshold Voltage		V_{IH}	With respect to Intel Spec.	0.65	--	--	V
		V_{IL}	With respect to Intel Spec.	--	--	0.45	
Leakage Current of VCLK, VDIO		I_{LEAK_IN}		–1	--	1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$\overline{\text{ALERT}}$						
$\overline{\text{ALERT}}$ Low Voltage	$V_{\overline{\text{ALERT}}}$	$I_{\overline{\text{ALERT}}\_SINK}$ = 4mA	--	--	0.4	V
VR Ready						
VRx_READY Low Voltage	V_{VRx_READY}	$I_{VRx\_READY\_SINK}$ = 4mA	--	--	0.4	V
VRx_READY Delay	t_{VRx_READY}	V_{ISENxN} = V_{BOOT} to V_{VRx_READY} high	70	100	160	µs
Thermal Throttling						
$\overline{\text{VRHOT}}$ Output Voltage	$V_{\overline{\text{VRHOT}}}$	$I_{\overline{\text{VRHOT}}\_SINK}$ = 40mA	--	0.4	--	V
High Impedance Output						
$\overline{\text{ALERT}}$, VRx_READY, $\overline{\text{VRHOT}}$	I_{LEAK_OUT}		–1	--	1	µA
Temperature Zone						
TSEN Threshold for Tmp_Zone [7] transition	V_{TSENx}	100°C	--	1.8725	--	V
TSEN Threshold for Tmp_Zone [6] transition		97°C	--	1.8175	--	V
TSEN Threshold for Tmp_Zone [5] transition		94°C	--	1.7625	--	V
TSEN Threshold for Tmp_Zone [4] transition		91°C	--	1.7075	--	V
TSEN Threshold for Tmp_Zone [3] transition		88°C	--	1.6525	--	V
TSEN Threshold for Tmp_Zone [2] transition	V_{TSENx}	85°C	--	1.5975	--	V
TSEN Threshold for Tmp_Zone [1] transition		82°C	--	1.5425	--	V
TSEN Threshold for Tmp_Zone [0] transition		75°C	--	1.4875	--	V
Update Period	t_{TSEN}		--	1600	--	µs
ADC						
Latency	t_{LAT}		--	--	400	µs
Digital Code of ICCMAX	$C_{ICCMAX1}$	V_{ICCMAX} = 0.637V	29	32	35	decimal
	$C_{ICCMAX2}$	V_{ICCMAX} = 1.2642V	61	64	67	decimal
	$C_{ICCMAX3}$	V_{ICCMAX} = 2.5186V	125	128	131	decimal
Digital Code of ICCMAXA	$C_{ICCMAXA1}$	$V_{ICCMAXA}$ = 0.1666V	5	8	11	decimal
	$C_{ICCMAXA2}$	$V_{ICCMAXA}$ = 0.3234V	13	16	19	decimal
	$C_{ICCMAXA3}$	$V_{ICCMAXA}$ = 0.637V	29	32	35	decimal
Digital Code of TMPMAX	$C_{TMPMAX1}$	V_{TMPMAX} = 1.6758V	82	85	88	decimal
	$C_{TMPMAX2}$	V_{TMPMAX} = 1.9698V	97	100	103	decimal
	$C_{TMPMAX3}$	V_{TMPMAX} = 2.4598V	122	125	128	decimal

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

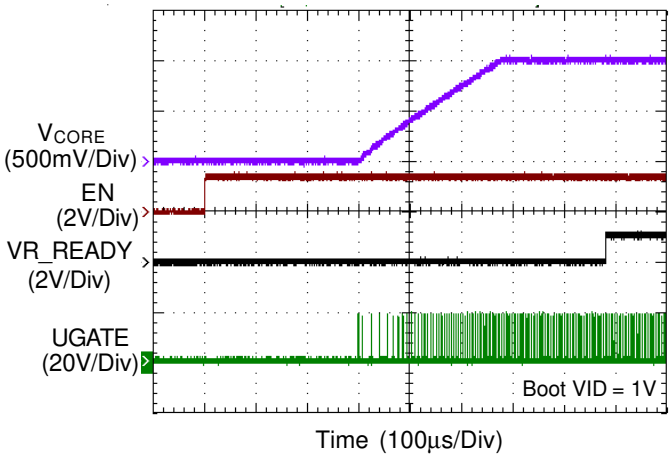
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

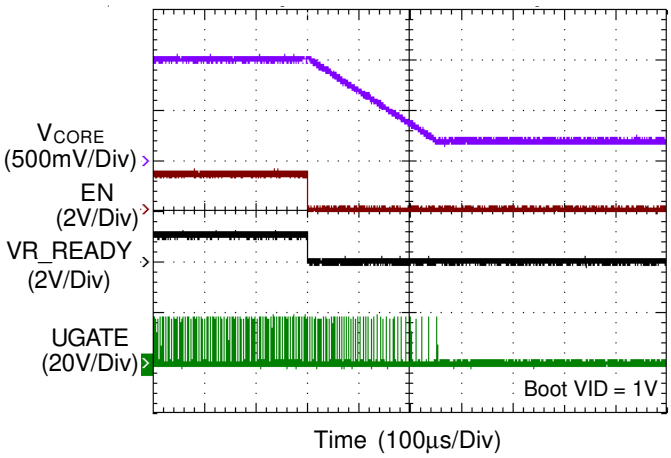
Note 5. Guaranteed by design.

Typical Operating Characteristics

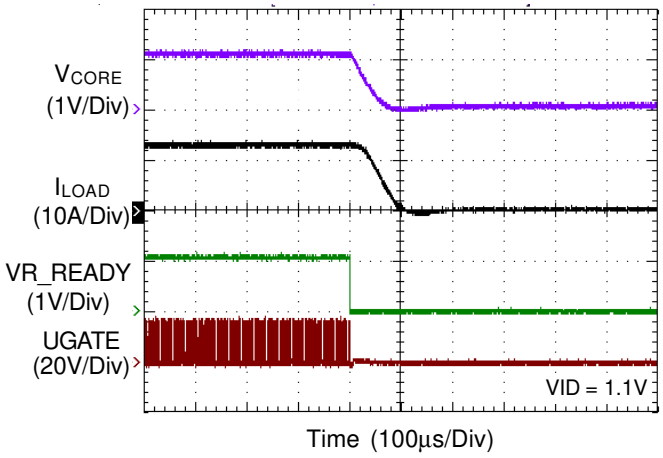
CORE VR Power On from EN



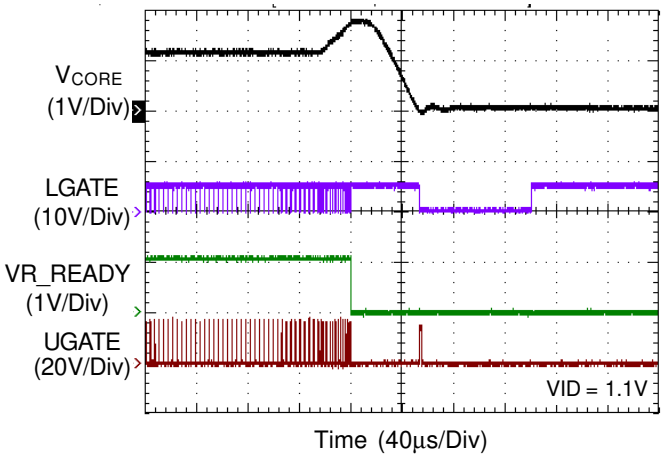
CORE VR Power Off from EN



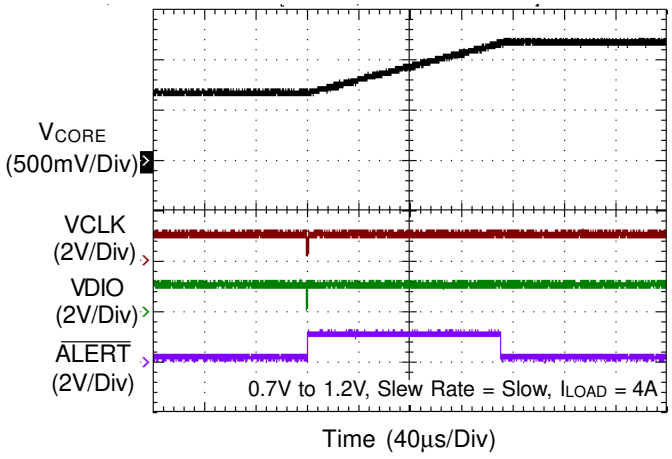
CORE VR OCP



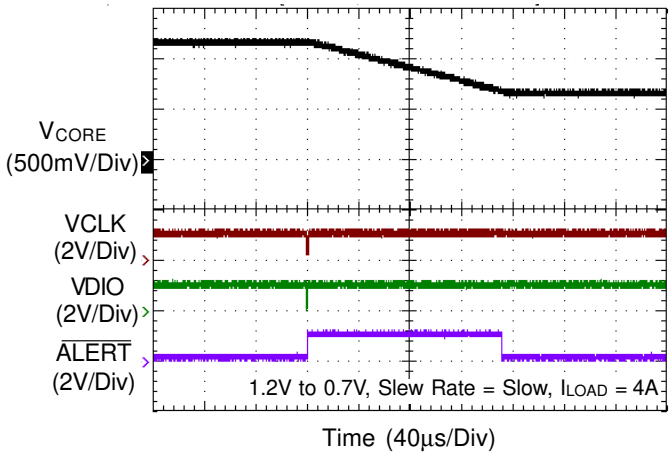
CORE VR OVP and NVP



CORE VR Dynamic VID Up



CORE VR Dynamic VID Down



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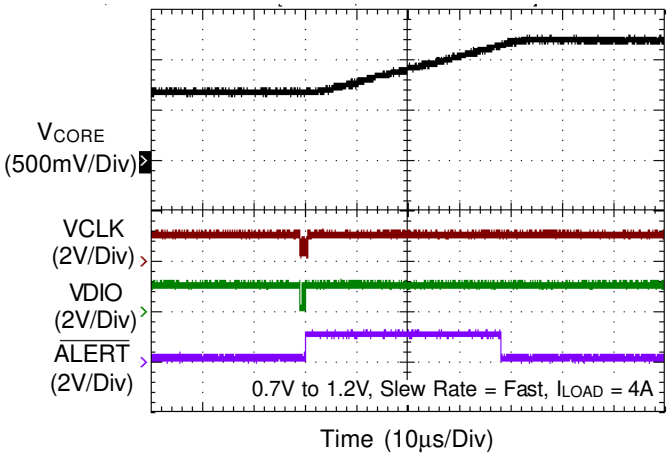
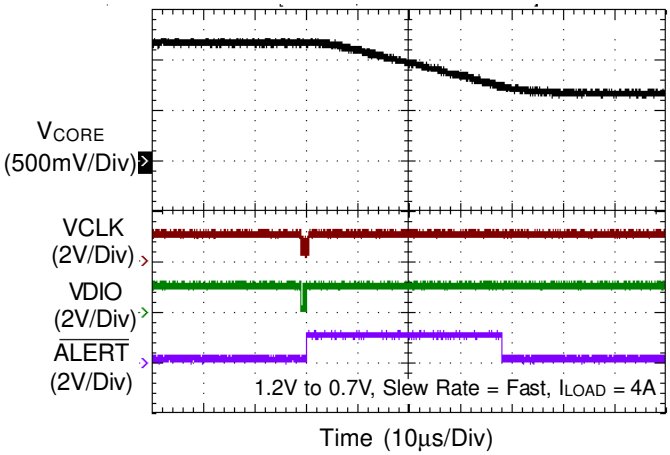
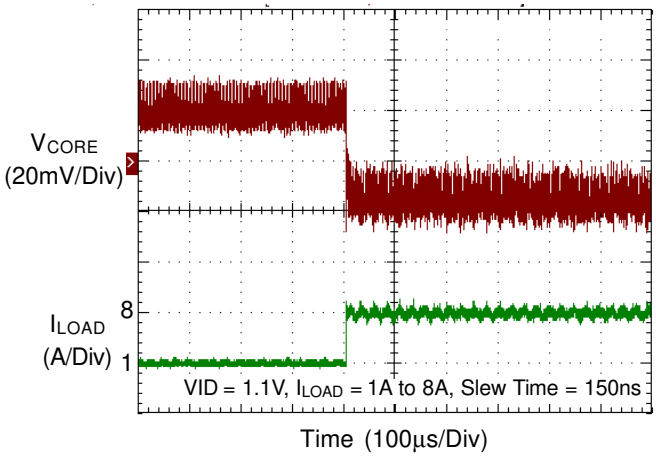


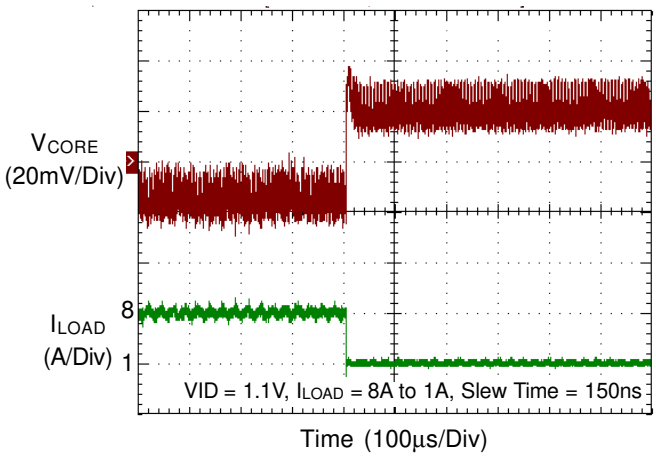
CORE VR Dynamic VID Down



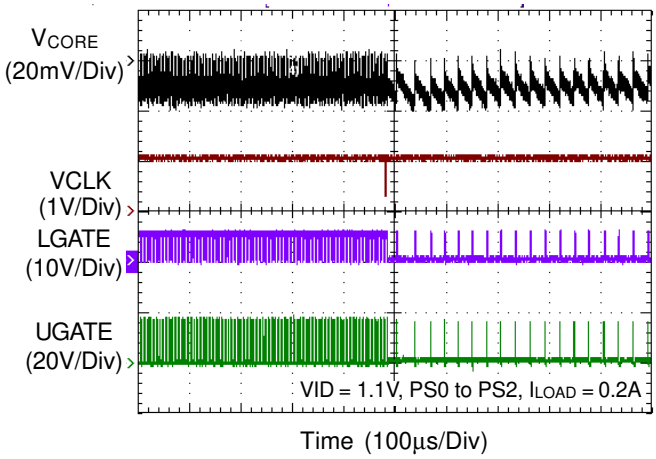
CORE VR Load Transient



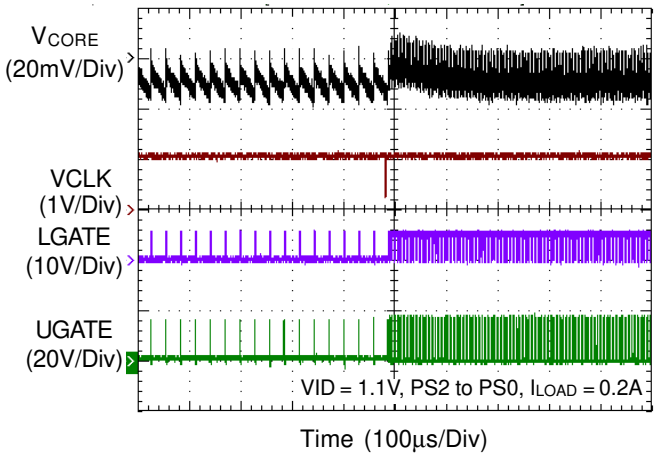
CORE VR Load Transient



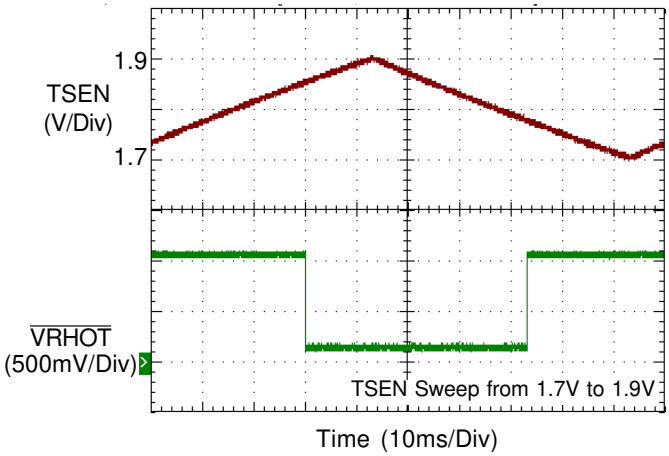
CORE VR Mode Transition



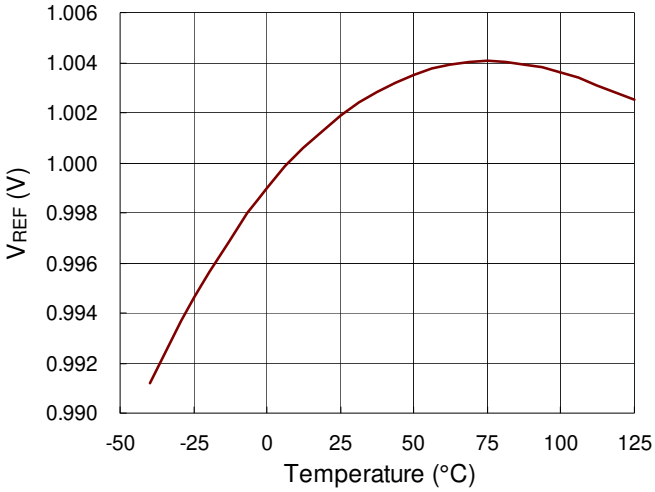
CORE VR Mode Transition



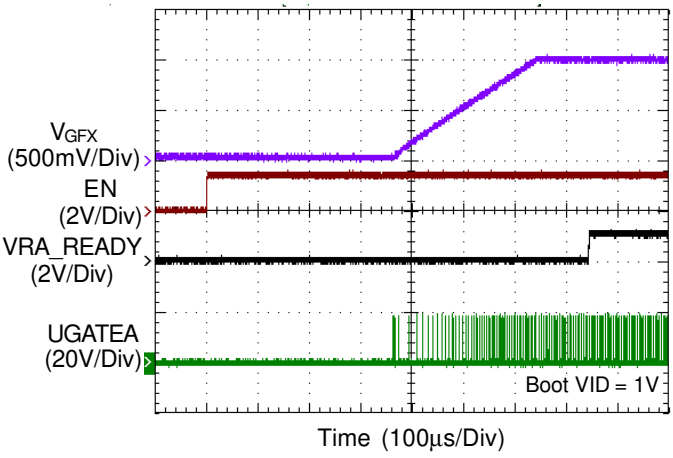
CORE VR Thermal Monitoring



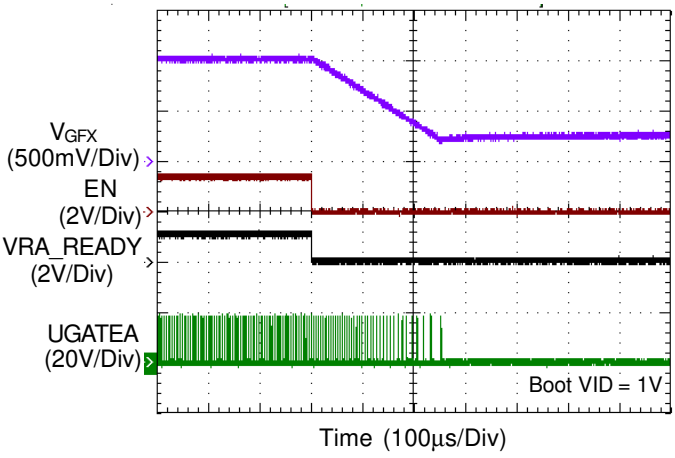
CORE VR V_{REF} vs. Temperature



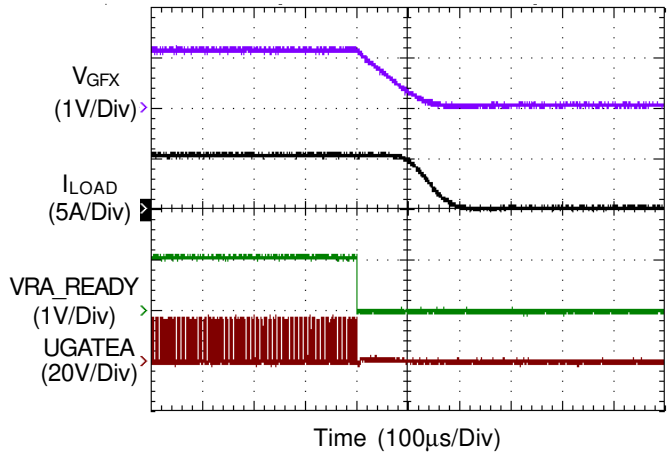
GFX VR Power On from EN



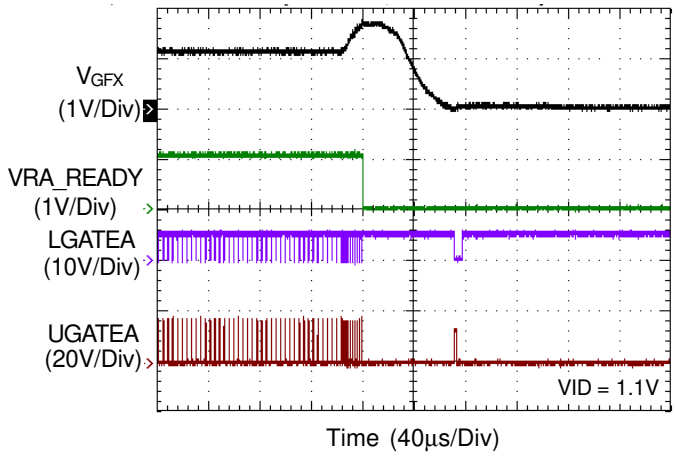
GFX VR Power Off from EN



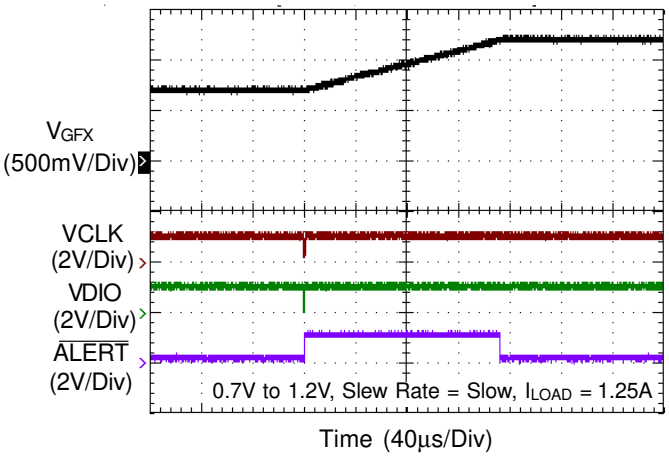
GFX VR OCP



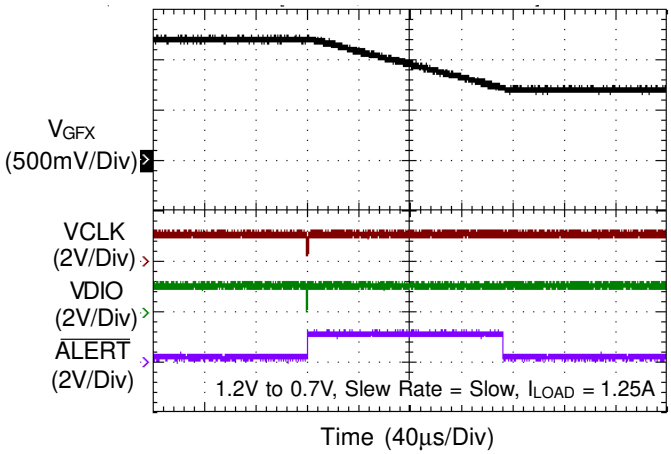
GFX VR OVP and NVP



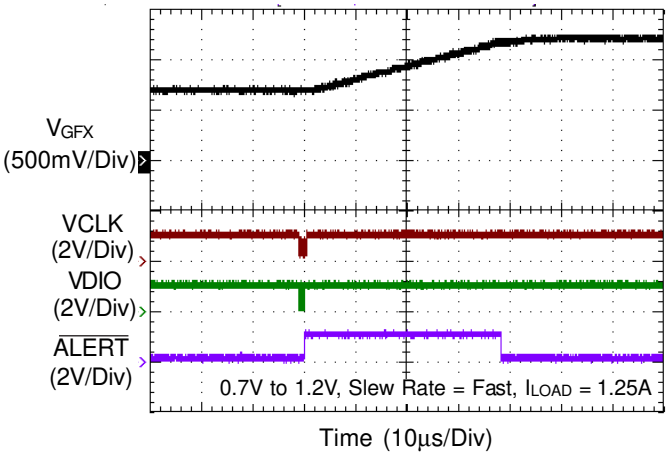
GFX VR Dynamic VID



GFX VR Dynamic VID



GFX VR Dynamic VID



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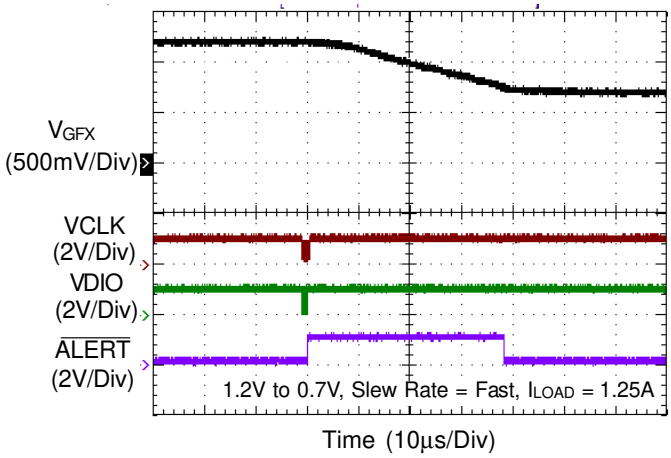

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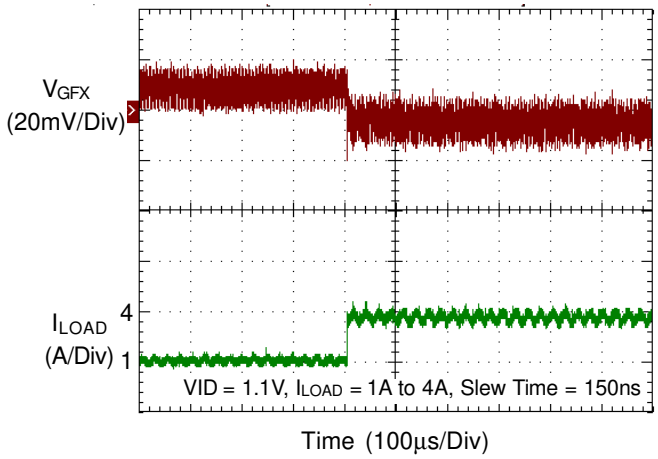

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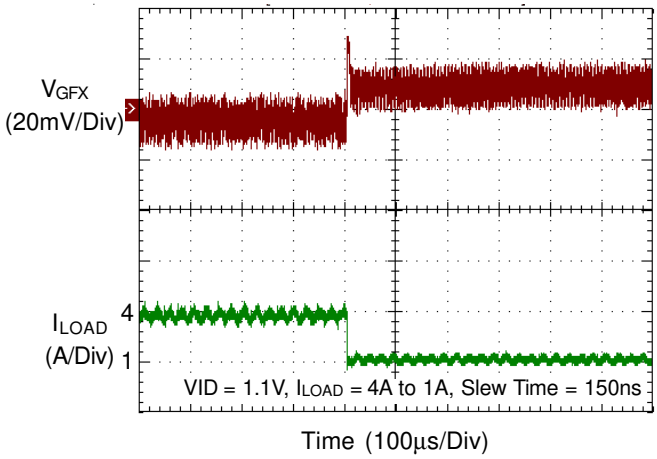
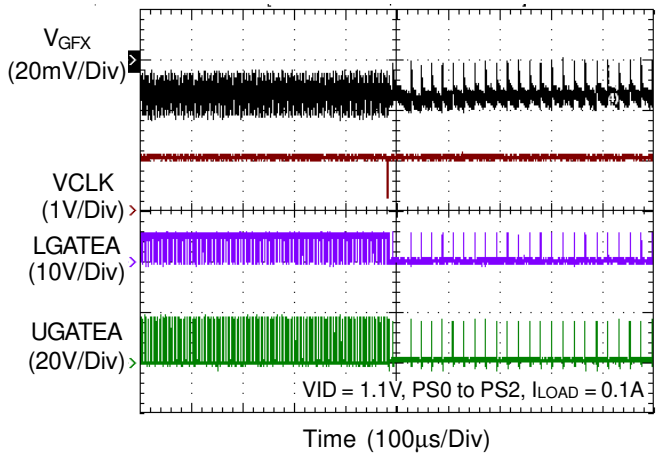
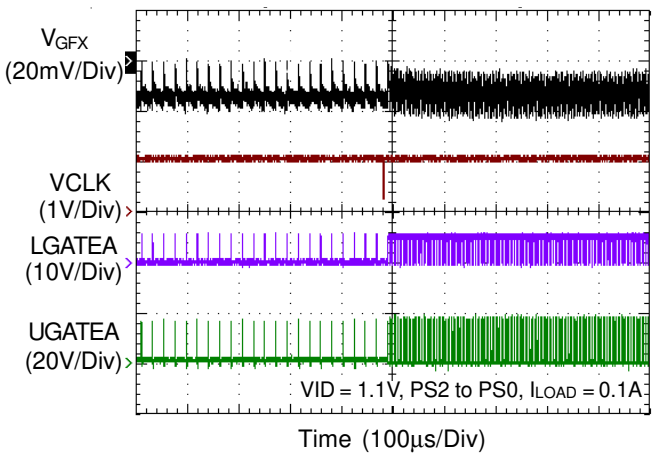


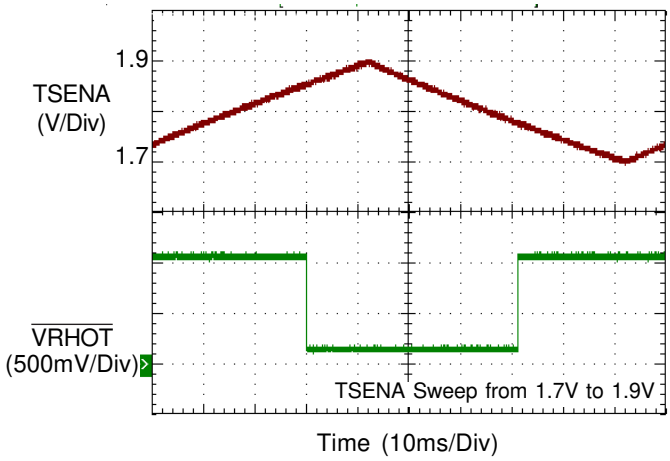
GFX VR Mode Transition



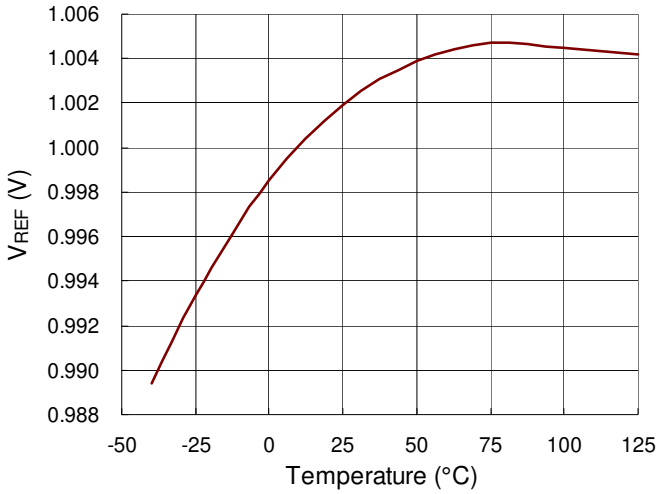
GFX VR Mode Transition



GFX VR Thermal Monitoring



GFX VR V_{REF} vs. Temperature



Application Information

The RT8168B is a VR12/IMVP7 compliant, dual single-phase synchronous Buck PWM controller for the CPU CORE VR and GFX VR. The gate drivers are embedded to facilitate PCB design and reduce the total BOM cost. A serial VID (SVID) interface is built-in in the RT8168B to communicate with Intel VR12/IMVP7 compliant CPU.

The RT8168B adopts G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology derived from finite DC gain compensator, making it an easy setting PWM controller to meet AVP requirements. The load line can be easily programmed by setting the DC gain of the error amplifier. The RT8168B has fast transient response due to the G-NAVP™ commanding variable switching frequency.

G-NAVP™ topology also represents a high efficiency system with green power concept. With G-NAVP™ topology, the RT8168B becomes a green power controller with high efficiency under heavy load, light load, and very light load conditions. The RT8168B supports mode transition function between CCM and DEM. These different operating states allow the overall power system to have low power loss. By utilizing the G-NAVP™ topology, the operating frequency of RT8168B varies with output voltage, load and VIN to further enhance the efficiency even in CCM.

The built-in high accuracy DAC converts the SVID code ranging from 0.25V to 1.52V with 5mV per step. The differential remote output voltage sense and high accuracy DAC allow the system to have high output voltage accuracy.

The RT8168B supports VR12/IMVP7 compatible power management states and VID on-the-fly function. The power management states include DEM in PS2/PS3 and Forced-CCM in PS1/PS0. The VID on-the-fly function has three different slew rates : Fast, Slow and Decay. The RT8168B integrates a high accuracy ADC for platform setting functions, such as no-load offset and over current level. The controller supports both DCR and sense-resistor current sensing. The RT8168B provides VR ready output signals of both CORE VR and GFX VR. It also features complete fault protection functions including over voltage, under voltage, negative voltage, over current and under voltage lockout. The RT8168B is available in a WQFN-48L 6x6 small foot print package.

Design Tool

To help users reduce efforts and errors caused by manual calculations, a user-friendly design tool is now available on request. This design tool calculates all necessary design parameters by entering user's requirements. Please contact Richtek's representatives for details.

Serial VID (SVID) Interface

SVID is a three-wire serial synchronous interface defined by Intel. The three wire bus includes VDIO, VCLK and $\overline{\text{ALERT}}$ signals. The master (Intel's VR12/IMVP7 CPU) initiates and terminates SVID transactions and drives the VDIO, VCLK, and $\overline{\text{ALERT}}$ during a transaction. The slave (RT8168B) receives the SVID transactions and acts accordingly.