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3A, 24V, 500kHz Synchronous Step-Down Converter

General Description

The RT8299 is a high efficiency, monolithic synchronous step-down DC/DC converter with internal power MOSFETs. It achieves 3A of continuous output current over a wide input supply range from 3V to 24V with excellent load and line regulation. Current mode operation provides fast transient response and eases loop stabilization. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. Thermal shutdown provides reliable, fault tolerant operation. The low current shutdown mode provides output disconnection, enabling easy power management in battery powered systems.

Ordering Information

RT8299□□

Package Type
SP : SOP-8 (Exposed Pad-Option 1)
QW: WDFN-10L 3x3 (W-Type)

Lead Plating System
G : Green (Halogen Free and Pb Free)
Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

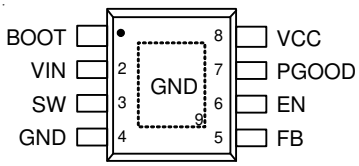
- **3V to 24V Input Voltage Range**
- **3A Output Current**
- **Internal N-MOSFETs**
- **Current Mode Control**
- **Fixed Frequency Operation : 500kHz**
- **Output Adjustable from 0.8V to 15V**
- **Up to 95% Efficiency**
- **Stable with Low ESR Ceramic Output Capacitors**
- **Cycle-by-Cycle Over Current Protection**
- **Input Under Voltage Lockout**
- **Output Under Voltage Protection**
- **Thermal Shutdown Protection**
- **SOP-8 (Exposed Pad) and 10-Lead WDFN Packages**
- **RoHS Compliant and Halogen Free**

Applications

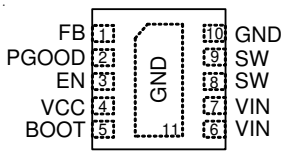
- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High Performance DSPs, FPGAs, and ASICs

Pin Configurations

(TOP VIEW)



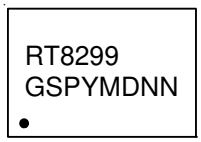
SOP-8 (Exposed Pad)



WDFN-10L 3x3

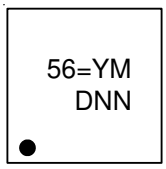
Marking Information

RT8299GSP



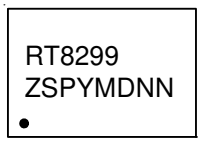
RT8299GSP : Product Number
YMDNN : Date Code

RT8299GQW



56= : Product Number
YMDNN : Date Code

RT8299ZSP



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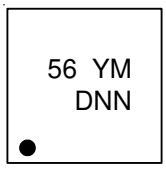
YMDNN : Date Code

RT8299ZQW



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YMDNN : Date Code

Typical Application Circuit

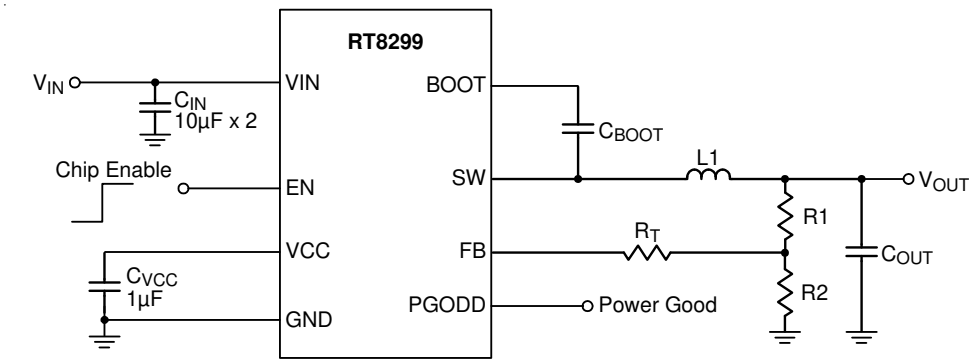


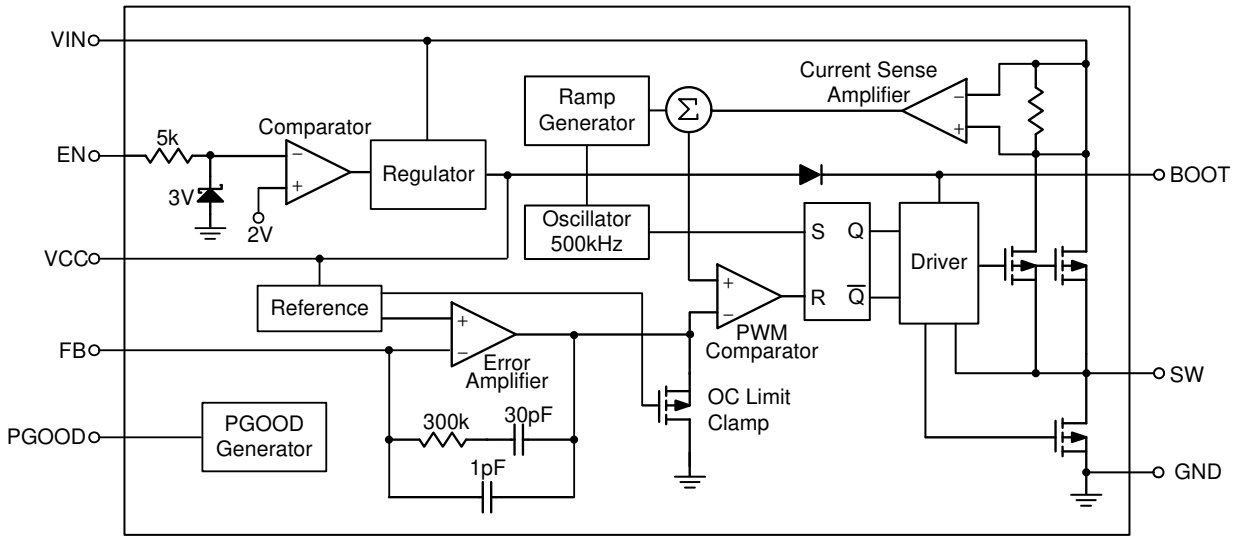
Table 1. Recommended Component Selection

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_T (kΩ)	L (µH)	C_{OUT} (µF)
1.2	15	30	50	2	22 x 2
2.5	25.5	12	40	3.6	22 x 2
3.3	16	5.1	30	4.7	22 x 2
5	27	5.1	18	6.8	22 x 2

Functional Pin Description

Pin No.		Pin Name	Pin Function
SOP-8 (Exposed Pad)	WDFN-10L 3x3		
1	5	BOOT	Bootstrap for High Side Gate Driver. Connect a 0.1μF or greater ceramic capacitor from BOOT to SW pin.
2	6, 7	VIN	Supply Input Voltage. Must bypass with a suitably large ceramic capacitor.
3	8, 9	SW	Switch Node. Connect to external LC filter.
4, 9 (Exposed Pad)	10, 11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	1	FB	Feedback Input. This pin is connected to the converter output. It is used to regulate the output of the converter to a desired value via an internal resistive voltage divider. For an adjustable output, an external resistive voltage divider is connected to this pin.
6	3	EN	Enable Input. A logic high enables the converter; a logic low forces the RT8299 into shutdown mode, reducing the supply current to less than 3μA. Attach this pin to VIN with a 100kΩ pull up resistor for automatic startup.
7	2	PGOOD	Power Good Output. The output of this pin is open drain.
8	4	VCC	Bias Supply.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, V_{IN} ---------- –0.3 to 26V
- Switching Voltage, SW ---------- –0.6 to (V_{IN} + 0.3V)
  < 20ns ---------- –5V to 30V
- Boot Voltage, BOOT ---------- (V_{SW} – 0.3V) to (V_{SW} + 6V)
- All Other Pins ---------- –0.3 to 6V
- Power Dissipation, P_D @ T_A = 25°C
  SOP-8 (Exposed Pad) ---------- 1.333W
  WDFN-10L 3x3 ---------- 1.429W
- Package Thermal Resistance (Note 2)
  SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
  WDFN-10L 3x3, θ_{JA} ---------- 70°C/W
  WDFN-10L 3x3, θ_{JC} ---------- 8.2°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Voltage, V_{IN} ---------- 3V to 24V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- 40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	--	3	μA
Supply Current			V_{EN} = 3V, V_{FB} = 1V	--	1	--	mA
Upper Switch On Resistance				--	100	--	mΩ
Lower Switch On Resistance				--	100	--	mΩ
Switch Leakage			V_{EN} = 0V, V_{SW} = 0V or 12V	--	0	10	μA
Current Limit		I_{LIM}	V_{BOOT} – V_{SW} = 4.8V	--	5.5	--	A
Oscillator Frequency		f_{OSC}	V_{FB} = 0.75V	425	500	575	kHz
Short Circuit Frequency			V_{FB} = 0V	--	150	--	kHz
Maximum Duty Cycle		D_{MAX}	V_{FB} = 0.8V	--	93	--	%
Minimum On-Time		t_{ON}		--	100	--	ns
Feedback Voltage		V_{FB}	4.5V ≤ V_{IN} ≤ 24V	788	800	812	mV
EN Input Threshold Voltage	Logic-High	V_{IH}		2	--	5.5	V
	Logic-Low	V_{IL}		--	--	0.4	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Under Voltage Lockout Threshold	V_{UVLO}	V_{IN} Rising	--	2.8	--	V
Under Voltage Lockout Threshold Hysteresis	ΔV_{UVLO}		--	300	--	mV
Power Good Threshold		VOUT Rising, with Respect to V_{FB}	--	90	--	%
		VOUT Falling, with Respect to V_{FB}	--	70	--	
VCC Regulator			--	5	--	V
VCC Load Regulation		I_{CC} = 5mA	–4	--	4	%
Soft-Start Period	t_{SS}		--	2	--	ms
Thermal Shutdown	T_{SD}		--	150	--	°C

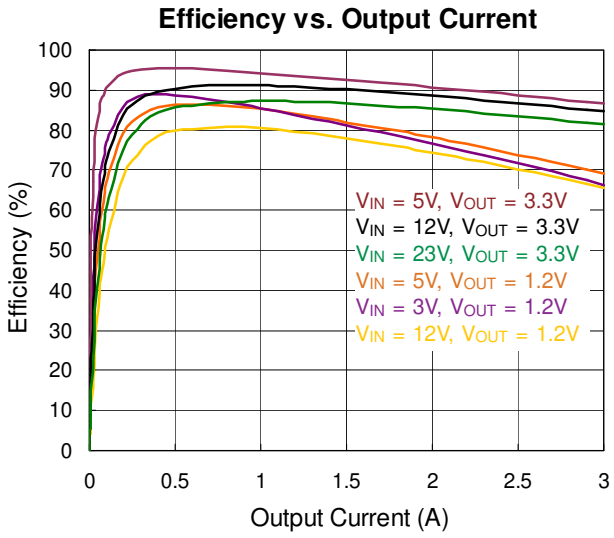
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

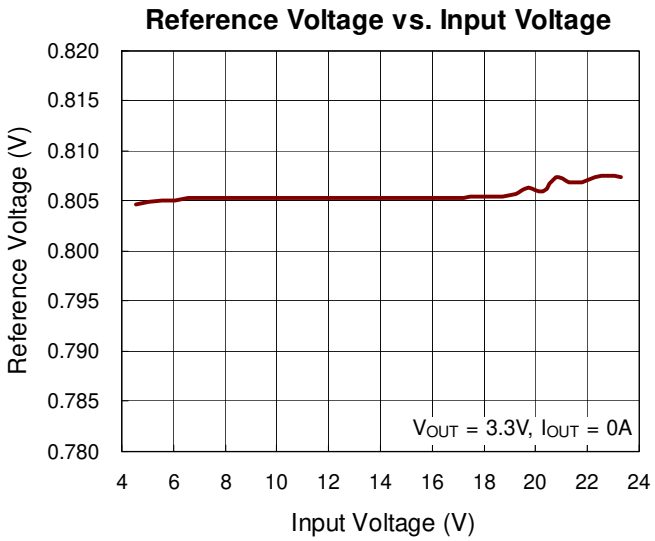
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

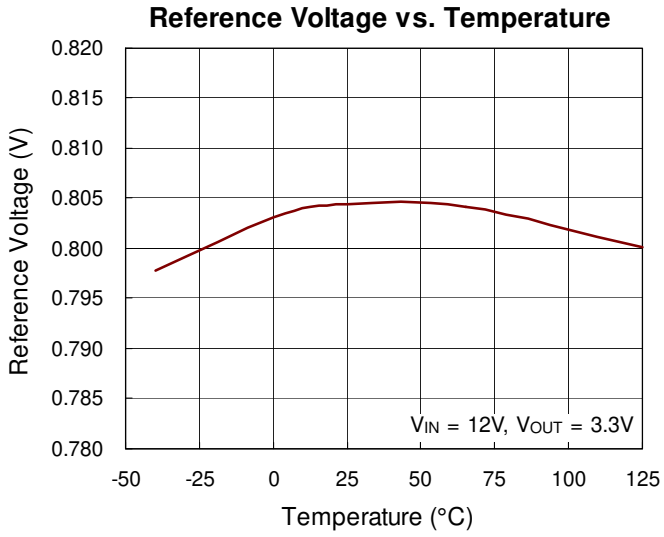
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

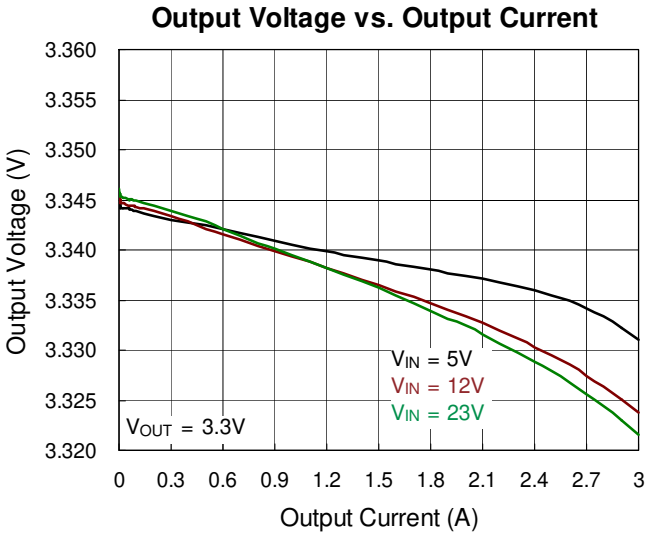
Note 4. The device is not guaranteed to function outside its operating conditions.

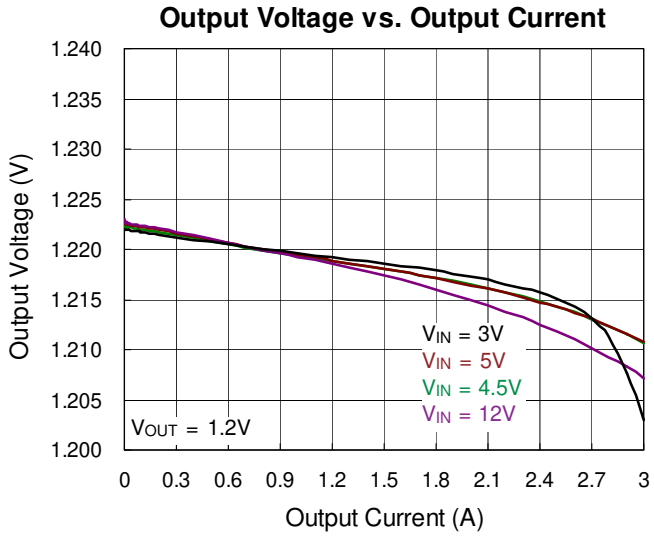
Typical Operating Characteristics

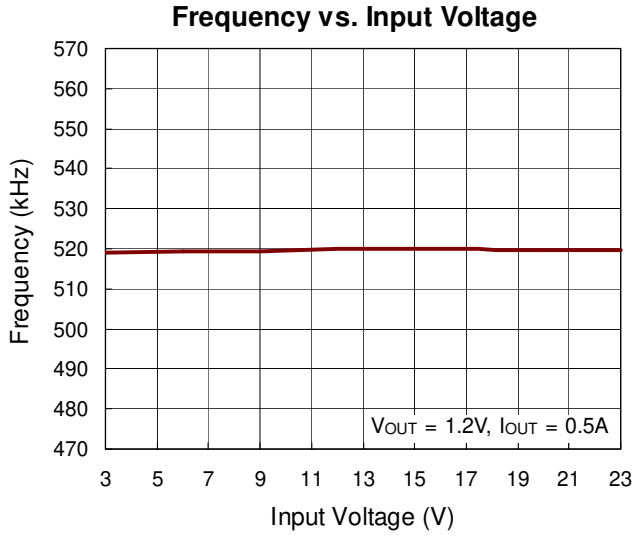




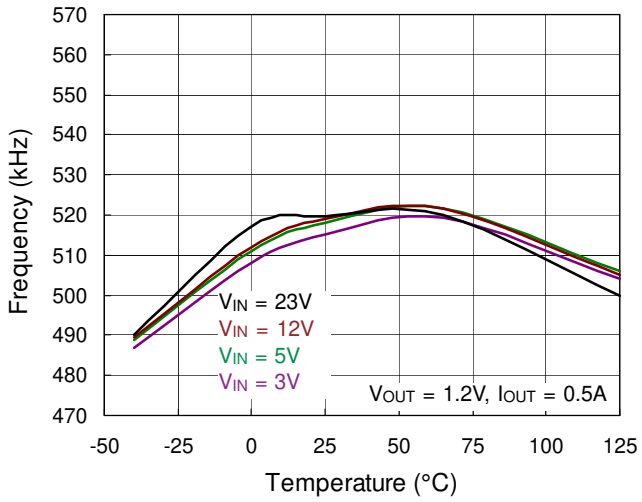




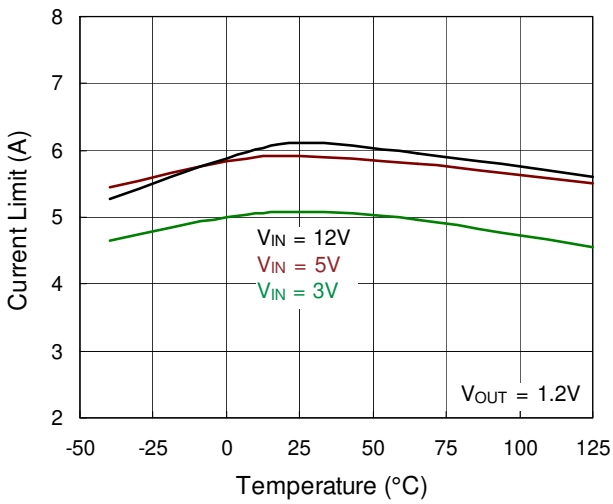




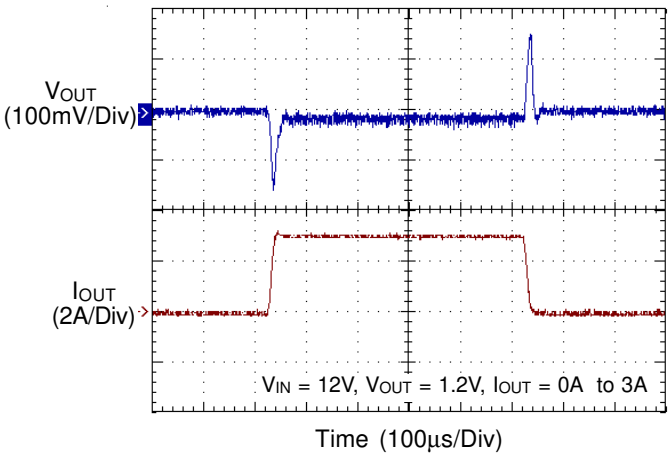
Frequency vs. Temperature



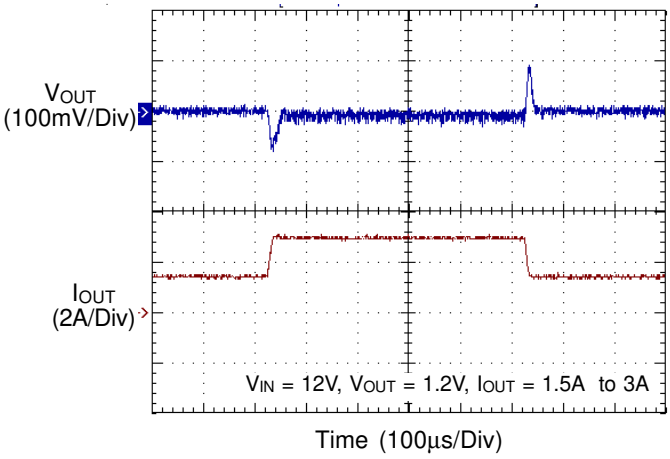
Current Limit vs. Temperature



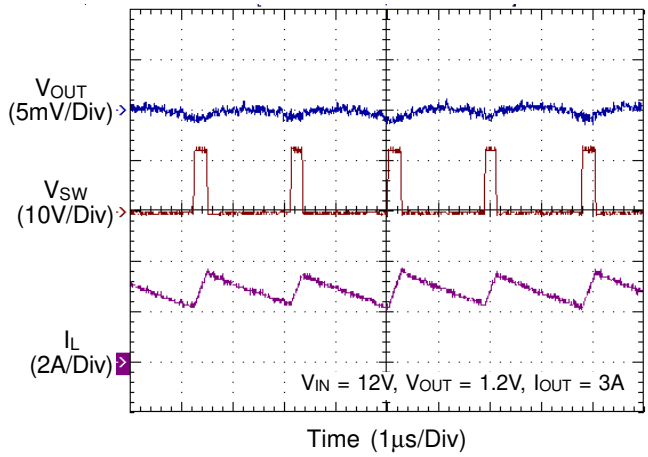
Load Transient Response



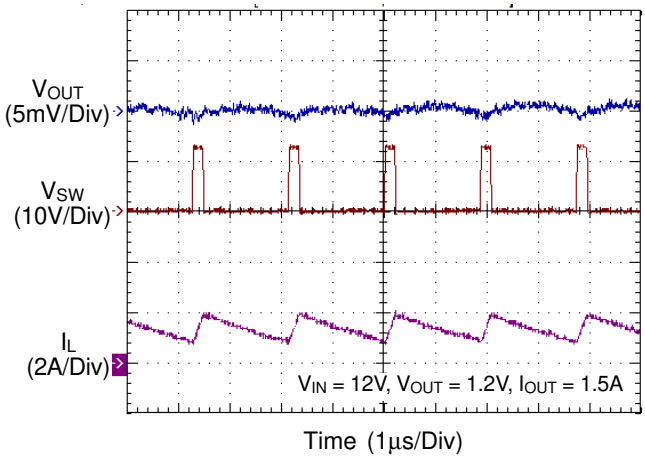
Load Transient Response



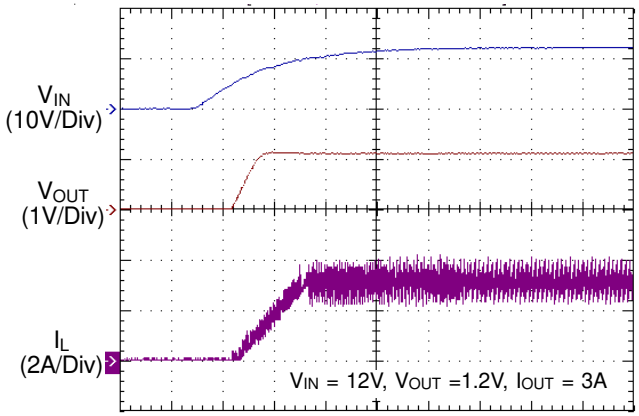
Switching



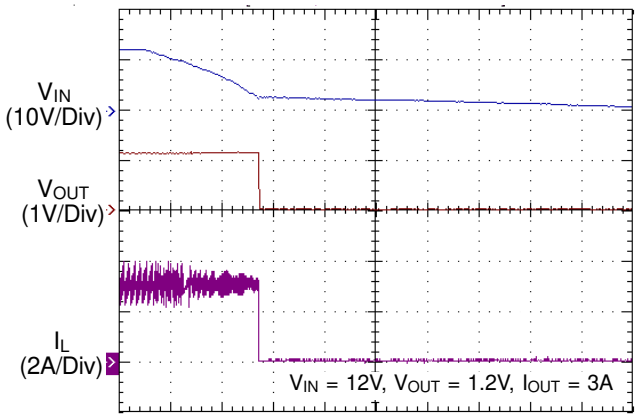
Switching



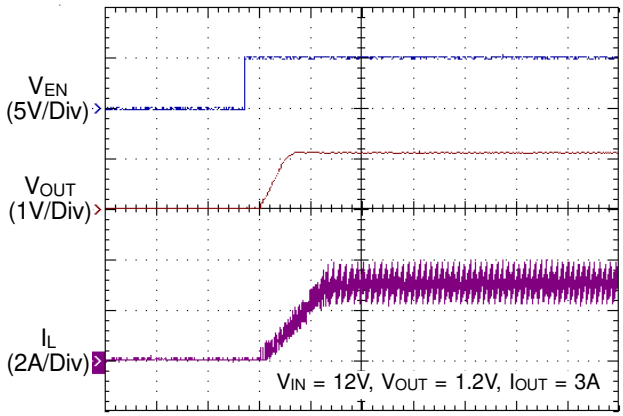
Power On from V_{IN}



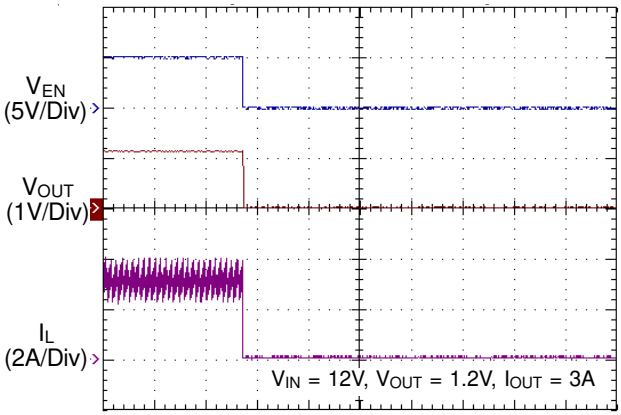
Power Off from V_{IN}



Power On from EN



Power Off from EN



Application Information

The RT8299 is a synchronous high voltage buck converter that can support the input voltage range from 3V to 24V and the output current can be up to 3A.

Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

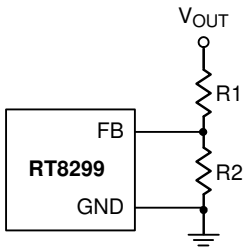


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right)$$

where V_{FB} is the feedback reference voltage (0.8V typ.).

External Bootstrap Diode

Connect a 100nF low ESR ceramic capacitor between the BOOT pin and SW pin. This capacitor provides the gate driver voltage for the high side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT8299. Note that the external boot voltage must be lower than 5.5V

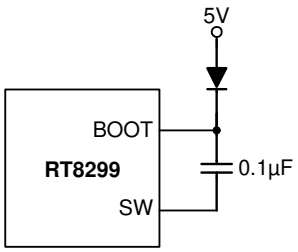


Figure 2. External Bootstrap Diode

Chip Enable Operation

The EN pin is the chip enable input. Pulling the EN pin low (<0.4V) will shutdown the device. During shutdown mode, the RT8299 quiescent current drops to lower than 3µA. Driving the EN pin high (>2V, < 5.5V) will turn on the device again. For external timing control (e.g.RC), the EN pin can also be externally pulled high by adding a R_{EN}* resistor and C_{EN}* capacitor from the VIN pin (see Figure 5).

An external MOSFET can be added to implement digital control on the EN pin when no system voltage above 2.5V is available, as shown in Figure 3. In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between V_{IN} and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin.

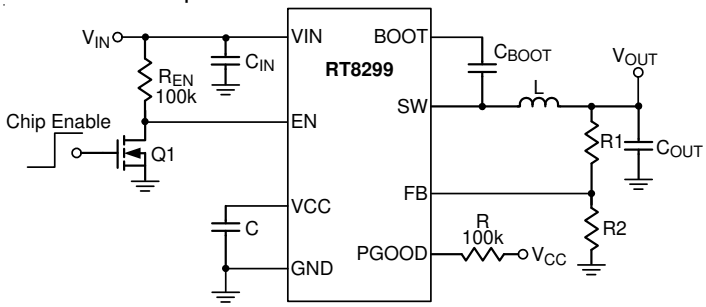


Figure 3. Enable Control Circuit for Logic Control with Low Voltage

To prevent enabling circuit when V_{IN} is smaller than the V_{OUT} target value, a resistive voltage divider can be placed between the input voltage and ground and connected to the EN pin to adjust IC lockout threshold, as shown in Figure 4. For example, if an 8V output voltage is regulated from a 12V input voltage, the resistor R_{EN2} can be selected to set input lockout threshold larger than 8V.

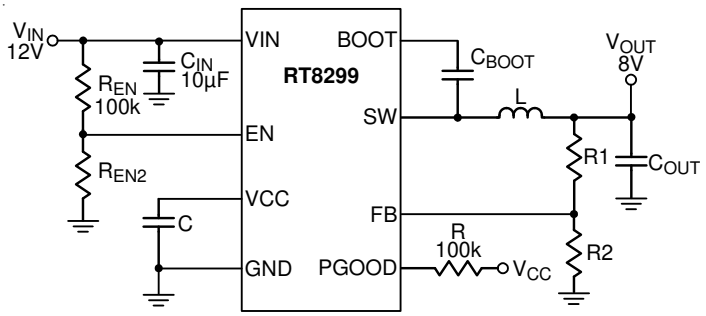


Figure 4. The Resistors can be Selected to Set IC Lockout Threshold

Under Voltage Protection

Hiccup Mode

For the RT8299, it provides Hiccup Mode Under Voltage Protection (UVP). When the FB voltage drops below half of the feedback reference voltage, V_{FB}, the UVP function will be triggered and the RT8299 will shut down for a period of time and then recover automatically. The Hiccup Mode UVP can reduce input current in short-circuit conditions.

Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of $\Delta I_L = 0.24(I_{MAX})$ will be a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference.

Table 2. Suggested Inductors for Typical Application Circuit

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. This simple worst case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

For the input capacitor, two 10µF low ESR ceramic capacitors are recommended.

The selection of C_{OUT} is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for C_{OUT} selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple, ΔV_{OUT}, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8fC_{OUT}}\right]$$

The output ripple will be highest at the maximum input voltage since ΔI_L increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR value. However, it provides lower capacitance density than other types. Although Tantalum capacitors have the highest capacitance density, it is important to only use types that pass the surge test for use in switching power supplies. Aluminum electrolytic capacitors have significantly higher ESR. However, it can be used in cost-sensitive applications

for ripple current rating and long term reliability considerations. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to ΔI_{LOAD} (ESR) also begins to charge or discharge C_{OUT} generating a feedback error signal for the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

EMI Consideration

Since parasitic inductance and capacitance effects in PCB circuitry would cause a spike voltage on SW pin when high side MOSFET is turned-on/off, this spike voltage on SW may impact on EMI performance in the system. In order to enhance EMI performance, there are two methods to suppress the spike voltage. One is to place an R-C snubber between SW and GND and make them as close as possible to the SW pin (see Figure 5). Another method is adding a resistor R_{BOOT}* in series with the bootstrap capacitor, C_{BOOT}. But this method will decrease the driving capability to the high side MOSFET. It is strongly recommended to reserve the R-C snubber during PCB layout for EMI improvement. Moreover, reducing the SW trace area and keeping the main power in a small loop will be helpful on EMI performance. For detailed PCB layout guide, please refer to the section of Layout Consideration.

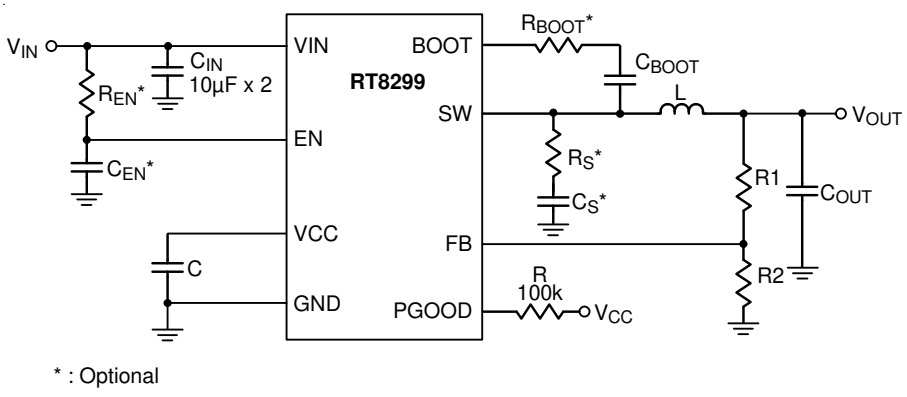


Figure 5. Reference Circuit with Snubber and Enable Timing Control

Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature , T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance, θ_{JA}, is 75°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-10L 3x3 packageS, the thermal resistance, θ_{JA}, is 70°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.333W for SOP-8 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.429W for WDFN-10L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 6 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

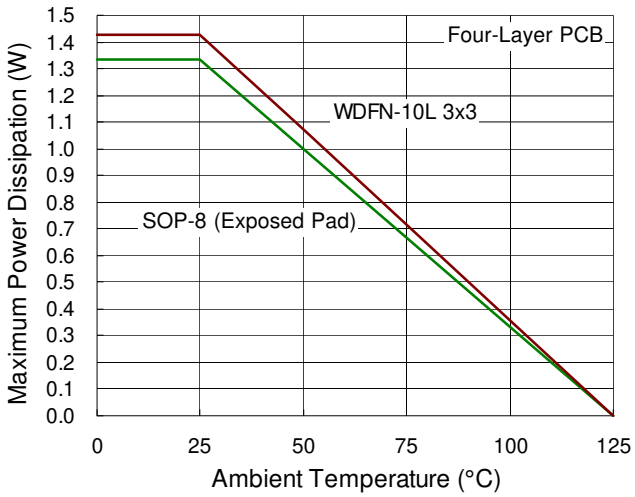


Figure 6. Derating Curve of Maximum Power Dissipation

Layout Consideration

Follow the PCB layout guidelines for optimal performance of the RT8299.

- Keep the traces of the main current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VIN and GND).
- SW node is with high frequency voltage swing and should be kept at small area. Keep analog components away from the SW node to prevent stray capacitive noise pick-up.
- Connect feedback network behind the output capacitors. Keep the loop area small. Place the feedback components near the RT8299.
- An example of PCB layout guide is shown in Figure 6 for reference.

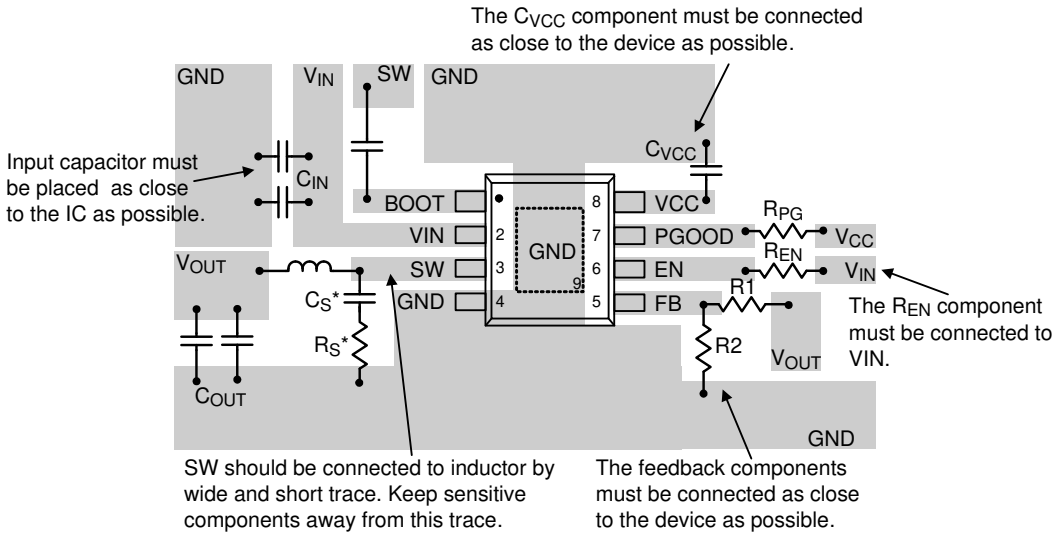
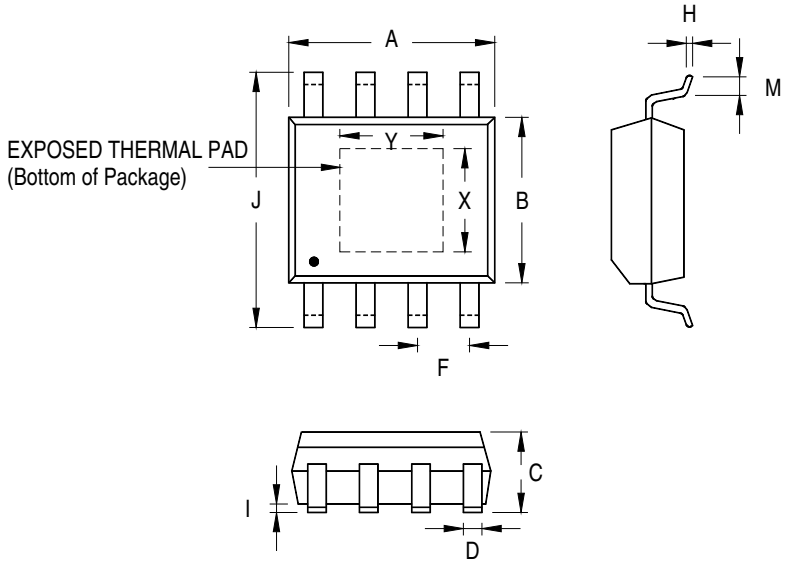


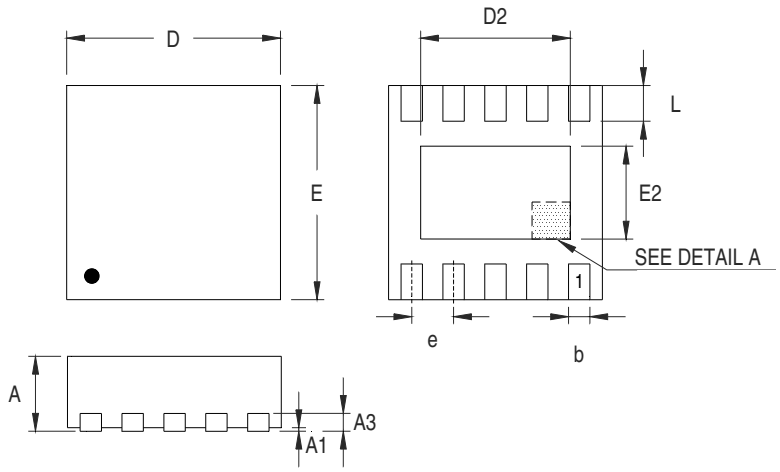
Figure 7. PCB Layout Guide

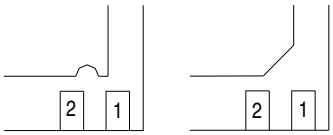
Outline Dimension



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

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