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Multi-Phase PWM Controller for CPU Core Power Supply

General Description

The RT8859M is a VR12/IMVP7 compliant CPU power controller which includes two voltage rails : a 4/3/2/1 phase synchronous buck controller, the CORE VR, and a single phase buck controller, the AXG VR. The RT8859M adopts G-NAVP™ (Green Native AVP), which is Richtek's proprietary topology derived from finite DC gain compensator with current mode control, making it an easy setting PWM controller, meeting all Intel CPU requirements of AVP (Active Voltage Positioning). Based on the G-NAVP™ topology, the RT8859M also features a quick response mechanism for optimized AVP performance during load transient. The RT8859M supports mode transition function with various operating states. A serial VID (SVID) interface is built in the RT8859M to communicate with Intel VR12/IMVP7 compliant CPU. The RT8859M supports VID on-the-fly function with three different slew rates: Fast, Slow and Decay. By utilizing the G-NAVP™ topology, the operating frequency of the RT8859M varies with VID, load and input voltage to further enhance the efficiency even in CCM. The built-in high accuracy DAC converts the SVID code ranging from 0.25V to 1.52V with 5mV per step. The RT8859M integrates a high accuracy ADC for platform setting functions, such as no-load offset or over-current level. The RT8859M provides VR ready output signals of both CORE VR and AXG VR. It also features complete fault protection functions including over voltage, under voltage, negative voltage, over current and under voltage lockout. The RT8859M is available in a WQFN-56L 7x7 small foot print package.

Applications

- VR12 / IMVP7 Intel Core Supply
- Notebook/ Desktop Computer/ Servers Multi-phase CPU Core Supply
- AVP Step-Down Converter

Features

- **4/3/2/1 + 1 Phase PWM Controller**
- **G-NAVP™ Topology**
- **Serial VID Interface**
- **0.5% DAC Accuracy**
- **Differential Remote Voltage Sensing**
- **Built-in ADC for Platform Programming**
- **Accurate Current Balance**
- **System Thermal Compensated AVP**
- **Diode Emulation Mode at Light Load Condition for Multiple and Single Phase**
- **Fast Transient Response**
- **VR12 / IMVP7 Compatible Power Management States**
- **VR Ready Indicator**
- **Thermal Throttling**
- **Current Monitor Output**
- **Switching Frequency up to 1MHz per Phase**
- **OVP, UVP, OCP, NVP, UVLO**
- **Slew Rate Setting/Address Flip Function**
- **External No-Load Offset Setting for both Rails**
- **DVID Improvement**
- **Small 56-Lead WQFN Package**
- **RoHS Compliant and Halogen Free**

Ordering Information

RT8859M□□

- Package Type
  QW : WQFN-56L 7x7 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
  Z : ECO (Ecological Element with Halogen Free and Pb free)

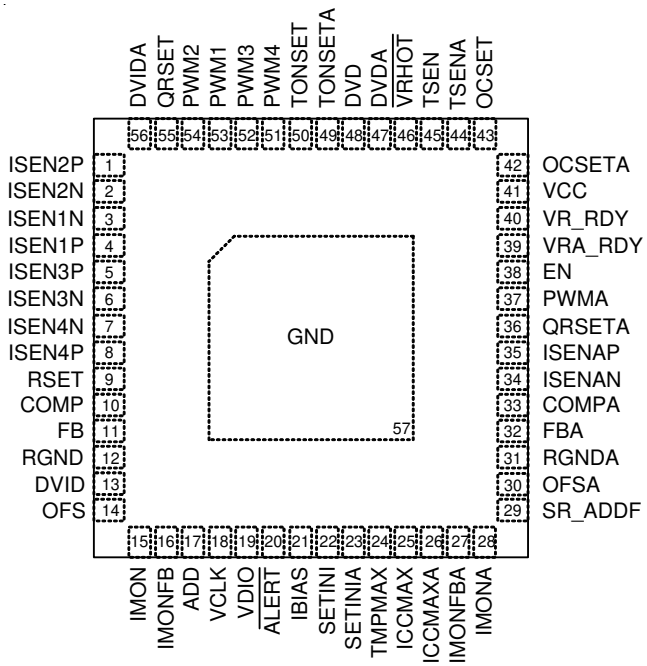
Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Pin Configurations

(TOP VIEW)



WQFN-56L 7x7

Marking Information

RT8859MGQW

RT8859MGQW : Product Number

YMDNN : Date Code

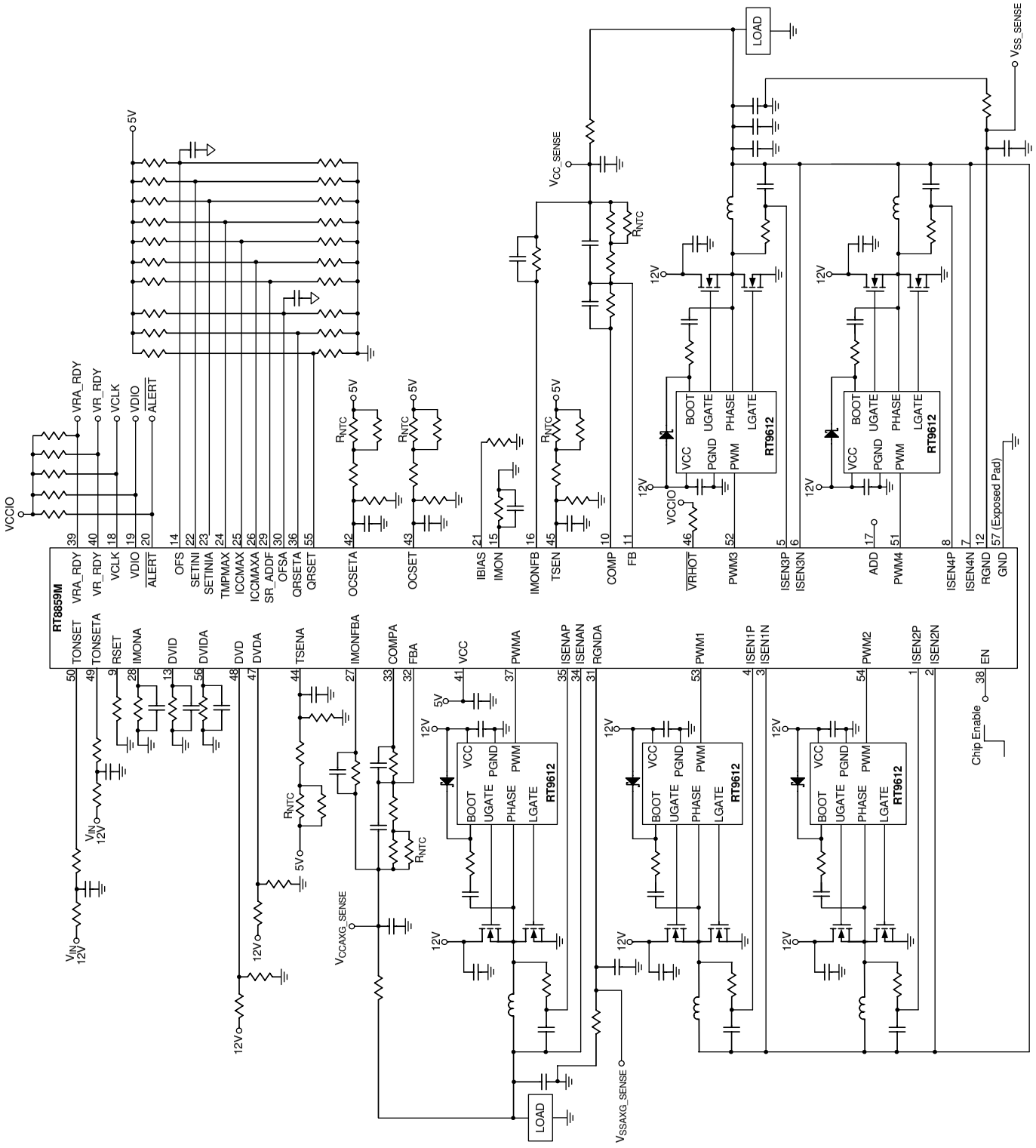
RT8859MZQW

RT8859MZQW : Product Number

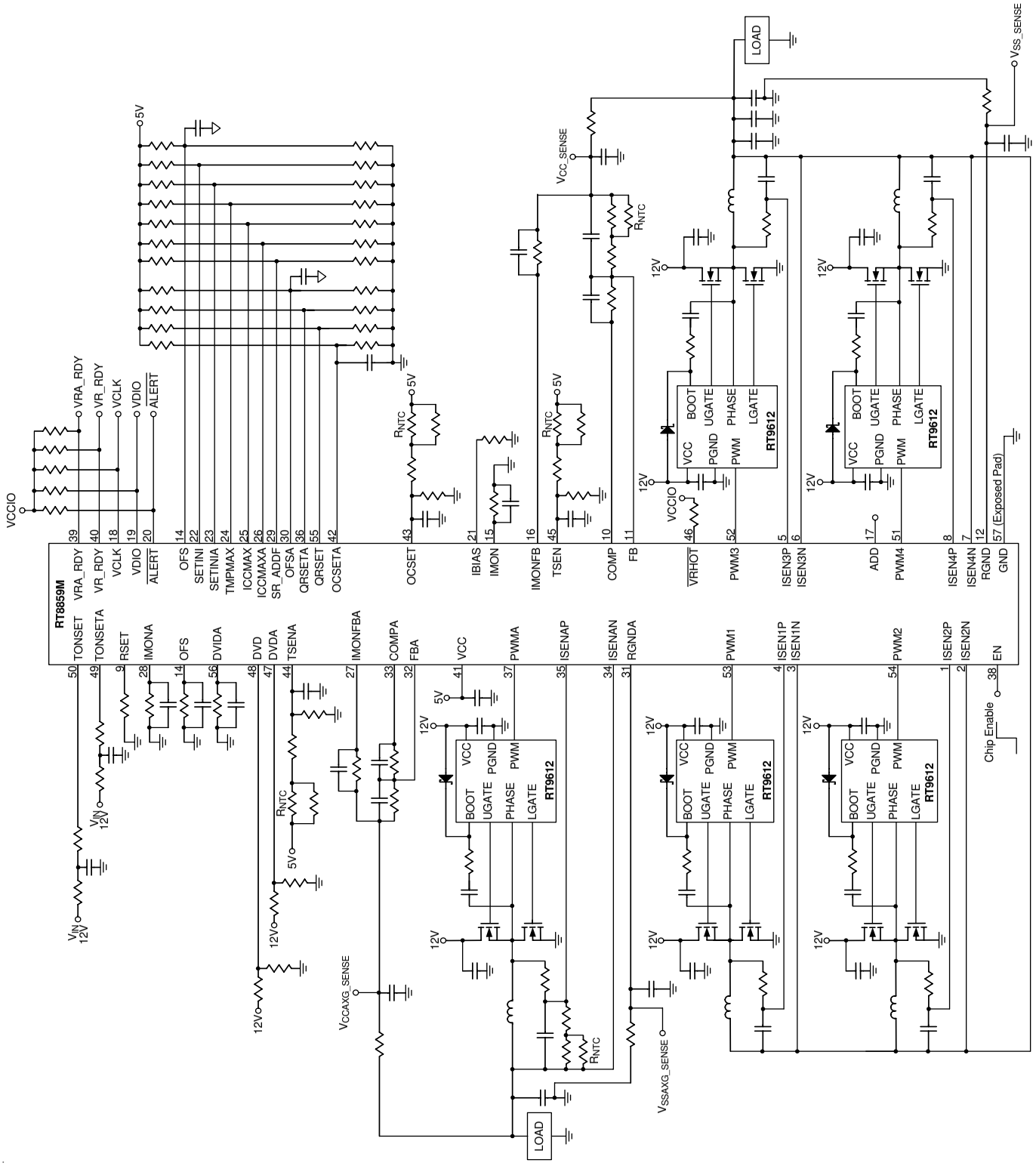
YMDNN : Date Code

Typical Application Circuit

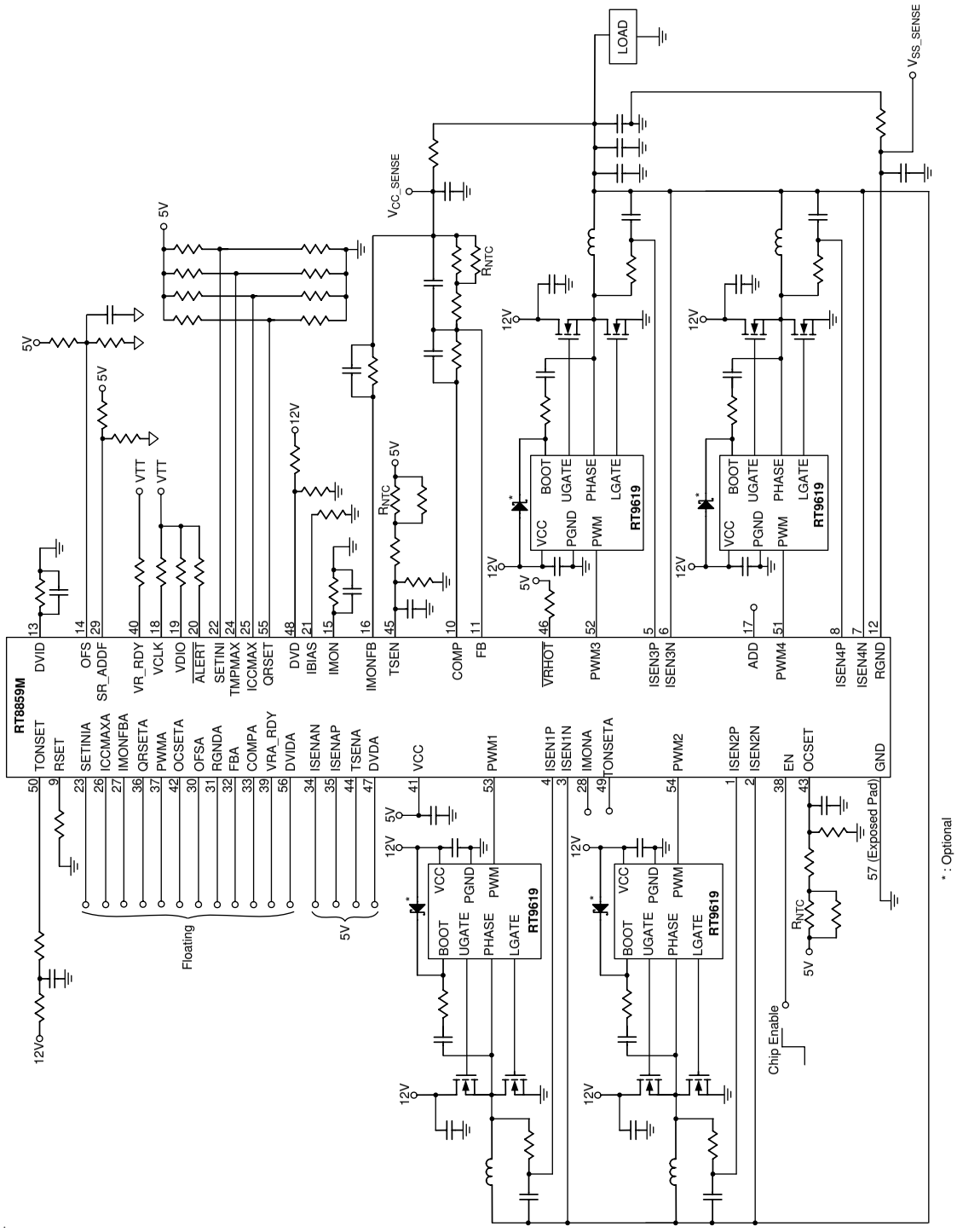
Thermal Compensation at Voltage Loop



Thermal Compensation at Current Loop



AXG VR Disabled



Functional Pin Description

Pin No.	Pin Name	Pin Function
4, 1, 5, 8	ISEN [1:4] P	Positive Current Sense Pin of Phase 1, 2, 3 and 4.
3, 2, 6, 7	ISEN [1:4] N	Negative Current Sense Pin of Phase 1, 2, 3 and 4.
9	RSET	Multi-Phase CORE VR Ramp Setting. This is used to set the multi-phase CORE VR loop external ramp slope.
10	COMP	Multi-Phase CORE VR Compensation. This pin is the output node of the error amplifier.
11	FB	Multi-Phase CORE VR Feedback. This is the negative input node of the error amplifier.
12	RGND	Return Ground for Multi-Phase CORE VR. This pin is the negative node of the differential remote voltage sensing.
13	DVID	Connect a resistor and a capacitor from this pin to GND to improve DVID performance. Short this pin to GND if this function is not needed.
14	OFS	Output Voltage Offset Setting.
15	IMON	Current Monitor Output. This pin outputs a voltage proportional to the output current.
16	IMONFB	Current Monitor Output Gain External Setting. Connect this pin with one resistor to CPU V_{CC_SENSE}, while the IMON pin is connected to ground with another resistor. The current monitor output gain can be set by the ratio of these two resistors.
17	ADD	VR Address Setting Pin.
18	VCLK	Synchronous Clock from CPU.
19	VDIO	Controller and CPU Data Transmission Interface.
20	$\overline{\text{ALERT}}$	SVID Alert Pin (Active Low).
21	IBIAS	Internal Bias Current Setting. Connect this pin to GND via a resistor to set the internal current.
22	SETINI	CORE VR $V_{INITIAL}$ Setting.
23	SETINIA	AXG VR $V_{INITIALA}$ Setting.
24	TMPMAX	ADC Input for Multi-Phase CORE VR Maximum Temperature Setting. This pin is also used for AXG VR's offset selection.
25	ICCMAX	ADC Input for Multi-Phase CORE VR Maximum Current Setting. This pin is also used for CORE VR's offset selection.
26	ICCMAXA	ADC Input for Single-Phase AXG VR Maximum Current Setting.
27	IMONFBA	Single-Phase AXG VR Current Monitor Output Gain External Setting. Connect this pin with one resistor to AXG rail V_{CCAXG_SENSE}, while IMONA pin is connected to ground with another resistor. The current monitor output gain can be set by the ratio of these two resistors.
28	IMONA	Single-Phase AXG VR Current Monitor Output. This pin outputs a voltage proportional to the output current.
29	SR_ADDF	Address Flip and DVID Slew Rate Setting. Set the pin to GND if fast slew rate= 10mV/μs and slow slew rate = 2.5mV/μs is used.
30	OFSA	AXG VR Output Voltage Offset Setting.
31	RGNDA	Return Ground for Single-Phase AXG VR. This pin is the negative node of the differential remote voltage sensing.

Pin No.	Pin Name	Pin Function
32	FBA	Single-Phase AXG VR Feedback. This is the negative input node of the error amplifier.
33	COMPA	Single-Phase AXG VR Compensation. This pin is the output node of the error amplifier.
34	ISENAN	Negative Current Sense Pin of Single-Phase AXG VR.
35	ISENAP	Positive Current Sense Pin of Single-Phase AXG VR.
36	QRSETA	Single-Phase AXG VR Quick Response Time Setting.
37	PWMA	PWM Output for Single-Phase AXG VR.
38	EN	Chip Enable (Active High)
39	VRA_RDY	VR Ready Indicator of Single-Phase AXG VR.
40	VR_RDY	VR Ready Indicator of Multi-Phase CORE VR.
41	VCC	Chip Power. Connect this pin to 5V via an RC filter.
42	OCSETA	Single-Phase AXG VR Over Current Protection Setting. Place a resistive voltage divider between VCC and ground and connect the joint of the voltage divider to the OCSETA pin. The voltage at the OCSET pin determines the over current threshold, I_{LIMITA}.
43	OCSET	Multi-Phase CORE VR Over Current Protection Setting. Place a resistive voltage divider between VCC and ground and connect the joint of the voltage divider to the OCSET pin. The voltage at the OCSET pin determines the over current threshold, I_{LIMIT}.
44	TSENA	Thermal Monitor Sense Point of AXG VR.
45	TSEN	Thermal Monitor Sense Point of CORE VR.
46	$\overline{\text{VRHOT}}$	Thermal Monitor Output (Active Low).
47	DVDA	Divided Voltage Detection of AXG VR. Connect this pin to a voltage divider from the single-phase power stage input power for input voltage detection.
48	DVD	Divided Voltage Detection of CORE VR. Connect this pin to a voltage divider from the multi-phase power stage input power for input voltage detection.
49	TONSETA	Single-Phase AXG VR On-Time Setting. Connect this pin to V_{IN} with one resistor to set ripple size in PWM mode.
50	TONSET	Multi-Phase CORE VR On-Time Setting. Connect this pin to V_{IN} with one resistor to set ripple size in PWM mode.
51, 52, 54, 53	PWM [4 :1]	PWM Output for CH1, 2, 3 and 4.
55	QRSET	Multi-Phase CORE VR Quick Response Time Setting.
56	DVIDA	Connect a resistor and a capacitor from this pin to GND to improve DVID performance. Short this pin to GND if this function is not needed.
57 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram

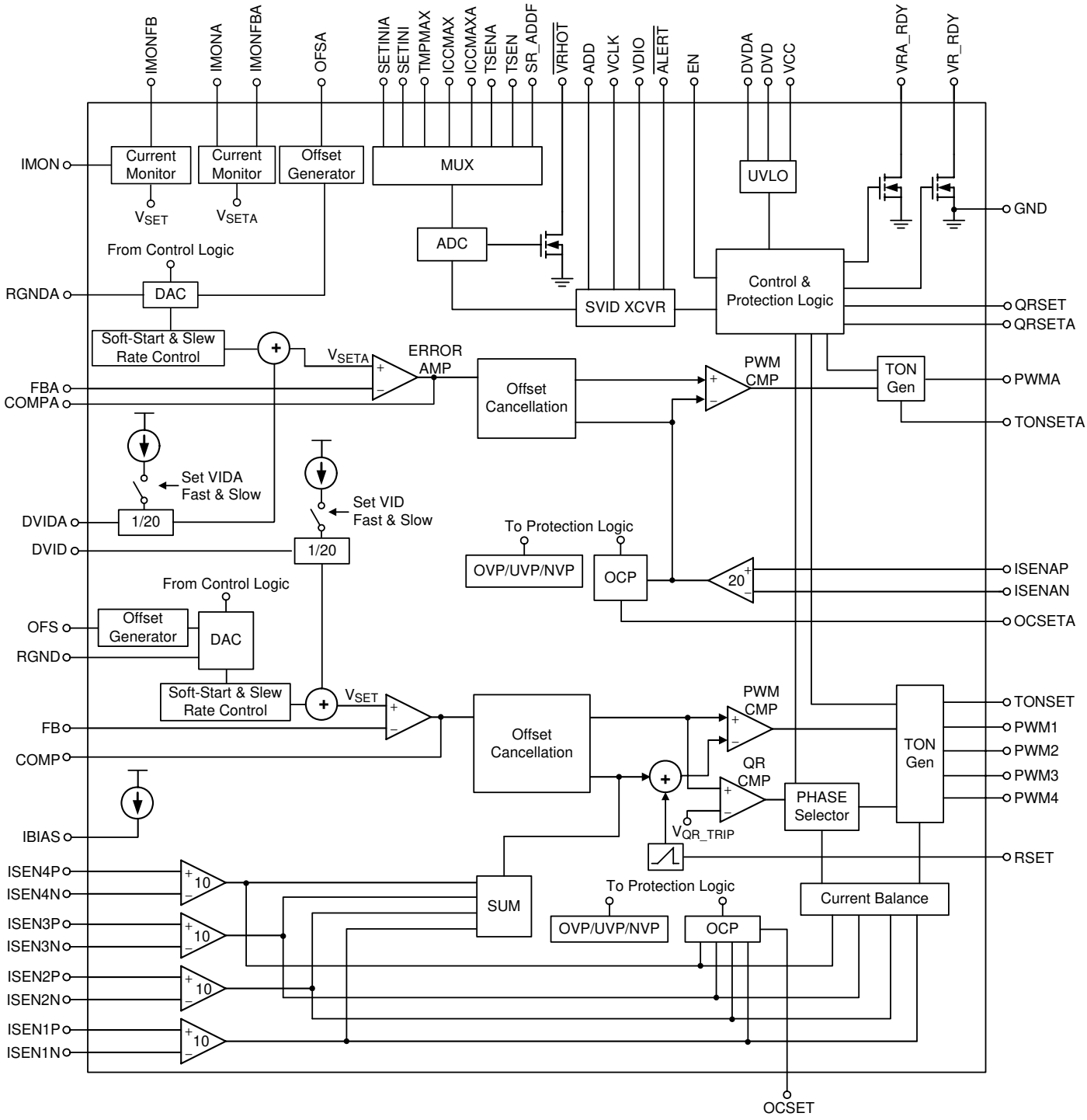


Table 1. VR12 VID Code Table

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		Voltage
0	0	0	0	0	0	0	0	0	0	0.000
0	0	0	0	0	0	0	1	0	1	0.250
0	0	0	0	0	0	1	0	0	2	0.255
0	0	0	0	0	0	1	1	0	3	0.260
0	0	0	0	0	1	0	0	0	4	0.265
0	0	0	0	0	1	0	1	0	5	0.270
0	0	0	0	0	1	1	0	0	6	0.275
0	0	0	0	0	1	1	1	0	7	0.280
0	0	0	0	1	0	0	0	0	8	0.285
0	0	0	0	1	0	0	1	0	9	0.290
0	0	0	0	1	0	1	0	0	A	0.295
0	0	0	0	1	0	1	1	0	B	0.300
0	0	0	0	1	1	0	0	0	C	0.305
0	0	0	0	1	1	0	1	0	D	0.310
0	0	0	0	1	1	1	0	0	E	0.315
0	0	0	0	1	1	1	1	0	F	0.320
0	0	0	1	0	0	0	0	1	0	0.325
0	0	0	1	0	0	0	1	1	1	0.330
0	0	0	1	0	0	1	0	1	2	0.335
0	0	0	1	0	0	1	1	1	3	0.340
0	0	0	1	0	1	0	0	1	4	0.345
0	0	0	1	0	1	0	1	1	5	0.350
0	0	0	1	0	1	1	0	1	6	0.355
0	0	0	1	0	1	1	1	1	7	0.360
0	0	0	1	1	0	0	0	1	8	0.365
0	0	0	1	1	0	0	1	1	9	0.370
0	0	0	1	1	0	1	0	1	A	0.375
0	0	0	1	1	0	1	1	1	B	0.380
0	0	0	1	1	1	0	0	1	C	0.385
0	0	0	1	1	1	0	1	1	D	0.390
0	0	0	1	1	1	1	0	1	E	0.395
0	0	0	1	1	1	1	1	1	F	0.400
0	0	1	0	0	0	0	0	2	0	0.405
0	0	1	0	0	0	0	1	2	1	0.410
0	0	1	0	0	0	1	0	2	2	0.415
0	0	1	0	0	0	1	1	2	3	0.420
0	0	1	0	0	1	0	0	2	4	0.425
0	0	1	0	0	1	0	1	2	5	0.430
0	0	1	0	0	1	1	0	2	6	0.435
0	0	1	0	0	1	1	1	2	7	0.440
0	0	1	0	1	0	0	0	2	8	0.445

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		Voltage
0	0	1	0	1	0	0	1	2	9	0.450
0	0	1	0	1	0	1	0	2	A	0.455
0	0	1	0	1	0	1	1	2	B	0.460
0	0	1	0	1	1	0	0	2	C	0.465
0	0	1	0	1	1	0	1	2	D	0.470
0	0	1	0	1	1	1	0	2	E	0.475
0	0	1	0	1	1	1	1	2	F	0.480
0	0	1	1	0	0	0	0	3	0	0.485
0	0	1	1	0	0	0	1	3	1	0.490
0	0	1	1	0	0	1	0	3	2	0.495
0	0	1	1	0	0	1	1	3	3	0.500
0	0	1	1	0	1	0	0	3	4	0.505
0	0	1	1	0	1	0	1	3	5	0.510
0	0	1	1	0	1	1	0	3	6	0.515
0	0	1	1	0	1	1	1	3	7	0.520
0	0	1	1	1	0	0	0	3	8	0.525
0	0	1	1	1	0	0	1	3	9	0.530
0	0	1	1	1	0	1	0	3	A	0.535
0	0	1	1	1	0	1	1	3	B	0.540
0	0	1	1	1	1	0	0	3	C	0.545
0	0	1	1	1	1	0	1	3	D	0.550
0	0	1	1	1	1	1	0	3	E	0.555
0	0	1	1	1	1	1	1	3	F	0.560
0	1	0	0	0	0	0	0	4	0	0.565
0	1	0	0	0	0	0	1	4	1	0.570
0	1	0	0	0	0	1	0	4	2	0.575
0	1	0	0	0	0	1	1	4	3	0.580
0	1	0	0	0	1	0	0	4	4	0.585
0	1	0	0	0	1	0	1	4	5	0.590
0	1	0	0	0	1	1	0	4	6	0.595
0	1	0	0	0	1	1	1	4	7	0.600
0	1	0	0	1	0	0	0	4	8	0.605
0	1	0	0	1	0	0	1	4	9	0.610
0	1	0	0	1	0	1	0	4	A	0.615
0	1	0	0	1	0	1	1	4	B	0.620
0	1	0	0	1	1	0	0	4	C	0.625
0	1	0	0	1	1	0	1	4	D	0.630
0	1	0	0	1	1	1	0	4	E	0.635
0	1	0	0	1	1	1	1	4	F	0.640
0	1	0	1	0	0	0	0	5	0	0.645
0	1	0	1	0	0	0	1	5	1	0.650
0	1	0	1	0	0	1	0	5	2	0.655

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		Voltage
0	1	0	1	0	0	1	1	5	3	0.660
0	1	0	1	0	1	0	0	5	4	0.665
0	1	0	1	0	1	0	1	5	5	0.670
0	1	0	1	0	1	1	0	5	6	0.675
0	1	0	1	0	1	1	1	5	7	0.680
0	1	0	1	1	0	0	0	5	8	0.685
0	1	0	1	1	0	0	1	5	9	0.690
0	1	0	1	1	0	1	0	5	A	0.695
0	1	0	1	1	0	1	1	5	B	0.700
0	1	0	1	1	1	0	0	5	C	0.705
0	1	0	1	1	1	0	1	5	D	0.710
0	1	0	1	1	1	1	0	5	E	0.715
0	1	0	1	1	1	1	1	5	F	0.720
0	1	1	0	0	0	0	0	6	0	0.725
0	1	1	0	0	0	0	1	6	1	0.730
0	1	1	0	0	0	1	0	6	2	0.735
0	1	1	0	0	0	1	1	6	3	0.740
0	1	1	0	0	1	0	0	6	4	0.745
0	1	1	0	0	1	0	1	6	5	0.750
0	1	1	0	0	1	1	0	6	6	0.755
0	1	1	0	0	1	1	1	6	7	0.760
0	1	1	0	1	0	0	0	6	8	0.765
0	1	1	0	1	0	0	1	6	9	0.770
0	1	1	0	1	0	1	0	6	A	0.775
0	1	1	0	1	0	1	1	6	B	0.780
0	1	1	0	1	1	0	0	6	C	0.785
0	1	1	0	1	1	0	1	6	D	0.790
0	1	1	0	1	1	1	0	6	E	0.795
0	1	1	0	1	1	1	1	6	F	0.800
0	1	1	1	0	0	0	0	7	0	0.805
0	1	1	1	0	0	0	1	7	1	0.810
0	1	1	1	0	0	1	0	7	2	0.815
0	1	1	1	0	0	1	1	7	3	0.820
0	1	1	1	0	1	0	0	7	4	0.825
0	1	1	1	0	1	0	1	7	5	0.830
0	1	1	1	0	1	1	0	7	6	0.835
0	1	1	1	0	1	1	1	7	7	0.840
0	1	1	1	1	0	0	0	7	8	0.845
0	1	1	1	1	0	0	1	7	9	0.850
0	1	1	1	1	0	1	0	7	A	0.855
0	1	1	1	1	0	1	1	7	B	0.860

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		Voltage
0	1	1	1	1	1	0	0	7	C	0.865
0	1	1	1	1	1	0	1	7	D	0.870
0	1	1	1	1	1	1	0	7	E	0.875
0	1	1	1	1	1	1	1	7	F	0.880
1	0	0	0	0	0	0	0	8	0	0.885
1	0	0	0	0	0	0	1	8	1	0.890
1	0	0	0	0	0	1	0	8	2	0.895
1	0	0	0	0	0	1	1	8	3	0.900
1	0	0	0	0	1	0	0	8	4	0.905
1	0	0	0	0	1	0	1	8	5	0.910
1	0	0	0	0	1	1	0	8	6	0.915
1	0	0	0	0	1	1	1	8	7	0.920
1	0	0	0	1	0	0	0	8	8	0.925
1	0	0	0	1	0	0	1	8	9	0.930
1	0	0	0	1	0	1	0	8	A	0.935
1	0	0	0	1	0	1	1	8	B	0.940
1	0	0	0	1	1	0	0	8	C	0.945
1	0	0	0	1	1	0	1	8	D	0.950
1	0	0	0	1	1	1	0	8	E	0.955
1	0	0	0	1	1	1	1	8	F	0.960
1	0	0	1	0	0	0	0	9	0	0.965
1	0	0	1	0	0	0	1	9	1	0.970
1	0	0	1	0	0	1	0	9	2	0.975
1	0	0	1	0	0	1	1	9	3	0.980
1	0	0	1	0	1	0	0	9	4	0.985
1	0	0	1	0	1	0	1	9	5	0.990
1	0	0	1	0	1	1	0	9	6	0.995
1	0	0	1	0	1	1	1	9	7	1.000
1	0	0	1	1	0	0	0	9	8	1.005
1	0	0	1	1	0	0	1	9	9	1.010
1	0	0	1	1	0	1	0	9	A	1.015
1	0	0	1	1	0	1	1	9	B	1.020
1	0	0	1	1	1	0	0	9	C	1.025
1	0	0	1	1	1	0	1	9	D	1.030
1	0	0	1	1	1	1	0	9	E	1.035
1	0	0	1	1	1	1	1	9	F	1.040
1	0	1	0	0	0	0	0	A	0	1.045
1	0	1	0	0	0	0	1	A	1	1.050
1	0	1	0	0	0	1	0	A	2	1.055
1	0	1	0	0	0	1	1	A	3	1.060
1	0	1	0	0	1	0	0	A	4	1.065

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		Voltage
1	0	1	0	0	1	0	1	A	5	1.070
1	0	1	0	0	1	1	0	A	6	1.075
1	0	1	0	0	1	1	1	A	7	1.080
1	0	1	0	1	0	0	0	A	8	1.085
1	0	1	0	1	0	0	1	A	9	1.090
1	0	1	0	1	0	1	0	A	A	1.095
1	0	1	0	1	0	1	1	A	B	1.100
1	0	1	0	1	1	0	0	A	C	1.105
1	0	1	0	1	1	0	1	A	D	1.110
1	0	1	0	1	1	1	0	A	E	1.115
1	0	1	0	1	1	1	1	A	F	1.120
1	0	1	1	0	0	0	0	B	0	1.125
1	0	1	1	0	0	0	1	B	1	1.130
1	0	1	1	0	0	1	0	B	2	1.135
1	0	1	1	0	0	1	1	B	3	1.140
1	0	1	1	0	1	0	0	B	4	1.145
1	0	1	1	0	1	0	1	B	5	1.150
1	0	1	1	0	1	1	0	B	6	1.155
1	0	1	1	0	1	1	1	B	7	1.160
1	0	1	1	1	0	0	0	B	8	1.165
1	0	1	1	1	0	0	1	B	9	1.170
1	0	1	1	1	0	1	0	B	A	1.175
1	0	1	1	1	0	1	1	B	B	1.180
1	0	1	1	1	1	0	0	B	C	1.185
1	0	1	1	1	1	0	1	B	D	1.190
1	0	1	1	1	1	1	0	B	E	1.195
1	0	1	1	1	1	1	1	B	F	1.200
1	1	0	0	0	0	0	0	C	0	1.205
1	1	0	0	0	0	0	1	C	1	1.210
1	1	0	0	0	0	1	0	C	2	1.215
1	1	0	0	0	0	1	1	C	3	1.220
1	1	0	0	0	1	0	0	C	4	1.225
1	1	0	0	0	1	0	1	C	5	1.230
1	1	0	0	0	1	1	0	C	6	1.235
1	1	0	0	0	1	1	1	C	7	1.240
1	1	0	0	1	0	0	0	C	8	1.245
1	1	0	0	1	0	0	1	C	9	1.250
1	1	0	0	1	0	1	0	C	A	1.255
1	1	0	0	1	0	1	1	C	B	1.260
1	1	0	0	1	1	0	0	C	C	1.265
1	1	0	0	1	1	0	1	C	D	1.270

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		Voltage
1	1	0	0	1	1	1	0	C	E	1.275
1	1	0	0	1	1	1	1	C	F	1.280
1	1	0	1	0	0	0	0	D	0	1.285
1	1	0	1	0	0	0	1	D	1	1.290
1	1	0	1	0	0	1	0	D	2	1.295
1	1	0	1	0	0	1	1	D	3	1.300
1	1	0	1	0	1	0	0	D	4	1.305
1	1	0	1	0	1	0	1	D	5	1.310
1	1	0	1	0	1	1	0	D	6	1.315
1	1	0	1	0	1	1	1	D	7	1.320
1	1	0	1	1	0	0	0	D	8	1.325
1	1	0	1	1	0	0	1	D	9	1.330
1	1	0	1	1	0	1	0	D	A	1.335
1	1	0	1	1	0	1	1	D	B	1.340
1	1	0	1	1	1	0	0	D	C	1.345
1	1	0	1	1	1	0	1	D	D	1.350
1	1	0	1	1	1	1	0	D	E	1.355
1	1	0	1	1	1	1	1	D	F	1.360
1	1	1	0	0	0	0	0	E	0	1.365
1	1	1	0	0	0	0	1	E	1	1.370
1	1	1	0	0	0	1	0	E	2	1.375
1	1	1	0	0	0	1	1	E	3	1.380
1	1	1	0	0	1	0	0	E	4	1.385
1	1	1	0	0	1	0	1	E	5	1.390
1	1	1	0	0	1	1	0	E	6	1.395
1	1	1	0	0	1	1	1	E	7	1.400
1	1	1	0	1	0	0	0	E	8	1.405
1	1	1	0	1	0	0	1	E	9	1.410
1	1	1	0	1	0	1	0	E	A	1.415
1	1	1	0	1	0	1	1	E	B	1.420
1	1	1	0	1	1	0	0	E	C	1.425
1	1	1	0	1	1	0	1	E	D	1.430
1	1	1	0	1	1	1	0	E	E	1.435
1	1	1	0	1	1	1	1	E	F	1.440
1	1	1	1	0	0	0	0	F	0	1.445
1	1	1	1	0	0	0	1	F	1	1.450
1	1	1	1	0	0	1	0	F	2	1.455
1	1	1	1	0	0	1	1	F	3	1.460
1	1	1	1	0	1	0	0	F	4	1.465
1	1	1	1	0	1	0	1	F	5	1.470
1	1	1	1	0	1	1	0	F	6	1.475

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	Hex		Voltage
1	1	1	1	0	1	1	1	F	7	1.480
1	1	1	1	1	0	0	0	F	8	1.485
1	1	1	1	1	0	0	1	F	9	1.490
1	1	1	1	1	0	1	0	F	A	1.495
1	1	1	1	1	0	1	1	F	B	1.500
1	1	1	1	1	1	0	0	F	C	1.505
1	1	1	1	1	1	0	1	F	D	1.510
1	1	1	1	1	1	1	0	F	E	1.515
1	1	1	1	1	1	1	1	F	F	1.520

Table 2. Serial VID Command

Code	Commands	Master Payload Contents	Slave Payload Contents	Description
00h	Not Supported	N/A	N/A	N/A
01h	SetVID_Fast	VID code	N/A	Set new target VID code, VR jumps to new VID target with controlled default “fast” slew rate 12.5mV/μs.
02h	SetVID_Slow	VID code	N/A	Set new target VID code, VR jumps to new VID target with controlled default “slow” slew rate 3.125mV/μs.
03h	SetVID_Decay	VID code	N/A	Set new target VID code, VR jumps to new VID target, but doest not control the slew rate. The output voltage decays at a rate proportional to the load current
04h	SetPS	Byte indicating power states	N/A	Set power state
05h	SetRegADR	Pointer of registers in data table	N/A	Set the pointer of the data register
06h	SetRegDAT	New data register content	N/A	Write the contents to the data register
07h	GetReg	Pointer of registers in data table	Specified register contents	Slave returns the contents of the specified register as the payload.
08h - 1Fh	Not Supported	N/A	N/A	N/A

Table 3. SVID Data and Configuration Register

Index	Register Name	Description	Access	Default
00h	Vendor_ID	Vendor ID	RO	1Eh
01h	Product_ID	Product ID	RO	59h
02h	Product_Revision	Product Revision	RO	03h
05h	Protocol_Version	SVID Protocol version	RO	01h
06h	VR_Capability	Bit mapped register, identifies the SVID VR Capabilities and which of the optional telemetry register are supported.	RO	81h
10h	Status_1	Data register containing the status of VR	R-M, W-PWM	00h
11h	Status_2	Data register containing the status of transmission.	R-M, W-PWM	00h
12h	Temperature_Zone	Data register showing temperature Zone that have been entered.	R-M, W-PWM	00h
15h	Output_Current	Data register showing direct ADC conversion of output current, scaled to ICC_MAX = ADC full range. Binary format (IE : 64h = 100/255 ICC_MAX)	R-M, W-PWM	00h
1Ch	Status_2_Lastread	The register contains a copy of the Status_2	R-M, W-PWM	00h
21h	ICC_Max	Data register containing the maximum ICC the platform supports. Binary format in A. (IE : 64h = 100A)	RO, Platform	N/A
22h	Temp_Max	Data register containing the maximum temperature the platform supports. Binary format in °C. (IE : 64h = 100°C) Not supported by AXG VR.	RO, Platform	N/A
24h	SR_fast	Data register containing the capability of fast slew rate the platform can sustain. Binary format in mV/μs. (IE : 0Ah = 10 mV/μs)	RO	0Ah
25h	SR_slow	Data register containing the capability of slow slew rate. Binary format in mV/μs. (IE : 02h = 2mV/μs)	RO	02h
30h	VOUT_Max	The register is programmed by the master and sets the maximum VID.	RW, Master	FBh
31h	VID_Setting	Data register containing currently programmed VID	RW, Master	00h
32h	Power_State	Register containing the current programmed power state	RW, Master	00h
33h	Offset	Set offset in VID steps	RW, Master	00h
34h	Multi_VR_Config	Bit mapped data register which configures multiple VRs' behavior on the same bus	RW, Master	00h
35h	Pointer	Scratch pad register for temporary storage of the SetRegADR pointer register	RW, Master	30h

Notes :

RO = Read Only

RW = Read/Write

R-M = Read by Master

W-PWM = Write by PWM only

Platform = programmed by platform

Master = programmed by the master

PWM = programmed by the VR control IC

Absolute Maximum Ratings (Note 1)

- VCC to GND ---------- –0.3V to 6.5V
- RGNDx to GND ---------- –0.3V to 0.3V
- TONSETx to GND ---------- –0.3V to 28V
- Others ---------- –0.3V to (VCC + 0.3V)
- Power Dissipation, P_D @ T_A = 25°C
  WQFN–56L 7x7 ---------- 3.226W
- Package Thermal Resistance (Note 2)
  WQFN–56L 7x7, θ_{JA} ---------- 31°C/W
  WQFN–56L 7x7, θ_{JC} ---------- 6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC ---------- 4.5V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Input						
Supply Current	I_{VCC}	V_{EN} = 1.05V, Not Switching	--	12	20	mA
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	5	μA
Reference and DAC						
DAC Accuracy	V_{FB}	V_{DAC} = 1.000 to 1.520 (No Load, Active Mode)	–0.5	0	0.5	%VID
		V_{DAC} = 0.800 to 1.000	–5	0	5	mV
		V_{DAC} = 0.500 to 0.800	–8	0	8	mV
		V_{DAC} = 0.250 to 0.500	–8	0	8	mV
RGND Current						
RGND Current	I_{RGND}	V_{EN} = 1.05V, Not Switching	--	--	500	μA
Slew Rate						
Dynamic VID Slew Rate	SR	Set VID Slow, SR_ADDF pin = 0V	2.5	3.125	3.75	mV/μs
		Set VID Fast, SR_ADDF pin = 0V	10	12.5	15	
Error Amplifier						
DC Gain	A_{DC}	R_{LOAD} = 47kΩ	--	80	--	dB
Gain-Bandwidth Product	GBW	C_{LOAD} = 5pF	--	10	--	MHz
Slew Rate	SR	C_{LOAD} = 10pF (Gain = –4, R_{LOAD} = 47kΩ, V_{OUT} = 0.5V to –3V)	--	5	--	V/μs

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage Range	V_{COMP}	R_{LOAD} = 47kΩ	0.3	--	3.6	V
MAX Source/Sink Current	I_{OUTEA}	V_{COMP} = 2V	--	250	--	μA
Current Sense Amplifier						
Input Offset Voltage	V_{OSCS}		–0.75	--	0.75	mV
Impedance at Negative Input	R_{ISENxN}		1	--	--	MΩ
Impedance at Positive Input	R_{ISENxP}		1	--	--	MΩ
DC Gain		CORE VR	--	10	--	V/V
		AXG VR	--	20	--	
Input Range	V_{ISEN_IN}		–50	--	100	mV
V_{ISEN} Linearity	V_{ISEN_ACC}	–30mV < V_{ISEN_IN} < 50mV	–1	--	1	%
t_{ON} Setting						
TONSETx Pin Voltage	V_{TON}	I_{RTON} = 80μA, V_{DAC} = 0.75V	--	1.07	--	V
CCM On-Time Setting	t_{ON}	I_{RTON} = 80μA, PS0, PS1	275	305	335	ns
TONSETx Input Current Range	I_{RTON}		25	--	280	μA
On-Time in PS2 (Core only)	t_{ON_PS2}	With Respect to PS0 t_{ON}	--	85	--	%
Minimum Off-Time	t_{OFF}		--	250	--	ns
IBIAS						
IBIAS Pin Voltage	V_{IBIAS}	R_{IBIAS} = 53.6kΩ	2.09	2.14	2.19	V
QRSET						
Quick Response On-Time Setting	t_{ONx_QR}	V_{DAC} = 0.75V, V_{QRSET} = 1.2V, I_{RTON} = 80μA	--	305	--	ns
QRSET Source Current	I_{QRSET}	Before UVLO	--	80	--	μA
No Load Line Setting Threshold	V_{IH}	QRSET Voltage before UVLO, Relative to V_{CC}	V_{CC} – 0.5	--	--	V
	V_{IL}		--	--	V_{CC} – 1.8	V
OFS Function						
OFS Enable/Disable Threshold Voltage	V_{EN_OFS}	V_{OFS} > V_{EN_OFS} before EN rising	0.7	1.2	--	V
Offset Voltage	V_{OUT}	VID = 1V, V_{OFS} = 1.83V	1.62	1.63	1.64	V
		VID = 1V, V_{OFS} = 0.9V	0.69	0.7	0.71	
		VID = 1V, V_{OFS} = 1.2V	0.9	1	1.01	
Impedance	R_{OFS}		1	--	--	MΩ
RSET Setting						
RSET Voltage	V_{RSET}	RSET Voltage, V_{DAC} = 1V	0.97	1	1.03	V
Zero Current Detection						
Zero Current Detection Threshold	V_{ZCD}	ISEN1P (AP) – ISEN1N (AN)	--	1	--	mV
Protection						
Under Voltage Lock-out (UVLO)Threshold	V_{UVLO}	Falling Edge, 100mV Hysteresis	4.04	4.24	4.44	V
	ΔV_{UVLO}	Falling Edge Hysteresis	--	100	--	mV
Absolute Over Voltage (OVP) Protection Threshold	V_{OVABS}	With respect to V_{OUT_Max}	100	150	200	mV

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Divided Input Voltage Detection (DVDx) Threshold		V_{DVDx}	V_{DVDx} Threshold	1.01	1.06	1.11	V
		V_{DVDHYS}	Falling Edge Hysteresis	--	25	--	mV
Delay of UVLO, DVDx		t_{UVLO}	Rising Above Threshold	--	3	--	μs
Delay of OVP		t_{OV}	V_{ISENxN} Rising Above Threshold, Pin OFS Disable	--	1	--	μs
Under Voltage Protection (UVP) Threshold		V_{UV}	Measured at ISEN1N/ISENAN with respect to unloaded output voltage (UOV) (for 0.8 < UOV < 1.52)	–350	–300	–250	mV
Delay of UVP		t_{UVP}	V_{ISENxN} Falling below Threshold	--	3	--	μs
Negative Voltage Protection Threshold		V_{NVP}	After OVP, Falling Edge	–100	–50	--	mV
Delay of NVP		t_{NVP}	V_{ISENxN} Falling below Threshold	--	1	--	μs
Current Limit Gain Setting (per phase)		G_{ILIMIT}	$G_{ILIMIT} = V_{OCSET} / (V_{ISENxP} - V_{ISENxN})$, V_{OCSET} = 2.400V, $(V_{ISENxP} - V_{ISENxN})$ = 50mV	43.2	48	52.8	V/V
			$G_{ILIMITA} = V_{OCSETA} / (V_{ISENAP} - V_{ISENAN})$, V_{OCSETA} = 2.4V, $(V_{ISENAP} - V_{ISENAN})$ = 50mV	43.2	48	52.8	
Current Limit Latch Counter (per phase)		N_{ILIM}	Times of UGATE Rising	--	15	--	Times
EN Input Threshold Voltage	Logic-High	V_{IH}		0.7	--	--	V
	Logic-Low	V_{IL}		--	--	0.3	
Logic Inputs							
EN Hysteresis		V_{ENHYS}		--	30	--	mV
Leakage Current of EN		I_{EN}		–1	--	1	μA
VCLK, VDIO Input Threshold Voltage	Logic-High	V_{IH}		0.665	--	--	V
	Logic-Low	V_{IL}		--	--	0.367	
VCLK,VDIO Hysteresis		V_{HYS}		--	70	--	mV
Leakage Current of ADD,VCLK,VDIO		I_{LEAK_IN}		–1	--	1	μA
$\overline{\text{ALERT}}$							
$\overline{\text{ALERT}}$ Low Voltage		$V_{\overline{ALERT}}$	$I_{\overline{ALERT}}$ = 10mA	--	--	0.13	V
Power On Sequence							
SVID Ready Delay Time		t_A	From EN = high until VR Controller is ready to accept SVID command	--	--	2	ms
VR_RDY Trip Threshold		$V_{TH\_VR\_RDY}$	V_{ISENxN} – 1st V_{DAC}	--	–100	--	mV
VR_RDY Low Voltage		V_{VR_RDY}	I_{VR_RDY} = 4mA	--	--	0.4	V
VR_RDY Delay		t_{VR_RDY}	V_{ISENxN} = $V_{INITIAL}$ to VR_RDY High	--	100	--	μs

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Throttling							
$\overline{\text{VRHOT}}$ Output Voltage		$V_{\overline{\text{VRHOT}}}$	$I_{\overline{\text{VRHOT}}}$ = 10mA	--	--	0.13	V
Current Monitor							
Current Monitor Maximum Output Voltage in Operating Range		V_{IMON}	V_{DAC} = 1V, $V_{FB} - V_{CC\_SENSE}$ = 100mV, R_{IMONFB} = 10kΩ, R_{IMON} = 330kΩ	3.2	3.3	3.4	V
High Impedance Output							
PWMx, $\overline{\text{ALERT}}$, VRx_RDY, $\overline{\text{VRHOT}}$		I_{LEAK_OUT}		–1	--	1	μA
PWM Driving Capability							
PWM Source Resistor		R_{PWM_SOURCE}		--	30	--	Ω
PWM Sink Resistor		R_{PWM_SINK}		--	15	--	Ω
DVID, DVIDA, ICCMAX, ICCMAXA, and TMPMAX Pin Current							
Current Sourcing Out from DVIDx Pin to GND		I_{DVIDx}	During dynamic VID fast event	6	8	10	μA
Current Sinking In from 5V to ICCMAX Pin		I_{ICCMAX}	After VR_RDY	--	16	--	μA
Current Sourcing Out from ICCMAXA Pin to GND		$I_{ICCMAXA}$	After VRA_RDY	--	128	--	μA
Current Sinking In from 5V to TMPMAX Pin		I_{TMPMAX}	After VR_RDY	--	16	--	μA
DVID and DVIDA Maximum Voltage							
Maximum Allowable Voltage at DVIDx Pin		V_{DVIDx_MAX}	During Dynamic VID Event	--	--	2	V
SVID							
SVID Frequency		f_{SVID}		5	25	26.25	MHz
SVID Clock to Data Delay		t_{CO}		4	--	8.3	ns
Setup Time of VDIO		t_{SU}		7	--	--	ns
Hold Time of VDIO		t_{HLD}		14	--	--	ns
$V_{INITIAL}$ Setting							
SETINIx Threshold Voltage		$V_{SETINI0}$	For $V_{INITIAL}$ = 0V	0	--	8	%V_{CC}
		$V_{SETINI0\_9}$	For $V_{INITIAL}$ = 0.9V	17	--	20	
		$V_{SETINI1\_0}$	For $V_{INITIAL}$ = 1V	32.5	--	42.5	
		$V_{SETINI1\_1}$	For $V_{INITIAL}$ = 1.1V	57.5	--	67.5	
		$V_{SETINI1\_5}$	For $V_{INITIAL}$ = 1.5V	82.5	--	100	
ADD Threshold							
ADD Input Threshold Voltage	Logic-Low	V_{IL}	Set SVID address 0000 0001	--	--	0.35	V
	Logic-Medium	V_{IM}	Set SVID address 0010 0011	0.7	--	3	
	Logic-High	V_{IH}	Set SVID address 0100 0101	V_{CC} – 0.2	--	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADC						
Digital Code of ICCMAX	$C_{ICCMAX1}$	V_{ICCMAX} = 12.74%V_{CC}	29	32	35	decimal
	$C_{ICCMAX2}$	V_{ICCMAX} = 25.284%V_{CC}	61	64	67	
	$C_{ICCMAX3}$	V_{ICCMAX} = 50.372%V_{CC}	125	128	131	
Digital Code of ICCMAXA	$C_{ICCMAXA1}$	V_{ICCMAX} = 3.332%V_{CC}	5	8	11	decimal
	$C_{ICCMAXA2}$	V_{ICCMAX} = 6.468%V_{CC}	13	16	19	
	$C_{ICCMAXA3}$	V_{ICCMAX} = 12.74%V_{CC}	29	32	35	
Digital Code of TMPMAX	$C_{TMPMAX1}$	V_{ICCMAX} = 33.516%V_{CC}	82	85	88	decimal
	$C_{TMPMAX2}$	V_{ICCMAX} = 39.396%V_{CC}	97	100	103	
	$C_{TMPMAX3}$	V_{ICCMAX} = 49.196%V_{CC}	122	125	128	
Digital Code of Output Current Report	C_{OCR1}	$V_{IMON(A)}$ = 3.3V	252	255	255	decimal
	C_{OCR2}	$V_{IMON(A)}$ = 2.208V	167	170	173	
	C_{OCR3}	$V_{IMON(A)}$ = 1.107V	82	85	88	
Updating Period of Output Current Report	t_{OCR}		--	--	500	μs
Tolerance Band of Temperature_Zone Trip Points b7, b6, b5	V_{TSEN}		20	--	20	mV
Updating Period of Temperature_Zone	t_{TZ}		--	--	4	ms

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

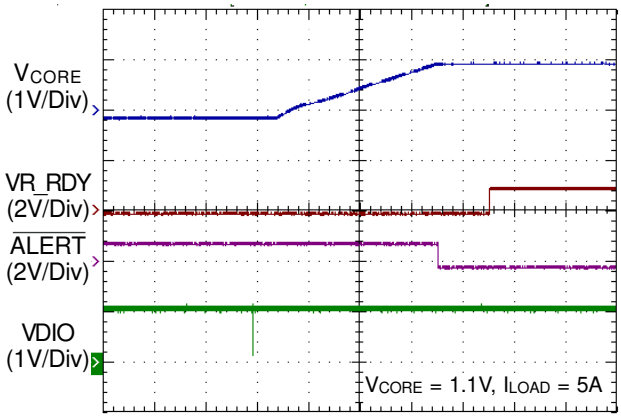
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

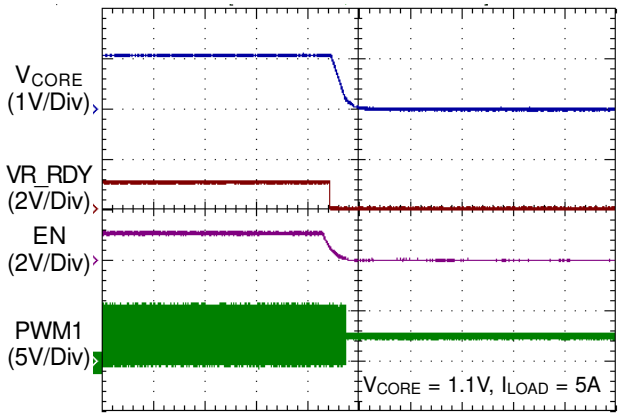
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

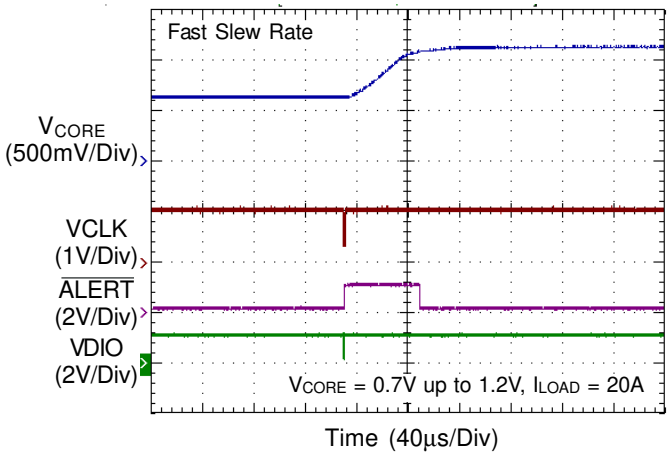
CORE VR Power On



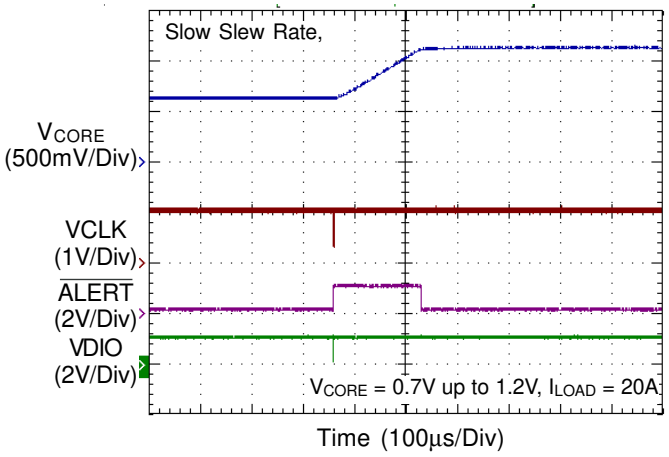
CORE VR Power Off from EN



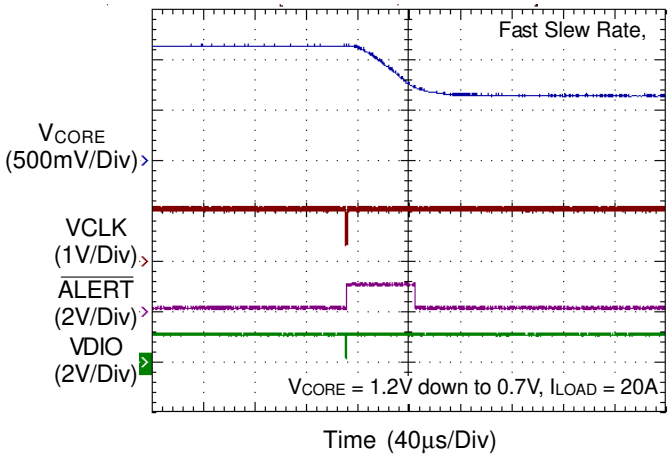
CORE VR Dynamic VID Up



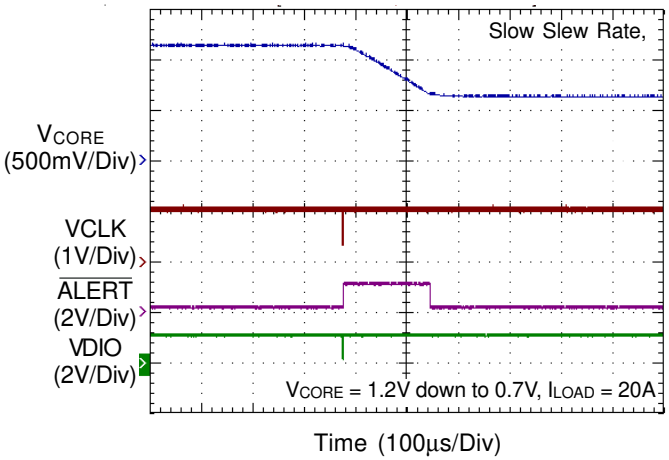
CORE VR Dynamic VID Up



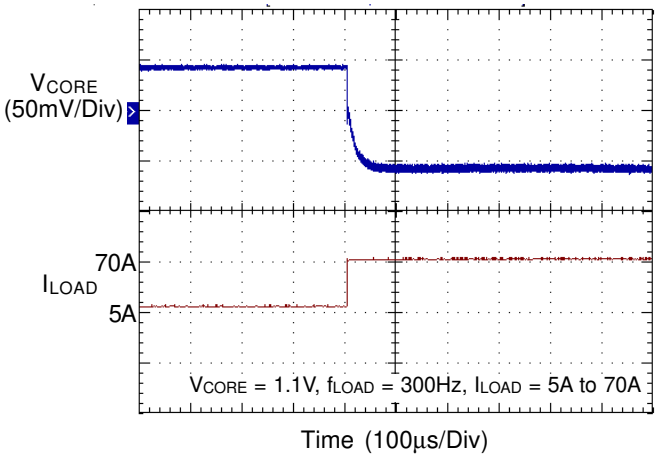
CORE VR Dynamic VID Down



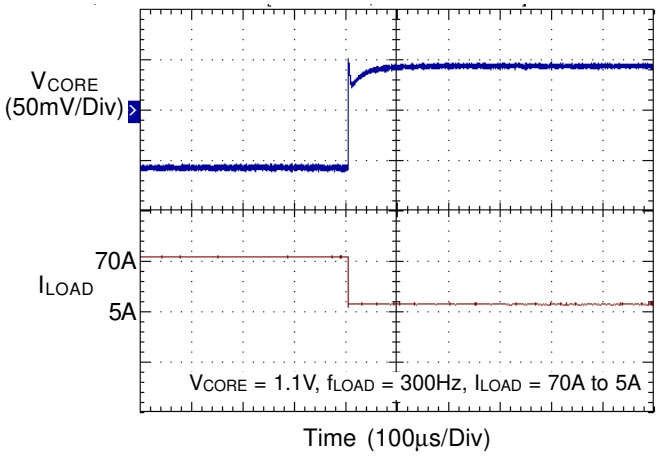
CORE VR Dynamic VID Down



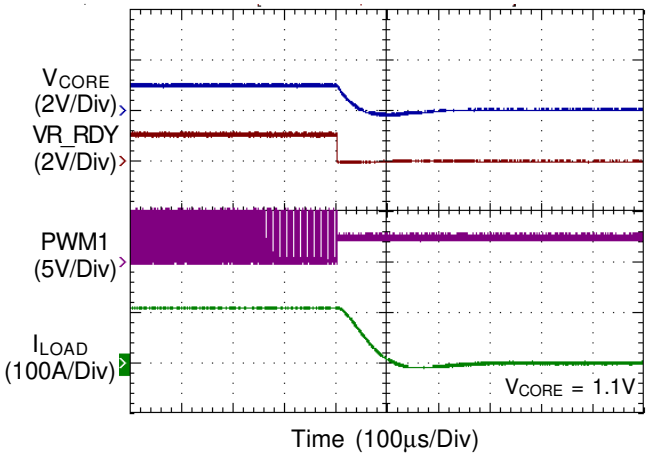
CORE VR Load Transient Response



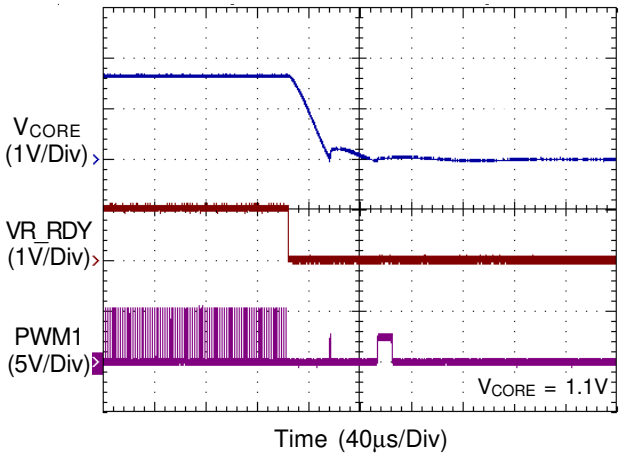
CORE VR Load Transient Response



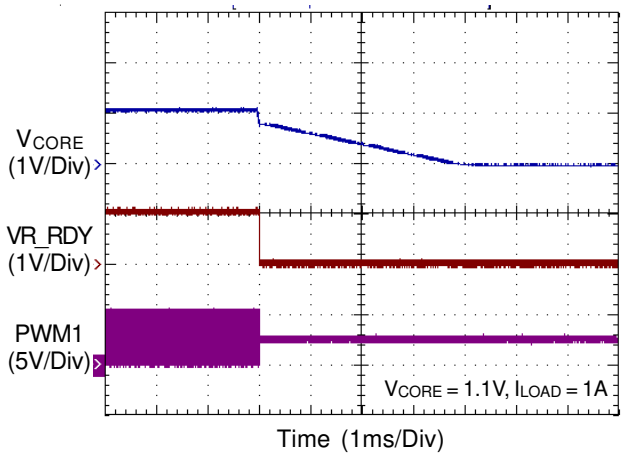
CORE VR OCP



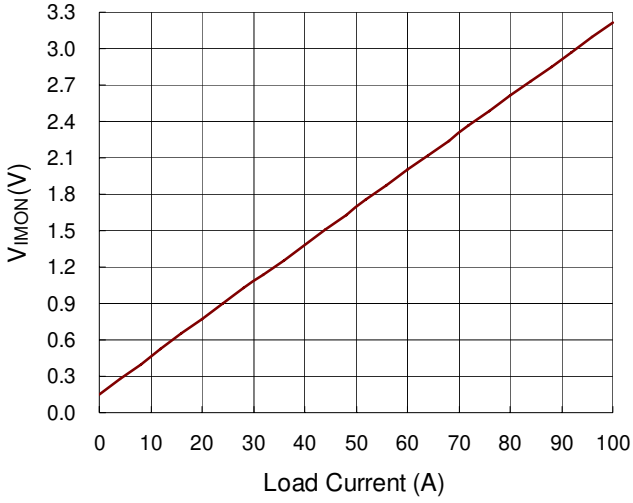
CORE VR OVP & NVP



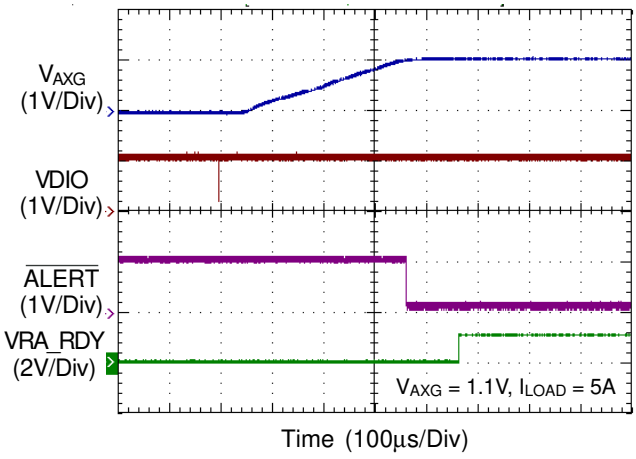
CORE VR UVP



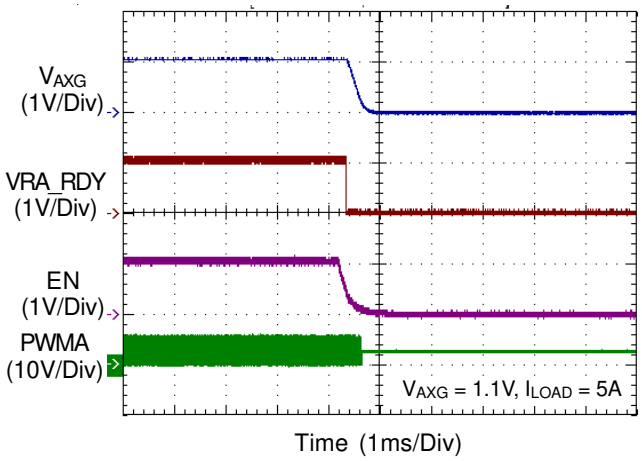
VIMON vs. Load Current



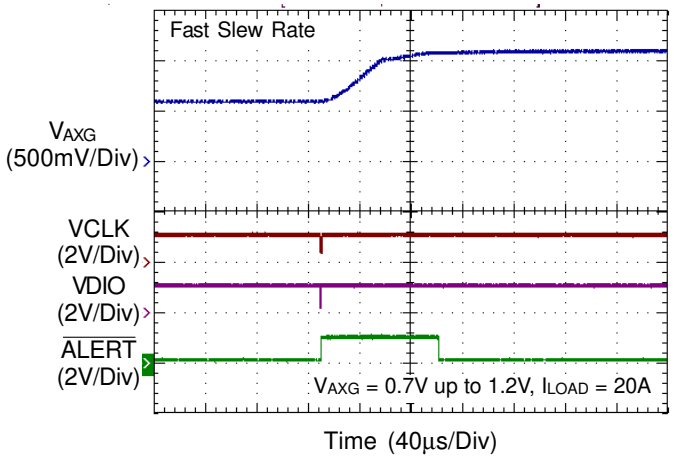
AXG VR Power On



AXG VR Power Off from EN



AXG VR Dynamic VID Up



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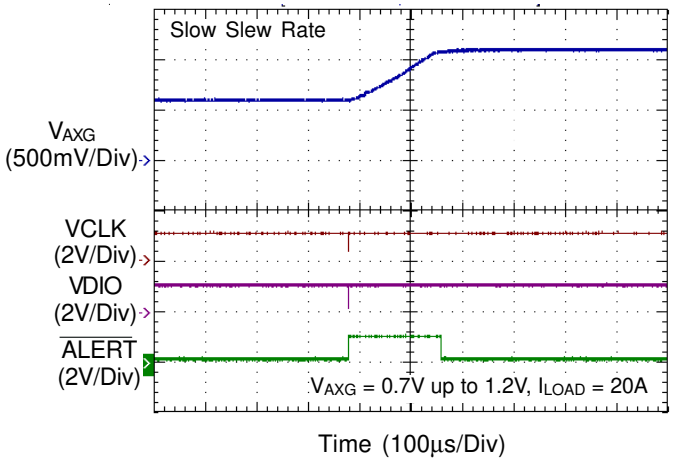
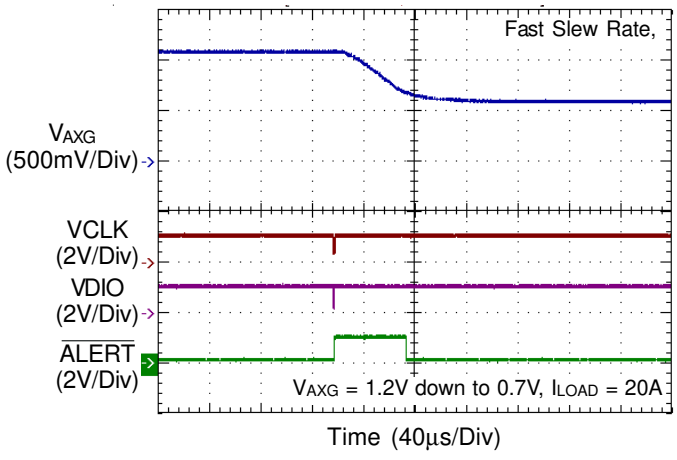


AXG VR Dynamic VID Down



AXG VR Dynamic VID Down