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5A Single Cell Li-Ion Switching Battery Charger with Power Path Management and USB-OTG Boost Mode

General Description

The RT9466 is a switch-mode single cell Li-Ion/Li-Polymer battery charger for portable applications. It integrates a synchronous PWM controller, power MOSFETs, input current sensing and regulation, high-accuracy voltage regulation, and charge termination. The charge current is regulated through integrated sensing resistors. The RT9466 also features USB On-The-Go (OTG) support.

The RT9466 optimizes for charging task by using a control algorithm to vary the charge rate for different modes, including pre-charge mode, fast charge mode (constant voltage and constant current). The key charge parameters are programmable through an I^2C interface. The RT9466 will resume the charge cycle whenever the battery voltage falls below an internal recharge threshold, and can automatically enter sleep mode if the input power supply is removed.

Other features include under-voltage protection, over voltage protection, thermal regulation and reverse leakage protection.

The RT9466 is available in a WQFN-24L 4x4 package.

Applications

- Cellular Telephones
- Personal Information Appliances
- Tablet PC, Power Bank
- Portable Instruments

Ordering Information

RT9466 □ □

- Package Type
  QW : WQFN-24L 4x4 (W-Type)
  (Exposed Pad-Option 2)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

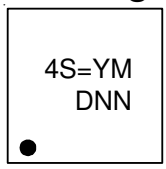
Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

- **High Efficiency 5A, 1.5MHz Switching Charger with Output Inductor DFE252012F, TOKO**
  - **Charging Efficiency 90.25% at ICHG = 2A**
  - **Charging Efficiency 88.86% at ICHG = 3A**
  - **Charging Efficiency 84.2% at ICHG = 5A**
- **Synchronous 1.5MHz/0.75MHz Fixed-Frequency PWM Controller with Up to 95% Duty Cycle**
- **Power Path Management by BATFET Control**
- **Support High Voltage Input (9V/12V)**
- **Support High Voltage Input Adapter (Pump Express 1.0/2.0)**
- **Support IR Compensation Function from Charger Output to Cell Terminal**
- **Optimize Input Sourcing Capability to Prevent Overload**
  - **AICR Current Limit Setting via I^2C**
  - **ILIM Pin for Current Limit Setting**
  - **Average Input Current Limit Measurement**
- **Shipping Mode for Battery Leakage Reduction**
  - **Wake Up System, Exit Shipping Mode, and Reset System by $\overline{QON}$ Pin**
- **Automatic Charging**
- **Average Input Current Regulation (AICR) : 0.1A to 3.25A in 50mA Steps**
- **Charge Current Regulation Accuracy : ± 7%**
- **Charge Voltage Regulation Accuracy : ± 1% (0 to 85°C)**
- **Protection for Overall System Considerations**
  - **Thermal Regulation for Current Reduction and Over-Temperature Protection**
  - **Input Over-Voltage Protection**
  - **Input Bad Adapter Protection**
  - **Battery Over-Voltage Protection**
- **Support ADC Conversion for**
  - **VBUS, VBAT, VSYS, REGN, TS_BAT, IBUS, IBAT, TEMP_JC**
- **INT Output for Communication with Host Through I^2C (Watch Dog/Polling Function)**

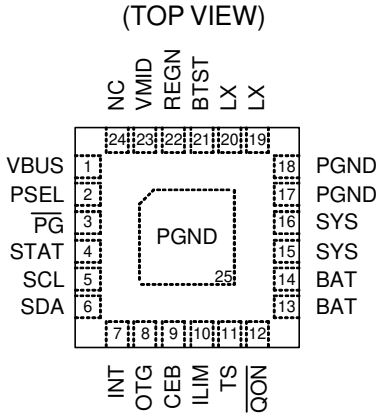
Marking Information



4S= : Product Code

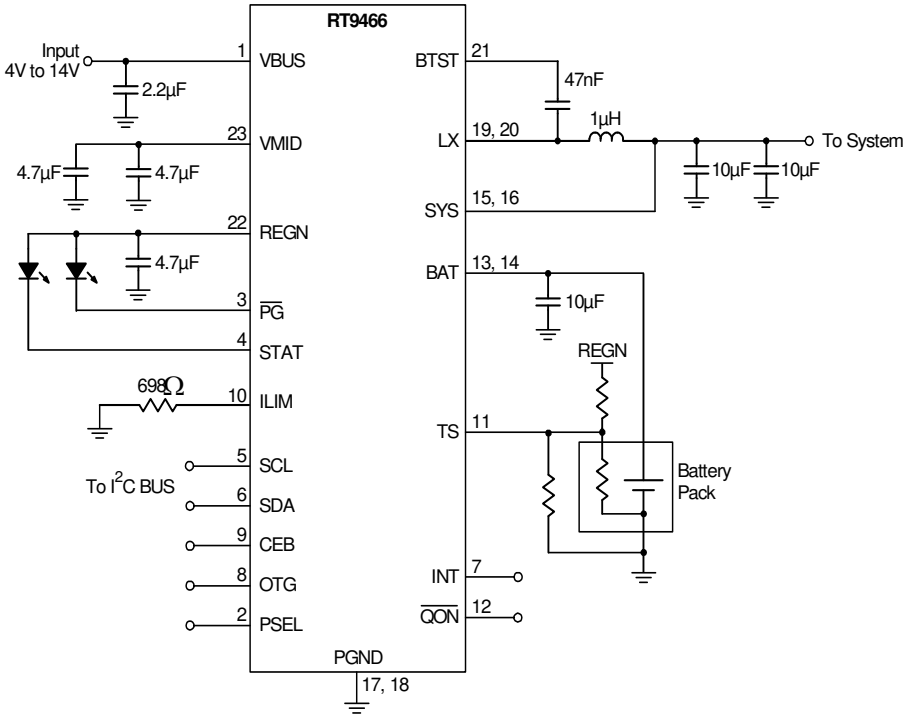
YMDNN : Date Code

Pin Configuration



WQFN-24L 4x4

Typical Application Circuit



Below are recommended components information

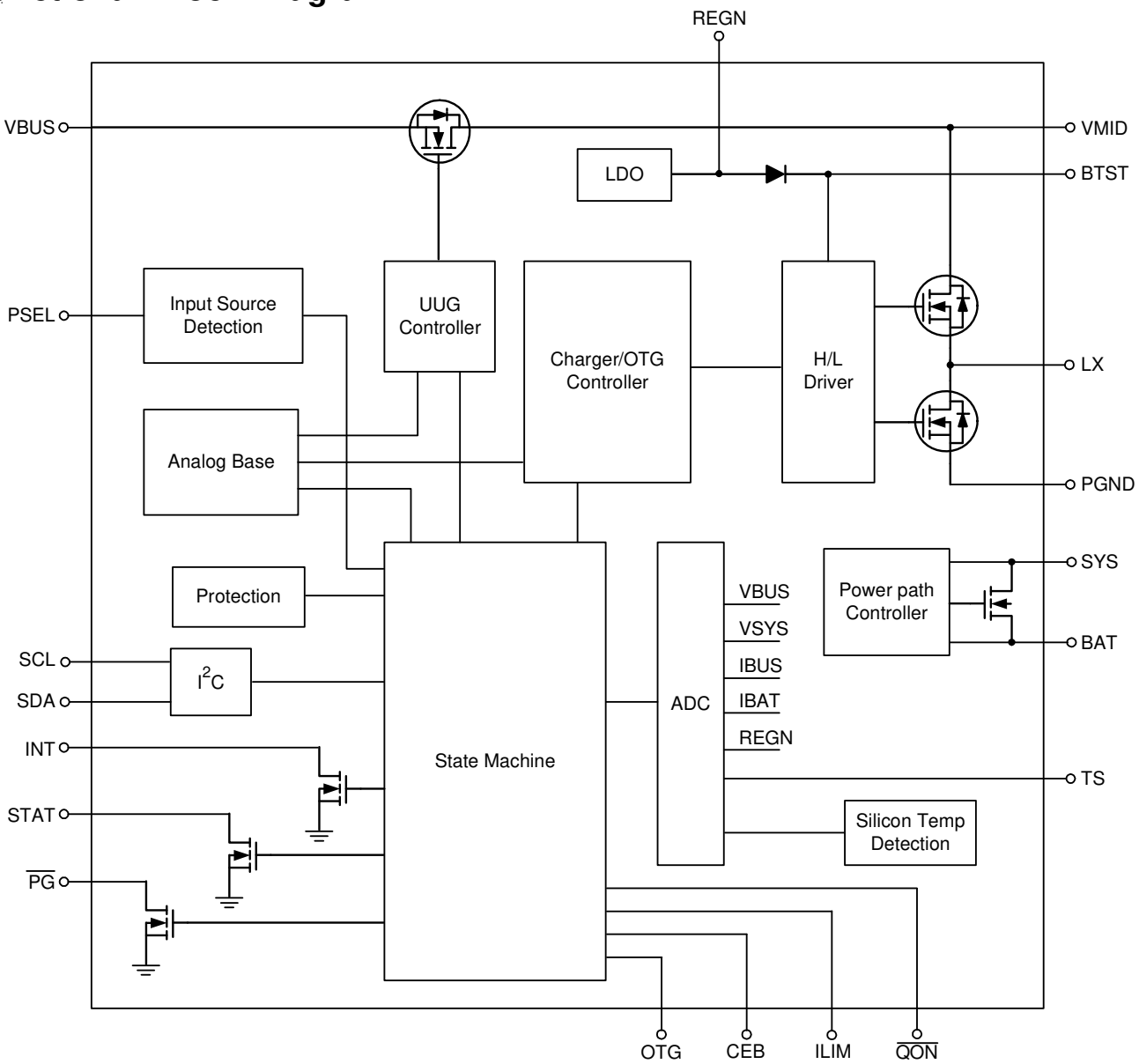
Pin	Description	Part Number	Package	Manufacturer
VBUS	2.2µF/25V/X5R	GRM155R61E225KE11	0402	muRata
VMID	4.7µF/25V/X5R	GRM188R61E475KE11	0603	muRata
BTST	47nF/16V/X5R	GRM033R61C473KE84	0201	muRata
SYS	10µF/6.3V/X5R	GRM185R60J106ME15	0603	muRata
BAT	10µF/6.3V/X5R	GRM185R60J106ME15	0603	muRata
REGN	4.7µF/6.3V/X5R	GRM155R60J475ME47	0402	muRata
LX	1µH/20%	DFE252012F-1R0	2.5 x 2mm	TOKO
ILIM	698Ω/1%	RR0306S-6980-FNH	0201	CYNTEC

Functional Pin Description

Pin No.	Pin Name	Pin Description
1	VBUS	Power input.
2	PSEL	Power source selection input : High : USB host, I_{BUS} = 500mA; Low : adapter source, I_{BUS} = 3.25A.
3	$\overline{PG}$	Open-drain output. Low if the VBUS voltage is between V_{UVLO} and V_{BUS_OVP}; VBUS is higher than VBAT. VBUS current capability is larger than 50mA.
4	STAT	Charge status indication, open-drain output that indicates charge is in progress when held low and charge is finished when held High. If any fault occurs, CHG_STAT will blink at the frequency of 1Hz. Connect a 2.2k-10kΩ pull-up resistor.
5	SCL	I^2C interface serial clock input. Open-drain. An external pull-up resistor is required
6	SDA	I^2C interface serial data input/output. Open-drain. An external pull-up resistor is required.
7	INT	Interrupt output, active-low open-drain. Indicator of the charger/Boost event for system processor.
8	OTG	OTG boost mode enable control, active-high. Act with OTG_PIN_EN (Addr0x01[1]).
9	CEB	Charger enable input, active-low.
10	ILIM	Input current limit setting pin. A resistor is connected from ILIM pin to ground to set the maximum input current limit. The actual input current limit is the lower value set through the ILIM pin and IAICR register bits.
11	TS	Battery temperature-sense input, connected to a resistor divider for temperature programming. If there is no need for the battery temperature-sense function, a 50kΩ resistor is connected to REGN and another 50kΩ resistor to ground.
12	$\overline{QON}$	Internal BATFET enable control input. In shipping mode, $\overline{QON}$ is pulled Low for the duration of $t_{SHIPMODE}$ (typical 0.9s) to exit shipping mode.
13, 14	BAT	Charge current output node for battery connection. The internal BATFET is connected between VSYS and BAT. Connect a 10μF ceramic capacitor between BAT and ground.
15, 16	SYS	System connection node. The internal BATFET is connected between SYS and BAT. Connect a 20μF ceramic capacitor between SYS and ground.
17, 18	PGND	Power ground.
19, 20	LX	Switch node for output inductor connection.
21	BTST	Bootstrap capacitor connection for High-Side Gate Driver. Connect a capacitor from BTST to LX to power the internal gate driver.
22	REGN	Regulated output voltage to supply for the PWM low-side gate driver and the bootstrap capacitor. Connect a 4.7μF ceramic capacitor from REGN to GND. 1. If VBUS is plugged in, REGN will be powered by VBUS and regulated to 4.9V. 2. If VBUS is unplugged, the charger will operate in sleep mode and the REGN voltage will be 0V. * For #2. : Since the REGN voltage is also used to power the TS resistor, when the charger is in sleep mode, the REGN will be woken up (be reactivated) if VBAT is greater than forward voltage (V_F) of the internal high-side (HS) MOS diode by V_{SLEEP_EXIT} with all function of the internal ADC being activated and I^2C R/W. The REGN wake-up time is 500ms.

Pin No.	Pin Name	Pin Description
23	VMID	Connection point between the reverse blocking MOSFET and the high-side switching MOSFET.
24	NC	No connection.
25 (Exposed Pad)	PGND	Power ground. The exposed pad must be connected to GND and well soldered to a large PCB copper area for maximum power dissipation.

Functional Block Diagram



Operation

The RT9466 is an integrated single cell Li-ion battery switching charger with power path controller.

Base Circuits

Base circuits provide the internal power, VREGN and reference voltage and bias current.

Protection Circuits

The protection circuits include the VINOVP, VINUVLO, BATOVP and OTP circuits. The protection circuits turn off the charging when the input power or die temperature is in abnormal level.

Buck Regulator for Charging and Boost Regulator as OTG

The multi-loop controller controls the operation of charging process and current supply to the system. It also controls the circuits as a Boost converter for OTG applications.

Battery Detection

The RT9466 is capable of doing the battery absence detection. The detection protects the charger when battery is removed accidentally.

Adapter Detection

If the poor input power source is connected to the RT9466, the operation will be shut down by the adapter detection.

Power Path Management and Control

Once the battery voltage increases to a defined system minimum regulation voltage, the internal path between SYS and BAT will be fully turned on. That is, a better charging efficiency can be achieved. When end of charge occurs, the charging will stop and the internal path will be turned off.

TS Detection

The RT9466 detects the temperature of the battery pack via REGN and TS pins. The REGN pin provides a constant voltage source to drive the voltage divider composed of a pulled-high resister and a NTC resister. The RT9466 reports the sensing results via IRQ and status bits for COLD, COOL, WARM and HOT.

I^2C Controller

The key parameters of charging and OTG are programmable through I^2C commands.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VBUS ---------- –0.3V to 22V
- Supply Input Voltage, VBUS (Peak <100ns duration) ---------- –2V
- VMID, BTST ---------- –0.3V to 22V
- LX ---------- –0.3V to 16V
- LX (Peak <100ns duration) ---------- –2V
- VMID – VBUS, BTST – LX ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-24L 4x4 ---------- 4.54W
- Package Thermal Resistance (Note 2)
  WQFN-24L 4x4, θ_{JA} ---------- 22°C/W
  WQFN-24L 4x4, θ_{JC} ---------- 5.4°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 4V to 14V
- Maximum Input Current (VBUS), I_{AICR} ---------- 3.25A
- Maximum SYS Output Current (SW), I_{SYS} ---------- 5A
- Maximum Battery Voltage, VBAT ---------- 4.71V
- Maximum I_{BAT} Fast Charging Current ---------- 5A
- Maximum I_{BAT} Discharging Current ---------- 6A
- Maximum I_{BAT} Discharging Current peak,1sec duration ---------- 9A
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{BUS} = 5V, V_{BAT} = 4.2V, L = 1µH, C_{IN} = 2.2µF, C_{BATS} = 10µF, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Quiescent Current						
V_{BUS} Supply Current	I_{VBUS_SW}	V_{LX} is switching, V_{BUS} = 5V, V_{SYS} = 3.8V	--	8	--	mA
	$I_{VBUS\_NON\_SW}$	V_{LX} Is non-switching, V_{BUS} = 5V, V_{SYS} = 4.4V	--	--	5	mA
	I_{VBUS_HZ}	V_{LX} is in high-impendence mode, V_{BUS} = 5V, V_{SYS} = 3.8V	--	--	170	µA
Battery Leakage Current	$I_{BAT\_LEAK\_OFF}$	V_{BAT} = 4.2V, power path is off	--	--	25	µA
	$I_{BAT\_LEAK\_ON}$	V_{BAT} = 4.2V	--	--	60	µA
Boost-Mode Battery Discharge Current	$I_{BAT\_BOOST\_SW}$	V_{BAT} = 4.2V, boost mode, I_{VBUS} = 0A, V_{LX} is switching	--	5	--	mA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{BUS} / V_{BAT} Power-Up						
Sleep-Mode Entry Threshold, V_{BUS}-V_{BAT}	V_{SLEEP_ENTER}	2.5V < V_{BAT} < V_{OREG}, V_{BUS} falling	0	40	100	mV
Sleep-Mode Exit Threshold, V_{BUS}-V_{BAT}	V_{SLEEP_EXIT}	2.5V < V_{BAT} < V_{OREG} , V_{BUS} rising	40	100	200	mV
Sleep-Mode Exit Deglitch Time	$t_{D\_SLEEP\_EXIT}$	Exit sleep-mode	--	120	--	ms
V_{BUS} Bad Adapter Threshold	V_{BAD_ADP}		--	3.8	--	V
V_{BUS} Bad Adapter Hysteresis	$V_{BAD\_ADP\_HYS}$		--	150	--	mV
V_{BUS} Bad Adapter Sink Current	$I_{BAD\_ADP\_SINK}$		--	50	--	mA
V_{BUS} Bad Adapter Detection Time	$t_{BAD\_ADP\_DET}$		--	30	--	ms
Input Current Limit Factor	K_{ILIM}	Input current regulation 508mA by ILIM pin with resistance = 698Ω	320	355	390	AΩ
Input Current Limit Regulation	I_{ILIM_MIN}	Minimum input current for regulation on ILIM pin	0.5	--	--	A
Input Power Regulation						
Minimum Input Voltage Regulation (MIVR) Threshold Range	V_{MIVR}	I^2C programmable in 0.1V steps	3.9	--	13.4	V
Default Minimum Input Voltage Regulation Threshold	V_{MIVR_DEF}	Default	--	4.4	--	V
Minimum Input Voltage Regulation Accuracy	$V_{MIVR\_ ACC}$	VMIVR = 4.4V, 9V	–3	--	3	%
Average Input Current Regulation Accuracy	I_{AICR_ACC}	USB charge mode, I_{AICR} = 100mA	86	93	100	mA
		USB charge mode, I_{AICR} = 500mA	440	470	500	
		USB charge mode, I_{AICR} = 1000mA	880	940	1000	mA
		Adapter 1.5A charge mode, I_{AICR} = 1500mA	1300	1400	1500	mA
Protection						
V_{BUS}						
V_{BUS} Under-Voltage Protection Threshold	V_{UVLO}	V_{BUS} rising	3.05	3.3	3.55	V
V_{BUS} Under-Voltage Protection Hysteresis	V_{UVLO_HYS}	V_{BUS} falling from UVLO	--	150	--	mV
V_{BUS} Over-Voltage Protection Threshold	V_{BUS_OVP}	V_{BUS} rising	13.5	14.5	15.5	V
V_{BUS} Over-Voltage Protection Hysteresis	$V_{BUS\_OVP\_HYS}$	V_{BUS} falling	--	250	--	mV

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
V_{BAT}							
Battery Over-Voltage Protection Threshold	V_{BAT_OVP}	V_{BAT} rising, as percentage of V_{OREG}, as (V_{BAT_OVP}-V_{OREG})/V_{OREG}		106	108	110	%
Battery Over-Voltage Protection Hysteresis	$V_{BAT\_OVP\_HYS}$	V_{BAT} falling, as ($V_{BAT\_OVP\_HYS}$)/V_{OREG}		--	4	--	%
Thermal Protection							
Over-Temperature Protection Threshold	T_{OTP}	Thermal shutdown threshold temperature		--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}	Thermal shutdown hysteresis temperature		--	30	--	°C
Thermal Regulation Threshold	T_{TR}	Charge current starts decreasing		--	120	--	°C
V_{SYS}							
V_{SYS} Over-Voltage Protection Threshold	V_{SYS_OVP}	V_{SYS} rising		--	5.25	--	V
V_{SYS} Under-Voltage Protection Threshold	V_{SYS_UVP}	V_{SYS} falling		--	2.4	--	V
Battery Charging Stages							
End of Charge							
Regulated Battery Voltage Range	V_{OREG}	I^2C programmable in 10mV steps		3.9	--	4.71	V
Regulated Battery Voltage	V_{OREG_DEF}	Default		--	4.2	--	V
Regulated Battery Voltage Accuracy	V_{OREG_ACC}	Temperature = 0°C to 85°C		–1	--	1	%
Re-Charge Mode Threshold	V_{RECH}	V_{BAT} falling, the difference below VOREG , (Addr 0x0B[2:0] = 00)		50	100	150	mV
Re-Charge Deglitch Time	t_{D_RECH}			--	120	--	ms
End-of-Charge Current	I_{EOC}	I^2C programmable in 50mA steps		100	--	850	mA
Default End-of-Charge Current	I_{EOC_DEF}	Default		--	250	--	mA
End-of-Charge Current Accuracy	I_{EOC_ACC}			–20	--	20	%
Default End-of-Charge Deglitch Time	t_{D_EOC}	Default		--	2	--	ms
Fast Charge							
Charge Current Range	I_{CHG}	I^2C programmable in 0.1A steps		0.1	--	5	A
Charge Current Accuracy	I_{CHG_ACC}	V_{BAT} = 3.8V	I_{CHG} < 500mA	–20	--	20	%
			500mA < I_{CHG} < 1000mA	–10	--	10	%
			I_{CHG} > 1000mA	–7	--	7	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Pre-Charge						
Pre-Charge Mode Threshold	V_{PRECHG}	I^2C programmable in 0.1V steps	2	--	3.5	V
Pre-Charge Mode Hysteresis	V_{PRECHG_HYS}	Pre-charge hysteresis	--	0.2	--	V
Pre-Charge Mode Threshold Accuracy	V_{PRECHG_ACC}		–5	--	5	%
Pre-Charge Current Range	I_{PRECHG}	I^2C programmable in 50mA steps	100	--	850	mA
Default Pre-Charge Current	I_{PRECHG_DEF}	Default	--	150	--	mA
Pre-Charge Current Accuracy	I_{PREC_ACC}		–20	--	20	%
Trickle charge						
Trickle Charge Threshold	V_{TRICHG}	VBAT falling	--	2	--	V
Trickle Charge Threshold Hysteresis	V_{TRICHG_Hys}	VBAT rising	--	200	--	mV
Trickle Charge Threshold accuracy	V_{TRICHG_acc}		–5	--	5	%
Trickle Current	I_{TRICHG}	VBAT< 2V, charge with ICC = 100mA VBAT < 1.6V, charge with AICR =100mA	--	100	--	mA
Trickle Current Accuracy	I_{TRICHG_acc}		–20	--	20	%
V_{SYS}						
System Regulation Voltage	V_{SYSREG}	Minimum system regulation voltage, I^2C programmable in 0.1V steps	3.3	--	4	V
Default System Regulation Voltage	V_{SYSREG_DEF}	Default minimum system regulation voltage	--	3.6	--	V
System Regulation Accuracy	V_{SYSREG_ACC}		–5	--	5	%
Battery Charger						
UUG On-Resistance	R_{ON_UUG}	From VBUS to VMID	--	17	32	mΩ
High-Side On-Resistance	$R_{ON\_UUG\_UG}$	From VBUS to LX	--	42	79	mΩ
Low-Side On-Resistance	R_{ON_LG}	From LX to PGND	--	28	40	mΩ
Power-Path-Side On-Resistance	R_{ON_PPMOS}	From SYS to BAT	--	13	30	mΩ
Switching Frequency (1.5MHz)	f_{OSC1}	I^2C programmable to 1.5 MHz (Addr 0x01[7] =0)	--	1.5	--	MHz
Switching Frequency (750kHz)	f_{OSC2}	I^2C programmable to 0.75MHz (Addr 0x01[7] =1)	--	0.75	--	MHz
Frequency Accuracy	f_{OSC_ACC}		–10	--	10	%
Maximum Duty Cycle	D_{MAX}	At minimum input voltage	--	97	--	%
Minimum Duty Cycle	D_{MIN}		0	--	--	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
REGN Regulation	V_{REGN}	V_{BUS} = 5V / 9V / 12V	--	4.9	--	V
REGN Current Limit	I_{LIM_REGN}	V_{BUS} = 5V / 9V / 12V	50	--	--	mA
Sink Current for Battery Detection	I_{BAT_SINK}		--	300	--	μA
Internal $\overline{QON}$ Pull-Up Resistance	$R_{\overline{QON}}$		--	200	--	kΩ
Internal $\overline{QON}$ Pull-Up	$V_{\overline{QON}}$	Battery only	--	VBAT	--	V
		V_{BUS} = 5V/9V	--	4.8	--	
$\overline{QON}$ Exit Shipping Mode Time	$t_{SHIPMODE}$	$\overline{QON}$ Low for BATFET on-time to exit shipping mode	--	0.9	--	sec
System Reset by $\overline{QON}$ Pin	$t_{\overline{QON}\_RST}$	$\overline{QON}$ low time to enable full system reset	--	10	--	sec
BATFET Reset Time	t_{BATFET_RST}	BATFET off-time during full system reset	--	0.41	--	sec
Shipping Mode Entry Deglitch Time	$t_{D\_SM\_ENTER}$	Enter shipping mode	--	9	--	sec
AICL	V_{AICL}	V_{BUS} rising, I^2C programmable	--	4.6	--	V
AICL Hysteresis	V_{AICL_HYS}		--	50	--	mV
Inductor Over-Current Protection Buck Threshold	I_{OCP_BUCK}	Inductor OCP level for buck mode	--	6	--	A
OTG Boost Mode Operation						
OTG Boost-Mode Output Regulation Voltage Range	V_{OTGBST}	To VBUS	4.425	--	5.825	V
OTG Boost-Mode Output Regulation Voltage Accuracy	V_{OTGBST_ACC}		–3	--	3	%
OTG Boost-Mode Over-Load Protection Threshold	I_{OTG_OLP}	I^2C programmable	0.5	--	2.4	A
OTG Boost-Mode Default Over-Load Protection Threshold	$I_{OTG\_OLP\_DEF}$	Addr 0x0A [2:0] = 000	0.5	--	--	A
OTG Low Battery Protection Threshold	V_{OTG_LBP}	I^2C programmable, hysteresis = 0.4 V	2.3	--	3.8	V
OTG Default Low Battery Protection Threshold	$V_{OTG\_LBP\_DEF}$	OTG_LBP = 2.8V (Addr0x0A[7:4] = 0101)	--	2.8	--	V
OTG Low Battery Protection Threshold Accuracy			–5	--	5	%
OTG VMID Over-Voltage Protection	$V_{OTG\_VMID\_OVP}$	V_{VMID} rising	--	6	--	V
OTG VMID Over-Voltage Protection Hysteresis	$V_{OTG\_VMID\_OVP\_HYS}$		--	200	--	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Inductor Over-Current Protection Boost Threshold	I_{OCP_BOOST}	Inductor OCP level for boost mode	--	5.5	--	A
Current Pulse Control, PE1.0						
Current Pulse Control Stop Pulse	t_{PUMPX_STOP}		430	--	570	ms
Current Pulse Control Long On Pulse	t_{PUMPX_ON1}		240	--	360	ms
Current Pulse Control Short On Pulse	t_{PUMPX_ON2}		70	--	130	ms
Current Pulse Control Off Pulse	t_{PUMPX_OFF}		70	--	130	ms
Current Pulse Control Stop Start Delay	t_{PUMPX_DLY}		80	--	225	ms
I^2C Characteristics						
Output Low Threshold Voltage	V_{OL_I2C}	I_{DS} = 10mA	--	--	0.4	V
SCL, SDA Input Logic High Threshold Voltage	V_{IH_I2C}		1.3	--	--	V
SCL, SDA Input Logic Low Threshold Voltage	V_{IL_I2C}		--	--	0.4	V
SCL Clock	f_{SCL}		--	--	400	kHz
High Level Leakage Current	I_{BIRS}	V_{PULL_UP} = 1.8V, SDA and SCL	--	--	1	µA
Load Capacitance	C_{LOAD}	V_{PULL_UP} = 1.8V	--	--	1	pF
Default Wait Time for Watch Dog Reset	t_{WDT_DEF}	Watch Dog timer selection, Default : 0x0D[6] = 1	--	500	--	ms
NTC Monitor						
Battery Temperature HOT Threshold	V_{VTS_HOT}	V_{TS} falling, the ratio of V_{REGN}	33.5	34.5	35.5	%
Battery Temperature WARM Threshold	V_{VTS_WARM}	V_{TS} falling, the ratio of V_{REGN}	44	45	46	%
Battery Temperature COOL Threshold	V_{VTS_COOL}	V_{TS} rising, the ratio of V_{REGN}	67.5	68.5	69.5	%
Battery Temperature COLD Threshold	V_{VTS_COLD}	V_{TS} rising, the ratio of V_{REGN}	72.5	73.5	74.5	%
Battery Temperature Hysteresis	V_{VTS_HYS}		--	2	--	%
Control I/O Pin (STAT, $\overline{PG}$, INT)						
Output Low Voltage	V_{OL_CTRL}	I_{DS} = 10mA	--	--	0.4	V
Control I/O Pin (OTG, CEB, PSEL, $\overline{QON}$)						
Input Threshold Voltage	V_{IH_CTRL}	Logic High Threshold	1.3	--	--	V
	V_{IL_CTRL}	Logic Low Threshold	--	--	0.4	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
ADC						
ADC Conversion Time each Channel	t_{CONV}		35	200	--	ms
Number of Bits for ADC Resolution	RES	Logic High Threshold	--	10	--	bit
ADC Accuracy and Measurement Range						
VBUS_DIV5 Measurement Range	$V_{VBUS\_DIV5ADC\_Range}$		1	--	22	V
VBUS_DIV5 Resolution	$V_{VBUS\_DIV5ADC\_RES}$		--	25	--	mV
VBUS_DIV5 Accuracy	$V_{VBUS\_DIV5ADC\_ACC}$		–2	--	2	LSB
VBUS_DIV2 Measurement Range	$V_{VBUS\_DIV2ADC\_Range}$		1	--	9.8	V
VBUS_DIV2 Resolution	$V_{VBUS\_DIV2ADC\_RES}$		--	10	--	mV
VBUS_DIV2 Accuracy	$V_{VBUS\_DIV2ADC\_ACC}$		–2	--	2	LSB
VBAT Measurement Range	$V_{VBAT\ ADC\_Range}$		0	--	4.9	V
VBAT Resolution	$V_{VBAT\ ADC\_RES}$		--	5	--	mV
VBAT Accuracy	$V_{VBAT\ ADC\_ACC}$		–2	--	2	LSB
VSYS Measurement Range	$V_{VSYS\ ADC\_Range}$		0	--	4.9	V
VSYS Resolution	$V_{VSYS\ ADC\_RES}$		--	5	--	mV
VSYS Accuracy	$V_{VSYS\ ADC\_ACC}$		–2	--	2	LSB
REGN Measurement Range	$V_{REGN\ ADC\_Range}$		0	--	4.9	V
REGN Resolution	$V_{REGN\ ADC\_RES}$		--	5	--	mV
REGN Accuracy	$V_{REGN\ ADC\_ACC}$		–2	--	2	LSB
TS_BAT Measurement Range	$Rate_{TS\_BAT}$		0	--	100	%
TS_BAT Resolution	$Rate_{TS\_BAT\_RES}$		--	0.25	--	%
TS_BAT Accuracy	$Rate_{TS\_BAT\ ACC}$		–2	--	2	LSB
IBUS Measurement Range	$I_{IBUS\ ADC\_Range}$		0	--	3.25	A
IBUS Resolution	$I_{IBUS\ ADC\_RES}$		--	50	--	mA
IBUS Accuracy	$I_{IBUS\ ADC\_ACC}$		–2	--	2	LSB
IBAT Measurement Range	$I_{IBAT\ ADC\_Range}$		0	--	5	A
IBAT Resolution	$I_{IBAT\ ADC\_RES}$		--	50	--	mA
IBAT Accuracy	$I_{IBAT\ ADC\_ACC}$		–2	--	2	LSB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TEMP_JC Measurement Range	$T_{TEMP\_JC\ ADC\_Range}$		–40	--	120	°C
TEMP_JC Resolution	$T_{TEMP\_JC\ ADC\_RES}$		--	2	--	°C
TEMP_JC Accuracy	$T_{TEMP\_JC\ ADC\_ACC}$	Temperature < 85 °C	–2	--	2	LSB

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

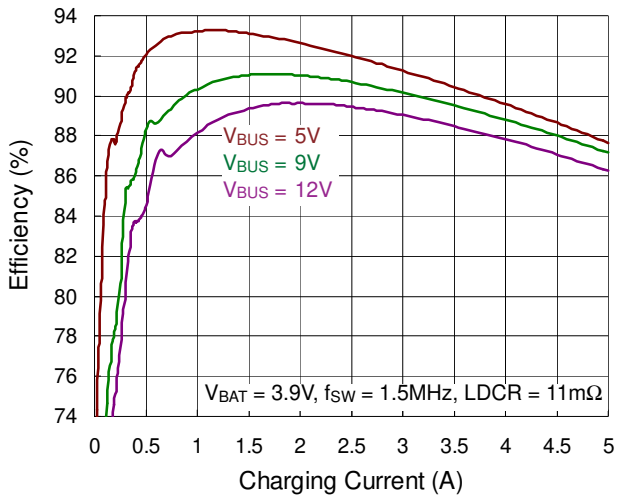
Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a Four-layer Richtek Evaluation Board. θ_{JC} is measured at the Top of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

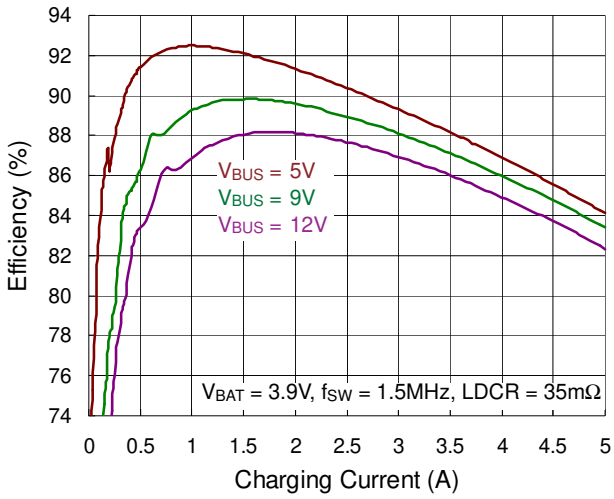
Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Operating Characteristics

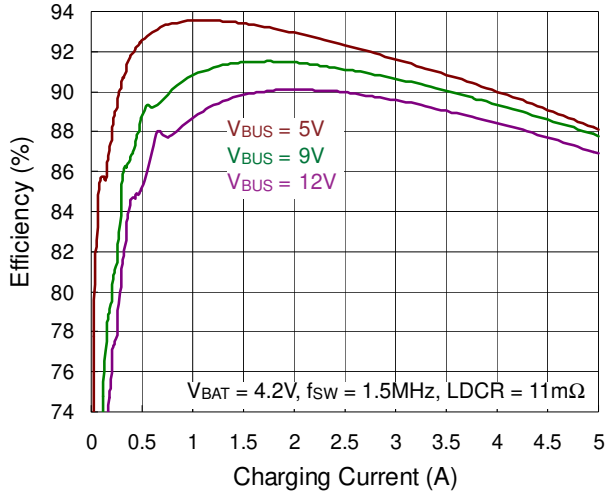
Charger Efficiency vs. Charging Current



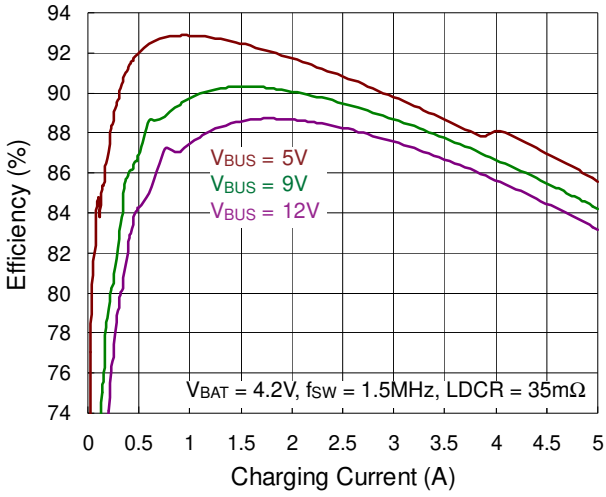
Charger Efficiency vs. Charging Current



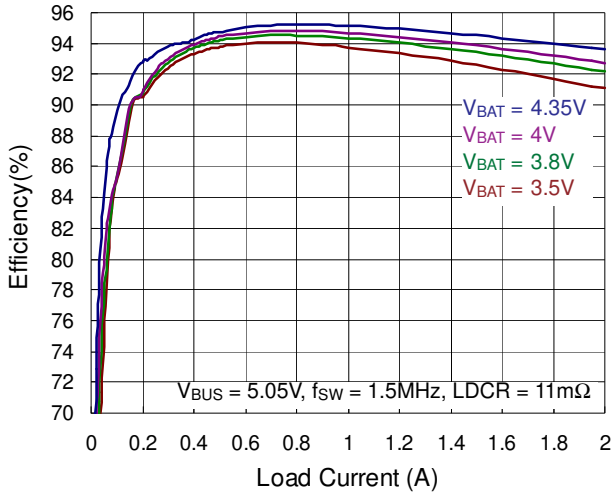
Charger Efficiency vs. Charging Current



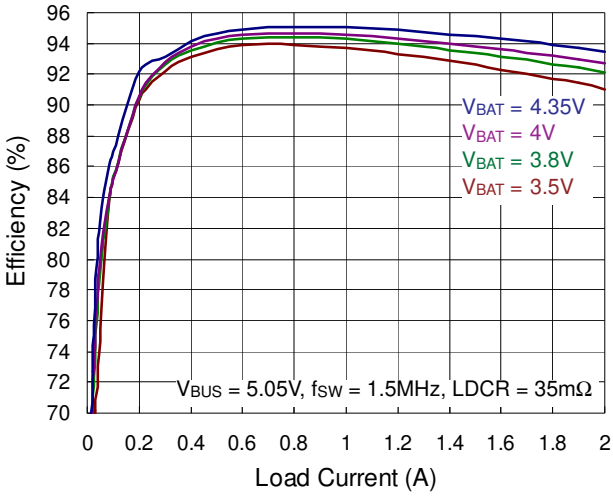
Charger Efficiency vs. Charging Current



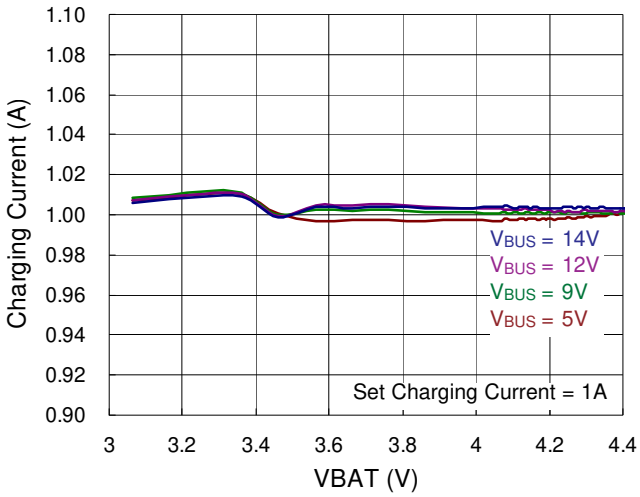
Boost Efficiency vs. Load Current



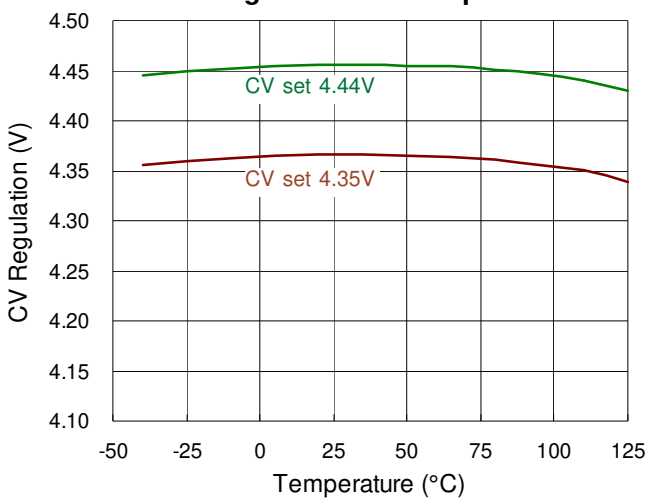
Boost Efficiency vs. Load Current



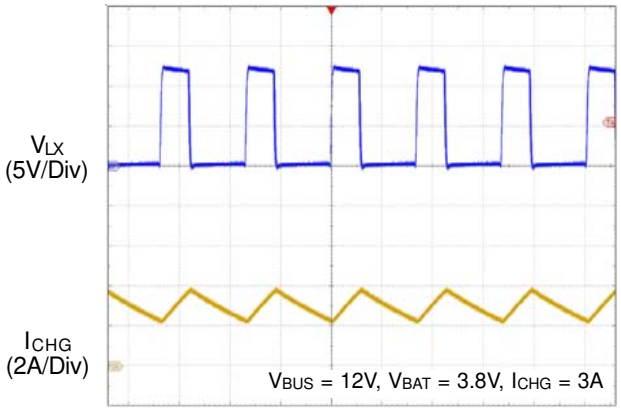
Charging Current vs. VBAT



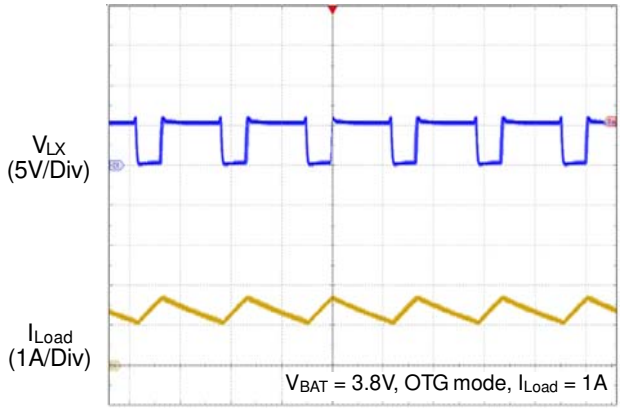
CV Regulation vs. Temperature



PWM Switching



Boost Mode Switching



Register Descriptions

I²C Slave Address : 1010011 (53H)

Name		Function	Addr	Reset
CORE_CTRL0		Control 0	0x00	0x00
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	RST_REG	0	All registers reset bit. 0: Don't reset all registers. 1: Reset all registers. (Notice: 1. This bit will be reset to "0" after reset procedure finish. 2. In high-impedance mode, this bit reset all registers after leave high-impedance mode.)
[6:0]	R/W	Reversed	0000000	Reversed

Name		Function	Addr	Reset
CHG_CTRL1		Control 1	0x01	0x10
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	SEL_SWFREQ	0	The switching frequency selection bit (Charger/OTG) 0 : The switching frequency is 1.5MHz. (Default) 1 : The switching frequency is 0.75MHz.
6	R/W	FIXFREQ	0	Charger switching frequency 0 : Charger switching frequency would be varied if VBUS is closed to VBAT(default) 1 : Charger switching frequency is fixed
5	R/W	Reversed	0	Reversed
4	R/W	STAT_EN	1	Charger STAT pin function 0 : Disable 1 : Enable (default)
3	R/W	IRQ_PULSE	0	IRQ reminder function 0 : IRQ reminder is disabled (default) 1 : IRQ reminder is enabled. If IRQ is triggered but no check action, INT pin will be released as well as being triggered again with every 2s intervals
2	R/W	HZ	0	High-impedance selection 0 : No high-impedance mode (default) 1 : High-impedance mode
1	R/W	OTG_PIN_EN	0	Boost mode enable with OTG pin 0 : Enable Boost mode by OPA_MODE (default) 1 : Enable Boost by both OPA_MODE bit and OTG pin
0	R/W	OPA_MODE	0	Boost mode enable 0 : Charge mode (default) 1 : Boost mode for OTG

Name		Function	Addr	Reset
CHG CTRL 2		Charger Control 2	0x02	0x03
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	SHIP_MODE	0	Shipping mode enable, force BATFET OFF 0 : Allow BATFET turn on (default) 1 : Force BATFET turn off
6	R/W	BATDET_DIS_DLY	0	BATFET turn off delay 0 : BATFET turn off immediately (default) 1 : BATFET turn off with 10s delay after SHIP_MODE bit is set
5	R/W	Reserved	0	Reserved
4	R/W	TE	0	Termination enable 0 : Disable charge current termination (default) 1 : Enable charge current termination
[3:2]	R/W	IINLMTSEL	00	Input current limit selection bit 00 : PSEL pin result is applied (default) 01 : Reserved 10 : IAICR[5:0] results is applied 11 : Input limit is set by the lower level of these three
1	R/W	CFO_EN	1	Charger and OTG enable 0 : CFO is disabled 1 : CFO is enabled (default)
0	R/W	CHG_EN	1	Charger and Boost enable 0 : Charger and Boost is disabled 1 : Charger and Boost is enabled (default)

Name		Function	Addr	Reset
CHG_CTRL3		Control 3	0x03	0x23
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:2]	R/W	IAICR[5:0]	001000	AICR setting 000000 : 100mA 000001 : 150mA 000010 : 200mA 000011 : 250mA ... 001000 : 500mA (default) 001001 : 550mA ... 100110 : 2A ... 111010 : 3A ... 111111 : 3.25A
1	R/W	AICR_EN	1	AICR loop enable 0 : AICR loop disable 1 : AICR loop enable (default)
0	R/W	ILIM_EN	1	ILIM function enable 0 : ILIM function disable 1 : ILIM function enable (default)

Name		Function	Addr	Reset
CHG_CTRL4		Control 4	0x04	0x3C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:1]	R/W	VOREG[6:0]	0011110	Battery regulation voltage. The delta-V of the Battery regulation voltage is 10mV. 0000000 : 3.9V 0000001 : 3.91V 0000010 : 3.92V 0000011 : 3.93V … 0011101 : 4.19V 0011110 : 4.2V (default) 0011111 : 4.21V … 0101100 : 4.34V 0101101 : 4.35V 0101110 : 4.36V ... 1010001 : 4.71V 1010001 ~ 1111111 : 4.71V
0	R/W	Reserved	0	Reserved

Name		Function	Addr	Reset
CHG_CTRL5		Control 5	0x05	0x67
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:2]	R/W	VOTGBST[5:0]	011001	OTG boost-mode output regulation voltage. The delta-V of the OTG regulation voltage is 25mV. 000000 : 4.425V 000001 : 4.45V 000010 : 4.475V … 010111 : 5V 011000 : 5.025V 011001 : 5.05V (default) 011010 : 5.075V 011011 : 5.1V ... 111000 : 5.825V 111001 to 111111 : 5.825V
[1:0]	R/W	THREG[1:0]	11	Charger thermal regulation threshold 00 : 60°C 01 : 80°C 10 : 100°C 11 : 120°C (default)

Name		Function	Addr	Reset
CHG_CTRL6		Control 6	0x06	0x0B
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:1]	R/W	VMIVR[6:0]	0000101	Input MIVR threshold setting 0000000 : 3.9V 0000001 : 4V 0000010 : 4.1V 0000011 : 4.2V 0000100 : 4.3V 0000101 : 4.4V (default) 0000110 : 4.5V … 0011110 : 6.9V 0011111 : 7V … 0110010 : 8.9V 0110011 : 9V … 1010000 : 11.9V 1010001 : 12V … 1011111 : 13.4V 1100000 to 1111111 : 13.4V
0	R/W	MIVR_EN	1	MIVR loop enable 0 : MIVR loop disable 1 : MIVR loop enable (default)

Name		Function	Addr	Reset
CHG_CTRL7		Control 7	0x07	0x4C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:2]	R/W	ICHG[5:0]	010011	Charging regulation current 000000 : 0.1A 000001 : 0.2A 000010 : 0.3A ... 001000 : 0.9A 001001 : 1A 001010 : 1.1A ... 010010 : 1.9A 010011 : 2A (default) ... 011100 : 2.9A 011101 : 3A … 100110 : 3.9A 100111 : 4A … 110000 : 4.9A 110001 : 5A 110010 to 111111 : 5A Note : When ICHG is set above 2.5A, recommend the OCP to set higher level. (Addr 0x0D[2] = 1)
[1:0]	R/W	EOC_TIMER[1:0]	00	EOC back-charging time 00 : 0mins (default) 01 : 30mins 10 : 45mins 11 : 60mins

Name		Function	Addr	Reset
CHG_CTRL8		Control 8	0x08	0xA1
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:4]	R/W	VPREC[3:0]	1010	Pre-Charge voltage threshold 0000 : 2V 0001 : 2.1V 0010 : 2.2V 0011 : 2.3V 0100 : 2.4V 0101 : 2.5V 0110 : 2.6V 0111 : 2.7V 1000 : 2.8V 1001 : 2.9V 1010 : 3.0V (default) 1011 : 3.1V 1100 : 3.2V 1101 : 3.3V 1110 : 3.4V 1111 : 3.5V
[3:0]	R/W	IPREC[3:0]	0001	Pre-Charge current threshold 0000 : 100mA 0001 : 150mA (default) 0010 : 200mA 0011 : 250mA 0100 : 300mA 0101 : 350mA 0110 : 400mA 0111 : 450mA 1000 : 500mA 1001 : 550mA 1010 : 600mA 1011 : 650mA 1100 : 700mA 1101 : 750mA 1110 : 800mA 1111 : 850mA

Name		Function	Addr	Reset
CHG_CTRL9		Control 9	0x09	0x3C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:4]	R/W	IEOC[3:0]	0011	EOC current setting 0000 : 100mA 0001 : 150mA 0010 : 200mA 0011 : 250mA (default) 0100 : 300mA 0101 : 350mA 0110 : 400mA 0111 : 450mA 1000 : 500mA 1001 : 550mA 1010 : 600mA 1011 : 650mA 1100 : 700mA 1101 : 750mA 1110 : 800mA 1111 : 850mA
3	R/W	EOC_EN	1	IEOC enable/disable 0: Disable 1: Enable (default)
[2:0]	R/W	CHG_TDEG_EOC[2:0]	100	EOC deglitch time 000 : 32μs 001 : 64μs 010 : 128μs 011 : 256μs 100 : 2ms (default) 101 : 4ms 110 : 8ms 111 : 16ms

Name		Function	Addr	Reset
CHG_CTRL10		Control 10	0x0A	0x58
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:4]	R/W	OTG_LBP[3:0]	0101	OTG Low battery protection voltage selection (falling edge threshold, hysteresis voltage = 0.4V) 0000 : 2.3V 0001 : 2.4V 0010 : 2.5V 0011 : 2.6V 0100 : 2.7V 0101 : 2.8V (default) 0110 : 2.9V 0111 : 3.0V 1000 : 3.1V 1001 : 3.2V 1010 : 3.3V 1011 : 3.4V 1100 : 3.5V 1101 : 3.6V 1110 : 3.7V 1111 : 3.8V
3	R/W	OTG_LBP_EN	1	OTG Low battery protection enable/disable 0 : Disable 1 : Enable (default)
[2:0]	R/W	OTG_OLP[2:0]	000	OTG over-load threshold (Minimum) 000 : 0.5A (default) 001 : 0.7A 010 : 1.1A 011 : 1.3A 100 : 1.8A 101 : 2.1A 110 : 2.4A 111 : Reserved Note : When OTG_OLP is set 2.1A or 2.4A, recommend the OCP to set higher level. (Addr 0x0D[2] = 1)

Name		Function	Addr	Reset
CHG_CTRL11		Control 11	0x0B	0x2C
Bit	**Mode**	**Name**	**Reset Value**	**Description**
7	R/W	ADP_DIS	0	Charger adapter detection disable 0 : Adapter detection is enabled (default) 1 : Adapter detection is disabled
6	R/W	BATD_EN	0	Charger battery detection when charge done 0 : Battery detection is disabled (default) 1 : Battery detection is enabled
5	R/W	SYSUV_HW_SEL	1	System UV protection selection bit 0 : Buck Switching is not turned off when System UVP 1 : Buck Switching is turned off when System UVP (default)
[4:2]	R/W	SYSREG[2:0]	011	Minimum system regulation voltage 000 : 3.3V 001 : 3.4V 010 : 3.5V 011 : 3.6V (default) 100 : 3.7V 101 : 3.8V 110 : 3.9V 111 : 4.0V
[1:0]	R/W	VRECH	00	Charging recharge voltage threshold with VOREG 00 : 100mV (default) 01 : 200mV 10 : 300mV 11 : 400mV

Name		Function	Addr	Reset
CHG_CTRL12		Control 12	0x0C	0x02
Bit	**Mode**	**Name**	**Reset Value**	**Description**
[7:5]	R/W	WT_FC[2:0]	000	Fast charge Timer 000 : 4hrs (default) 001 : 6hrs 010 : 8hrs 011 : 10hrs 100 : 12hrs 101 : 14hrs 110 : 16hrs 111 : 20hrs
[4:3]	R/W	WT_PRC[1:0]	00	Pre-charge Timer 00 : 30mins (default) 01 : 45mins 10 : 60mins 11 : 60mins
2	R/W	TMR2X_EN	0	Double charger timer during MIVR, AICR, and thermal regulation 0 : Disable 2x extended charger timer (default) 1 : Enable 2x extended charger timer
1	R/W	TMR_EN	1	Charger timer enable/disable 0 : Disable 1 : Enable (default)
0	R/W	TMR_PAUSE	0	Timer control bit 0: Timer is active (default) 1: Timer is pause