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UG0617
User Guide
RTG4 FPGA Development Kit

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Contents

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 5.0

Removed information about the manufacturing test and renamed Chapter 8 as Software Installation, page 42.

1.2 Revision 4.0

The following is a summary of the changes made in revision 4.0 of this document.

- Information about the jumper settings required for programming the device using FlashPro4 was updated. The concerned section is deleted.

1.3 Revision 3.0

The following is a summary of the changes made in revision 3.0 of this document.

- The procedure for measuring 1.2 V current sensing during normal operation was updated. For more information, see 1.2 V Current Sensing for Normal Operation, page 11 (SAR 75660).

1.4 Revision 2.0

The following is a summary of the changes made in revision 2.0 of this document.

- The J34 and J12 FMC connector pinouts were updated. For more information, see Table 15, page 25 and Table 16, page 31 (SAR 75871).
- The specifications for the Marvell PHY were updated. For more information, see Marvell PHY (88E1340S), page 18 (SAR 74316).
- The clock oscillator specifications were updated. For more information, see Clock Oscillator, page 21 (SAR 77521).
- The kit contents were updated. For more information, see Kit Contents, page 2 (SAR 79281).
- The RTG4 Development Kit Block Diagram was updated. For more information, see Figure 1, page 3 (SAR 80330).

1.5 Revision 1.0

Revision 1.0 was the first publication of this document.

2 Introduction

The Microsemi RTG4™ Field Programmable Gate Array (FPGA) Development Kit provides designers with an evaluation and development platform for applications such as data transmission, serial connectivity, bus interface, and high-speed designs using the RTG4 devices. The development board features an RT4G150 device offering 151,824 logic elements in a ceramic package with 1,657 pins.

The RTG4 Development Board includes two 1 GB Double Data Rate 3 (DDR3) memories and two 1 GB of SPI flash memories. The board also has several standard and advanced peripherals, such as PCIe x4 edge connector, two FMC connectors for using several off-the-shelf daughter cards, USB, Philips interintegrated circuit (I^2C), gigabit Ethernet port, serial peripheral interface (SPI), and UART. A high-precision operational amplifier circuitry on the board helps measure the device core power consumption. A FlashPro programmer is embedded on the board, which allows RTG4 FPGA programming through the JTAG interface.

2.1 Kit Contents

The following table lists the contents of the RTG4 Development Kit.

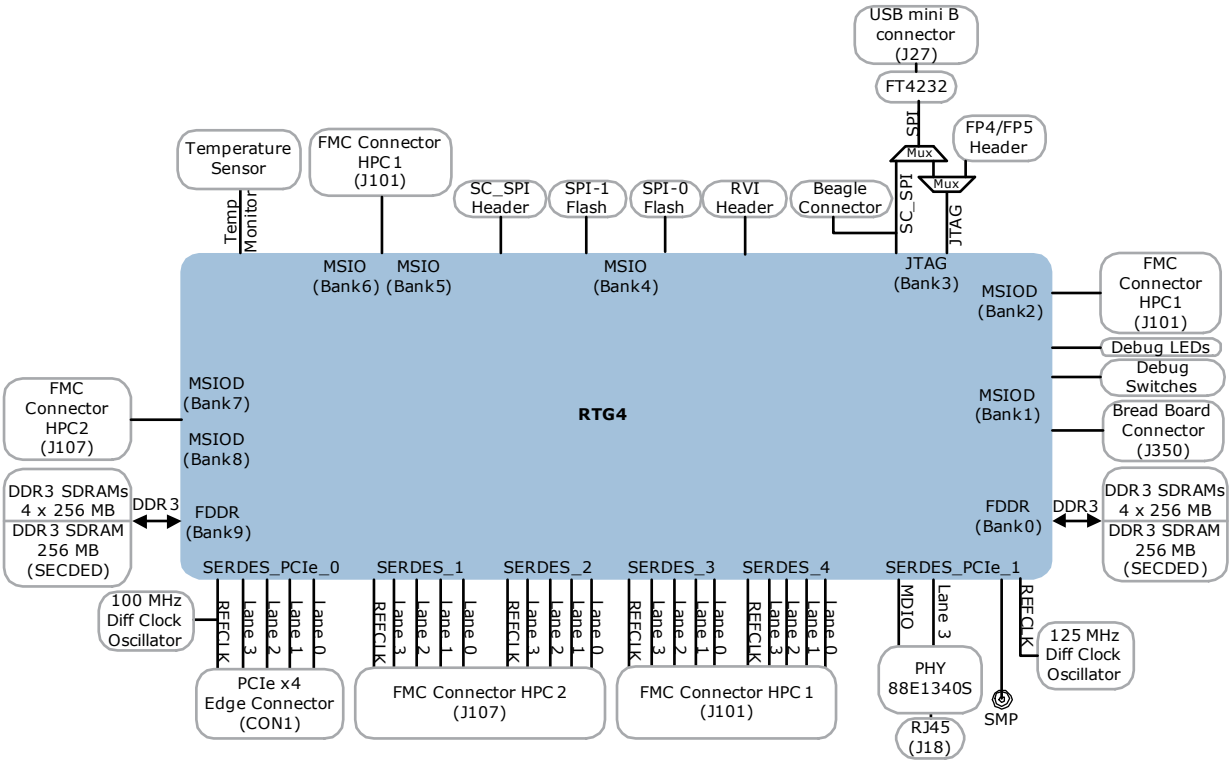
Table 1 • **Kit Contents**

Item	Quantity
RTG4 Development Board with one RT4G150 PROTO FPGA in either a CB1657 or CG1657 package	1
USB A-male to micro-B male cable, three feet long 28/28AWG USB 2	1
USB A to mini-B cable	1
12 V, 5 A AC power adapter	1
Quickstart card	1

2.2 Block Diagram

The following figure shows the RTG4 Development Kit block diagram.

Figure 1 • **RTG4 Development Kit Block Diagram**



2.3 Web Resources

More information about the RTG4 Development Kit is available at *http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/rtg4-development-kit*.

2.4 Board Description

The RTG4 Development Kit offers a full-featured 150,000 logic element (LE) RTG4 FPGA. The board integrates the following features on a single chip:

- Radiation-tolerant, flash-based FPGA fabric.
- Industry standard 4-input lookup table-based (LUT) FPGA fabric with integrated math blocks.
- High-performance SerDes.
- Integrated hard DDR3 memory controllers with error correction.
- Static random-access memory (SRAM).
- Programmable read-only memory (µPROM).

The RTG4 Development Kit has as the following standard interfaces:

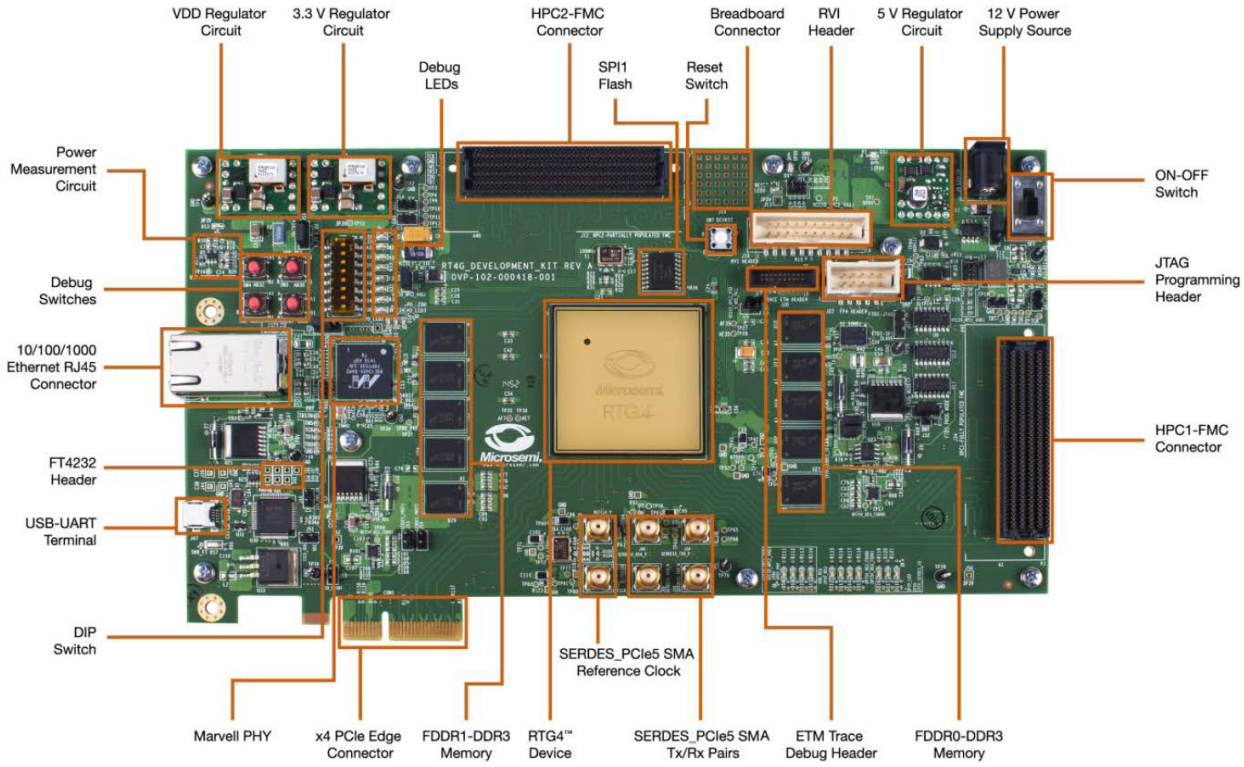
- Two independent 1 GB DDR3 synchronous dynamic random access memory (SDRAM).
- Two independent 1 GB SPI flash memories.
- PCIe (Gen1) x1 interface accessible through SMA cables.
- PCIe x4 edge connector.
- One pair SMA connectors for testing the full-duplex SerDes channel.
- Two FMC connectors with HPC pin-out for expansion.
- RJ45 interface for 10/100/1000 Ethernet.
- USB micro-AB connector.
- Headers for SPI and GPIOs.
- FTDI programmer interface to program the external SPI flash.

- JTAG programming interface.
- RVI header for application programming and debug.
- FlashPro4 or FlashPro5 programming header and embedded FlashPro5 programmer.
- Dual in-line package (DIP) switches for user application.
- Push-button switches and LEDs for demo purposes.
- Current measurement test points.

The unused MSIO signals are routed to the on-board FMC connectors and unused MSIOD signals are routed to bread board connector (J10) space.

The following figure shows the RTG4 Development Board.

Figure 2 • **RTG4 Development Board**



2.5 Board Key Components

The following table lists key components of the RTG4 Development Board.

Table 2 • **RTG4 Development Board Components**

Name	Description
RTG4 FPGA	Microsemi RT4G150 device in a ceramic package with 1,657 pins.
DDR3 synchronous dynamic random access memory (SDRAM)	8 × 256 MB (256 MB Micron DDR3 memories MT41K256M8DA-125 IT:K) for storing data. 2 × 256 MB (512 MB Micron DDR3 memory MT41K256M8DA-125 IT:K) for storing the ECC bits.
SPI Flash	2 gigabit (2 ×1 Gigabit) SPI flash Micron N25Q00AA13GSF40G chips connected to the MSIO pins of the RTG4 FPGA.
Ethernet	RJ45 connector (Ethernet jack with magnetics) interfacing with a Marvell 10/100/1000 BASE-T PHY chip 88E1304S in Serial Gigabit Media Independent Interface (SGMII) mode, interfacing with the Ethernet port of the RTG4 device (on-chip MAC and external PHY).

Table 2 • **RTG4 Development Board Components**

Name	Description
RVI Header	RVI header for application programming and debug from Keil ULINK or IAR J-Link.
Embedded FlashPro5	Embedded FlashPro5 for RTG4 programming and debugging with Microsemi tools.
Future Technology Devices International (FTDI) programmer	FTDI programmer interface (J47) to program the external SPI flash. An FTDI chip is also used to change the JTAG_SEL signal (high or low) remotely for switching between the RVI header and JTAG mode.
Embedded trace macro (ETM) cell header	ETM header for debug.
PCIe edge connector	PCI Express edge connector with four lanes.
Light-emitting diodes (LEDs)	Eight active-low LEDs connected to some of the user I/Os for debugging/ testing.
Push-button reset	Active-low push-button system reset for the RTG4 device.
Push-button and DIP switches	Four active-low push-button switches and one DIP switch for test and navigation.
FMC connectors	Two FMC connectors to connect the external daughter boards. Connector array socket 400 pins (40 × 10), 1.27 mm pitch. The SerDes pins and unused user MSIO/MSIOD are routed from the RTG4 device to the J34 and J12 connectors.
Chip	A simple three-pin voltage monitor and power-on reset that holds reset for 150 ms for stabilization after the power returns to tolerance.
OSC-100	100 MHz clock oscillator (differential output) used for SERDES_PCIe_0 interface.
OSC-100	100 MHz clock oscillator (differential output) connected to RTG4 pins AB37 and AB3.
OSC-125	125 MHz clock oscillator (differential output) used for SERDES_PCIe_1 interface.
OSC-50	50 MHz single-ended clock source connected to RTG4 pin AA39 (MSIOD73PB1/GB12_23/CCC_NE0_CLKI2).
FT4232H	USB-to-quad serial ports in various configurations.
TPS3808G09DBVR	A supervisory circuit that monitors system core voltage, asserting an open-drain reset signal when the sense voltage drops below a preset threshold or when the manual reset (MR) pin drops to a logical low.
LM99CIMM	A remote diode temperature sensor with a two-wire System Management Bus (SMBus) serial interface connected to pin AK31 - Temp Monitor.
HTST-110-01-L-DV	RVI header J18.

3 Installation and Settings

This section provides information about the software and hardware settings for the RTG4 Development Kit.

3.1 Software Installation

Download and install the latest Microsemi Libero® System-on-Chip (SoC) software from the Microsemi website and obtain a Platinum license, which is not included in the RTG4 Development Kit. Libero v11.4 or later installer has FlashPro5 drivers. For instructions on how to install the Libero software and SoftConsole, see *Libero Software Installation and Licensing Guide*.

For instructions on how to download and install Microsemi DirectCores, SGCores, and driver firmware cores, see *Installing IP Cores and Drivers User Guide*. In order to design with Microsemi FPGAs and SoC, these IP cores must be installed on the PC where Libero SoC is installed while designing with Microsemi FPGAs and SoCs.

3.2 Hardware Settings

This section provides information about default jumper settings, switches, LEDs, and DIP switches for the RTG4 Development Kit.

3.2.1 Default Jumpers Settings

Connect the jumpers with the default settings specified in the following table to evaluate the pre-programmed demo design.

Table 3 • **Jumper Settings**

Jumper	Description	Pin	Default Settings
Power Supply			
J16	Jumper to select the RTG4 core voltage VDD_REG to 1.2 V	Pin 1-2 for 1.0 V core voltage. Core supply 1.0 V operation is not supported.	Open
		Pin 2-3 for 1.2 V core voltage.	Closed
J19	Jumper to select the voltage levels for MSIO-FMC connector (VCCIO_HPC1_VADJ) to 3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V	Pin 1-2 for 3.3 V.	Closed
		Pin 3-4 for 2.5 V.	Open
		Pin 5-6 for 1.8 V.	Open
		Pin 7-8 for 1.5 V.	Open
		Pin 9-10 for 1.2 V.	Open
J11	Jumper to select the voltage levels for MSIOD-FMC connector (VCCIO_HPC2_VADJ) to 2.5 V or 1.8 V or 1.5 V or 1.2 V	Pin 1-2 for 2.5 V.	Closed
		Pin 3-4 for 1.8 V.	Open
		Pin 5-6 for 1.5 V.	Open
		Pin 7-8 for 1.2 V.	Open
J26	Jumper to short VCCIO_HPC1_VIO_B_M2C_FMC supply to 2P5	Two-pin header.	Closed
J21	Jumper to short VCCIO_HPC2_VIO_B_M2C_FMC supply to VCCIO_HPC2_VADJ	Two-pin header.	Closed

Table 3 • **Jumper Settings *(continued)***

Jumper	Description	Pin	Default Settings
Power Supply			
J17	Jumper to select either SW6 input or ENABLE_FT4232 signal from FT4232H chip	Pin 1-2 for SW6 selection.	Closed
		Pin 2-3 for Enable_FT4232 signal control.	Open
J23	Jumper to short VPP with 3P3V_LDO	Two-pin header.	Closed
J33	Jumper for SERDES VDDIO	Pin 1-2.	Closed
		Pin 3-4.	Closed
Marvell PHY			
J28	Jumper to select either PHY_CONFIG1 or M2S_PHY_CONFIG1 for Global hardware configuration CONFIG[1]	Pin 1-2 to connect CONFIG [1] to P2_LED[2] pin of 88E1340S.	Open
		Pin 2-3 to connect CONFIG [1] to RTG4-B31 pin MSIO328PB4.	Open
J31	Jumper to short AC test points for debugging (It is recommended not to connect, refer to Marvell PHY Datasheet)	Two-pin header.	Open
Programming			
J32	JTAG selection jumper to select between JTAG programming mode or FTDI programming mode	Pin 1-2 for embedded FlashPro5 JTAG programming.	Closed
		Pin 2-3 for external FlashPro4 programming header.	Open
		Pin 2-4 for JTAG_SEL pin to DD1 signal of FT4232H chip.	Open
J27	Jumper to select FTDI JTAG/SPI slave programming	Pin 1-2 for FTDI JTAG programming.	Closed
		Pin 2-3 for FTDI SPI Slave programming.	Open
J51	Jumper to short BD2 and BD1 pins of FT4232 chip	Two-pin header.	Open
J46	Jumper to control the signal “ENABLE_FT4232” through FTDI chip	Two-pin header.	Open

For locations of various jumpers and test points on the RTG4 Development Board, see Figure 19, page 39.

3.2.2 LEDs

The following table lists the power supply and Ethernet LEDs.

Table 4 • **LEDs**

LED	Description
DS12	VDD_REG supply
DS13	1P5V_REG supply
DS14	0P75V_REG_FDDR0 supply
DS15	0P75V_REG_FDDR1 supply

Table 4 • **LEDs *(continued)***

LED	Description
DS8	VCCIO_HPC1_VADJ supply
DS9	VCCIO_HPC2_VADJ supply
DS10	1P8V supply
DS11	1P0V_PHY supply
DS16	3P3V_LDO supply
DS17	2P5V supply
DS18	1P2V_SERDES_IO supply
DS3	3P3V supply
DS2	5P0V supply
DS1	12P0V supply
DS7	VCC_BUS supply
DS5	Power supply connected to parallel LED output port 0 (P0_LED[0]) of Marvell PHY
DS4	Power supply connected to parallel LED output port 0 (P0_LED[2]) of Marvell PHY
DS6	Power supply connected to parallel LED output port 0 (P0_LED[3]) of Marvell PHY

3.2.3 Test Points

The following table lists USB, ground, and other test points.

Table 5 • **Test Points**

Test Point	Description
TP1, TP2, TP76	GND
TP14	VDD_REG
TP7	5 V
TP12	3.3 V
TP19	3P3V_LDO
TP30	2P5V
TP59	1.5 V
TP57	0.75 V (FDDR0)
TP69	0.75 V (FDDR1)
TP18	VCCIO_HPC1_VAD
TP5	VCCIO_HPC2_VAD
TP43	1.8 V
TP37	PHY 1.0 V
TP48	1P2V_SERDES_IO

3.3 Power Sources

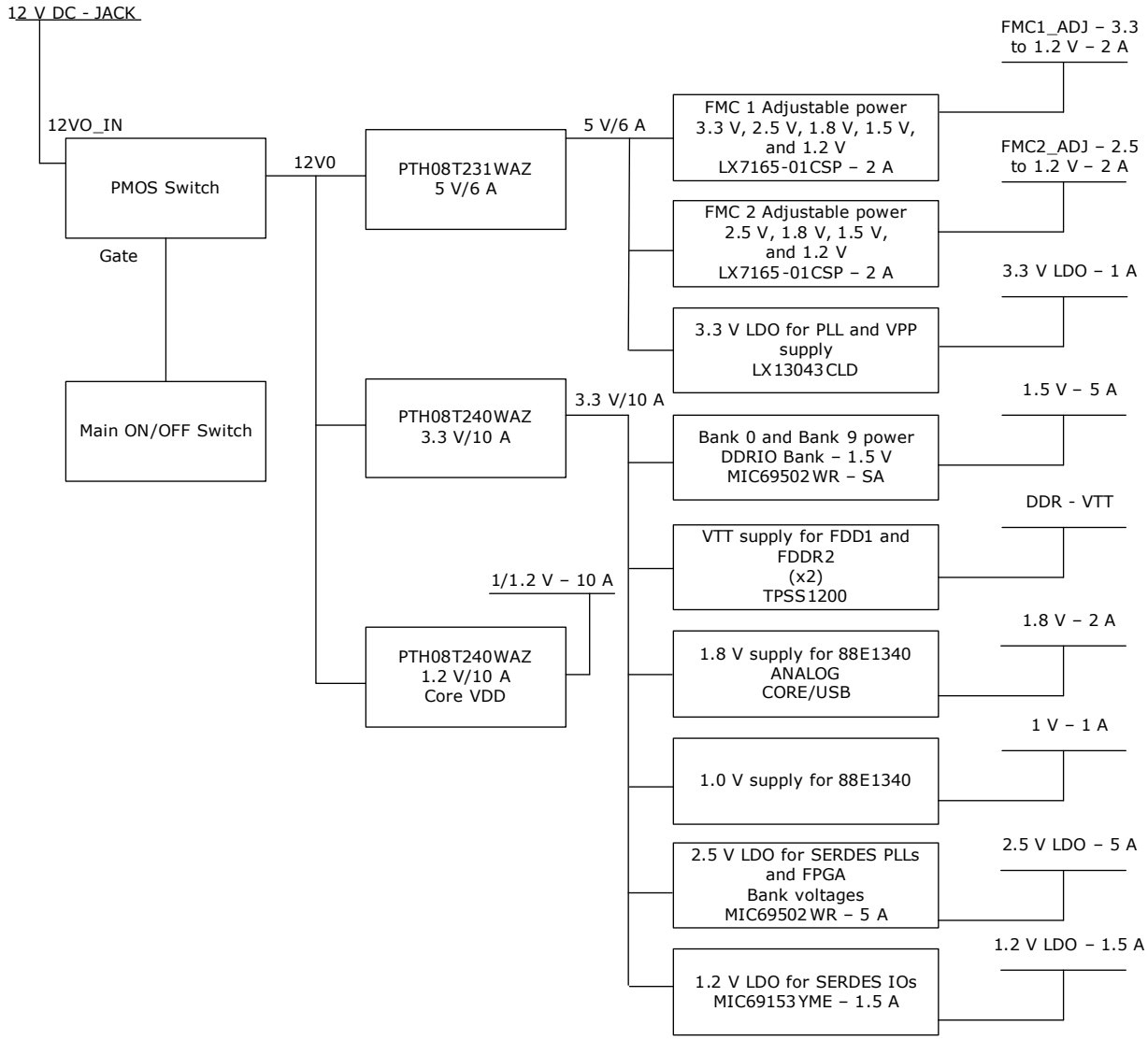
The following table lists the key power supplies required for normal operation of the RTG4 Development Kit.

Table 6 • **I/O Voltage Rails**

RTG4 Bank	I/O Rail	Voltage
Bank0	1P5V_REG	1.5 V
Bank1	2P5V	2.5 V
Bank2	VCCIO_HPC1_VIO_B_M2C_FMC	1.5 V
Bank3	3P3V	3.3 V
Bank4	3P3V	3.3 V
Bank5	VCCIO_HPC1_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank6	VCCIO_HPC1_VADJ	3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank7	VCCIO_HPC2_VIO_B_M2C_FMC	2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank8	VCCIO_HPC2_VADJ	2.5 V, 1.8 V, 1.5 V, or 1.2 V
Bank9	1P5V_REG	2.5 V
VDD	VDD_REG	1.2 V or 1.0 V
VPP	VPP	3.3 V
VREF0	0P75V_VTT_REF_FDDR0	0.75 V
VREF9	0P75V_VTT_REF_FDDR1	0.75 V
SERDES_VDDI	2P5V	2.5 V
VDDPLL	3P3V_LDO	3.3 V

The following figure shows the voltage rails (12 V, 5 V, 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, 1.0 V, and 0.75 V) available in the RTG4 Development Kit.

Figure 3 • **Voltage Rails in the RTG4 Development Kit**



4 Key Components Description and Operation

This section describes the key component interfaces of the RTG4 Development Kit. For device datasheets, see *http://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/rtg4-development-kit*.

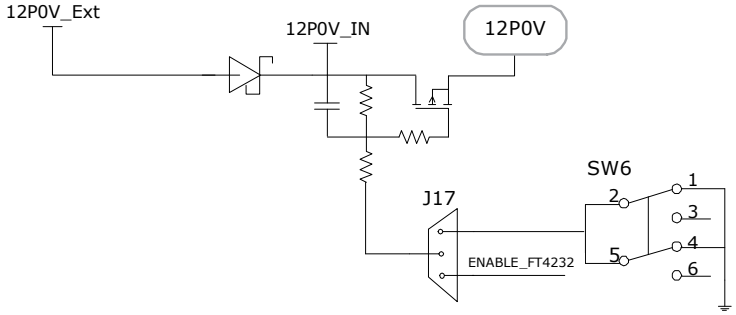
4.1 Powering Up the Board

The RTG4 Development Board is powered using a 12 V external DC jack (12P0V_Ext), as shown in the following figure.

To power up the board:

1. Connect the 12 V power supply brick to the **J9** to supply power to the board.
2. Switch ON the **SW6** power supply switch.

Figure 4 • **Powering Up the Board**



4.2 Current Measurement

This section provides information about current sensing in various modes.

4.2.1 1.2 V Current Sensing for Normal Operation

For applications that require current measurement, high-precision operational amplifier circuitry (U5 with gain 5) is provided on the board to measure the output voltage at the **TP16** test point.

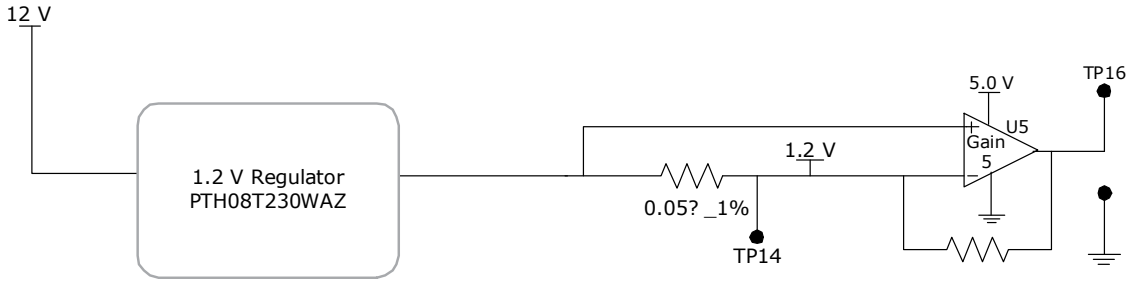
The following steps describe how to measure the core power.

1. Measure the output voltage (V_{out}) at TP16.
2. I = V_{out}/(5*0.05), where 5 is the gain of the operational amplifier U5 and 0.05 is the current sense resistor value in ohms.
3. P = VI, where V is voltage at TP14 and I is voltage at TP16*4.
4. Therefore, core power consumed (P) = V(TP14)*V(TP16)*4.

For example, when the voltage measured across TP16 is 0.5 V, the core power consumed is 2.4 W.

The following figure shows the on-board core power measurement circuity.

Figure 5 • **Core Power Measurement**



4.3 Memory Interface

RTG4 fabric I/Os are provided for the FDRR_E and FDDR_W memories shown in the following figure.

4.3.1 FDDR_E and FDDR_W—DDR3 SDRAM

Each FDDR is provided with four chips of 256 MB DDR3 memory as flexible volatile memory for storing user data. A chip with 256 MB DDR3 memory is provided for ECC. The single-error correction and double-error detection (SECDED) feature can be enabled using ECC. The DDR3 interface is implemented in Bank2.

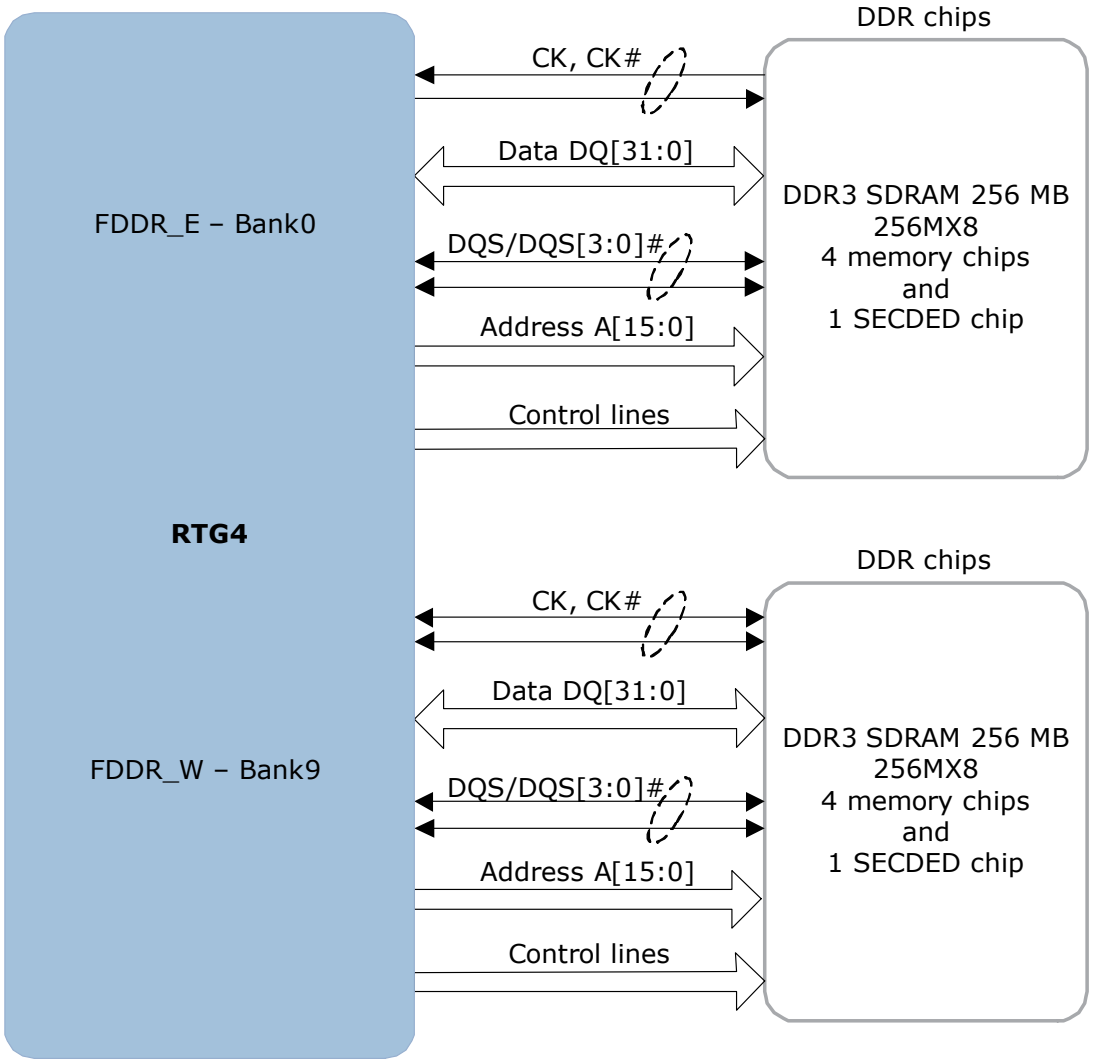
The following list describes features of the memory interface:

- MT41K256M8: 32 Meg × 8 × 8 banks
- Density: 256 MB
- Clock rate: 333 MHz
- Data rate: DDR3, 666 MHz
- Total capacity: 1 GB from four chips

Note: For more information, see the Board Level Schematics document (provided separately).

The following figure shows the memory interface of the RTG4 Development Board.

Figure 6 • **Memory Interface**



Note: DDR3 chip supports single bit error correction and dual bit error detection.

4.4 SerDes Interface

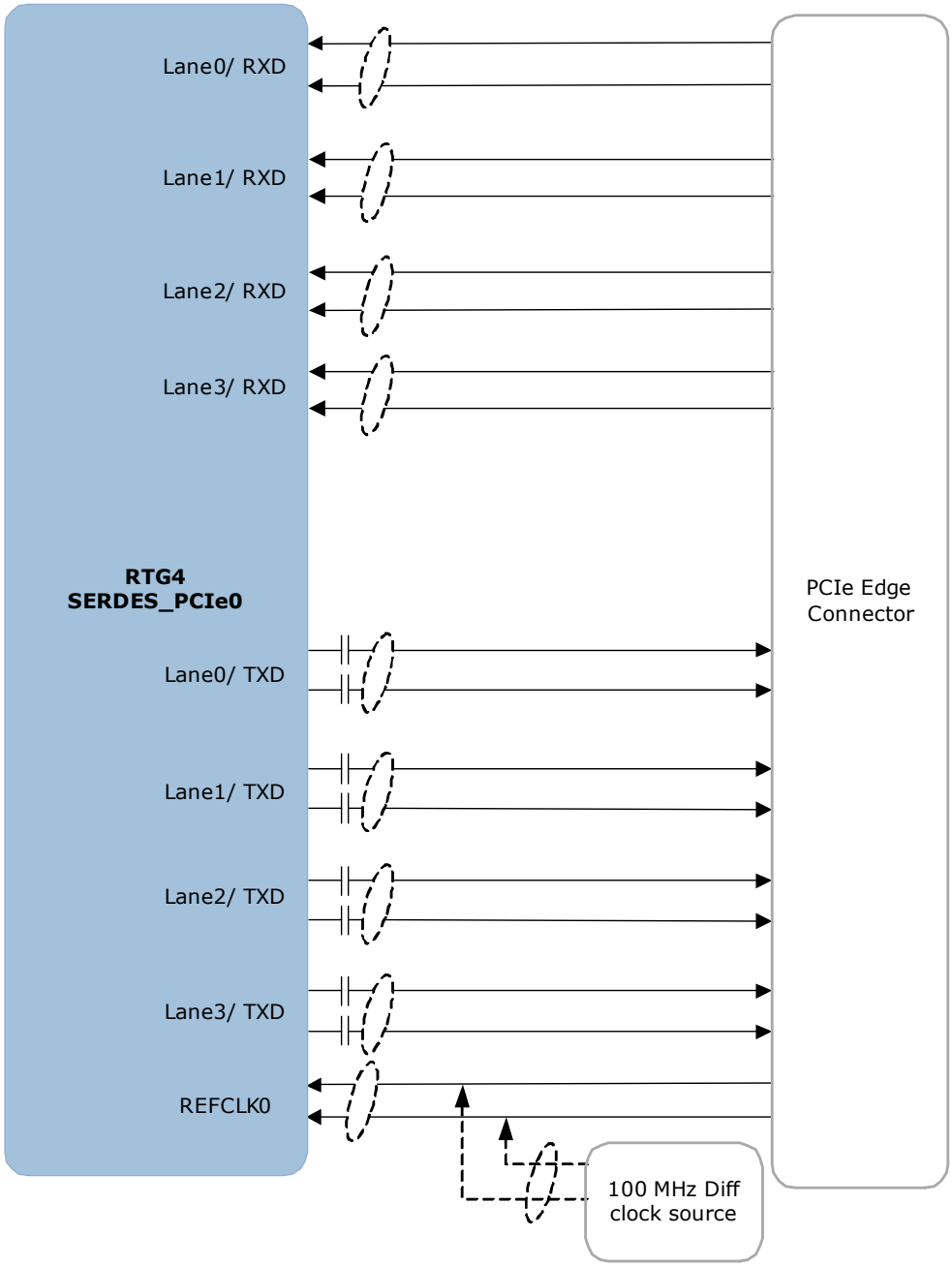
The RT4G150 FPGA device on the RTG4 Development Kit has 24 SerDes lanes. The SerDes block can be accessed using the PCIe edge connector, high-speed SMA connectors, and on-board FMC connectors.

4.4.1 SERDES PCIe0 Interface

The SERDES PCIe 0 interface (lanes 0/1/2/3) are directly routed to the PCIe connector. The reference clock is directly routed from the PCIe connector and optionally from the 100 MHz differential clock source.

The following figure shows the SERDES PCIe0 interface of the RTG4 Development Board.

Figure 7 • **SERDES_PCIe0 Interface**



TXD pairs are capacitively coupled to the RTG4 device. Series AC-coupling capacitors are used to set the common-mode voltage.

Mount R365 and R363 (remove R370 and R361) to source the clock from the100 MHz differential oscillator to the reference clock.

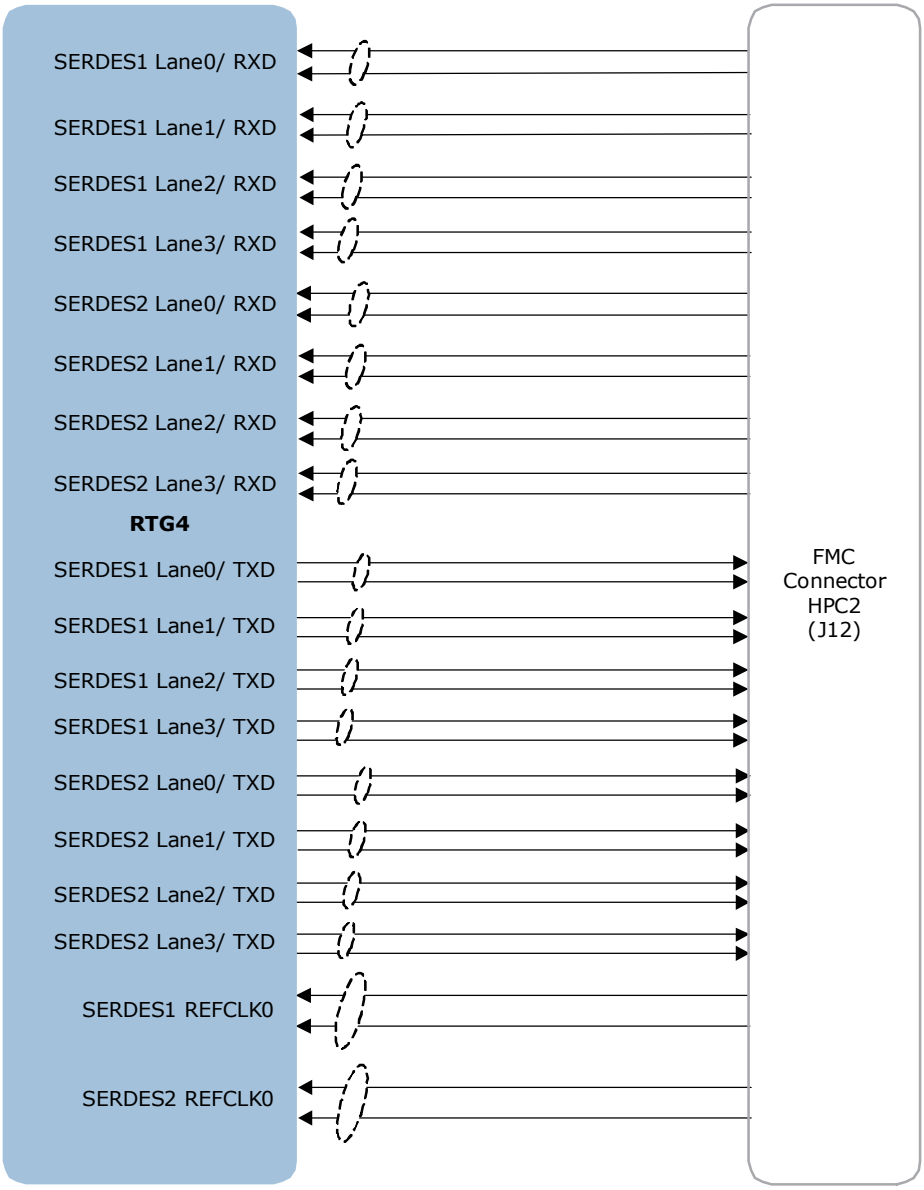
For more information, see the Board Level Schematics document (provided separately).

4.4.2 SERDES1 and SERDES2 Interfaces

The SERDES1 and SERDES2 interfaces (lanes 0/1/2/3) are routed to the FMC connector J12. Reference clocks of the SERDES1 and SERDES2 interfaces are routed from the FMC connector.

The following figure shows the SERDES1 and SERDES1 interfaces of the RTG4 Development Board.

Figure 8 • **SERDES1 and SERDES2 Interfaces**



According to the VITA-57 standard, series capacitors should be placed on the daughter board for TXD and RXD pins.

For more information, see the Board Level Schematics document (provided separately).

The following table lists the J34 pinout of the SERDES3 and SERDES4 interfaces.

Table 7 • **SERDES1 and SERDES2 Interfaces—J12 Pinout**

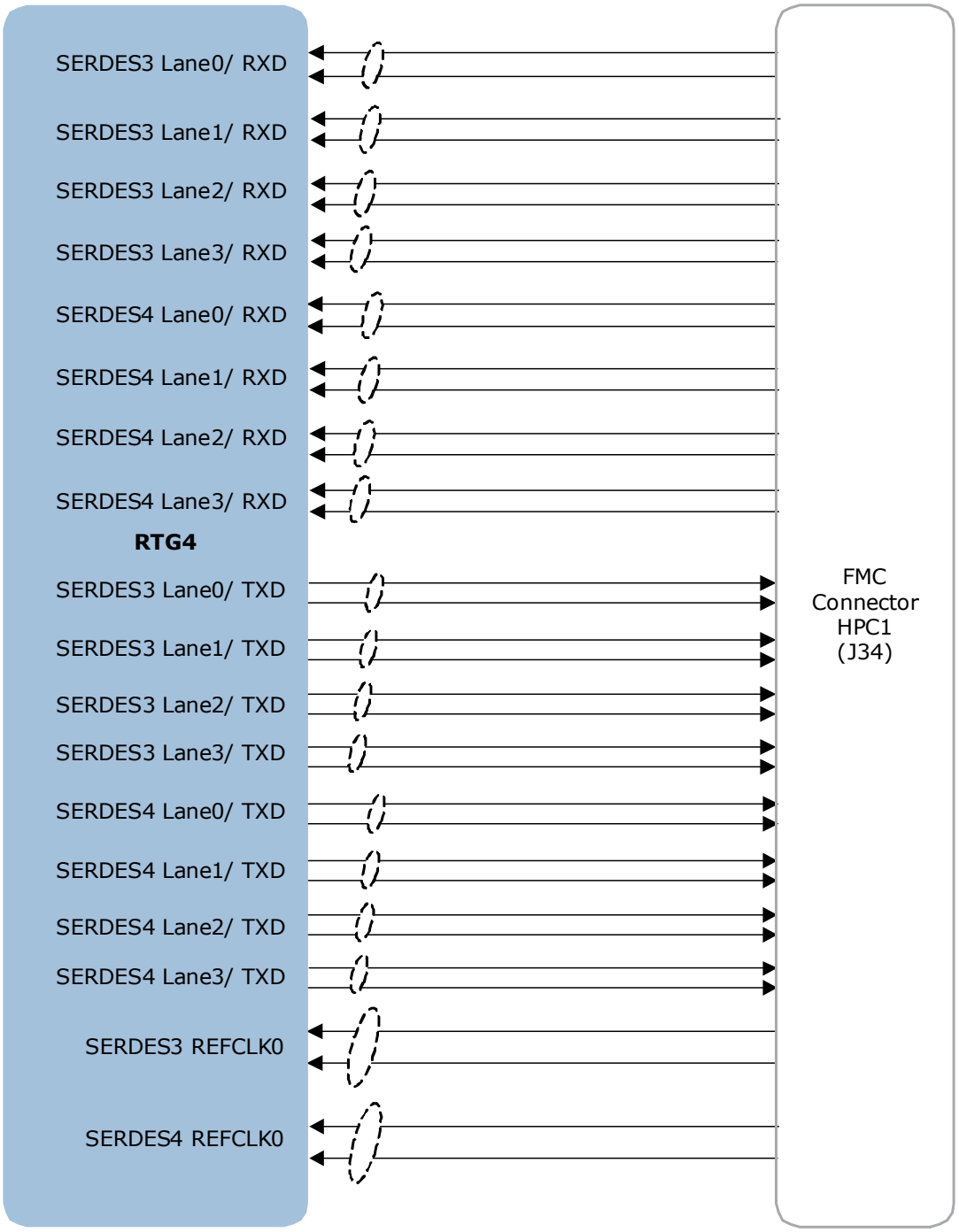
FMC Pin Number-J12	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
A2	HPC2_SERDES1_RXD1_P	AY11	SERDES_1_RXD1_P
A3	HPC2_SERDES1_RXD1_N	BA11	SERDES_1_RXD1_N
A6	HPC2_SERDES1_RXD2_P	AV12	SERDES_1_RXD2_P
A7	HPC2_SERDES1_RXD2_N	AW12	SERDES_1_RXD2_N
A10	HPC2_SERDES1_RXD3_P	AY13	SERDES_1_RXD3_P
A11	HPC2_SERDES1_RXD3_N	BA13	SERDES_1_RXD3_N
A14	HPC2_SERDES2_RXD0_P	AY15	SERDES_2_RXD0_P
A15	HPC2_SERDES2_RXD0_N	BA15	SERDES_2_RXD0_N
A18	HPC2_SERDES2_RXD1_P	AV16	SERDES_2_RXD1_P
A19	HPC2_SERDES2_RXD1_N	AW16	SERDES_2_RXD1_N
A22	HPC2_SERDES1_TXD1_P	AU11	SERDES_1_TXD1_P
A23	HPC2_SERDES1_TXD1_N	AT11	SERDES_1_TXD1_N
A26	HPC2_SERDES1_TXD2_P	AU13	SERDES_1_TXD2_P
A27	HPC2_SERDES1_TXD2_N	AT13	SERDES_1_TXD2_N
A30	HPC2_SERDES1_TXD3_P	AW14	SERDES_1_TXD3_P
A31	HPC2_SERDES1_TXD3_N	AV14	SERDES_1_TXD3_N
A34	HPC2_SERDES2_TXD0_P	AU15	SERDES_2_TXD0_P
A35	HPC2_SERDES2_TXD0_N	AT15	SERDES_2_TXD0_N
A38	HPC2_SERDES2_TXD1_P	AU17	SERDES_2_TXD1_P
A39	HPC2_SERDES2_TXD1_N	AT17	SERDES_2_TXD1_N
B12	HPC2_SERDES2_RXD3_P	AY19	SERDES_2_RXD3_P
B13	HPC2_SERDES2_RXD3_N	BA19	SERDES_2_RXD3_N
B16	HPC2_SERDES2_RXD2_P	AY17	SERDES_2_RXD2_P
B17	HPC2_SERDES2_RXD2_N	BA17	SERDES_2_RXD2_N
B20	HPC2_SERDES2_REFCLK0_P	AR16	SERDES_2_REFCLK_P
B21	HPC2_SERDES2_REFCLK0_N	AP16	SERDES_2_REFCLK_N
B32	HPC2_SERDES2_TXD3_P	AU19	SERDES_2_TXD3_P
B33	HPC2_SERDES2_TXD3_N	AT19	SERDES_2_TXD3_N
B36	HPC2_SERDES2_TXD2_P	AW18	SERDES_2_TXD2_P
B37	HPC2_SERDES2_TXD2_N	AV18	SERDES_2_TXD2_N
C2	HPC2_SERDES1_TXD0_P	AU9	SERDES_1_TXD0_P
C3	HPC2_SERDES1_TXD0_N	AT9	SERDES_1_TXD0_N
C6	HPC2_SERDES1_RXD0_P	AV10	SERDES_1_RXD0_P
C7	HPC2_SERDES1_RXD0_N	AW10	SERDES_1_RXD0_N
D4	HPC2_SERDES1_REFCLK0_P	AR12	SERDES_1_REFCLK_P
D5	HPC2_SERDES1_REFCLK0_N	AP12	SERDES_1_REFCLK_N

4.4.3 SERDES3 and SERDES4 Interfaces

The SERDES3 and SERDES4 interfaces (lanes 0/1/2/3) are routed to the FMC connector J34. Reference clocks of the SERDES3 and SERDES4 interfaces are routed from the FMC connector.

The following figure shows the SERDES3 and SERDES4 interfaces of the RTG4 Development Board.

Figure 9 • **SERDES3 and SERDES4 Interfaces**



According to the VITA-57 standard, series capacitors should be placed on the daughter board for TXD and RXD pins.

For more information, see the Board Level Schematics document (provided separately).

The following table lists the J34 pinout of the SERDES3 and SERDES4 interfaces.

Table 8 • **SERDES3 and SERDES4 Interfaces—J34 Pinout**

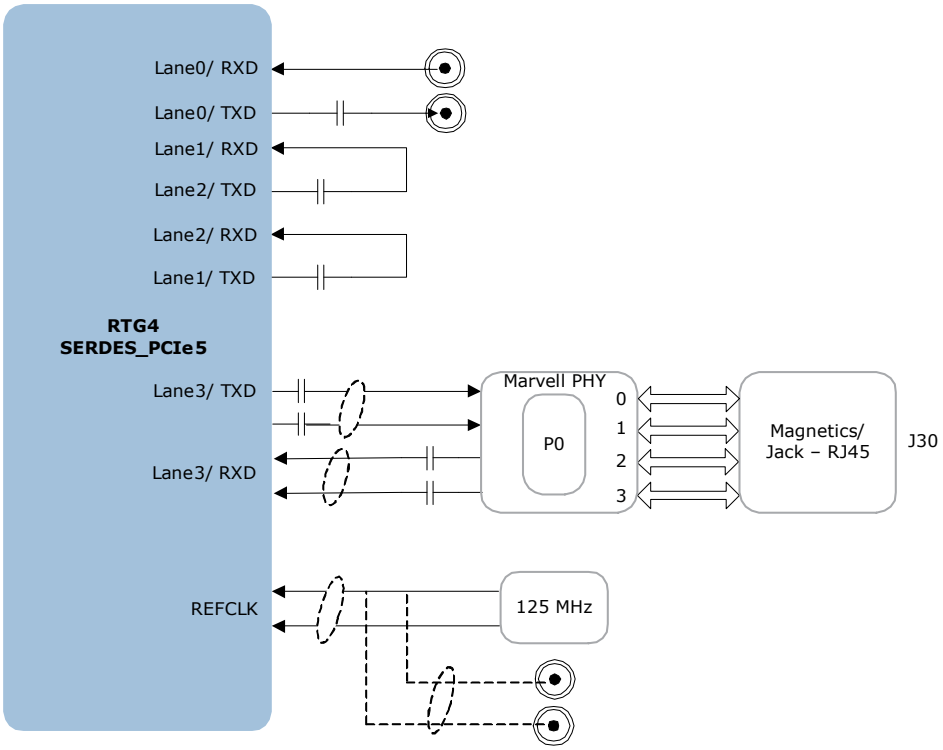
FMC Pin Number-J34	FMC Net Name	RTG4 Pin Number	RTG4 Pin Name
A2	HPC1_SERDES3_RXD1_P	BA25	SERDES_3_RXD1_P
A3	HPC1_SERDES3_RXD1_N	AY25	SERDES_3_RXD1_N
A6	HPC1_SERDES3_RXD2_P	AW26	SERDES_3_RXD2_P
A7	HPC1_SERDES3_RXD2_N	AV26	SERDES_3_RXD2_N
A10	HPC1_SERDES3_RXD3_P	BA27	SERDES_3_RXD3_P
A11	HPC1_SERDES3_RXD3_N	AY27	SERDES_3_RXD3_N
A14	HPC1_SERDES4_RXD0_P	BA29	SERDES_4_RXD0_P
A15	HPC1_SERDES4_RXD0_N	AY29	SERDES_4_RXD0_N
A18	HPC1_SERDES4_RXD1_P	AW30	SERDES_4_RXD1_P
A19	HPC1_SERDES4_RXD1_N	AV30	SERDES_4_RXD1_N
A22	HPC1_SERDES3_TXD1_P	AV24	SERDES_3_TXD1_P
A23	HPC1_SERDES3_TXD1_N	AW24	SERDES_3_TXD1_N
A26	HPC1_SERDES3_TXD2_P	AT25	SERDES_3_TXD2_P
A27	HPC1_SERDES3_TXD2_N	AU25	SERDES_3_TXD2_N
A30	HPC1_SERDES3_TXD3_P	AT27	SERDES_3_TXD3_P
A31	HPC1_SERDES3_TXD3_N	AU27	SERDES_3_TXD3_N
A34	HPC1_SERDES4_TXD0_P	AW28	SERDES_4_TXD0_N
A35	HPC1_SERDES4_TXD0_N	AV28	SERDES_4_TXD0_P
A38	HPC1_SERDES4_TXD1_P	AT29	SERDES_4_TXD1_P
A39	HPC1_SERDES4_TXD1_N	AU29	SERDES_4_TXD1_N
B12	HPC1_SERDES4_RXD3_P	AW32	SERDES_4_RXD3_P
B13	HPC1_SERDES4_RXD3_N	AV32	SERDES_4_RXD3_N
B16	HPC1_SERDES4_RXD2_P	BA31	SERDES_4_RXD2_P
B17	HPC1_SERDES4_RXD2_N	AY31	SERDES_4_RXD2_N
B20	HPC1_SERDES4_REFCLK0_P	AP30	SERDES_4_REFCLK_P
B21	HPC1_SERDES4_REFCLK0_N	AR30	SERDES_4_REFCLK_N
B32	HPC1_SERDES4_TXD3_P	AT33	SERDES_4_TXD3_P
B33	HPC1_SERDES4_TXD3_N	AU33	SERDES_4_TXD3_N
B36	HPC1_SERDES4_TXD2_P	AT31	SERDES_4_TXD2_P
B37	HPC1_SERDES4_TXD2_N	AU31	SERDES_4_TXD2_N
C2	HPC1_SERDES3_TXD0_P	AT23	SERDES_3_TXD0_P
C3	HPC1_SERDES3_TXD0_N	AU23	SERDES_3_TXD0_N
C6	HPC1_SERDES3_RXD0_P	BA23	SERDES_3_RXD0_P
C7	HPC1_SERDES3_RXD0_N	AY23	SERDES_3_RXD0_N
D4	HPC1_SERDES3_REFCLK0_P	AP26	SERDES_3_REFCLK_P
D5	HPC1_SERDES3_REFCLK0_N	AR26	SERDES_3_REFCLK_N

4.4.4 SERDES PCIe5 Interface

Lane 0 is connected to the SMA connectors, Lane 1 (RXD) is connected to Lane 2 (TXD), Lane 2 (RXD) is connected to Lane 1 (TXD), and Lane 3 (TXD and RXD) is connected to the Marvell PHY device of Port 0. The reference clock is connected from the 125 MHz differential clock oscillator and optionally connected from the SMA connectors.

The following figure shows the SERDES PCIe5 interface of the RTG4 Development Board.

Figure 10 • **SERDES_PCIe5 Interface**



For more information, see the Board Level Schematics document (provided separately).

4.5 Marvell PHY (88E1340S)

The RTG4 Development Kit uses the on-board Marvell Alaska PHY device (88E1340S) for Ethernet communications at 100 Mbps or 1000 Mbps. The 88E1340S device has four independent gigabit Ethernet transceivers, but the board uses only one transceiver. The transceiver performs all the physical layer functions for 100BASE-TX and 1000BASE-T full- or half-duplex Ethernet on a CAT5 twisted-pair cable. The PHY device is connected to a user-provided Ethernet cable through an RJ45 connector with built-in magnetics.

The 88E1340S device supports the quad SGMII for direct connection to a RTG4 chip (see Figure 11, page 19).

It is configured through the CONFIG [3:0] and CLK_SEL [1:0] pins.

The CLK_SEL [1:0] pin is used to select the reference clock input option. On the board, the status of the CLK_SEL0 and CLK_SEL1 pins is high. REF_CLK is a 25 MHz reference differential clock input (Y3). It consists of LVDS differential inputs with a 100 Ω differential internal termination resistor.

- RCLK—Gigabit recovered clock
- SCLK—25 MHz synchronous input reference clock

Expected reference clock (REF_CLK) specifications:

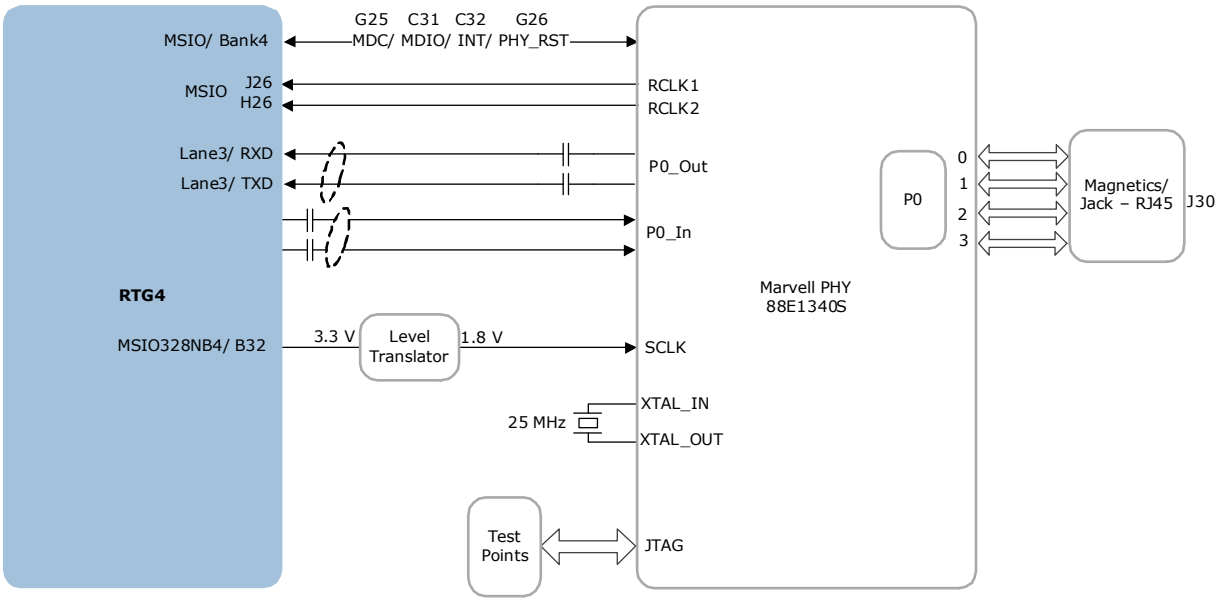
- Voltage level: 3.3 (± 0.3) V
- Differential LVDS

- Symmetry: 50% (± 10%)
- Rise/Fall Time: 1 ns Max—20% to 80% of supply (3.3 V)
- Output Voltage Levels: 0 = 0.90 minimum, 1.10 typical and 1 = 1.43 typical, 1.60 maximum

- Differential Output Voltage: 247 mV minimum, 454 mV maximum

The following figure shows the RTG4 Marvell PHY interface.

Figure 11 • **RTG4 Marvell PHY Interface**



For more information, see the Board Level Schematics document (provided separately).

4.6 Programming

RTG4 FPGAs support multiple programming interfaces and can address a wide range of platform requirements. An RTG4 device can be programmed through the JTAG and SPI interfaces.

The dedicated programming SPI port can operate in SPI slave mode.

For more information about SPI programming, see *RTG4 Programming Guide*.

The following figure shows the programming interface of the RTG4 Development Board.

Figure 12 • **Programming Interface**