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RX130 Group
Renesas MCUs

R01DS0273EJ0200
Rev.2.00
Sep 01, 2017

32-MHz, 32-bit RX MCUs, 50 DMIPS, up to 512-KB flash memory, up to 36 pins capacitive touch sensing unit, up to 6 comms channels, 12-bit A/D, D/A, RTC, IEC60730 compliance, 1.8-V to 5.5-V single supply

Features

■ 32-bit RX CPU core
- Max. operating frequency: 32 MHz
  Capable of 50 DMIPS in operation at 32 MHz
- Accumulator handles 64-bit results (for a single instruction) from 32-bit × 32-bit operations
- Multiplication and division unit handles 32-bit × 32-bit operations (multiplication instructions take one CPU clock cycle)
- Fast interrupt
- CISC Harvard architecture with 5-stage pipeline
- Variable-length instructions, ultra-compact code
- On-chip debugging circuit

■ Low power design and architecture
- Operation from a single 1.8-V to 5.5-V supply
- Three low power consumption modes
- Low power timer (LPT) that operates during the software standby state
- Supply current
  High-speed operating mode: 96 µA/MHz
  Supply current in software standby mode: 0.37 µA
- Recovery time from software standby mode: 4.8 µs

■ On-chip flash memory for code, no wait states
- 64 K/128 K/256 K/383 K/512 Kbytes
- Operation at 32 MHz, read cycle of 31.25 ns
- No wait states for reading at full CPU speed
- Programmable at 1.8 V
- For instructions and operands

■ On-chip data flash memory
- 8 Kbytes (1,000,000 program/erase cycles (typ.))
- BGO (Background Operation)

■ On-chip SRAM, no wait states
- 10 K/16 K/32 K/48 Kbytes size capacities

■ DTC
- Four transfer modes
- Transfer can be set for each interrupt source.

■ ELC
- Module operation can be initiated by event signals without using interrupts.
- Linked operation between modules is possible while the CPU is sleeping.

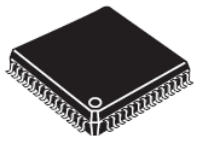
■ Reset and supply management
- Eight types of reset, including the power-on reset (POR)
- Low voltage detection (LVD) with voltage settings

■ Clock functions
- External clock input frequency: Up to 20 MHz
- Main clock oscillator frequency: 1 to 20 MHz
- Sub clock oscillator frequency: 32.768 kHz
- PLL circuit input: 4 MHz to 8 MHz
- Low-speed on-chip oscillator: 4 MHz
- High-speed on-chip oscillator: 32 MHz ± 1 %
- IWDT-dedicated on-chip oscillator: 15 kHz
- Generate a 32.768 kHz clock for the real-time clock
- On-chip clock frequency accuracy measurement circuit (CAC)

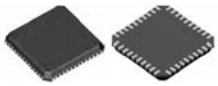
■ Realtime clock
- Adjustment functions (30 seconds, leap year, and error)
- Calendar count mode or binary count mode selectable

■ Independent watchdog timer
- 15-kHz on-chip oscillator produces a dedicated clock signal to drive IWDT operation.

■ Useful functions for IEC60730 compliance
- Self-diagnostic and disconnection-detection assistance functions for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test assistance functions using the DOC, etc.



PLQP0100KB-B 14 × 14mm, 0.5mm pitch
PLQP0080KB-B 12 × 12mm, 0.5mm pitch
PLQP0064GA-A 14 × 14mm, 0.8mm pitch
PLQP0064KB-C 10 × 10mm, 0.5mm pitch
PLQP0048KB-B 7 × 7mm, 0.5mm pitch



PWQN0048KB-A 7 × 7mm, 0.5mm pitch

■ MPC
- Input/output functions selectable from multiple pins

■ Up to 6 communication functions
- SCI with many useful functions (up to 4 channels)
  Asynchronous mode (Fine adjustable baud rate: 0 to 255/255), clock synchronous mode, smart card interface mode
- I^2C bus interface: Transfer at up to 400 kbps, capable of SMBus operation (one channel)
- RSPI (one channel): Transfer at up to 16 Mbps

■ Remote control signal reception
- Two units integrated
- Four pattern waveform matching supported

■ Up to 12 extended-function timersMPC
- 16-bit MTU: input capture, output compare, complementary PWM output, phase counting mode (six channels)
- 8-bit TMR (four channels)
- 16-bit compare-match timers (two channels)

■ 12-bit A/D converter
- Capable of conversion within 1.4 µs
- 17 channels
- Sampling time can be set for each channel
- Conversion results compare features
- Self-diagnostic function and analog input disconnection detection assistance function
- Double trigger (data duplication) function for motor control

■ D/A converter
- Two channels

■ Capacitive touch sensing unit
- Self-capacitance method: A single pin configures a single key, supporting up to 36 keys
- Mutual capacitance method: Matrix configuration with 36pins, supporting up to 324 keys

■ Comparator B
- Two channels

■ General I/O ports
- 5-V tolerant, open drain, input pull-up, switching of driving capacity

■ Temperature sensor

■ Unique ID
- 32-byte ID code for the MCU

■ Operating temperature range
- –40 to +85°C
- –40 to +105°C

■ Applications
- General industrial and consumer equipment

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications, and Table 1.2 gives a comparison of the functions of the products in different packages.
Table 1.1 is for products with the greatest number of functions, so the number of peripheral modules and channels will differ in accordance with the package type. For details, see Table 1.2, Comparison of Functions for Different Packages in the RX130 Group.

Table 1.1 Outline of Specifications (1/3)

Classification	Module/Function	Description
CPU	CPU	• Maximum operating frequency: 32 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: 4-Gbyte linear • Register set General purpose: Sixteen 32-bit registers Control: Eight 32-bit registers Accumulator: One 64-bit registers • Basic instructions: 73 (variable-length instruction format) • DSP instructions: 9 • Addressing modes: 10 • Data arrangement Instructions: Little endian Data: Selectable as little endian or big endian • On-chip 32-bit multiplier: 32-bit × 32-bit → 64-bit • On-chip divider: 32-bit ÷ 32-bit → 32 bits • Barrel shifter: 32 bits
Memory	ROM	• Capacity: 64 K/128 K/256 K/383 K/512 Kbytes • No-wait memory access • Programming/erasing method: Serial programming (asynchronous serial communication), self-programming
	RAM	• Capacity: 10 K/16 K/32 K/48 Kbytes • No-wait memory access
	E2 DataFlash	• Capacity: 8 Kbytes • Number of erase/write cycles: 1,000,000 (typ)
MCU operating mode		Single-chip mode
Clock	Clock generation circuit	• Main clock oscillator, sub-clock oscillator, low-speed on-chip oscillator, high-speed on-chip oscillator, PLL frequency synthesizer, and IWDT-dedicated on-chip oscillator • Oscillation stop detection: Available • Clock frequency accuracy measurement circuit (CAC) • Independent settings for the system clock (ICLK), peripheral module clock (PCLK), and FlashIF clock (FCLK) The CPU and system sections such as other bus masters run in synchronization with the system clock (ICLK): 32 MHz (at max.) Peripheral modules run in synchronization with the PCLKB: 32 MHz (at max.) The flash peripheral circuit runs in synchronization with the FCLK: 32 MHz (at max.) • The ICLK frequency can only be set to FCLK, PCLKB, or PCLKD multiplied by n (n: 1,2,4,8,16,32,64)
Resets		RES# pin reset, power-on reset, voltage monitoring reset, independent watchdog timer reset, and software reset
Voltage detection	Voltage detection circuit (LVDAb)	• When the voltage on VCC falls below the voltage detection level, an internal reset or internal interrupt is generated. Voltage detection circuit 0 is capable of selecting the detection voltage from 4 levels Voltage detection circuit 1 is capable of selecting the detection voltage from 14 levels Voltage detection circuit 2 is capable of selecting the detection voltage from 4 levels
Low power consumption	Low power consumption functions	• Module stop function • Three low power consumption modes Sleep mode, deep sleep mode, and software standby mode
	Function for lower operating power consumption	• Operating power control modes High-speed operating mode, middle-speed operating mode, and low-speed operating mode
Interrupt	Interrupt controller (ICUb)	• Interrupt vectors: 115 • External interrupts: 9 (NMI, IRQ0 to IRQ7 pins) • Non-maskable interrupts: 5 (The NMI pin, oscillation stop detection interrupt, voltage monitoring 1 interrupt, voltage monitoring 2 interrupt, and IWDT interrupt) • 16 levels specifiable for the order of priority

Table 1.1 Outline of Specifications (2/3)

Classification	Module/Function	Description
DMA	Data transfer controller (DTCa)	• Transfer modes: Normal transfer, repeat transfer, and block transfer • Activation sources: Interrupts • Chain transfer function
I/O ports	General I/O ports	100-pin /80-pin /64-pin /48-pin • I/O: 88/68/52/38 • Input: 1/1/1/1 • Pull-up resistors: 88/68/52/38 • Open-drain outputs: 67/47/35/26 • 5-V tolerance: 4/4/2/2
Event link controller (ELC)		• Event signals of 47 types can be directly connected to the module • Operations of timer modules are selectable at event input • Capable of event link operation for port B
Multi-function pin controller (MPC)		Capable of selecting the input/output function from multiple pins
Timers	Multi-function timer pulse unit 2 (MTU2a)	• (16 bits × 6 channels) × 1 unit • Up to 16 pulse-input/output lines and three pulse-input lines are available based on the six 16-bit timer channels • Select from among eight or seven counter-input clock signals for each channel (PCLK/1, PCLK/4, PCLK/16, PCLK/64, PCLK/256, PCLK/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD) other than channel 5, for which only four signals are available. • Input capture function • 21 output compare/input capture registers • Pulse output mode • Complementary PWM output mode • Reset synchronous PWM mode • Phase-counting mode • Capable of generating conversion start triggers for the A/D converter
	Port output enable 2 (POE2a)	Controls the high-impedance state of the MTU's waveform output pins
	Compare match timer (CMT)	• (16 bits × 2 channels) × 1 unit • Select from among four clock signals (PCLK/8, PCLK/32, PCLK/128, PCLK/512)
	Independent watchdog timer (IWDTa)	• 14 bits × 1 channel • Count clock: Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 1, 16, 32, 64, 128, or 256
	Realtime clock (RTCc)*1	• Clock source: Sub-clock • Calendar count mode or binary count mode selectable • Interrupts: Alarm interrupt, periodic interrupt, and carry interrupt
	Low power timer (LPT)	• 16 bits × 1 channel • Clock source: Sub-clock, Dedicated low-speed on-chip oscillator for the IWDT Frequency divided by 2, 4, 8, 16, or 32
	8-bit timer (TMR)	• (8 bits × 2 channels) × 2 units • Seven internal clocks (PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1024, and PCLK/8192) and an external clock can be selected • Pulse output and PWM output with any duty cycle are available • Two channels can be cascaded and used as a 16-bit timer
Communication functions	Serial communications interfaces (SCIg, SCIh)	• 7 channels (channel 0, 1, 5, 6, 8, 9: SCIg, channel 12: SCIh) • SCIg Serial communications modes: Asynchronous, clock synchronous, and smart-card interface On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Start-bit detection: Level or edge detection is selectable. Simple I^2C Simple SPI 9-bit transfer mode Bit rate modulation Event linking by the ELC (only on channel 5) • SCIh (The following functions are added to SCIg) Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format
	I^2C bus interface (RIICa)	• 1 channel • Communications formats: I^2C bus format/SMBus format • Master mode or slave mode selectable • Supports fast mode

Table 1.1 Outline of Specifications (3/3)

Classification	Module/Function	Description
Communication functions	Serial peripheral interface (RSPIa)	• 1 channel • Transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPI clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) • Capable of handling serial transfer as a master or slave • Data formats • Choice of LSB-first or MSB-first transfer The number of bits in each transfer can be changed to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Double buffers for both transmission and reception
	Remote control signal receiver (REMC)	• 2 channels • Four pattern matching (header, data 0, data 1, and special data detection) • 8-byte receive buffer per unit • The operating clock can be selected from among the PCLK, sub-clock, HOCO, IWDTCLK, and TMR.
12-bit A/D converter (S12ADE)		• 12 bits (24 channels × 1 unit) • 12-bit resolution • Minimum conversion time: 1.4 µs per channel when the ADCLK is operating at 32 MHz • Operating modes Scan mode (single scan mode, continuous scan mode, and group scan mode) Group A priority control (only for group scan mode) • Sampling variable Sampling time can be set up for each channel. • Self-diagnostic function • Double trigger mode (A/D conversion data duplicated) • Detection of analog input disconnection • Conversion results compare features • A/D conversion start conditions A software trigger, a trigger from a timer (MTU), an external trigger signal, or ELC • Event linking by the ELC
Temperature sensor (TEMPSA)		• 1 channel • The voltage output from the temperature sensor is converted into a digital value by the 12-bit A/D converter.
D/A converter (DA)		• 2 channels • 8-bit resolution • Output voltage: 0V to AVCC0
CRC calculator (CRC)		• CRC code generation for arbitrary amounts of data in 8-bit units • Select any of three generating polynomials: $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, or $X^{16} + X^{12} + X^5 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable.
Comparator B (CMPBa)		• 2 channels • Function to compare the reference voltage and the analog input voltage • Window comparator operation or standard comparator operation is selectable
Capacitive touch sensing unit (CTSUa)		Detection pin: 36 channels
Data operation circuit (DOC)		Comparison, addition, and subtraction of 16-bit data
Unique ID		32-byte ID code for the MCU
Power supply voltages/Operating frequencies		VCC = 1.8 to 2.4 V: 8 MHz, VCC = 2.4 to 2.7 V: 16 MHz, VCC = 2.7 to 5.5 V: 32 MHz
Operating temperature range		D version: –40 to +85°C, G version: –40 to +105°C
Packages		100-pin LFQFP (PLQP0100KB-B) 14 × 14 mm, 0.5 mm pitch 80-pin LFQFP (PLQP0080KB-B) 12 × 12 mm, 0.5 mm pitch 64-pin LFQFP (PLQP0064KB-C) 10 × 10 mm, 0.5 mm pitch 64-pin LQFP (PLQP0064GA-A) 14 × 14 mm, 0.8 mm pitch 48-pin LFQFP (PLQP0048KB-B) 7 × 7 mm, 0.5 mm pitch 48-pin HWQFN (PWQN0048KB-A) 7 × 7 mm, 0.5 mm pitch
On-chip debugging system		E1 emulator (FINE interface)

Note 1. When the realtime clock is not to be used, refer to section 24.5.7, Initialization Procedure When the Realtime Clock is Not to be Used.

Table 1.2 Comparison of Functions for Different Packages in the RX130 Group

Module/Functions		RX130 Group			
		100 Pins	80 Pins	64 Pins	48 Pins
Interrupts	External interrupts	NMI, IRQ0 to IRQ7		NMI, IRQ0 to IRQ2, IRQ4 to IRQ7	NMI, IRQ0, IRQ1, IRQ4 to IRQ7
DMA	Data transfer controller	Available			
Timers	Multi-function timer pulse unit 2	6 channels (MTU0 to MTU5)			
	Port output enable 2	POE0# to POE3#, POE8#			
	8-bit timer	2 channels × 2 units			
	Compare match timer	2 channels × 1 unit			
	Low power timer	1 channel			
	Realtime clock	Available			Not supported
	Independent watchdog timer	Available			
Communication functions	Serial communications interfaces (SCIg)	6 channels (SCI0, 1, 5, 6, 8, 9)	3 channels (SCI1, 5, 6)		
	Serial communications interfaces (SCIh)	1 channel (SCI12)			
	I²C bus interface	1 channel			
	Serial peripheral interface	1 channel			
	Remote control signal receiver (REMC)	2 channels	Not supported		
Capacitive touch sensing unit		36 channels	36 channels	32 channels	24 channels
12-bit A/D converter		24 channels	17 channels	14 channels	10 channels
Temperature sensor		Available			
D/A converter		2 channels			Not supported
CRC calculator		Available			
Event link controller		Available			
Comparator B		2 channels			
Packages		100-pin LFQFP (0.5 mm)	80-pin LFQFP (0.5 mm)	64-pin LQFP (0.8 mm) 64-pin LFQFP (0.5 mm)	48-pin LFQFP (0.5 mm) 48-pin HWQFN (0.5 mm)

1.2 List of Products

Table 1.3 is a lists of products, and Figure 1.1 shows how to read the product part no., memory capacity, and package type.

Table 1.3 List of Products (1/2)

Group	Part No.	Part No. (for Orders)	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature
RX130	R5F51308ADFP	R5F51308ADFP#30	PLQP0100KB-B	512 Kbytes	48 Kbytes	8 Kbytes	32 MHz	–40 to +85°C
	R5F51308ADFN	R5F51308ADFN#30	PLQP0080KB-B					
	R5F51308ADFM	R5F51308ADFM#30	PLQP0064KB-C					
	R5F51308ADFK	R5F51308ADFK#30	PLQP0064GA-A					
	R5F51308ADFL	R5F51308ADFL#30	PLQP0048KB-B					
	R5F51308ADNE	R5F51308ADNE#U0	PWQN0048KB-A					
	R5F51307ADFP	R5F51307ADFP#30	PLQP0100KB-B	384 Kbytes				
	R5F51307ADFN	R5F51307ADFN#30	PLQP0080KB-B					
	R5F51307ADFM	R5F51307ADFM#30	PLQP0064KB-C					
	R5F51307ADFK	R5F51307ADFK#30	PLQP0064GA-A					
	R5F51307ADFL	R5F51307ADFL#30	PLQP0048KB-B					
	R5F51307ADNE	R5F51307ADNE#U0	PWQN0048KB-A					
	R5F51306ADFP	R5F51306ADFP#30	PLQP0100KB-B	256 Kbytes	32 Kbytes			
	R5F51306ADFN	R5F51306ADFN#30	PLQP0080KB-B					
	R5F51306ADFM	R5F51306ADFM#30	PLQP0064KB-C					
	R5F51306ADFK	R5F51306ADFK#30	PLQP0064GA-A					
	R5F51306ADFL	R5F51306ADFL#30	PLQP0048KB-B					
	R5F51306ADNE	R5F51306ADNE#U0	PWQN0048KB-A					
	R5F51305ADFP	R5F51305ADFP#30	PLQP0100KB-B	128 Kbytes	16 Kbytes			
	R5F51305ADFN	R5F51305ADFN#30	PLQP0080KB-B					
	R5F51305ADFM	R5F51305ADFM#30	PLQP0064KB-C					
	R5F51305ADFK	R5F51305ADFK#30	PLQP0064GA-A					
	R5F51305ADFL	R5F51305ADFL#30	PLQP0048KB-B					
	R5F51305ADNE	R5F51305ADNE#U0	PWQN0048KB-A					
	R5F51303ADFN	R5F51303ADFN#30	PLQP0080KB-B	64 Kbytes	10 Kbytes			
	R5F51303ADFM	R5F51303ADFM#30	PLQP0064KB-C					
	R5F51303ADFK	R5F51303ADFK#30	PLQP0064GA-A					
	R5F51303ADFL	R5F51303ADFL#30	PLQP0048KB-B					
	R5F51303ADNE	R5F51303ADNE#U0	PWQN0048KB-A					

Table 1.3 List of Products (2/2)

Group	Part No.	Part No. (for Orders)	Package	ROM Capacity	RAM Capacity	E2 DataFlash	Operating Frequency (Max.)	Operating Temperature
RX130	R5F51308AGFP	R5F51308AGFP#30	PLQP0100KB-B	512 Kbytes	48 Kbytes	8 Kbytes	32 MHz	–40 to +105°C
	R5F51308AGFN	R5F51308AGFN#30	PLQP0080KB-B					
	R5F51308AGFM	R5F51308AGFM#30	PLQP0064KB-C					
	R5F51308AGFK	R5F51308AGFK#30	PLQP0064GA-A					
	R5F51308AGFL	R5F51308AGFL#30	PLQP0048KB-B					
	R5F51308AGNE	R5F51308AGNE#U0	PWQN0048KB-A					
	R5F51307AGFP	R5F51307AGFP#30	PLQP0100KB-B	384 Kbytes				
	R5F51307AGFN	R5F51307AGFN#30	PLQP0080KB-B					
	R5F51307AGFM	R5F51307AGFM#30	PLQP0064KB-C					
	R5F51307AGFK	R5F51307AGFK#30	PLQP0064GA-A					
	R5F51307AGFL	R5F51307AGFL#30	PLQP0048KB-B					
	R5F51307AGNE	R5F51307AGNE#U0	PWQN0048KB-A					
	R5F51306AGFP	R5F51306AGFP#30	PLQP0100KB-B	256 Kbytes	32 Kbytes			
	R5F51306AGFN	R5F51306AGFN#30	PLQP0080KB-B					
	R5F51306AGFM	R5F51306AGFM#30	PLQP0064KB-C					
	R5F51306AGFK	R5F51306AGFK#30	PLQP0064GA-A					
	R5F51306AGFL	R5F51306AGFL#30	PLQP0048KB-B					
	R5F51306AGNE	R5F51306AGNE#U0	PWQN0048KB-A					
	R5F51305AGFP	R5F51305AGFP#30	PLQP0100KB-B	128 Kbytes	16 Kbytes			
	R5F51305AGFN	R5F51305AGFN#30	PLQP0080KB-B					
	R5F51305AGFM	R5F51305AGFM#30	PLQP0064KB-C					
	R5F51305AGFK	R5F51305AGFK#30	PLQP0064GA-A					
	R5F51305AGFL	R5F51305AGFL#30	PLQP0048KB-B					
	R5F51305AGNE	R5F51305AGNE#U0	PWQN0048KB-A					
	R5F51303AGFN	R5F51303AGFN#30	PLQP0080KB-B	64 Kbytes	10 Kbytes			
	R5F51303AGFM	R5F51303AGFM#30	PLQP0064KB-C					
	R5F51303AGFK	R5F51303AGFK#30	PLQP0064GA-A					
	R5F51303AGFL	R5F51303AGFL#30	PLQP0048KB-B					
	R5F51303AGNE	R5F51303AGNE#U0	PWQN0048KB-A					

Note: The part numbers for orders above are used for products in mass production or under development when this manual is issued. Refer to the Renesas Electronics Corporation website for the latest part numbers.

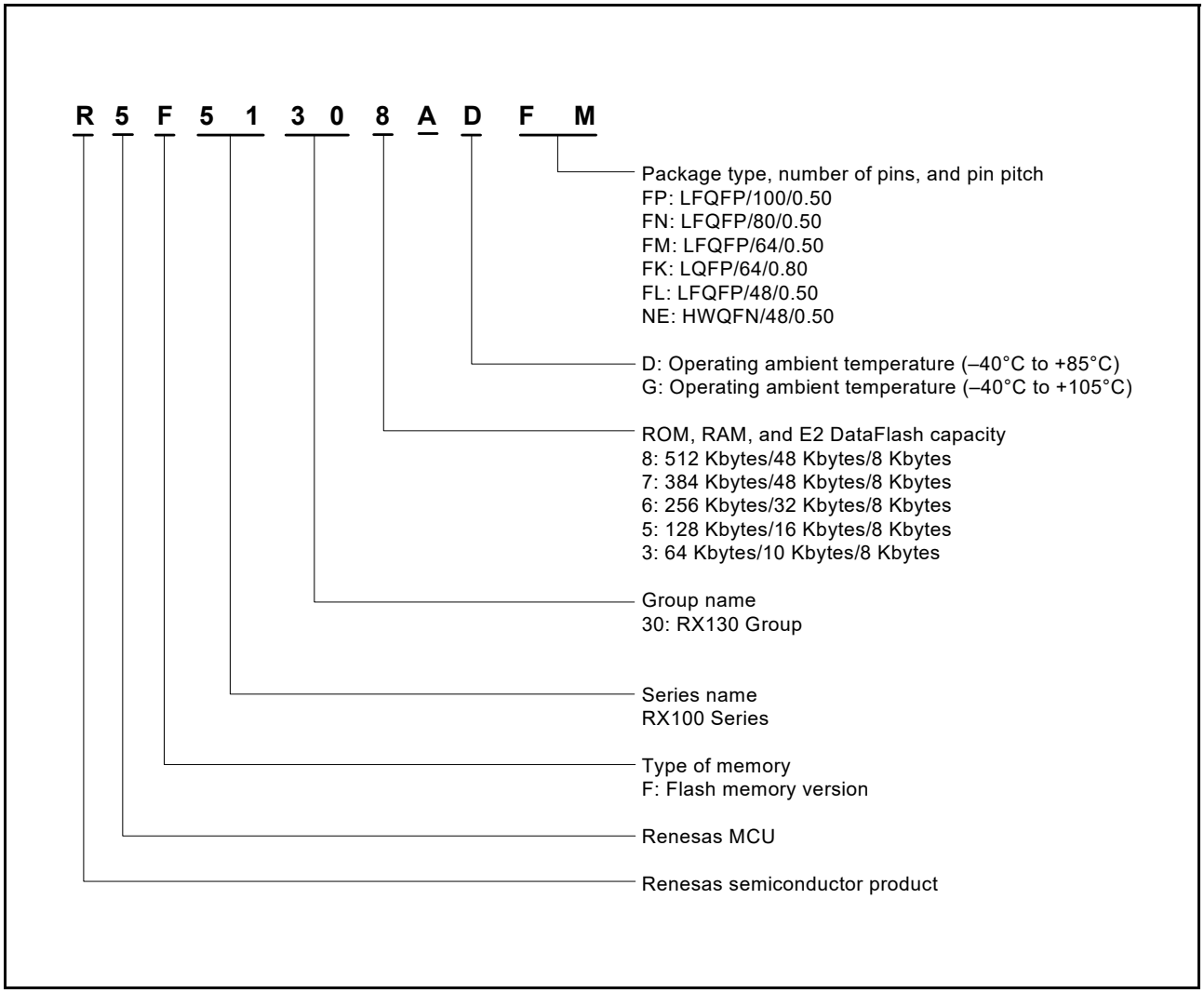


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.

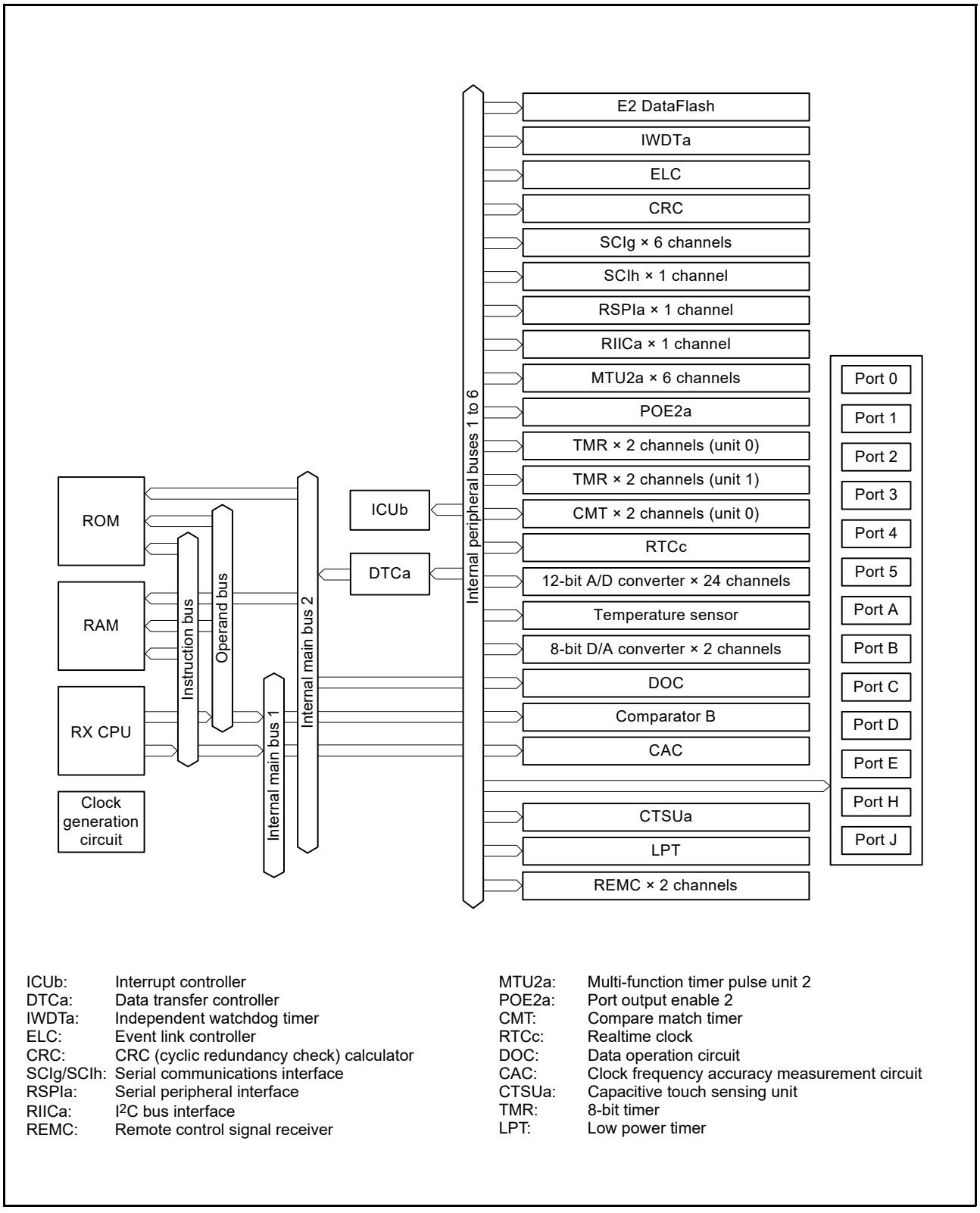


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/3)

Classifications	Pin Name	I/O	Description
Power supply	VCC	Input	Power supply pin. Connect it to the system power supply.
	VCL	—	Connect this pin to the VSS pin via the 4.7 μF smoothing capacitor used to stabilize the internal power supply. Place the capacitor close to the pin.
	VSS	Input	Ground pin. Connect it to the system power supply (0 V).
Clock	XTAL	Output	Pins for connecting a crystal. An external clock can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal between XCIN and XCOUT.
	XCOUT	Output	
	CLKOUT	Output	Clock output pin.
Operating mode control	MD	Input	Pin for setting the operating mode. The signal levels on this pin must not be changed during operation.
System control	RES#	Input	Reset pin. This MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Input pin for the clock frequency accuracy measurement circuit.
On-chip emulator	FINED	I/O	FINE interface pin.
Interrupts	NMI	Input	Non-maskable interrupt request pin.
	IRQ0 to IRQ7	Input	Interrupt request pins.
Multi-function timer pulse unit 2	MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D	I/O	The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins.
	MTIOC1A, MTIOC1B	I/O	The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins.
	MTIOC2A, MTIOC2B	I/O	The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins.
	MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D	I/O	The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins.
	MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D	I/O	The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins.
	MTIC5U, MTIC5V, MTIC5W	Input	The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins.
	MTCLKA, MTCLKB, MTCLKC, MTCLKD	Input	Input pins for the external clock.
Port output enable 2	POE0# to POE3#, POE8#	Input	Input pins for request signals to place the MTU pins in the high impedance state.
Realtime clock	RTCOUT	Output	Output pin for the 1-Hz/64-Hz clock.
8-bit timer	TMO0 to TMO3	Output	Compare match output pins.
	TMCI0 to TMCI3	Input	Input pins for the external clock to be input to the counter.
	TMRI0 to TMRI3	Input	Counter reset input pins.

Table 1.4 Pin Functions (2/3)

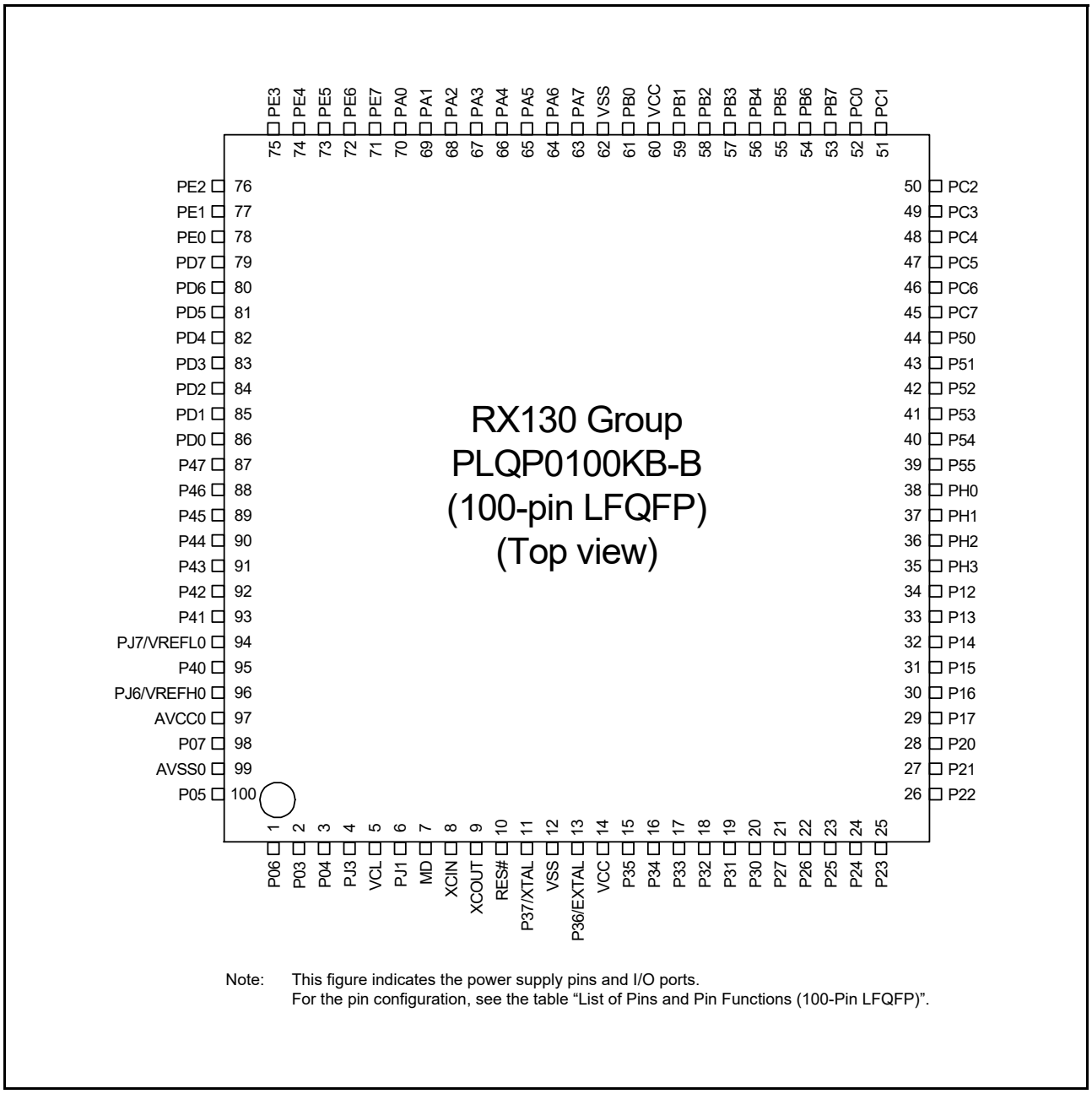
Classifications	Pin Name	I/O	Description
Serial communications interface (SCIg)	• Asynchronous mode/clock synchronous mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	RXD0, RXD1, RXD5, RXD6, RXD8, RXD9	Input	Input pins for received data.
	TXD0, TXD1, TXD5, TXD6, TXD8, TXD9	Output	Output pins for transmitted data.
	CTS0#, CTS1#, CTS5#, CTS6#, CTS8#, CTS9#	Input	Input pins for controlling the start of transmission and reception.
	RTS0#, RTS1#, RTS5#, RTS6#, RTS8#, RTS9#	Output	Output pins for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL0, SSCL1, SSCL5, SSCL6, SSCL8, SSCL9	I/O	Input/output pins for the I^2C clock.
	SSDA0, SSDA1, SSDA5, SSDA6, SSDA8, SSDA9	I/O	Input/output pins for the I^2C data.
	• Simple SPI mode		
	SCK0, SCK1, SCK5, SCK6, SCK8, SCK9	I/O	Input/output pins for the clock.
	SMISO0, SMISO1, SMISO5, SMISO6, SMISO8, SMISO9	I/O	Input/output pins for slave transmit data.
	SMOSI0, SMOSI1, SMOSI5, SMOSI6, SMOSI8, SMOSI9	I/O	Input/output pins for master transmit data.
	SS0#, SS1#, SS5#, SS6#, SS8#, SS9#	Input	Slave-select input pins.
Serial communications interface (SCIh)	• Asynchronous mode/clock synchronous mode		
	SCK12	I/O	Input/output pin for the clock.
	RXD12	Input	Input pin for receiving data.
	TXD12	Output	Output pin for transmitting data.
	CTS12#	Input	Input pin for controlling the start of transmission and reception.
	RTS12#	Output	Output pin for controlling the start of transmission and reception.
	• Simple I^2C mode		
	SSCL12	I/O	Input/output pin for the I^2C clock.
	SSDA12	I/O	Input/output pin for the I^2C data.
	• Simple SPI mode		
	SCK12	I/O	Input/output pin for the clock.
	SMISO12	I/O	Input/output pin for slave transmit data.
	SMOSI12	I/O	Input/output pin for master transmit data.
	SS12#	Input	Slave-select input pin.
	• Extended serial mode		
	RXDX12	Input	Input pin for data reception by SCIf.
	TXDX12	Output	Output pin for data transmission by SCIf.
	SIOX12	I/O	Input/output pin for data reception or transmission by SCIf.
I^2C bus interface	SCL	I/O	Input/output pin for I^2C bus interface clocks. Bus can be directly driven by the N-channel open drain output.
	SDA	I/O	Input/output pin for I^2C bus interface data. Bus can be directly driven by the N-channel open drain output.

Table 1.4 Pin Functions (3/3)

Classifications	Pin Name	I/O	Description
Serial peripheral interface	RSPCKA	I/O	Input/output pin for the RSPI clock.
	MOSIA	I/O	Input/output pin for transmitting data from the RSPI master.
	MISOA	I/O	Input/output pin for transmitting data from the RSPI slave.
	SSLA0	I/O	Input/output pin to select the slave for the RSPI.
	SSLA1 to SSLA3	Output	Output pins to select the slave for the RSPI.
Remote control signal receiver (REMC)	PMC0	Input	Input pin for external pulse signal
	PMC1	Input	Input pin for external pulse signal
12-bit A/D converter	AN000 to AN007, AN016 to AN031	Input	Input pins for the analog signals to be processed by the A/D converter.
	ADTRG0#	Input	Input pin for the external trigger signal that start the A/D conversion.
D/A converter	DA0, DA1	Output	Analog output pins of the D/A converter.
Comparator B	CMPB0, CMPB1	Input	Input pin for the analog signal to be processed by comparator B.
	CVREFB0, CVREFB1	Input	Analog reference voltage supply pin for comparator B.
	CMPOB0, CMPOB1	Output	Output pin for comparator B.
CTSU	TS0 to TS35	I/O	Electrostatic capacitance measurement pins (touch pins).
	TSCAP	—	Connect to the VSS via a decoupling capacitor (10 nF) for stabilizing the internal voltage
Analog power supply	AVCC0	Input	Analog voltage supply pin for the 12-bit A/D converter and D/A converter. Connect this pin to VCC when not using the 12-bit A/D converter and D/A converter.
	AVSS0	Input	Analog ground pin for the 12-bit A/D converter and D/A converter. Connect this pin to VSS when not using the 12-bit A/D converter and D/A converter.
	VREFH0	Input	Analog reference voltage supply pin for the 12-bit A/D converter.
	VREFL0	Input	Analog reference ground pin for the 12-bit A/D converter.
I/O ports	P03 to P07	I/O	5-bit input/output pins.
	P12 to P17	I/O	6-bit input/output pins.
	P20 to P27	I/O	8-bit input/output pins.
	P30 to P37	I/O	8-bit input/output pins (P35 input pin).
	P40 to P47	I/O	8-bit input/output pins.
	P50 to P55	I/O	6-bit input/output pins.
	PA0 to PA7	I/O	8-bit input/output pins.
	PB0 to PB7	I/O	8-bit input/output pins.
	PC0 to PC7	I/O	8-bit input/output pins.
	PD0 to PD7	I/O	8-bit input/output pins.
	PE0 to PE7	I/O	8-bit input/output pins.
	PH0 to PH3	I/O	4-bit input/output pins.
	PJ1, PJ3, PJ6, PJ7	I/O	4-bit input/output pins.

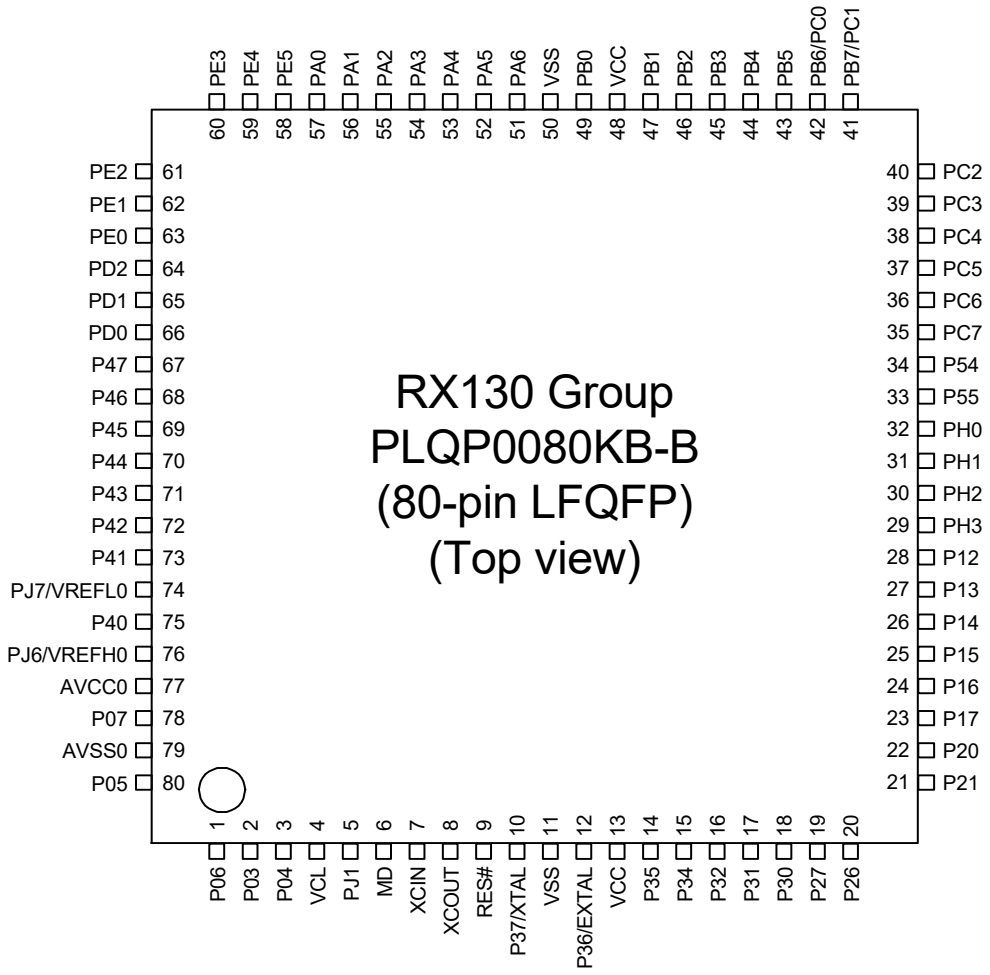
1.5 Pin Assignments

Figure 1.3 to Figure 1.7 show the pin assignments. Table 1.5 to Table 1.8 show the lists of pins and pin functions.



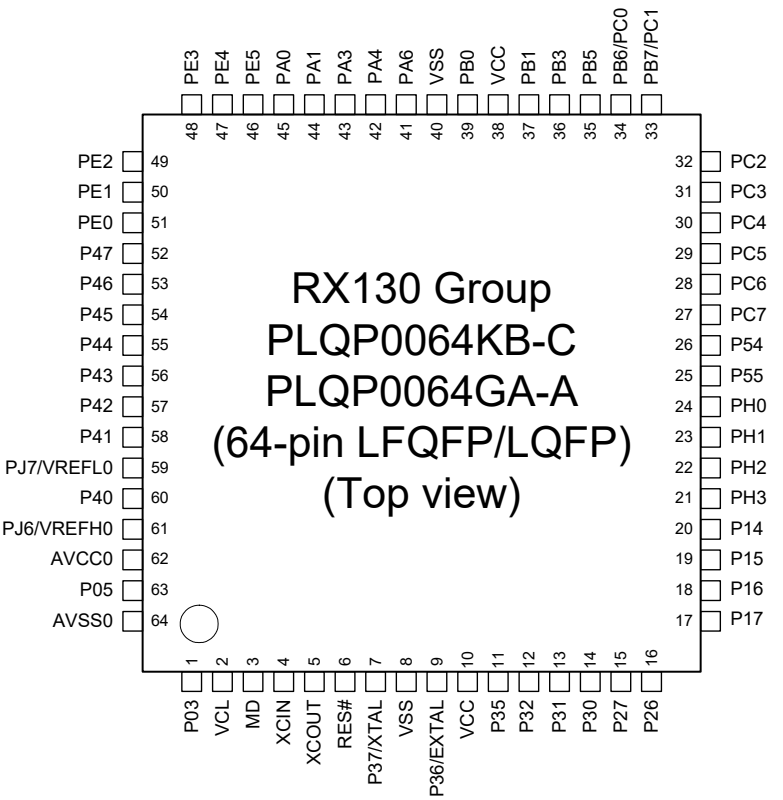
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (100-Pin LFQFP)”.

Figure 1.3 Pin Assignments of the 100-Pin LFQFP



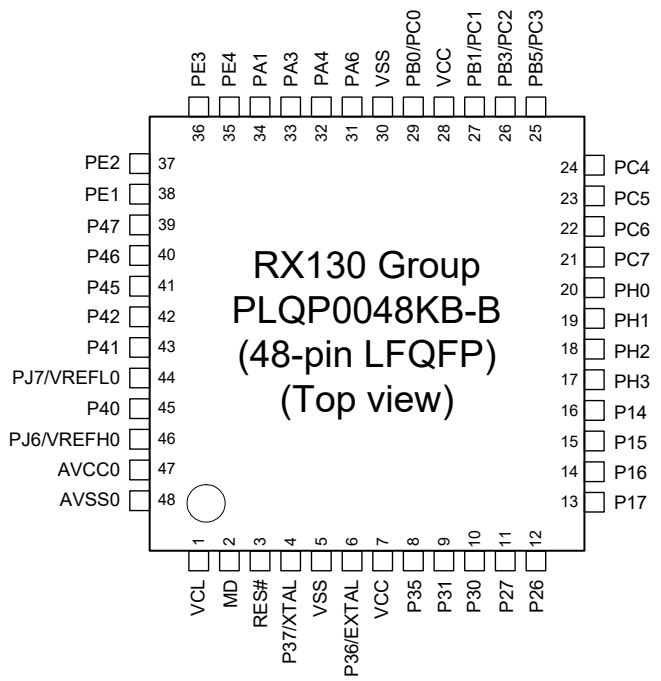
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (80-Pin LFQFP)”.

Figure 1.4 Pin Assignments of the 80-Pin LFQFP



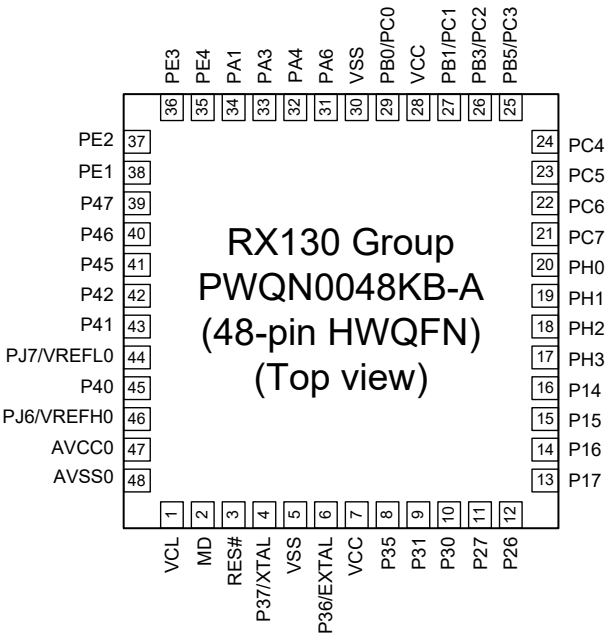
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (64-Pin LFQFP/LQFP)”.

Figure 1.5 Pin Assignments of the 64-Pin LFQFP/LQFP



Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP/ HWQFN)”.

Figure 1.6 Pin Assignments of the 48-Pin LQFP



Note: It is recommended to connect an exposed die pad to VSS.
Note: This figure indicates the power supply pins and I/O ports.
For the pin configuration, see the table “List of Pins and Pin Functions (48-Pin LFQFP/ HWQFN)”.

Figure 1.7 Pin Assignments of the 48-Pin HWQFN

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC, REMC)	Touch sensing	Others
1		P06*1				
2		P03*1				DA0
3		P04*1				
4		PJ3	MTIOC3C	CTS6#/RTS6#/SS6#		
5	VCL					
6		PJ1	MTIOC3A			
7	MD					FINED
8	XCIN					
9	XCOUT					
10	RES#					
11	XTAL	P37				
12	VSS					
13	EXTAL	P36				
14	VCC					
15		P35				NMI
16		P34	MTIOC0A/TMCI3/POE2#	SCK6		IRQ4
17		P33	MTIOC0D/TMRI3/POE3#	RXD6/SMISO6/SSCL6		IRQ3
18		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	TS0	IRQ2/RTCOUT
19		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	TS1	IRQ1
20		P30	MTIOC4B/POE8#/TMRI3	RXD1/SMISO1/SSCL1	TS2	IRQ0
21		P27	MTIOC2B/TMCI3	SCK1	TS3	
22		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	TS4	
23		P25	MTIOC4C/MTCLKB			ADTRG0#
24		P24	MTIOC4A/MTCLKA/TMRI1			
25		P23	MTIOC3D/MTCLKD	CTS0#/RTS0#/SS0#		
26		P22	MTIOC3B/MTCLKC/TMO0	SCK0		
27		P21	MTIOC1B/TMCI0	RXD0/SMISO0/SSCL0		
28		P20	MTIOC1A/TMRI0	TXD0/SMOSI0/SSDA0		
29	(5V tolerant)	P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA		IRQ7
30	(5V tolerant)	P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/SCL		IRQ6/RTCOUT/ ADTRG0#
31		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	TS5	IRQ5
32		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	TS6	IRQ4
33	(5V tolerant)	P13	MTIOC0B/TMO3	SDA		IRQ3
34	(5V tolerant)	P12	TMCI1	SCL		IRQ2
35		PH3	TMCI0		TS7	
36		PH2	TMRI0		TS8	IRQ1
37		PH1	TMO0		TS9	IRQ0
38		PH0			TS10	CACREF
39		P55	MTIOC4D/TMO3		TS11	
40		P54	MTIOC4B/TMCI1		TS12	
41		P53				
42		P52		PMC1		
43		P51		PMC0		
44		P50				
45		PC7	MTIOC3A/MTCLKB/TMO2	TXD8/SMOSI8/SSDA8/MISOA	TS13	CACREF
46		PC6	MTIOC3C/MTCLKA/TMCI2	RXD8/SMISO8/SSCL8/MOSIA	TS14	
47		PC5	MTIOC3B/MTCLKD/TMRI2	SCK8/RSPCKA	TS15	
48		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/CTS8#/RTS8#/SS8#/SSLA0	TSCAP	
49		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	TS16	
50		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	TS17	
51		PC1	MTIOC3A	SCK5/SSLA2		
52		PC0	MTIOC3C	CTS5#/RTS5#/SS5#/SSLA1		

Table 1.5 List of Pins and Pin Functions (100-Pin LFQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC, REMC)	Touch sensing	Others
53		PB7	MTIOC3B	TXD9/SMOSI9/SSDA9	TS18	
54		PB6	MTIOC3D	RXD9/SMISO9/SSCL9	TS19	
55		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#	SCK9	TS20	
56		PB4		CTS9#/RTS9#/SS9#	TS21	
57		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	TS22	
58		PB2		CTS6#/RTS6#/SS6#	TS23	
59		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	TS24	IRQ4/CMPOB1
60	VCC					
61		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	TS25	
62	VSS					
63		PA7		MISOA		
64		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	TS26	
65		PA5		RSPCKA	TS27	
66		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	TS28	IRQ5/CVREFB1
67		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	TS29	IRQ6/CMPB1
68		PA2		RXD5/SMISO5/SSCL5/SSLA3	TS30	
69		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	TS31	
70		PA0	MTIOC4A	SSLA1	TS32	CACREF
71		PE7				IRQ7/AN023
72		PE6				IRQ6/AN022
73		PE5	MTIOC4C/MTIOC2B			IRQ5/AN021/CMPOB0
74		PE4	MTIOC4D/MTIOC1A		TS33	AN020/CMPA2/ CLKOUT
75		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	TS34	AN019/CLKOUT
76		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12	TS35	IRQ7/AN018/CVREFB0
77		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12		AN017/CMPB0
78		PE0		SCK12		AN016
79		PD7	MTIC5U/POE0#			IRQ7/AN031
80		PD6	MTIC5V/POE1#			IRQ6/AN030
81		PD5	MTIC5W/POE2#			IRQ5/AN029
82		PD4	POE3#			IRQ4/AN028
83		PD3	POE8#			IRQ3/AN027
84		PD2	MTIOC4D	SCK6		IRQ2/AN026
85		PD1	MTIOC4B	RXD6/SMISO6/SSCL6		IRQ1/AN025
86		PD0		TXD6/SMOSI6/SSDA6		IRQ0/AN024
87		P47*1				AN007
88		P46*1				AN006
89		P45*1				AN005
90		P44*1				AN004
91		P43*1				AN003
92		P42*1				AN002
93		P41*1				AN001
94	VREFL0	PJ7*1				
95		P40*1				AN000
96	VREFH0	PJ6*1				
97	AVCC0					
98		P07*1				ADTRG0#
99	AVSS0					
100		P05*1				DA1

Note 1. The power source of the I/O buffer for these pins is AVCC0.

Table 1.6 List of Pins and Pin Functions (80-Pin LFQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC)	Touch sensing	Others
1		P06*1				
2		P03*1				DA0
3		P04*1				
4	VCL					
5		PJ1	MTIOC3A			
6	MD					FINED
7	XCIN					
8	XCOUT					
9	RES#					
10	XTAL	P37				
11	VSS					
12	EXTAL	P36				
13	VCC					
14		P35				NMI
15		P34	MTIOC0A/TMCI3/POE2#	SCK6		IRQ4
16		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	TS0	IRQ2/RTCOUT
17		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	TS1	IRQ1
18		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	TS2	IRQ0
19		P27	MTIOC2B/TMCI3	SCK1	TS3	
20		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	TS4	
21		P21	MTIOC1B/TMCI0			
22		P20	MTIOC1A/TMRI0			
23	(5V tolerant)	P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA		IRQ7
24	(5V tolerant)	P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/SCL		IRQ6/RTCOUT/ ADTRG0#
25		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	TS5	IRQ5
26		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	TS6	IRQ4
27	(5V tolerant)	P13	MTIOC0B/TMO3	SDA		IRQ3
28	(5V tolerant)	P12	TMCI1	SCL		IRQ2
29		PH3	TMCI0		TS7	
30		PH2	TMRI0		TS8	IRQ1
31		PH1	TMO0		TS9	IRQ0
32		PH0			TS10	CACREF
33		P55	MTIOC4D/TMO3		TS11	
34		P54	MTIOC4B/TMCI1		TS12	
35		PC7	MTIOC3A/TMO2/MTCLKB	MISOA	TS13	CACREF
36		PC6	MTIOC3C/MTCLKA/TMCI2	MOSIA	TS14	
37		PC5	MTIOC3B/MTCLKD/TMRI2	RSPCKA	TS15	
38		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/SSLA0	TSCAP	
39		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	TS16	
40		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	TS17	
41		PB7/ PC1*2	MTIOC3B		TS18	
42		PB6/ PC0*2	MTIOC3D		TS19	
43		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#		TS20	
44		PB4			TS21	
45		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	TS22	
46		PB2		CTS6#/RTS6#/SS6#	TS23	
47		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	TS24	IRQ4/CMPOB1
48	VCC					
49		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	TS25	

Table 1.6 List of Pins and Pin Functions (80-Pin LFQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC)	Touch sensing	Others
50	VSS					
51		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	TS26	
52		PA5		RSPCKA	TS27	
53		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	TS28	IRQ5/CVREFB1
54		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	TS29	IRQ6/CMPB1
55		PA2		RXD5/SMISO5/SSCL5/SSLA3	TS30	
56		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	TS31	
57		PA0	MTIOC4A	SSLA1	TS32	CACREF
58		PE5	MTIOC4C/MTIOC2B			IRQ5/AN021/CMPOB0
59		PE4	MTIOC4D/MTIOC1A		TS33	AN020/CMPA2/ CLKOUT
60		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	TS34	AN019/CLKOUT
61		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12	TS35	IRQ7/AN018/CVREFB0
62		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12		AN017/CMPB0
63		PE0		SCK12		AN016
64		PD2	MTIOC4D	SCK6		IRQ2/AN026
65		PD1	MTIOC4B	RXD6/SMISO6/SSCL6		IRQ1/AN025
66		PD0		TXD6/SMOSI6/SSDA6		IRQ0/AN024
67		P47*1				AN007
68		P46*1				AN006
69		P45*1				AN005
70		P44*1				AN004
71		P43*1				AN003
72		P42*1				AN002
73		P41*1				AN001
74	VREFL0	PJ7*1				
75		P40*1				AN000
76	VREFH0	PJ6*1				
77	AVCC0					
78		P07*1				ADTRG0#
79	AVSS0					
80		P05*1				DA1

Note 1. The power source of the I/O buffer for these pins is AVCC0.
Note 2. PC0 and PC1 are valid only when the port switching function is selected.

Table 1.7 List of Pins and Pin Functions (64-Pin LFQFP/LQFP) (1/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC)	Touch sensing	Others
1		P03*1				DA0
2	VCL					
3	MD					FINED
4	XCIN					
5	XCOUT					
6	RES#					
7	XTAL	P37				
8	VSS					
9	EXTAL	P36				
10	VCC					
11		P35				NMI
12		P32	MTIOC0C/TMO3	TXD6/SMOSI6/SSDA6	TS0	IRQ2/RTCOUT
13		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	TS1	IRQ1
14		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	TS2	IRQ0
15		P27	MTIOC2B/TMCI3	SCK1	TS3	
16		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	TS4	
17	(5V tolerant)	P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA		IRQ7
18	(5V tolerant)	P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/SCL		IRQ6/RTCOUT/ ADTRG0#
19		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	TS5	IRQ5
20		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	TS6	IRQ4
21		PH3	TMCI0		TS7	
22		PH2	TMRI0		TS8	IRQ1
23		PH1	TMO0		TS9	IRQ0
24		PH0			TS10	CACREF
25		P55	MTIOC4D/TMO3		TS11	
26		P54	MTIOC4B/TMCI1		TS12	
27		PC7	MTIOC3A/TMO2/MTCLKB	MISOA	TS13	CACREF
28		PC6	MTIOC3C/MTCLKA/TMCI2	MOSIA	TS14	
29		PC5	MTIOC3B/MTCLKD/TMRI2	RSPCKA	TS15	
30		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/SSLA0	TSCAP	
31		PC3	MTIOC4D	TXD5/SMOSI5/SSDA5	TS16	
32		PC2	MTIOC4B	RXD5/SMISO5/SSCL5/SSLA3	TS17	
33		PB7/ PC1*2	MTIOC3B		TS18	
34		PB6/ PC0*2	MTIOC3D		TS19	
35		PB5	MTIOC2A/MTIOC1B/TMRI1/ POE1#		TS20	
36		PB3	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	TS22	
37		PB1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	TS24	IRQ4/CMPOB1
38	VCC					
39		PB0	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	TS25	
40	VSS					
41		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	TS26	
42		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	TS28	IRQ5/CVREFB1
43		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	TS29	IRQ6/CMPB1
44		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	TS31	
45		PA0	MTIOC4A	SSLA1	TS32	CACREF
46		PE5	MTIOC4C/MTIOC2B			IRQ5/AN021/CMPOB0
47		PE4	MTIOC4D/MTIOC1A		TS33	AN020/CMPA2/ CLKOUT
48		PE3	MTIOC4B/POE8#	CTS12#/RTS12#/SS12#	TS34	AN019/CLKOUT

Table 1.7 List of Pins and Pin Functions (64-Pin LFQFP/LQFP) (2/2)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC)	Touch sensing	Others
49		PE2	MTIOC4A	RXD12/RXDX12/SMISO12/SSCL12	TS35	IRQ7/AN018/CVREFB0
50		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SMOSI12/ SSDA12		AN017/CMPB0
51		PE0		SCK12		AN016
52		P47*1				AN007
53		P46*1				AN006
54		P45*1				AN005
55		P44*1				AN004
56		P43*1				AN003
57		P42*1				AN002
58		P41*1				AN001
59	VREFL0	PJ7*1				
60		P40*1				AN000
61	VREFH0	PJ6*1				
62	AVCC0					
63		P05*1				DA1
64	AVSS0					

Note 1. The power source of the I/O buffer for these pins is AVCC0.
Note 2. PC0 and PC1 are valid only when the port switching function is selected.

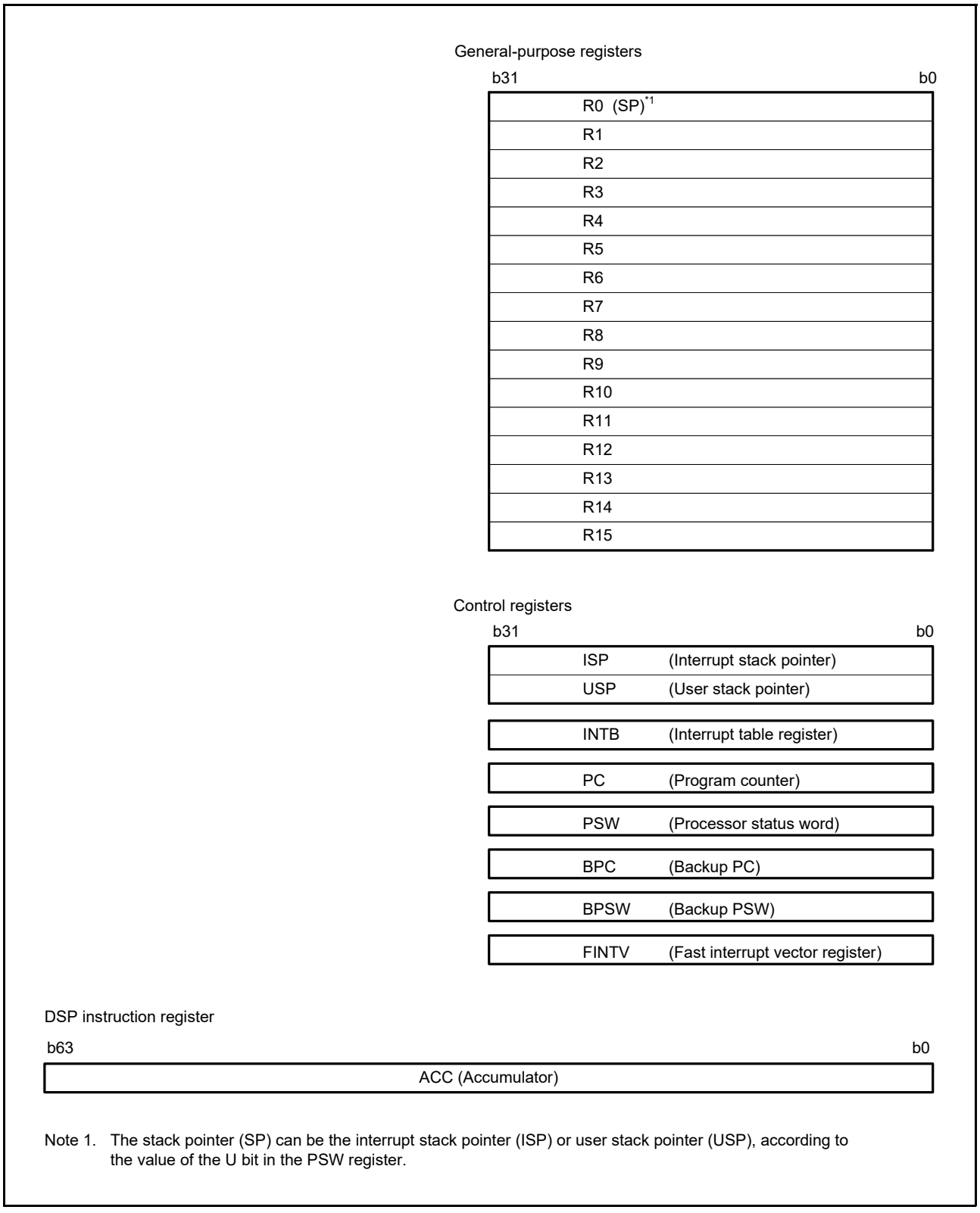
Table 1.8 List of Pins and Pin Functions (48-Pin LFQFP/HWQFN)

Pin No.	Power Supply, Clock, System Control	I/O Port	Timers (MTU, TMR, POE)	Communications (SCIg, SCIh, RSPI, RIIC)	Touch sensing	Others
1	VCL					
2	MD					FINED
3	RES#					
4	XTAL	P37				
5	VSS					
6	EXTAL	P36				
7	VCC					
8		P35				NMI
9		P31	MTIOC4D/TMCI2	CTS1#/RTS1#/SS1#	TS1	IRQ1
10		P30	MTIOC4B/TMRI3/POE8#	RXD1/SMISO1/SSCL1	TS2	IRQ0
11		P27	MTIOC2B/TMCI3	SCK1	TS3	
12		P26	MTIOC2A/TMO1	TXD1/SMOSI1/SSDA1	TS4	
13	(5V tolerant)	P17	MTIOC3A/MTIOC3B/TMO1/ POE8#	SCK1/MISOA/SDA		IRQ7
14	(5V tolerant)	P16	MTIOC3C/MTIOC3D/TMO2	TXD1/SMOSI1/SSDA1/MOSIA/SCL		IRQ6/ADTRG0#
15		P15	MTIOC0B/MTCLKB/TMCI2	RXD1/SMISO1/SSCL1	TS5	IRQ5
16		P14	MTIOC3A/MTCLKA/TMRI2	CTS1#/RTS1#/SS1#	TS6	IRQ4
17		PH3	TMCI0		TS7	
18		PH2	TMRI0		TS8	IRQ1
19		PH1	TMO0		TS9	IRQ0
20		PH0			TS10	CACREF
21		PC7	MTIOC3A/TMO2/MTCLKB	MISOA	TS13	CACREF
22		PC6	MTIOC3C/MTCLKA/TMCI2	MOSIA	TS14	
23		PC5	MTIOC3B/MTCLKD/TMRI2	RSPCKA	TS15	
24		PC4	MTIOC3D/MTCLKC/TMCI1/ POE0#	SCK5/SSLA0	TSCAP	
25		PB5/PC3*1	MTIOC2A/MTIOC1B/TMRI1/ POE1#		TS20	
26		PB3/PC2*1	MTIOC0A/MTIOC4A/TMO0/ POE3#	SCK6	TS22	
27		PB1/PC1*1	MTIOC0C/MTIOC4C/TMCI0	TXD6/SMOSI6/SSDA6	TS24	IRQ4/CMPOB1
28	VCC					
29		PB0/PC0*1	MTIC5W	RXD6/SMISO6/SSCL6/RSPCKA	TS25	
30	VSS					
31		PA6	MTIC5V/MTCLKB/TMCI3/ POE2#	CTS5#/RTS5#/SS5#/MOSIA	TS26	
32		PA4	MTIC5U/MTCLKA/TMRI0	TXD5/SMOSI5/SSDA5/SSLA0	TS28	IRQ5/CVREFB1
33		PA3	MTIOC0D/MTCLKD	RXD5/SMISO5/SSCL5	TS29	IRQ6/CMPB1
34		PA1	MTIOC0B/MTCLKC	SCK5/SSLA2	TS31	
35		PE4	MTIOC4D/MTIOC1A		TS33	AN020/CMPA2/ CLKOUT
36		PE3	MTIOC4B/POE8#	CTS12#/RTS12#	TS34	AN019/CLKOUT
37		PE2	MTIOC4A	RXD12/RXDX12/SSCL12	TS35	IRQ7/AN018/CVREFB0
38		PE1	MTIOC4C	TXD12/TXDX12/SIOX12/SSDA12		AN017/CMPB0
39		P47*2				AN007
40		P46*2				AN006
41		P45*2				AN005
42		P42*2				AN002
43		P41*2				AN001
44	VREFL0	PJ7*2				
45		P40*2				AN000
46	VREFH0	PJ6*2				
47	AVCC0					
48	AVSS0					

Note 1. PC0 to PC3 are valid only when the port switching function is selected.
Note 2. The power source of the I/O buffer for these pins is AVCC0.

2. CPU

Figure 2.1 shows the register set of the CPU.



Note 1. The stack pointer (SP) can be the interrupt stack pointer (ISP) or user stack pointer (USP), according to the value of the U bit in the PSW register.

Figure 2.1 Register Set of the CPU

2.1 General-Purpose Registers (R0 to R15)

This CPU has 16 general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers. R0, a general-purpose register, also functions as the stack pointer (SP). The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP)/User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).
Set the ISP or USP to a multiple of 4, as this reduces the numbers of cycles required to execute interrupt sequences and instructions entailing stack manipulation.

(2) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the relocatable vector table starts.

(3) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(4) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(5) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(6) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.
After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(7) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.
The FINTV register specifies a branch destination address when a fast interrupt has been generated.

2.3 Register Associated with DSP Instructions

(1) Accumulator (ACC)

The accumulator (ACC) is a 64-bit register used for DSP instructions. The accumulator is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, MUL, and RMPA, in which case the prior value in the accumulator is modified by execution of the instruction.
Use the MVTACHI and MVTACLO instructions for writing to the accumulator. The MVTACHI and MVTACLO instructions write data to the higher-order 32 bits (bits 63 to 32) and the lower-order 32 bits (bits 31 to 0), respectively.
Use the MVFACHI and MVFACMI instructions for reading data from the accumulator. The MVFACHI and MVFACMI instructions read data from the higher-order 32 bits (bits 63 to 32) and the middle 32 bits (bits 47 to 16), respectively.