



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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1.5V Drive Pch MOSFET

RZL035P01

●Structure

Silicon P-channel MOSFET

●Features

- 1) Low on-resistance.
- 2) High power package.
- 3) Low voltage drive. (1.5V)

●Application

Switching

●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
RZL035P01		○

●Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V_{DSS}	-12	V	
Gate-source voltage	V_{GSS}	± 10	V	
Drain current	Continuous	I_D	± 3.5	A
	Pulsed	I_{DP} *1	± 14	A
Source current (Body diode)	Continuous	I_S	-0.8	A
	Pulsed	I_{SP} *1	-14	A
Total power dissipation	P_D *2	1.0	W	
Channel temperature	T_{ch}	150	°C	
Range of Storage temperature	T_{stg}	-55 to +150	°C	

*1 $P_w \leq 10\mu s$, Duty cycle $\leq 1\%$

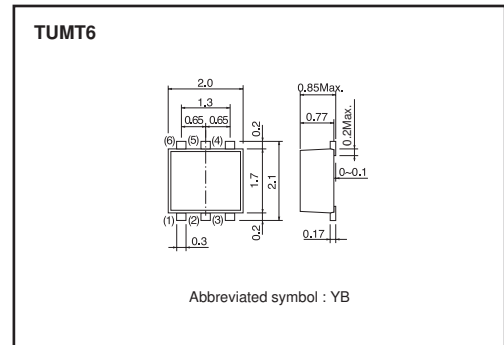
*2 Mounted on a ceramic board

●Thermal resistance

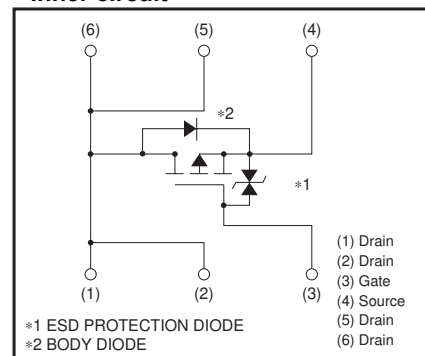
Parameter	Symbol	Limits	Unit
Channel to ambient	$R_{th}(ch-a)$ *	125	°C / W

* When mounted on a ceramic board.

●Dimensions (Unit : mm)



●Inner circuit



●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	± 10	μA	$V_{GS}=\pm 10V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	-12	-	-	V	$I_D=-1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	-	-	-1	μA	$V_{DS}=-12V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	-0.3	-	-1.0	V	$V_{DS}=-6V, I_D=-1mA$
Static drain-source on-state resistance	$R_{DS(on)}$ *	-	26	36	m Ω	$I_D=-3.5A, V_{GS}=-4.5V$
		-	36	50	m Ω	$I_D=-1.7A, V_{GS}=-2.5V$
		-	46	69	m Ω	$I_D=-1.7A, V_{GS}=-1.8V$
		-	66	132	m Ω	$I_D=-0.7A, V_{GS}=-1.5V$
Forward transfer admittance	$ Y_{fs} $ *	5.5	-	-	S	$V_{DS}=-6V, I_D=-3.5A$
Input capacitance	C_{iss}	-	1940	-	pF	$V_{DS}=-6V$
Output capacitance	C_{oss}	-	260	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	-	240	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}$ *	-	10	-	ns	$V_{DD}\doteq -6V$
Rise time	t_r *	-	50	-	ns	$I_D=-1.7A$
Turn-off delay time	$t_{d(off)}$ *	-	350	-	ns	$V_{GS}=-4.5V$
Fall time	t_f *	-	180	-	ns	$R_L\doteq 3.5\Omega$
Total gate charge	Q_g *	-	20	-	nC	$V_{DD}\doteq -6V, I_D=-3.5A$
Gate-source charge	Q_{gs} *	-	3.5	-	nC	$V_{GS}=-4.5V$
Gate-drain charge	Q_{gd} *	-	3.0	-	nC	$R_L\doteq 1.7\Omega, R_G=10\Omega$

*Pulsed

●Body diode characteristics (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	-	-	-1.2	V	$I_S=-3.5A, V_{GS}=0V$

* Pulsed

●Electrical characteristics curves

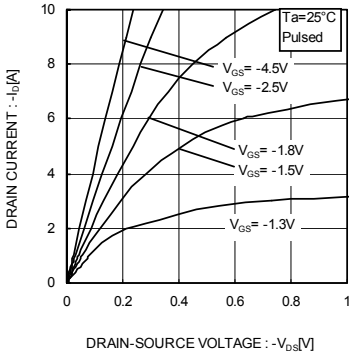


Fig.1 Typical output characteristics (I)

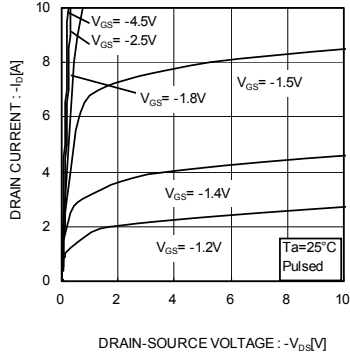


Fig.2 Typical output characteristics (II)

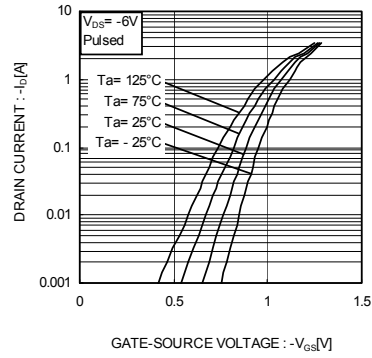


Fig.3 Typical Transfer Characteristics

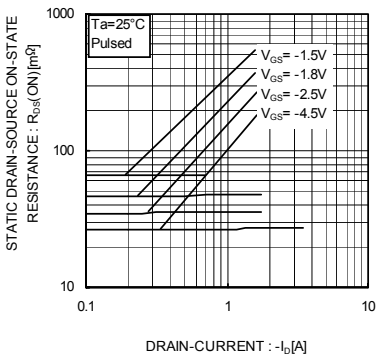


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

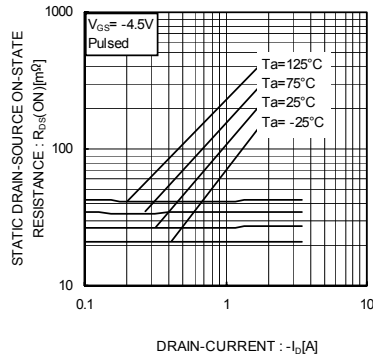


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

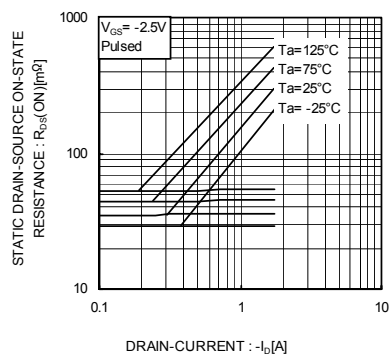


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(III)

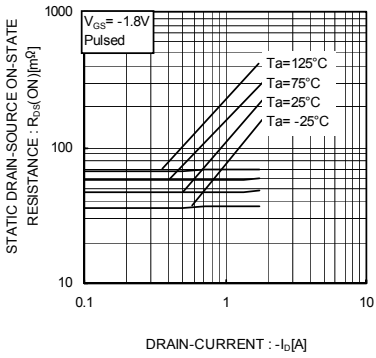


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

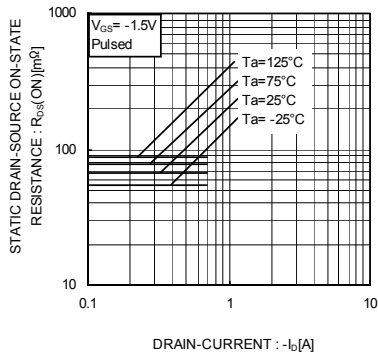


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(IV)

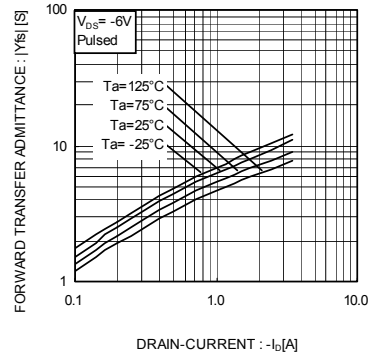


Fig.9 Forward Transfer Admittance vs. Drain Current

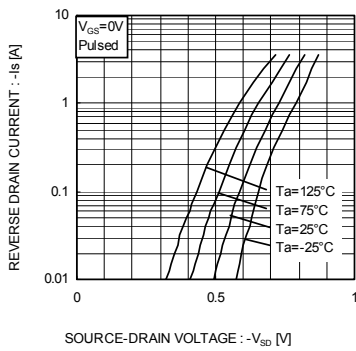


Fig.10 Reverse Drain Current vs. Source-Drain Voltage

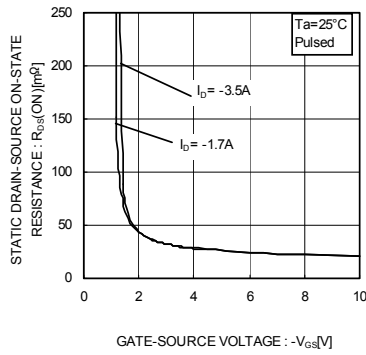


Fig.11 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

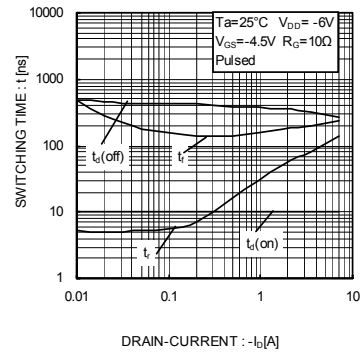


Fig.12 Switching Characteristics

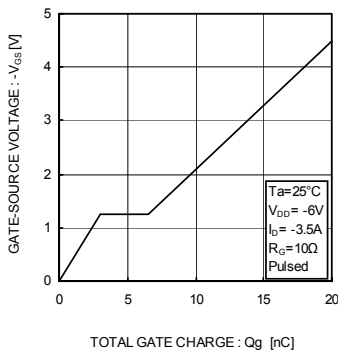


Fig.13 Dynamic Input Characteristics

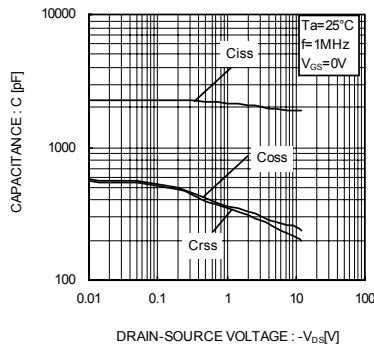


Fig.14 Typical Capacitance vs. Drain-Source Voltage

●Measurement circuits

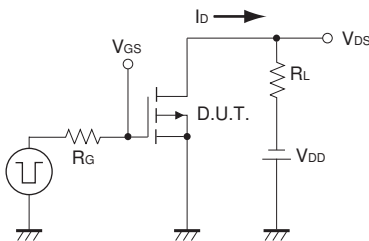


Fig.1-1 Switching Time Measurement Circuit

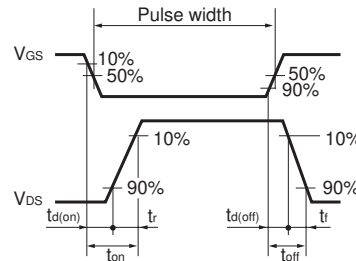


Fig.1-2 Switching Waveforms

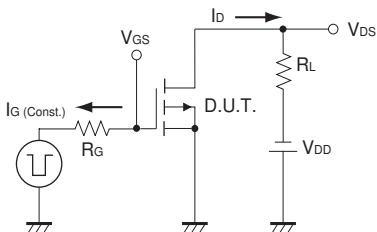


Fig.2-1 Gate Charge Measurement Circuit

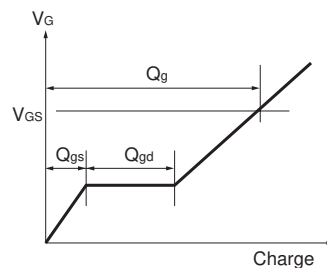


Fig.2-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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