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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# S-1002 Series

## VOLTAGE DETECTOR WITH SENSE PIN

www.sii-ic.com





The S-1002 Series is a high-accuracy voltage detector developed using CMOS technology. The detection voltage is fixed internally with an accuracy of ±1.0% ($-V_{DET(S)} \geq 2.2$ V). It operates with current consumption of 500 nA typ.
Apart from the power supply pin, the detection voltage input pin (SENSE pin) is also prepared, so the output is stable even if the SENSE pin falls to 0 V.
Two output forms Nch open-drain output and CMOS output are available.

## ■ Features

- Detection voltage: 1.0 V to 5.0 V (0.1 V step)
- Detection voltage accuracy: ±1.0% ($2.2\ V \leq -V_{DET(S)} \leq 5.0\ V$)
  ±22 mV ($1.0\ V \leq -V_{DET(S)} < 2.2\ V$)
- Current consumption: 500 nA typ.
- Operation voltage range: 0.95 V to 10.0 V
- Hysteresis width: 5% ± 2%
- Output form: Nch open-drain output (Active "L")
  CMOS output (Active "L")
- Operation temperature range: Ta = −40°C to +85°C
- Lead-free (Sn 100%), halogen-free

## ■ Applications

- Power supply monitor for microcomputer and reset for CPU
- Constant voltage power supply monitor for TV, Blu-ray recorder and home appliance
- Power supply monitor for portable devices such as notebook PC, digital still camera and mobile phone

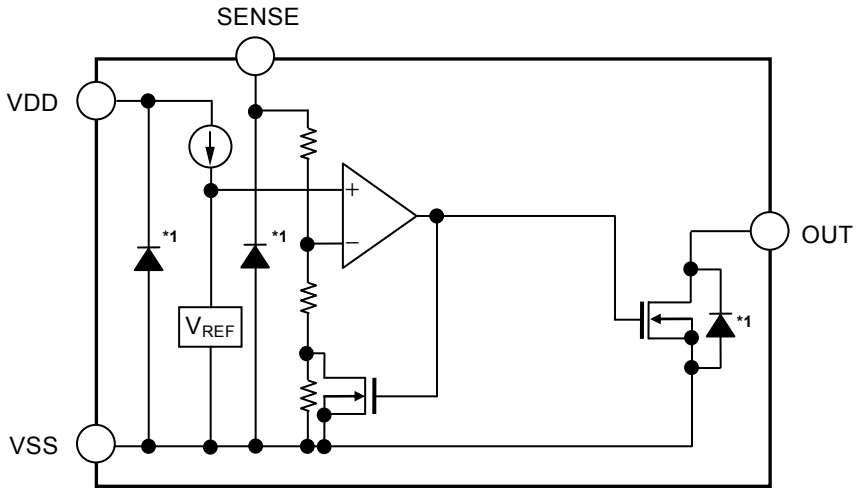
## ■ Packages

- SOT-23-5
- SC-82AB

## ■ Block Diagrams

### 1. S-1002 Series NA / NB type (Nch open-drain output)

| Function | Status |
|---|---|
| Output logic | Active "L" |

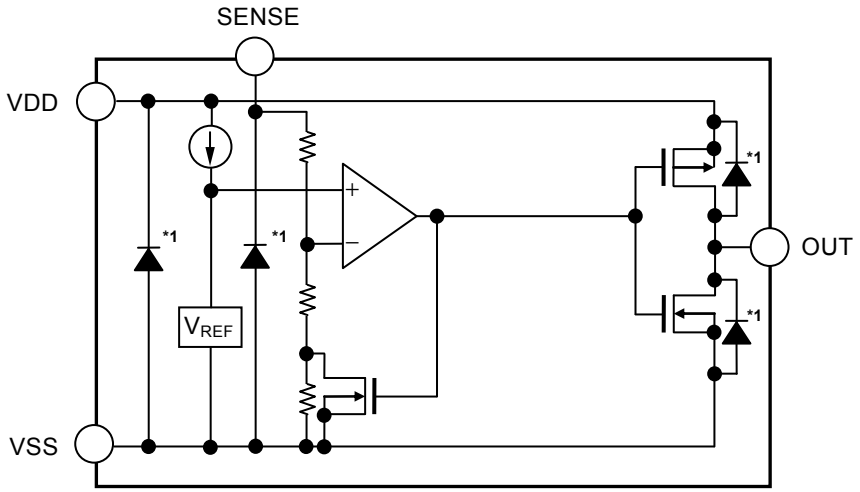



***1.** Parasitic diode

**Figure 1**

### 2. S-1002 Series CA / CB type (CMOS output)

| Function | Status |
|---|---|
| Output logic | Active "L" |




***1.** Parasitic diode

**Figure 2**

## ■ Product Name Structure

Users can select the output form, detection voltage value, and package type for the S-1002 Series.
Refer to "**1. Product name**" regarding the contents of product name, "**2. Function list of product types**" regarding the product types, "**3. Packages**" regarding the package drawings and "**4. Product name list**" regarding details of product name.

### 1. Product name

**S-1002 x x xx I - xxxx U**

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications*1
  - M5T1: SOT-23-5, Tape
  - N4T1: SC-82AB, Tape
- Operation temperature
  - I: Ta = −40°C to +85°C
- Detection voltage value
  - 10 to 50
  - (e.g., when the detection voltage is 1.0 V, it is expressed as 10.)
- Pin configuration*2
  - A, B
- Output form*3
  - N: Nch open-drain output (Active "L")*4
  - C: CMOS output (Active "L")*4

***1.** Refer to the tape drawing.
***2.** Refer to "■ **Pin Configurations**".
***3.** Refer to "**2. Function list of product types**".
***4.** If you request the product with output logic active "H", contact our sales office.

### 2. Function list of product types

**Table 1**

| Product Type | Output Form | Output Logic | Pin Configuration | Package |
|---|---|---|---|---|
| NA | Nch open-drain output | Active "L" | A | SOT-23-5 |
| NB | | Active "L" | B | SOT-23-5, SC-82AB |
| CA | CMOS output | Active "L" | A | SOT-23-5 |
| CB | | Active "L" | B | SOT-23-5, SC-82AB |

### 3. Packages

**Table 2 Package Drawing Codes**

| Package Name | Dimension | Tape | Reel |
|---|---|---|---|
| SOT-23-5 | MP005-A-P-SD | MP005-A-C-SD | MP005-A-R-SD |
| SC-82AB | NP004-A-P-SD | NP004-A-C-SD<br>NP004-A-C-S1 | NP004-A-R-SD |

## 4. Product name list

### 4. 1 S-1002 Series NA type

Output form: Nch open-drain output (Active "L")

**Table 3**

| Detection Voltage | SOT-23-5 |
|---|---|
| 1.0 V ± 22 mV | S-1002NA10I-M5T1U |
| 1.1 V ± 22 mV | S-1002NA11I-M5T1U |
| 1.2 V ± 22 mV | S-1002NA12I-M5T1U |
| 1.3 V ± 22 mV | S-1002NA13I-M5T1U |
| 1.4 V ± 22 mV | S-1002NA14I-M5T1U |
| 1.5 V ± 22 mV | S-1002NA15I-M5T1U |
| 1.6 V ± 22 mV | S-1002NA16I-M5T1U |
| 1.7 V ± 22 mV | S-1002NA17I-M5T1U |
| 1.8 V ± 22 mV | S-1002NA18I-M5T1U |
| 1.9 V ± 22 mV | S-1002NA19I-M5T1U |
| 2.0 V ± 22 mV | S-1002NA20I-M5T1U |
| 2.1 V ± 22 mV | S-1002NA21I-M5T1U |
| 2.2 V ± 1.0% | S-1002NA22I-M5T1U |
| 2.3 V ± 1.0% | S-1002NA23I-M5T1U |
| 2.4 V ± 1.0% | S-1002NA24I-M5T1U |
| 2.5 V ± 1.0% | S-1002NA25I-M5T1U |
| 2.6 V ± 1.0% | S-1002NA26I-M5T1U |
| 2.7 V ± 1.0% | S-1002NA27I-M5T1U |
| 2.8 V ± 1.0% | S-1002NA28I-M5T1U |
| 2.9 V ± 1.0% | S-1002NA29I-M5T1U |
| 3.0 V ± 1.0% | S-1002NA30I-M5T1U |
| 3.1 V ± 1.0% | S-1002NA31I-M5T1U |
| 3.2 V ± 1.0% | S-1002NA32I-M5T1U |
| 3.3 V ± 1.0% | S-1002NA33I-M5T1U |
| 3.4 V ± 1.0% | S-1002NA34I-M5T1U |
| 3.5 V ± 1.0% | S-1002NA35I-M5T1U |
| 3.6 V ± 1.0% | S-1002NA36I-M5T1U |
| 3.7 V ± 1.0% | S-1002NA37I-M5T1U |
| 3.8 V ± 1.0% | S-1002NA38I-M5T1U |
| 3.9 V ± 1.0% | S-1002NA39I-M5T1U |
| 4.0 V ± 1.0% | S-1002NA40I-M5T1U |
| 4.1 V ± 1.0% | S-1002NA41I-M5T1U |
| 4.2 V ± 1.0% | S-1002NA42I-M5T1U |
| 4.3 V ± 1.0% | S-1002NA43I-M5T1U |
| 4.4 V ± 1.0% | S-1002NA44I-M5T1U |
| 4.5 V ± 1.0% | S-1002NA45I-M5T1U |
| 4.6 V ± 1.0% | S-1002NA46I-M5T1U |
| 4.7 V ± 1.0% | S-1002NA47I-M5T1U |
| 4.8 V ± 1.0% | S-1002NA48I-M5T1U |
| 4.9 V ± 1.0% | S-1002NA49I-M5T1U |
| 5.0 V ± 1.0% | S-1002NA50I-M5T1U |

### 4. 2 S-1002 Series NB type

Output form: Nch open-drain output (Active "L")

**Table 4**

| Detection Voltage | SOT-23-5 | SC-82AB |
|---|---|---|
| 1.0 V ± 22 mV | S-1002NB10I-M5T1U | S-1002NB10I-N4T1U |
| 1.1 V ± 22 mV | S-1002NB11I-M5T1U | S-1002NB11I-N4T1U |
| 1.2 V ± 22 mV | S-1002NB12I-M5T1U | S-1002NB12I-N4T1U |
| 1.3 V ± 22 mV | S-1002NB13I-M5T1U | S-1002NB13I-N4T1U |
| 1.4 V ± 22 mV | S-1002NB14I-M5T1U | S-1002NB14I-N4T1U |
| 1.5 V ± 22 mV | S-1002NB15I-M5T1U | S-1002NB15I-N4T1U |
| 1.6 V ± 22 mV | S-1002NB16I-M5T1U | S-1002NB16I-N4T1U |
| 1.7 V ± 22 mV | S-1002NB17I-M5T1U | S-1002NB17I-N4T1U |
| 1.8 V ± 22 mV | S-1002NB18I-M5T1U | S-1002NB18I-N4T1U |
| 1.9 V ± 22 mV | S-1002NB19I-M5T1U | S-1002NB19I-N4T1U |
| 2.0 V ± 22 mV | S-1002NB20I-M5T1U | S-1002NB20I-N4T1U |
| 2.1 V ± 22 mV | S-1002NB21I-M5T1U | S-1002NB21I-N4T1U |
| 2.2 V ± 1.0% | S-1002NB22I-M5T1U | S-1002NB22I-N4T1U |
| 2.3 V ± 1.0% | S-1002NB23I-M5T1U | S-1002NB23I-N4T1U |
| 2.4 V ± 1.0% | S-1002NB24I-M5T1U | S-1002NB24I-N4T1U |
| 2.5 V ± 1.0% | S-1002NB25I-M5T1U | S-1002NB25I-N4T1U |
| 2.6 V ± 1.0% | S-1002NB26I-M5T1U | S-1002NB26I-N4T1U |
| 2.7 V ± 1.0% | S-1002NB27I-M5T1U | S-1002NB27I-N4T1U |
| 2.8 V ± 1.0% | S-1002NB28I-M5T1U | S-1002NB28I-N4T1U |
| 2.9 V ± 1.0% | S-1002NB29I-M5T1U | S-1002NB29I-N4T1U |
| 3.0 V ± 1.0% | S-1002NB30I-M5T1U | S-1002NB30I-N4T1U |
| 3.1 V ± 1.0% | S-1002NB31I-M5T1U | S-1002NB31I-N4T1U |
| 3.2 V ± 1.0% | S-1002NB32I-M5T1U | S-1002NB32I-N4T1U |
| 3.3 V ± 1.0% | S-1002NB33I-M5T1U | S-1002NB33I-N4T1U |
| 3.4 V ± 1.0% | S-1002NB34I-M5T1U | S-1002NB34I-N4T1U |
| 3.5 V ± 1.0% | S-1002NB35I-M5T1U | S-1002NB35I-N4T1U |
| 3.6 V ± 1.0% | S-1002NB36I-M5T1U | S-1002NB36I-N4T1U |
| 3.7 V ± 1.0% | S-1002NB37I-M5T1U | S-1002NB37I-N4T1U |
| 3.8 V ± 1.0% | S-1002NB38I-M5T1U | S-1002NB38I-N4T1U |
| 3.9 V ± 1.0% | S-1002NB39I-M5T1U | S-1002NB39I-N4T1U |
| 4.0 V ± 1.0% | S-1002NB40I-M5T1U | S-1002NB40I-N4T1U |
| 4.1 V ± 1.0% | S-1002NB41I-M5T1U | S-1002NB41I-N4T1U |
| 4.2 V ± 1.0% | S-1002NB42I-M5T1U | S-1002NB42I-N4T1U |
| 4.3 V ± 1.0% | S-1002NB43I-M5T1U | S-1002NB43I-N4T1U |
| 4.4 V ± 1.0% | S-1002NB44I-M5T1U | S-1002NB44I-N4T1U |
| 4.5 V ± 1.0% | S-1002NB45I-M5T1U | S-1002NB45I-N4T1U |
| 4.6 V ± 1.0% | S-1002NB46I-M5T1U | S-1002NB46I-N4T1U |
| 4.7 V ± 1.0% | S-1002NB47I-M5T1U | S-1002NB47I-N4T1U |
| 4.8 V ± 1.0% | S-1002NB48I-M5T1U | S-1002NB48I-N4T1U |
| 4.9 V ± 1.0% | S-1002NB49I-M5T1U | S-1002NB49I-N4T1U |
| 5.0 V ± 1.0% | S-1002NB50I-M5T1U | S-1002NB50I-N4T1U |

### 4. 3 S-1002 Series CA type

Output form: CMOS output (Active "L")

**Table 5**

| Detection Voltage | SOT-23-5 |
|---|---|
| 1.0 V ± 22 mV | S-1002CA10I-M5T1U |
| 1.1 V ± 22 mV | S-1002CA11I-M5T1U |
| 1.2 V ± 22 mV | S-1002CA12I-M5T1U |
| 1.3 V ± 22 mV | S-1002CA13I-M5T1U |
| 1.4 V ± 22 mV | S-1002CA14I-M5T1U |
| 1.5 V ± 22 mV | S-1002CA15I-M5T1U |
| 1.6 V ± 22 mV | S-1002CA16I-M5T1U |
| 1.7 V ± 22 mV | S-1002CA17I-M5T1U |
| 1.8 V ± 22 mV | S-1002CA18I-M5T1U |
| 1.9 V ± 22 mV | S-1002CA19I-M5T1U |
| 2.0 V ± 22 mV | S-1002CA20I-M5T1U |
| 2.1 V ± 22 mV | S-1002CA21I-M5T1U |
| 2.2 V ± 1.0% | S-1002CA22I-M5T1U |
| 2.3 V ± 1.0% | S-1002CA23I-M5T1U |
| 2.4 V ± 1.0% | S-1002CA24I-M5T1U |
| 2.5 V ± 1.0% | S-1002CA25I-M5T1U |
| 2.6 V ± 1.0% | S-1002CA26I-M5T1U |
| 2.7 V ± 1.0% | S-1002CA27I-M5T1U |
| 2.8 V ± 1.0% | S-1002CA28I-M5T1U |
| 2.9 V ± 1.0% | S-1002CA29I-M5T1U |
| 3.0 V ± 1.0% | S-1002CA30I-M5T1U |
| 3.1 V ± 1.0% | S-1002CA31I-M5T1U |
| 3.2 V ± 1.0% | S-1002CA32I-M5T1U |
| 3.3 V ± 1.0% | S-1002CA33I-M5T1U |
| 3.4 V ± 1.0% | S-1002CA34I-M5T1U |
| 3.5 V ± 1.0% | S-1002CA35I-M5T1U |
| 3.6 V ± 1.0% | S-1002CA36I-M5T1U |
| 3.7 V ± 1.0% | S-1002CA37I-M5T1U |
| 3.8 V ± 1.0% | S-1002CA38I-M5T1U |
| 3.9 V ± 1.0% | S-1002CA39I-M5T1U |
| 4.0 V ± 1.0% | S-1002CA40I-M5T1U |
| 4.1 V ± 1.0% | S-1002CA41I-M5T1U |
| 4.2 V ± 1.0% | S-1002CA42I-M5T1U |
| 4.3 V ± 1.0% | S-1002CA43I-M5T1U |
| 4.4 V ± 1.0% | S-1002CA44I-M5T1U |
| 4.5 V ± 1.0% | S-1002CA45I-M5T1U |
| 4.6 V ± 1.0% | S-1002CA46I-M5T1U |
| 4.7 V ± 1.0% | S-1002CA47I-M5T1U |
| 4.8 V ± 1.0% | S-1002CA48I-M5T1U |
| 4.9 V ± 1.0% | S-1002CA49I-M5T1U |
| 5.0 V ± 1.0% | S-1002CA50I-M5T1U |

### 4. 4 S-1002 Series CB type

Output form: CMOS output (Active "L")

**Table 6**

| Detection Voltage | SOT-23-5 | SC-82AB |
|---|---|---|
| 1.0 V ± 22 mV | S-1002CB10I-M5T1U | S-1002CB10I-N4T1U |
| 1.1 V ± 22 mV | S-1002CB11I-M5T1U | S-1002CB11I-N4T1U |
| 1.2 V ± 22 mV | S-1002CB12I-M5T1U | S-1002CB12I-N4T1U |
| 1.3 V ± 22 mV | S-1002CB13I-M5T1U | S-1002CB13I-N4T1U |
| 1.4 V ± 22 mV | S-1002CB14I-M5T1U | S-1002CB14I-N4T1U |
| 1.5 V ± 22 mV | S-1002CB15I-M5T1U | S-1002CB15I-N4T1U |
| 1.6 V ± 22 mV | S-1002CB16I-M5T1U | S-1002CB16I-N4T1U |
| 1.7 V ± 22 mV | S-1002CB17I-M5T1U | S-1002CB17I-N4T1U |
| 1.8 V ± 22 mV | S-1002CB18I-M5T1U | S-1002CB18I-N4T1U |
| 1.9 V ± 22 mV | S-1002CB19I-M5T1U | S-1002CB19I-N4T1U |
| 2.0 V ± 22 mV | S-1002CB20I-M5T1U | S-1002CB20I-N4T1U |
| 2.1 V ± 22 mV | S-1002CB21I-M5T1U | S-1002CB21I-N4T1U |
| 2.2 V ± 1.0% | S-1002CB22I-M5T1U | S-1002CB22I-N4T1U |
| 2.3 V ± 1.0% | S-1002CB23I-M5T1U | S-1002CB23I-N4T1U |
| 2.4 V ± 1.0% | S-1002CB24I-M5T1U | S-1002CB24I-N4T1U |
| 2.5 V ± 1.0% | S-1002CB25I-M5T1U | S-1002CB25I-N4T1U |
| 2.6 V ± 1.0% | S-1002CB26I-M5T1U | S-1002CB26I-N4T1U |
| 2.7 V ± 1.0% | S-1002CB27I-M5T1U | S-1002CB27I-N4T1U |
| 2.8 V ± 1.0% | S-1002CB28I-M5T1U | S-1002CB28I-N4T1U |
| 2.9 V ± 1.0% | S-1002CB29I-M5T1U | S-1002CB29I-N4T1U |
| 3.0 V ± 1.0% | S-1002CB30I-M5T1U | S-1002CB30I-N4T1U |
| 3.1 V ± 1.0% | S-1002CB31I-M5T1U | S-1002CB31I-N4T1U |
| 3.2 V ± 1.0% | S-1002CB32I-M5T1U | S-1002CB32I-N4T1U |
| 3.3 V ± 1.0% | S-1002CB33I-M5T1U | S-1002CB33I-N4T1U |
| 3.4 V ± 1.0% | S-1002CB34I-M5T1U | S-1002CB34I-N4T1U |
| 3.5 V ± 1.0% | S-1002CB35I-M5T1U | S-1002CB35I-N4T1U |
| 3.6 V ± 1.0% | S-1002CB36I-M5T1U | S-1002CB36I-N4T1U |
| 3.7 V ± 1.0% | S-1002CB37I-M5T1U | S-1002CB37I-N4T1U |
| 3.8 V ± 1.0% | S-1002CB38I-M5T1U | S-1002CB38I-N4T1U |
| 3.9 V ± 1.0% | S-1002CB39I-M5T1U | S-1002CB39I-N4T1U |
| 4.0 V ± 1.0% | S-1002CB40I-M5T1U | S-1002CB40I-N4T1U |
| 4.1 V ± 1.0% | S-1002CB41I-M5T1U | S-1002CB41I-N4T1U |
| 4.2 V ± 1.0% | S-1002CB42I-M5T1U | S-1002CB42I-N4T1U |
| 4.3 V ± 1.0% | S-1002CB43I-M5T1U | S-1002CB43I-N4T1U |
| 4.4 V ± 1.0% | S-1002CB44I-M5T1U | S-1002CB44I-N4T1U |
| 4.5 V ± 1.0% | S-1002CB45I-M5T1U | S-1002CB45I-N4T1U |
| 4.6 V ± 1.0% | S-1002CB46I-M5T1U | S-1002CB46I-N4T1U |
| 4.7 V ± 1.0% | S-1002CB47I-M5T1U | S-1002CB47I-N4T1U |
| 4.8 V ± 1.0% | S-1002CB48I-M5T1U | S-1002CB48I-N4T1U |
| 4.9 V ± 1.0% | S-1002CB49I-M5T1U | S-1002CB49I-N4T1U |
| 5.0 V ± 1.0% | S-1002CB50I-M5T1U | S-1002CB50I-N4T1U |

## ■ Pin Configurations

### 1. S-1002 Series NA / CA type

#### 1. 1 SOT-23-5

Top view

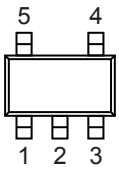



**Figure 3**

**Table 7 Pin Configuration A**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | OUT | Voltage detection output pin |
| 2 | VDD | Power supply pin |
| 3 | VSS | GND pin |
| 4 | NC*1 | No connection |
| 5 | SENSE | Detection voltage input pin |

***1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

### 2. S-1002 Series NB / CB type

#### 2. 1 SOT-23-5

Top view

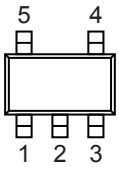



**Figure 4**

**Table 8 Pin Configuration B**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | OUT | Voltage detection output pin |
| 2 | VSS | GND pin |
| 3 | VDD | Power supply pin |
| 4 | SENSE | Detection voltage input pin |
| 5 | NC*1 | No connection |

***1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

#### 2. 2 SC-82AB

Top view

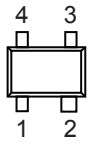



**Figure 5**

**Table 9 Pin Configuration B**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | SENSE | Detection voltage input pin |
| 2 | VDD | Power supply pin |
| 3 | OUT | Voltage detection output pin |
| 4 | VSS | GND pin |

## ■ Absolute Maximum Ratings

**Table 10**

(Ta = +25°C unless otherwise specified)

| Item | | | Symbol | Absolute Maximum Rating | Unit |
|---|---|---|---|---|---|
| Power supply voltage | | | $V_{DD} - V_{SS}$ | 12.0 | V |
| SENSE pin input voltage | | | $V_{SENSE}$ | $V_{SS}$ – 0.3 to 12.0 | V |
| Output voltage | Nch open-drain output product | | $V_{OUT}$ | $V_{SS}$ – 0.3 to 12.0 | V |
| | CMOS output product | | | $V_{SS}$ – 0.3 to $V_{DD}$ + 0.3 | V |
| Output current | | | $I_{OUT}$ | 50 | mA |
| Power dissipation | | SOT-23-5 | $P_D$ | 600[*1] | mW |
| | | SC-82AB | | 350[*1] | mW |
| Operation ambient temperature | | | $T_{opr}$ | –40 to +85 | °C |
| Storage temperature | | | $T_{stg}$ | –40 to +125 | °C |

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Name: JEDEC STANDARD51-7

**Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

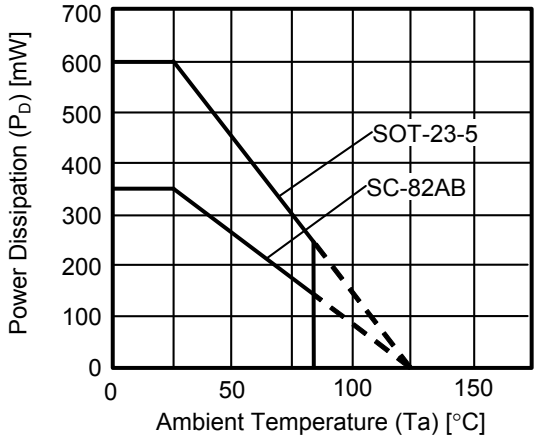



**Figure 6 Power Dissipation of Package (When Mounted on Board)**

## ■ Electrical Characteristics

### 1. Nch open-drain output product

**Table 11**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Detection voltage[*1] | $-V_{DET}$ | 0.95 V ≤ $V_{DD}$ ≤ 10.0 V | 1.0 V ≤ $-V_{DET(S)}$ < 2.2 V | $-V_{DET(S)}$ − 0.022 | $-V_{DET(S)}$ | $-V_{DET(S)}$ + 0.022 | V | 1 |
| | | | 2.2 V ≤ $-V_{DET(S)}$ ≤ 5.0 V | $-V_{DET(S)}$ × 0.99 | $-V_{DET(S)}$ | $-V_{DET(S)}$ × 1.01 | V | 1 |
| Hysteresis width | $V_{HYS}$ | – | | $-V_{DET}$ × 0.03 | $-V_{DET}$ × 0.05 | $-V_{DET}$ × 0.07 | V | 1 |
| Current consumption[*2] | $I_{SS}$ | $V_{DD}$ = 10.0 V, $V_{SENSE}$ = $-V_{DET(S)}$ + 1.0 V | | – | 0.50 | 0.90 | μA | 2 |
| Operation voltage | $V_{DD}$ | – | | 0.95 | – | 10.0 | V | 1 |
| Output current | $I_{OUT}$ | Output transistor Nch $V_{DS}$[*3] = 0.5 V $V_{SENSE}$ = 0.0 V | $V_{DD}$ = 0.95 V | 0.59 | 1.00 | – | mA | 3 |
| | | | $V_{DD}$ = 1.2 V | 0.73 | 1.33 | – | mA | 3 |
| | | | $V_{DD}$ = 2.4 V | 1.47 | 2.39 | – | mA | 3 |
| | | | $V_{DD}$ = 4.8 V | 1.86 | 2.50 | – | mA | 3 |
| Leakage current | $I_{LEAK}$ | Output transistor Nch $V_{DD}$ = 10.0 V, $V_{DS}$[*3] = 10.0 V, $V_{SENSE}$ = 10.0 V | | – | – | 0.08 | μA | 3 |
| Detection voltage temperature coefficient[*4] | $\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$ | Ta = −40°C to +85°C | | – | ±100 | ±350 | ppm/°C | 1 |
| Detection delay time[*5] | $t_{DET}$ | $V_{DD}$ = 5.0 V | | – | 40 | – | μs | 4 |
| Release delay time[*6] | $t_{RESET}$ | $V_{DD}$ = 5.0 V | $-V_{DET(S)}$ ≤ 2.4 V | – | 40 | – | μs | 4 |
| | | | 2.4 V < $-V_{DET(S)}$ | – | 80 | – | μs | 4 |
| SENSE pin resistance | $R_{SENSE}$ | 1.0 V ≤ $-V_{DET(S)}$ < 1.2 V | | 5.0 | 19.0 | 42.0 | MΩ | 2 |
| | | 1.2 V ≤ $-V_{DET(S)}$ ≤ 5.0 V | | 6.0 | 30.0 | 98.0 | MΩ | 2 |

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (the center value of the detection voltage range in **Table 3** or **Table 4**)

***2.** The current flowing through the SENSE pin resistance is not included.

***3.** $V_{DS}$: Drain-to-source voltage of the output transistor

***4.** The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta -V_{DET}}{\Delta Ta}\ [mV/°C]^{*1} = -V_{DET(S)}\ (typ.)[V]^{*2} \times \frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}\ [ppm/°C]^{*3} \div 1000$$

- ***1.** Temperature change of the detection voltage
- ***2.** Set detection voltage
- ***3.** Detection voltage temperature coefficient

***5.** The time period from when the pulse voltage of 6.0 V → $-V_{DET(S)}$ − 2.0 V or 0 V is applied to the SENSE pin to when $V_{OUT}$ reaches $V_{DD}$ / 2, after the output pin is pulled up to 5.0 V by the resistance of 470 kΩ.

***6.** The time period from when the pulse voltage of 0 V → $-V_{DET(S)}$ + 2.0 V or 6.0 V is applied to the SENSE pin to when $V_{OUT}$ reaches $V_{DD}$ / 2, after the output pin is pulled up to 5.0 V by the resistance of 470 kΩ.

## 2. CMOS output product

**Table 12**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Detection voltage[*1] | $-V_{DET}$ | 0.95 V ≤ $V_{DD}$ ≤ 10.0 V | 1.0 V ≤ $-V_{DET(S)}$ < 2.2 V | $-V_{DET(S)}$ − 0.022 | $-V_{DET(S)}$ | $-V_{DET(S)}$ + 0.022 | V | 1 |
| | | | 2.2 V ≤ $-V_{DET(S)}$ ≤ 5.0 V | $-V_{DET(S)}$ × 0.99 | $-V_{DET(S)}$ | $-V_{DET(S)}$ × 1.01 | V | 1 |
| Hysteresis width | $V_{HYS}$ | − | | $-V_{DET}$ × 0.03 | $-V_{DET}$ × 0.05 | $-V_{DET}$ × 0.07 | V | 1 |
| Current consumption[*2] | $I_{SS}$ | $V_{DD}$ = 10.0 V, $V_{SENSE}$ = $-V_{DET(S)}$ + 1.0 V | | − | 0.50 | 0.90 | μA | 2 |
| Operation voltage | $V_{DD}$ | − | | 0.95 | − | 10.0 | V | 1 |
| Output current | $I_{OUT}$ | Output transistor Nch<br>$V_{DS}$[*3] = 0.5 V<br>$V_{SENSE}$ = 0.0 V | $V_{DD}$ = 0.95 V | 0.59 | 1.00 | − | mA | 3 |
| | | | $V_{DD}$ = 1.2 V | 0.73 | 1.33 | − | mA | 3 |
| | | | $V_{DD}$ = 2.4 V | 1.47 | 2.39 | − | mA | 3 |
| | | | $V_{DD}$ = 4.8 V | 1.86 | 2.50 | − | mA | 3 |
| | | Output transistor Pch<br>$V_{DS}$[*3] = 0.5 V<br>$V_{SENSE}$ = 10.0 V | $V_{DD}$ = 4.8 V | 1.62 | 2.60 | − | mA | 5 |
| | | | $V_{DD}$ = 6.0 V | 1.78 | 2.86 | − | mA | 5 |
| Detection voltage temperature coefficient[*4] | $\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$ | Ta = −40°C to +85°C | | − | ±100 | ±350 | ppm/°C | 1 |
| Detection delay time[*5] | $t_{DET}$ | $V_{DD}$ = 5.0 V | | − | 40 | − | μs | 4 |
| Release delay time[*6] | $t_{RESET}$ | $V_{DD}$ = 5.0 V | $-V_{DET(S)}$ ≤ 2.4 V | − | 40 | − | μs | 4 |
| | | | 2.4 V < $-V_{DET(S)}$ | − | 80 | − | μs | 4 |
| SENSE pin resistance | $R_{SENSE}$ | 1.0 V ≤ $-V_{DET(S)}$ < 1.2 V | | 5.0 | 19.0 | 42.0 | MΩ | 2 |
| | | 1.2 V ≤ $-V_{DET(S)}$ ≤ 5.0 V | | 6.0 | 30.0 | 98.0 | MΩ | 2 |

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (the center value of the detection voltage range in **Table 5** or **Table 6**)

***2.** The current flowing through the SENSE pin resistance is not included.

***3.** $V_{DS}$: Drain-to-source voltage of the output transistor

***4.** The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta -V_{DET}}{\Delta Ta}\ [\text{mV/°C}]^{*1} = -V_{DET(S)}\ (\text{typ.})[\text{V}]^{*2} \times \frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}\ [\text{ppm/°C}]^{*3} \div 1000$$

***1.** Temperature change of the detection voltage
***2.** Set detection voltage
***3.** Detection voltage temperature coefficient

***5.** The time period from when the pulse voltage of 6.0 V → $-V_{DET(S)}$ − 2.0 V or 0 V is applied to the SENSE pin to when $V_{OUT}$ reaches $V_{DD}$ / 2.

***6.** The time period from when the pulse voltage of 0 V → $-V_{DET(S)}$ + 2.0 V or 6.0 V is applied to the SENSE pin to when $V_{OUT}$ reaches $V_{DD}$ / 2.

## ■ Test Circuits

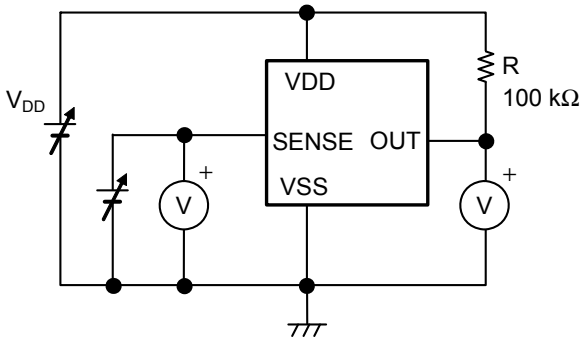



**Figure 7 Test Circuit 1**
**(Nch open-drain output product)**

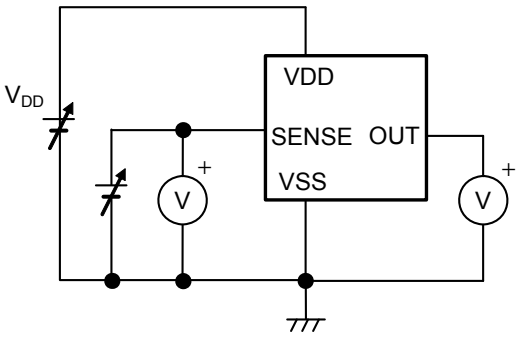



**Figure 8 Test Circuit 1**
**(CMOS output product)**

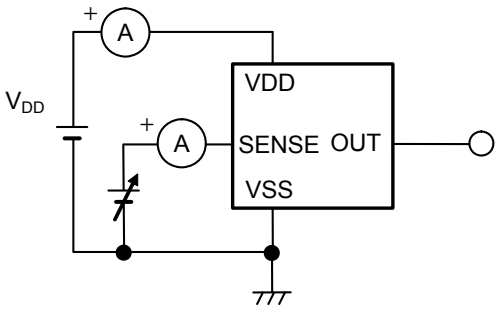



**Figure 9 Test Circuit 2**

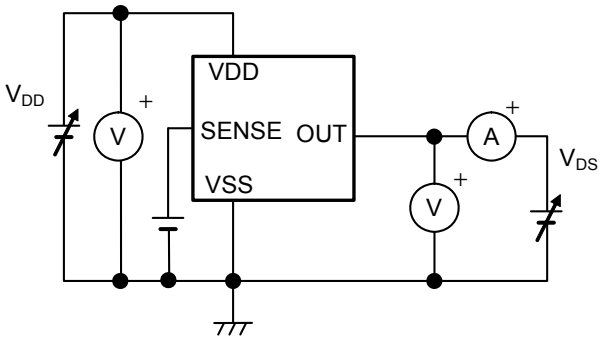



**Figure 10 Test Circuit 3**

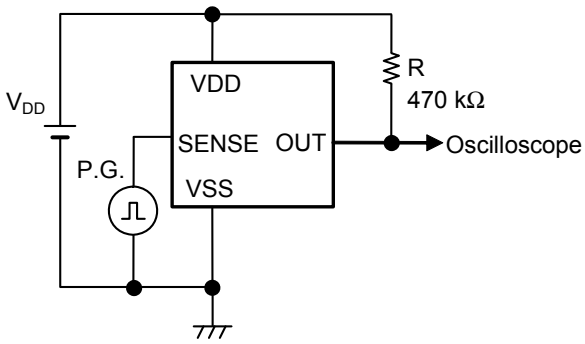



**Figure 11 Test Circuit 4**
**(Nch open-drain output product)**

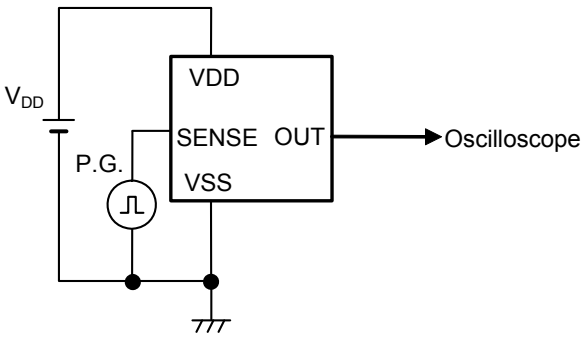



**Figure 12 Test Circuit 4**
**(CMOS output product)**

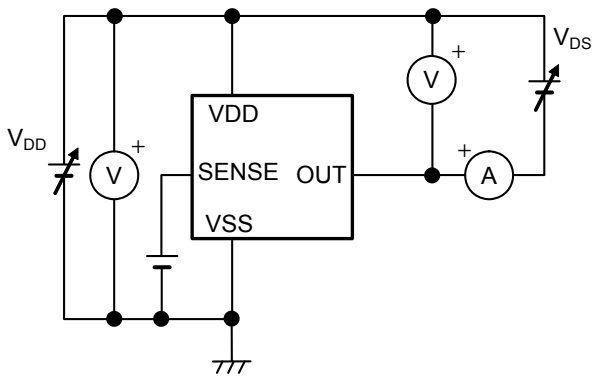



**Figure 13 Test Circuit 5**

## ■ Standard Circuits

### 1. Nch open-drain output product

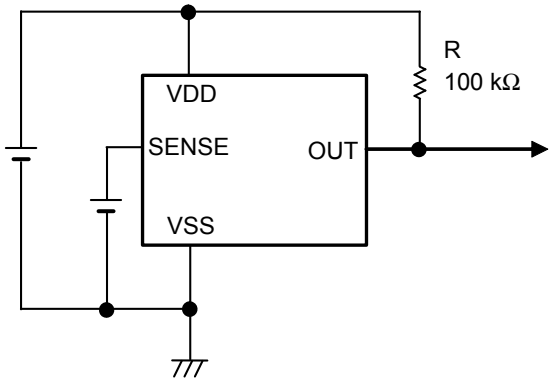



**Figure 14**

### 2. CMOS output product

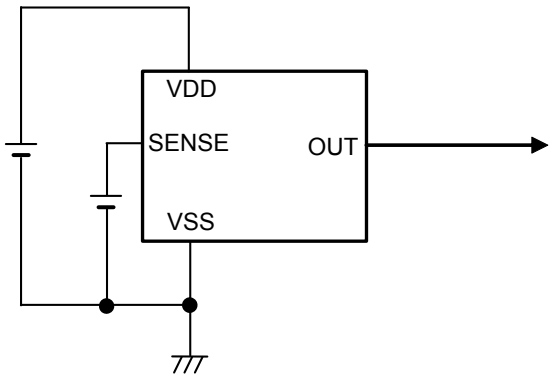



**Figure 15**

**Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**

## ■ Explanation of Terms

### 1. Detection voltage ($-V_{DET}$)

The detection voltage is a voltage at which the output in **Figure 18** or **Figure 19** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$ min.) and the maximum ($-V_{DET}$ max.) is called the detection voltage range (Refer to **Figure 16**).

Example: In the S-1002Cx18, the detection voltage is either one in the range of $1.778\ V \le -V_{DET} \le 1.822\ V$.
This means that some S-1002Cx18 have $-V_{DET} = 1.778$ V and some have $-V_{DET} = 1.822$ V.

### 2. Release voltage ($+V_{DET}$)

The release voltage is a voltage at which the output in **Figure 18** or **Figure 19** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum ($+V_{DET}$ min.) and the maximum ($+V_{DET}$ max.) is called the release voltage range (Refer to **Figure 17**). The range is calculated from the actual detection voltage ($-V_{DET}$) of a product and is in the range of $-V_{DET} \times 1.03 \le +V_{DET} \le -V_{DET} \times 1.07$.

Example: For the S-1002Cx18, the release voltage is either one in the range of $1.832\ V \le +V_{DET} \le 1.949\ V$.
This means that some S-1002Cx18 have $+V_{DET} = 1.832$ V and some have $+V_{DET} = 1.949$ V.

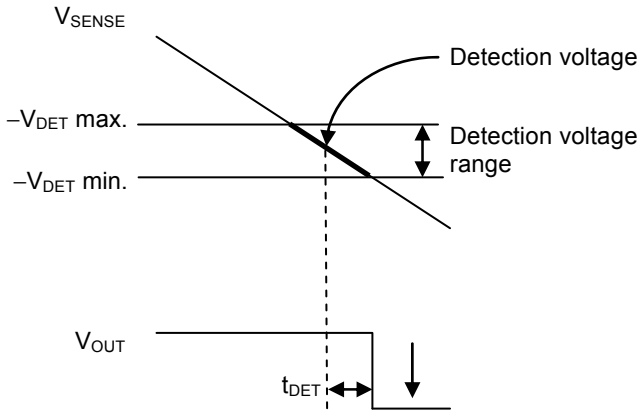



**Figure 16 Detection Voltage**

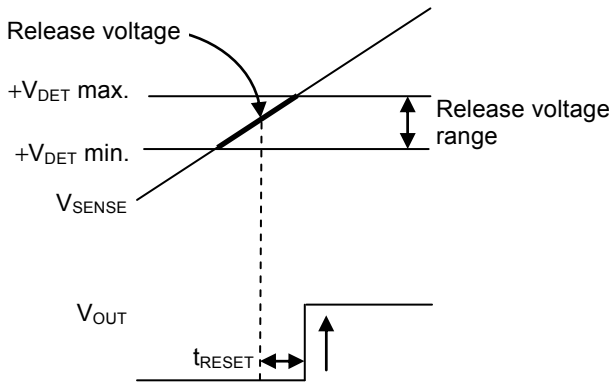



**Figure 17 Release Voltage**

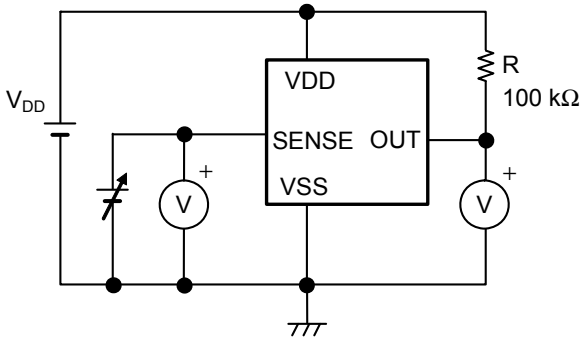



**Figure 18 Test Circuit of Detection Voltage and Release Voltage (Nch open-drain output product)**

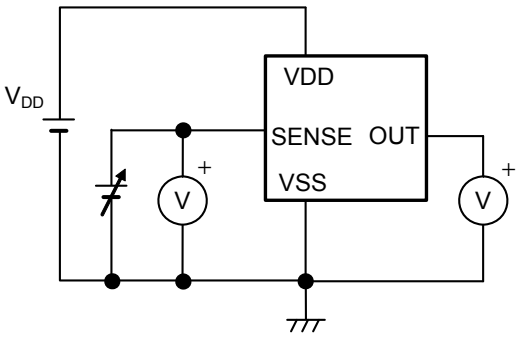



**Figure 19 Test Circuit of Detection Voltage and Release Voltage (CMOS output product)**

### 3. Hysteresis width ($V_{HYS}$)

The hysteresis width is the voltage difference between the detection voltage and the release voltage (the voltage at point B − the voltage at point A = $V_{HYS}$ in "**Figure 22 Timing Chart of S-1002 Series NA / NB Type**" and "**Figure 24 Timing Chart of S-1002 Series CA / CB Type**"). Setting the hysteresis width between the detection voltage and the release voltage, prevents malfunction caused by noise on the input voltage.

### 4. Feed-through current

The feed-through current is a current that flows instantaneously to the VDD pin at the time of detection and release of a voltage detector. The feed-through current is large in CMOS output product, small in Nch open-drain output product.

### 5. Oscillation

In applications where an input resistor is connected (**Figure 20**), taking a CMOS output (active "L") product for example, the feed-through current which is generated when the output goes from "L" to "H" (at the time of release) causes a voltage drop equal to [feed-through current] × [input resistance]. Since the VDD pin and the SENSE pin are shorted as in **Figure 20**, the SENSE pin voltage drops at the time of release. Then the SENSE pin voltage drops below the detection voltage and the output goes from "H" to "L". In this status, the feed-through current stops and its resultant voltage drop disappears, and the output goes from "L" to "H". The feed-through current is then generated again, a voltage drop appears, and repeating the process finally induces oscillation.

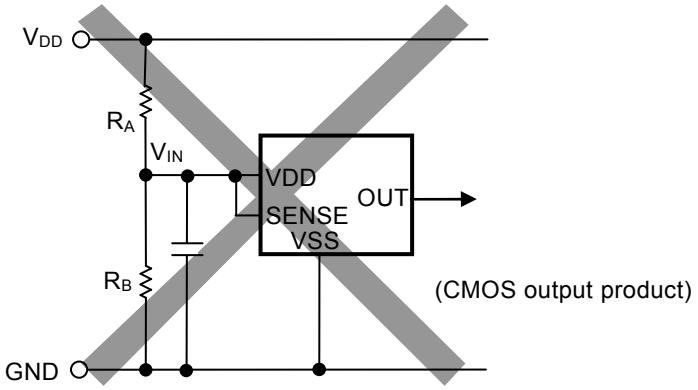



**Figure 20 Example for Bad Implementation Due to Detection Voltage Change**

## ■ Operation

### 1. Basic operation

#### 1. 1 S-1002 Series NA / NB type

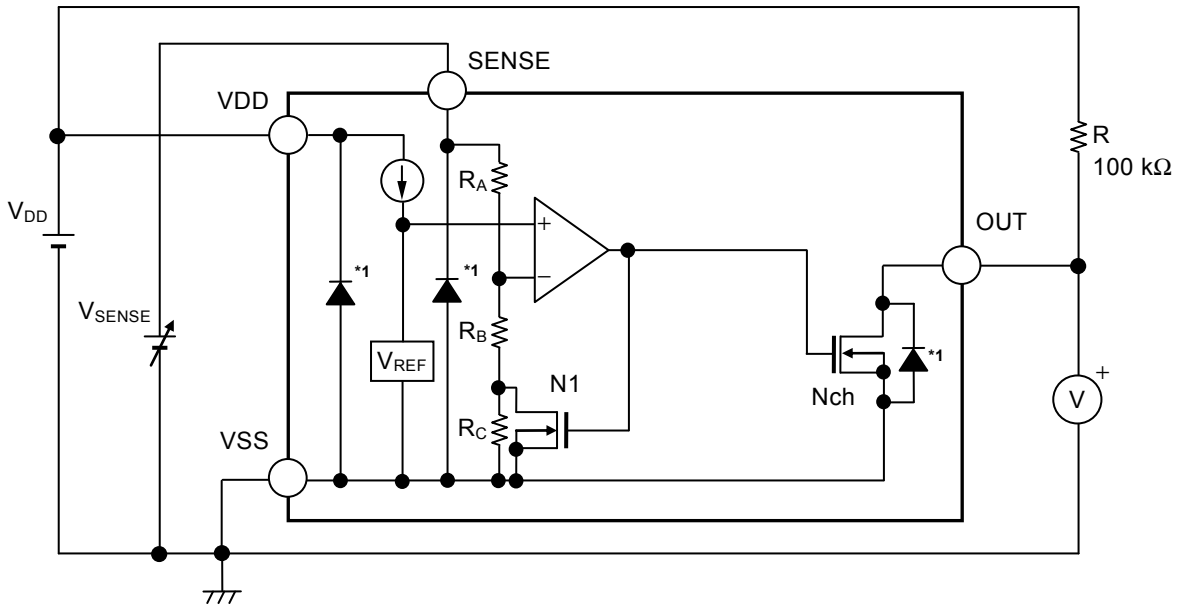
(1) When the power supply voltage ($V_{DD}$) is the minimum operation voltage or higher, and the SENSE pin voltage ($V_{SENSE}$) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off to output $V_{DD}$ ("H") when the output is pulled up. Since the Nch transistor (N1) is turned off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) Even if $V_{SENSE}$ decreases to $+V_{DET}$ or lower, $V_{DD}$ is output when $V_{SENSE}$ is higher than the detection voltage ($-V_{DET}$).
When $V_{SENSE}$ decreases to $-V_{DET}$ or lower (point A in **Figure 22**), the Nch transistor is turned on. And then $V_{SS}$ ("L") is output from the OUT pin after the elapse of the detection delay time ($t_{DET}$).
At this time, N1 is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{SENSE}}{R_A + R_B}$.

(3) Even if $V_{SENSE}$ further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when $V_{DD}$ is minimum operation voltage or higher.

(4) Even if $V_{SENSE}$ exceeds $-V_{DET}$, $V_{SS}$ is output when $V_{SENSE}$ is lower than $+V_{DET}$.

(5) When $V_{SENSE}$ increases to $+V_{DET}$ or higher (point B in **Figure 22**), the Nch transistor is turned off. And then $V_{DD}$ is output from the OUT pin after the elapse of the release delay time ($t_{RESET}$) when the output is pulled up.




***1.** Parasitic diode

**Figure 21 Operation of S-1002 Series NA / NB Type**

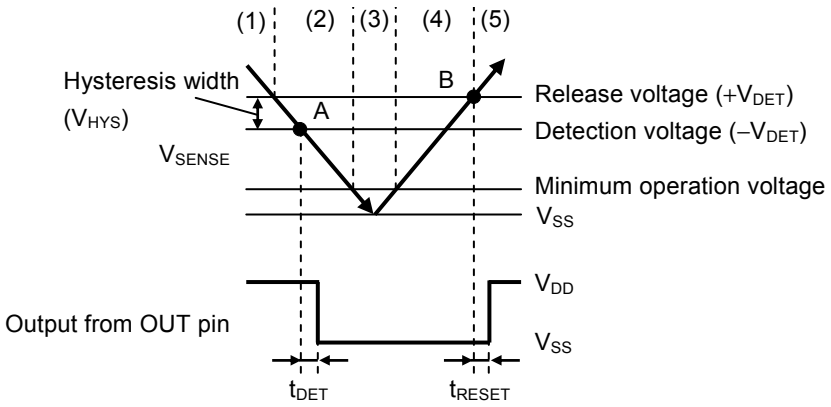



**Figure 22 Timing Chart of S-1002 Series NA / NB Type**

### 1. 2 S-1002 Series CA / CB type

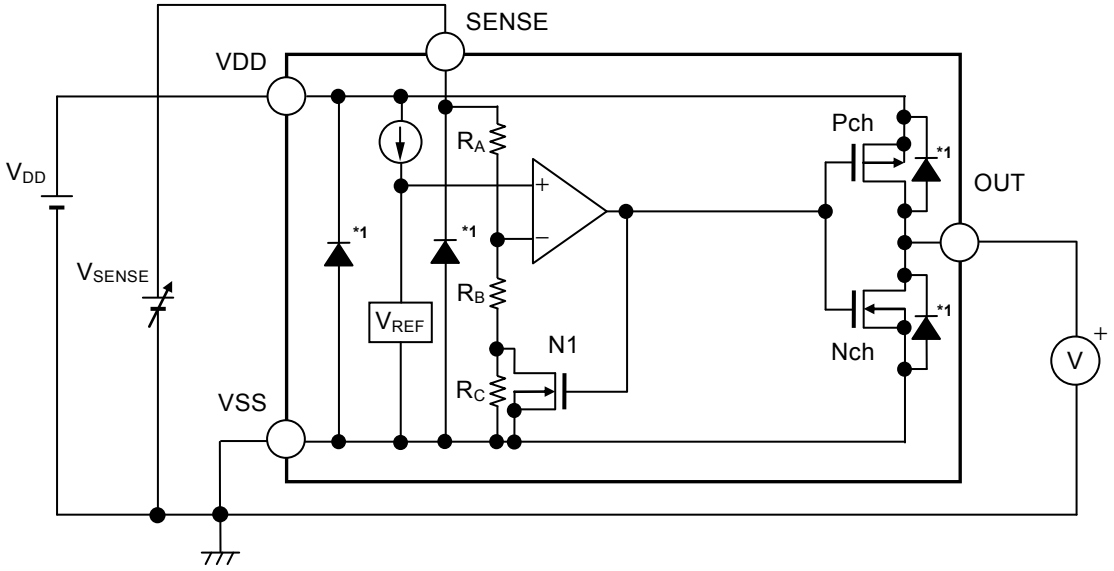
(1) When the power supply voltage ($V_{DD}$) is the minimum operation voltage or higher, and the SENSE pin voltage ($V_{SENSE}$) is the release voltage ($+V_{DET}$) or higher, the Nch transistor is turned off and the Pch transistor is turned on to output $V_{DD}$ ("H"). Since the Nch transistor (N1) is turned off, the input voltage to the comparator is $\frac{(R_B + R_C) \bullet V_{SENSE}}{R_A + R_B + R_C}$.

(2) Even if $V_{SENSE}$ decreases to $+V_{DET}$ or lower, $V_{DD}$ is output when $V_{SENSE}$ is higher than the detection voltage ($-V_{DET}$).
When $V_{SENSE}$ decreases to $-V_{DET}$ or lower (point A in **Figure 24**), the Nch transistor is turned on and the Pch transistor is turned off. And then $V_{SS}$ ("L") is output from the OUT pin after the elapse of the detection delay time ($t_{DET}$).
At this time, N1 is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{SENSE}}{R_A + R_B}$.

(3) Even if $V_{SENSE}$ further decreases to the IC's minimum operation voltage or lower, the output from the OUT pin is stable when $V_{DD}$ is minimum operation voltage or higher.

(4) Even if $V_{SENSE}$ exceeds $-V_{DET}$, $V_{SS}$ is output when $V_{SENSE}$ is lower than $+V_{DET}$.

(5) When $V_{SENSE}$ increases to $+V_{DET}$ or higher (point B in **Figure 24**), the Nch transistor is turned off and the Pch transistor is turned on. And then $V_{DD}$ is output from the OUT pin after the elapse of the release delay time ($t_{RESET}$).




***1.** Parasitic diode

**Figure 23 Operation of S-1002 Series CA / CB Type**

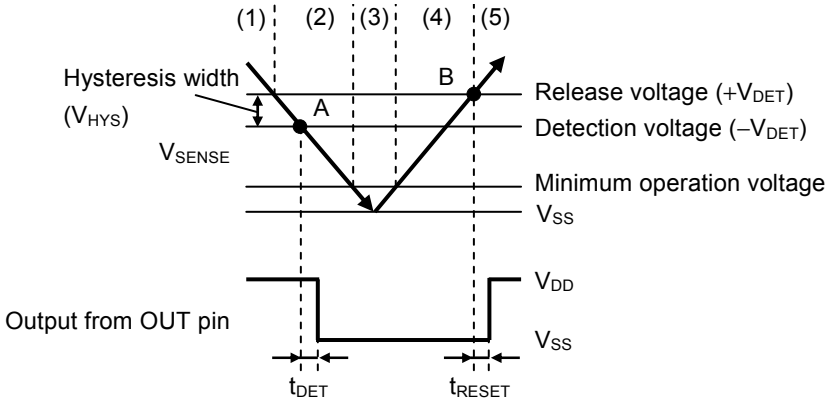



**Figure 24 Timing Chart of S-1002 Series CA / CB Type**

## 2. SENSE pin

### 2. 1 Error when detection voltage is set externally

By connecting a node that was resistance-divided by the resistor ($R_A$) and the resistor ($R_B$) to the SENSE pin as seen in **Figure 25**, the detection voltage can be set externally.
For conventional products without the SENSE pin, $R_A$ cannot be too large since the resistance-divided node must be connected to the VDD pin. This is because a feed-through current will flow through the VDD pin when it goes from detection to release, and if $R_A$ is large, problems such as oscillation or larger error in the hysteresis width may occur.
In the S-1002 Series, $R_A$ and $R_B$ are easily made larger since the resistance-divided node can be connected to the SENSE pin through which no feed-through current flows. However, be careful of error in the current flowing through the internal resistance ($R_{SENSE}$) that will occur.
Although $R_{SENSE}$ in the S-1002 Series is large (5 MΩ min.) to make the error small, $R_A$ and $R_B$ should be selected such that the error is within the allowable limits.

### 2. 2 Selection of $R_A$ and $R_B$

In **Figure 25**, the relation between the external setting detection voltage ($V_{DX}$) and the actual detection voltage ($-V_{DET}$) is ideally calculated by the equation below.

$$V_{DX} = -V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) \quad \cdots (1)$$

However, in reality there is an error in the current flowing through $R_{SENSE}$.
When considering this error, the relation between $V_{DX}$ and $-V_{DET}$ is calculated as follows.

$$\begin{aligned} V_{DX} &= -V_{DET} \times \left(1 + \frac{R_A}{R_B \parallel R_{SENSE}}\right) \\ &= -V_{DET} \times \left(1 + \frac{R_A}{\dfrac{R_B \times R_{SENSE}}{R_B + R_{SENSE}}}\right) \\ &= -V_{DET} \times \left(1 + \frac{R_A}{R_B}\right) + \frac{R_A}{R_{SENSE}} \times -V_{DET} \quad \cdots (2) \end{aligned}$$

By using equations (1) and (2), the error is calculated as $-V_{DET} \times \dfrac{R_A}{R_{SENSE}}$.
The error rate is calculated as follows by dividing the error by the right-hand side of equation (1).

$$\frac{R_A \times R_B}{R_{SENSE} \times (R_A + R_B)} \times 100\ [\%] = \frac{R_A \parallel R_B}{R_{SENSE}} \times 100\ [\%] \quad \cdots (3)$$

As seen in equation (3), the smaller the resistance values of $R_A$ and $R_B$ compared to $R_{SENSE}$, the smaller the error rate becomes.
Also, the relation between the external setting hysteresis width ($V_{HX}$) and the hysteresis width ($V_{HYS}$) is calculated by equation below. Error due to $R_{SENSE}$ also occurs to the relation in a similar way to the detection voltage.

$$V_{HX} = V_{HYS} \times \left(1 + \frac{R_A}{R_B}\right) \quad \cdots (4)$$

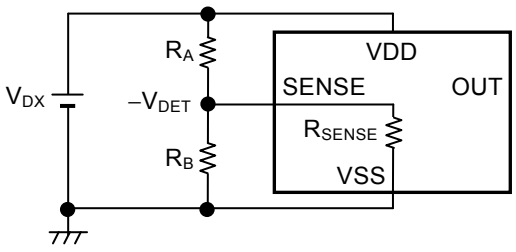



**Figure 25 Detection Voltage External Setting Circuit**

**Caution If $R_A$ and $R_B$ are large, the SENSE pin input impedance becomes higher and may cause a malfunction due to noise. In this case, connect a capacitor between the SENSE pin and the VSS pin.**

### 2. 3 Power on sequence

Apply power in the order, the VDD pin then the SENSE pin.
As seen in **Figure 26**, when $V_{SENSE} \geq +V_{DET}$, the OUT pin output ($V_{OUT}$) rises and the S-1002 Series becomes the release status (normal operation).

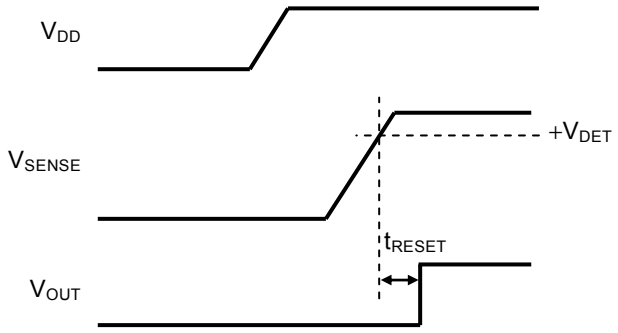



**Figure 26**

**Caution If power is applied in the order the SENSE pin then the VDD pin, an erroneous release may occur even if $V_{SENSE} < +V_{DET}$.**

### 2. 4 Precautions when shorting between the VDD pin and the SENSE pin

#### 2. 4. 1 Input resistor

Do not connect the input resistor ($R_A$) when shorting between the VDD pin and the SENSE pin.
A feed-through current flows through the VDD pin at the time of release. When connecting the circuit shown as **Figure 27**, the feed-through current of the VDD pin flowing through $R_A$ will cause a drop in $V_{SENSE}$ at the time of release.
At that time, oscillation may occur if $V_{SENSE} \leq -V_{DET}$.

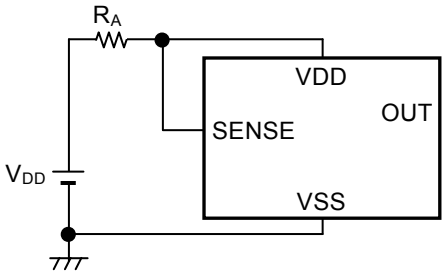



**Figure 27**

#### 2. 4. 2 Parasitic resistance and parasitic capacitance

Due to the difference in parasitic resistance and parasitic capacitance of the VDD pin and the SENSE pin, power may be applied to the SENSE pin first.
Note that an erroneous release may occur if this happens (refer to "**2. 3 Power on sequence**").

**Caution In CMOS output product, make sure that the VDD pin input impedance does not become too high, regardless of the above. Since a feed-through current is large, a malfunction may occur if the VDD pin voltage changes greatly at the time of release.**

### 2. 5 Malfunction when $V_{DD}$ falls

As seen in **Figure 28**, note that if the VDD pin voltage ($V_{DD}$) drops steeply below 1.2 V when $-V_{DET} < V_{SENSE} < +V_{DET}$, erroneous detection may occur.
When $V_{DD\_Low} \geq 1.2$ V, erroneous detection does not occur.
When $V_{DD\_Low} < 1.2$ V, the more the $V_{DD}$ falling amplitude increases or the shorter the falling time becomes, the easier the erroneous detection.
Perform thorough evaluation in actual application.

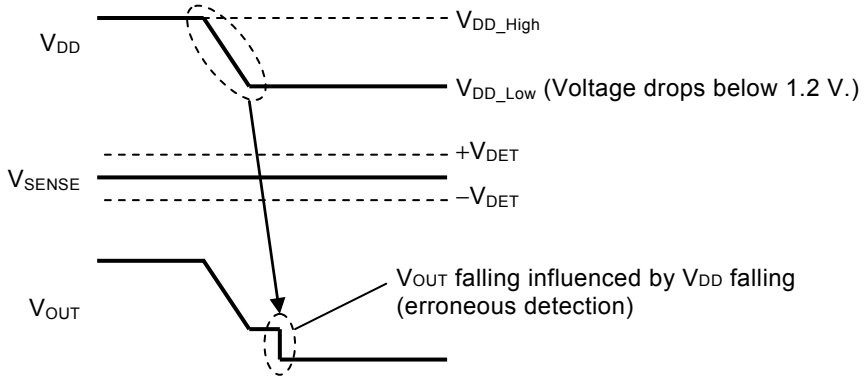



**Figure 28**

The S-1002Cx50 example in **Figure 29** shows an example of erroneous detection boundary conditions.

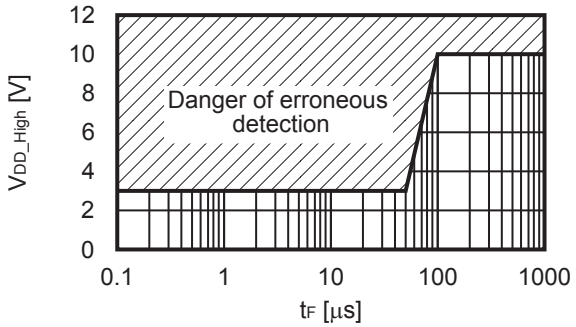



**Figure 29**

**Remark** Test conditions

| | |
|---|---|
| Product name: | S-1002Cx50 |
| $V_{SENSE}$: | $-V_{DET(S)} + 0.1$ V |
| $V_{DD\_High}$: | VDD pin voltage before falling |
| $V_{DD\_Low}$: | VDD pin voltage after falling (0.95 V) |
| $\Delta V_{DD}$: | $V_{DD\_High} - V_{DD\_Low}$ |
| $t_F$: | Falling time of $V_{DD}$ from $V_{DD\_High} - \Delta V_{DD} \times 10\%$ to $V_{DD\_Low} + \Delta V_{DD} \times 10\%$ |

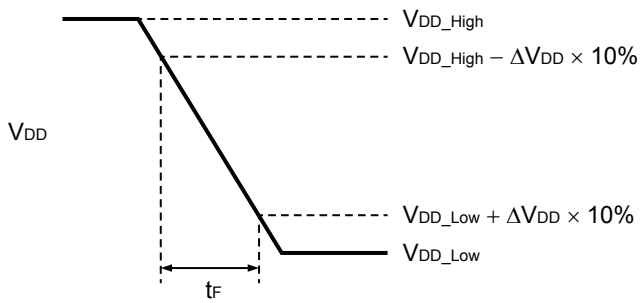
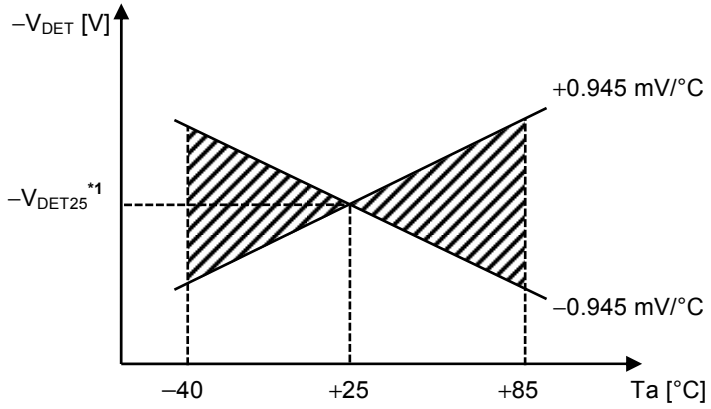



**Figure 30**

## 3. Other characteristics

### 3. 1 Temperature characteristics of detection voltage

The shaded area in **Figure 31** shows the temperature characteristics of detection voltage in the operation temperature range.




***1.** $-V_{DET25}$ is a detection voltage value at Ta = +25°C.

**Figure 31 Temperature Characteristics of Detection Voltage (Example for $-V_{DET}$ = 2.7 V)**

### 3. 2 Temperature characteristics of release voltage

The temperature change $\frac{\Delta+V_{DET}}{\Delta Ta}$ of the release voltage is calculated by using the temperature change $\frac{\Delta-V_{DET}}{\Delta Ta}$ of the detection voltage as follows:

$$\frac{\Delta+V_{DET}}{\Delta Ta} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta-V_{DET}}{\Delta Ta}$$

The temperature change of the release voltage and the detection voltage has the same sign consequently.

### 3. 3 Temperature characteristics of hysteresis voltage

The temperature change of the hysteresis voltage is expressed as $\frac{\Delta+V_{DET}}{\Delta Ta} - \frac{\Delta-V_{DET}}{\Delta Ta}$ and is calculated as follows:

$$\frac{\Delta+V_{DET}}{\Delta Ta} - \frac{\Delta-V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta-V_{DET}}{\Delta Ta}$$

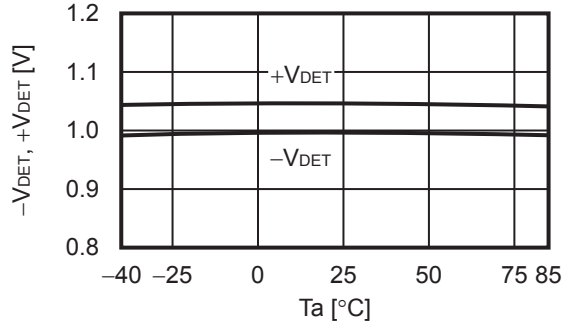
## ■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- In CMOS output product of the S-1002 Series, the feed-through current flows at the time of detection and release. If the VDD pin input impedance is high, malfunction may occur due to the voltage drop by the feed-through current when releasing.
- In CMOS output product, oscillation may occur if a pull-down resistor is connected and falling speed of the SENSE pin voltage ($V_{SENSE}$) is slow near the detection voltage when the VDD pin and the SENSE pin are shorted.
- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. SII Semiconductor Corporation shall not bear any responsibility for patent infringements related to products using the circuits described herein.
- SII Semiconductor Corporation claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

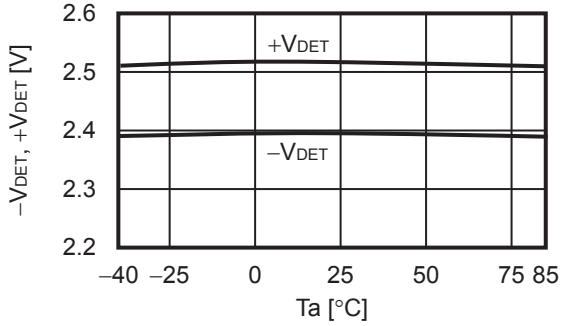
## ■ Characteristics (Typical Data)

### 1. Detection voltage ($-V_{DET}$), Release voltage ($+V_{DET}$) vs. Temperature (Ta)

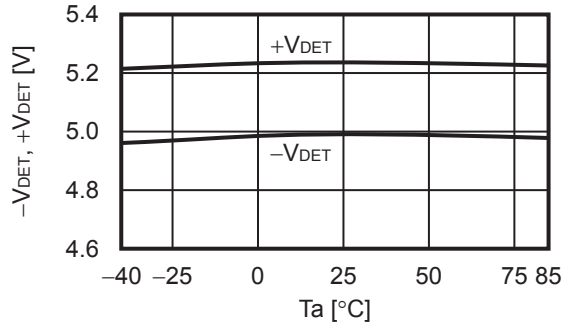
S-1002Cx10 $V_{DD}$ = 5.0 V




S-1002Cx24 $V_{DD}$ = 5.0 V

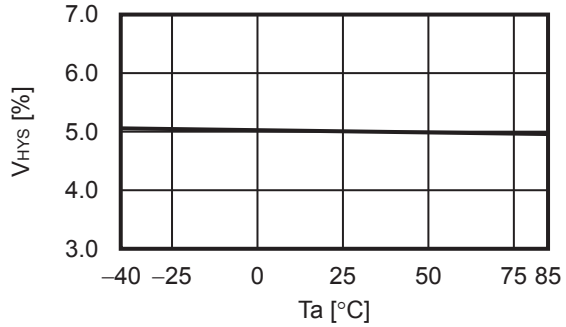



S-1002Cx50 $V_{DD}$ = 5.0 V

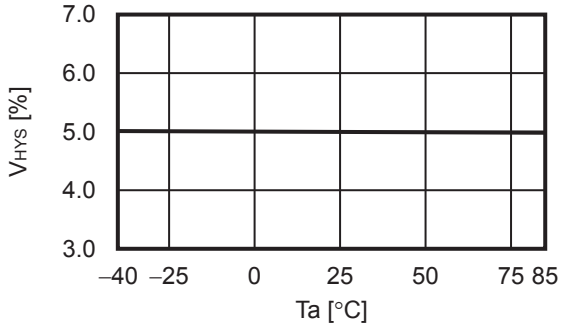



### 2. Hysteresis width ($V_{HYS}$) vs. Temperature (Ta)

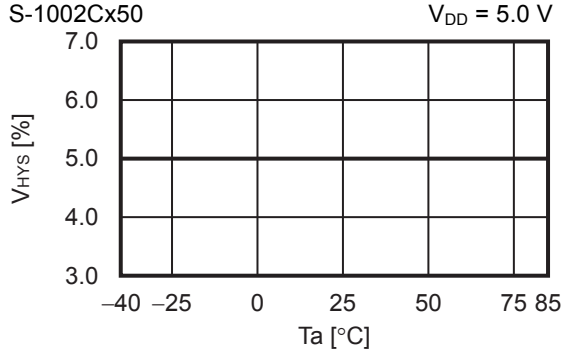
S-1002Cx10 $V_{DD}$ = 5.0 V




S-1002Cx24 $V_{DD}$ = 5.0 V

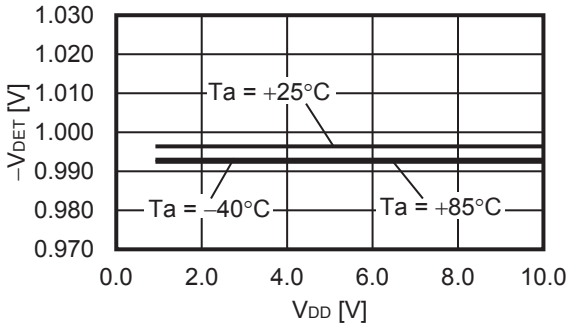



S-1002Cx50 $V_{DD}$ = 5.0 V

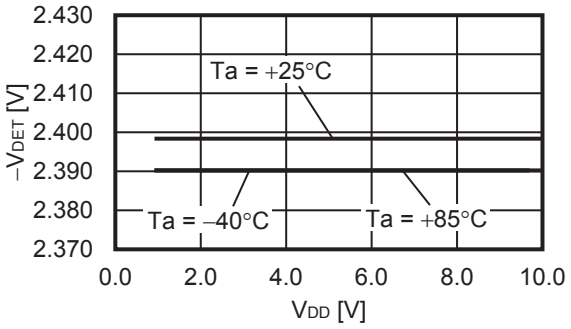


### 3. Detection voltage ($-V_{DET}$) vs. Power supply voltage ($V_{DD}$)

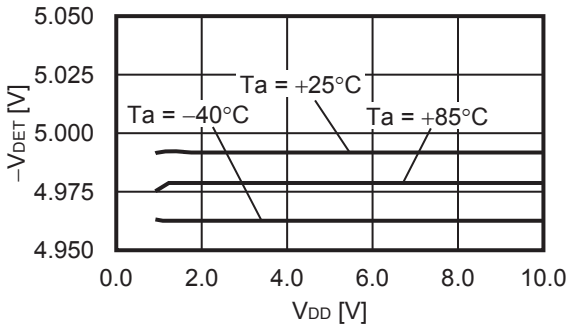
S-1002Cx10




S-1002Cx24

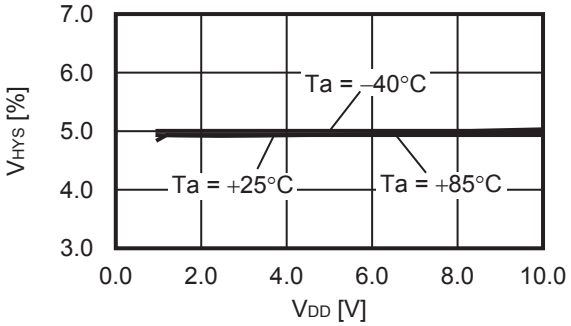



S-1002Cx50

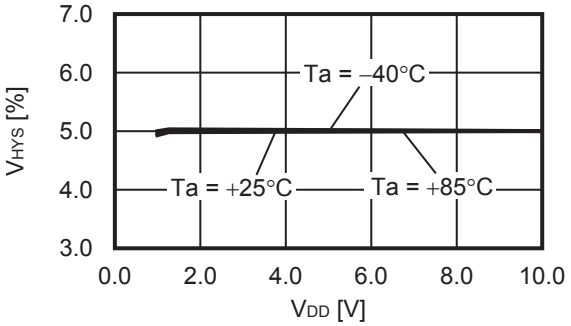



### 4. Hysteresis width ($V_{HYS}$) vs. Power supply voltage ($V_{DD}$)

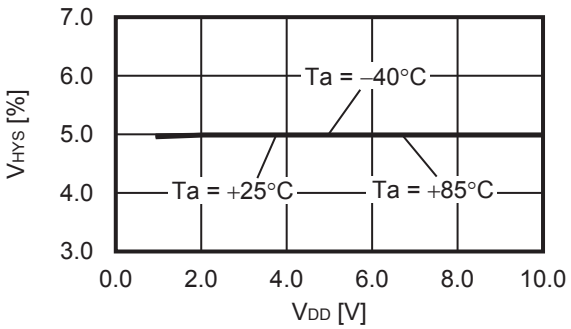
S-1002Cx10




S-1002Cx24

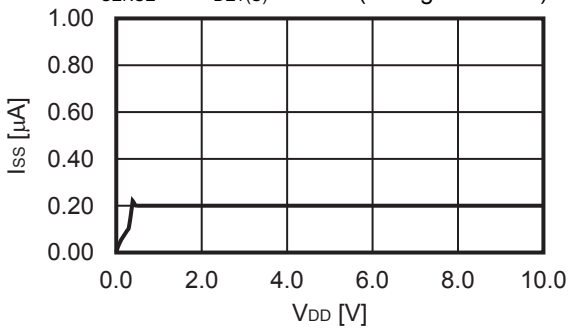



S-1002Cx50

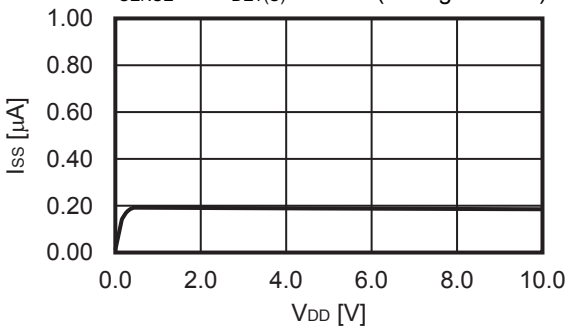


### 5. Current consumption ($I_{SS}$) vs. Power supply voltage ($V_{DD}$)

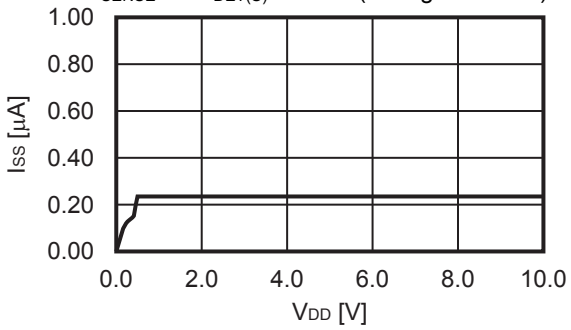
S-1002Cx10 Ta = +25°C,
$V_{SENSE} = -V_{DET(S)} - 0.1$ V (during detection)



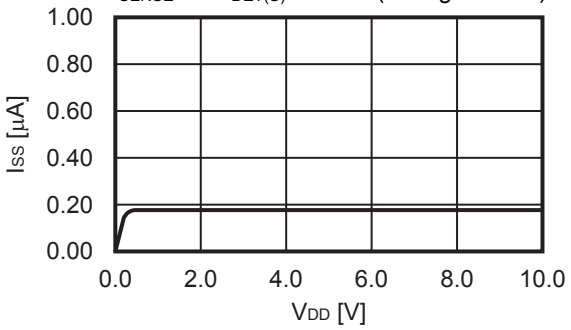

S-1002Cx10 Ta = +25°C,
$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)



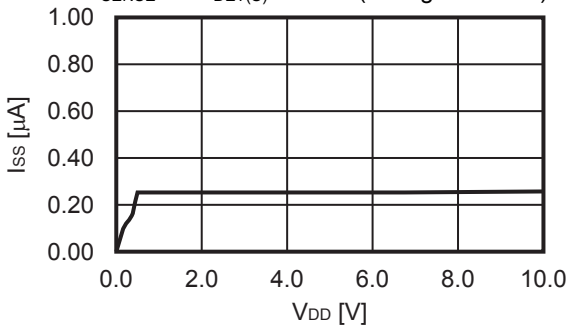

S-1002Cx24 Ta = +25°C,
$V_{SENSE} = -V_{DET(S)} - 0.1$ V (during detection)




S-1002Cx24 Ta = +25°C,
$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)




S-1002Cx50 Ta = +25°C,
$V_{SENSE} = -V_{DET(S)} - 0.1$ V (during detection)




S-1002Cx50 Ta = +25°C,
$V_{SENSE} = -V_{DET(S)} + 1.0$ V (during release)