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SII

# S-1003 Series

## MANUAL RESET BUILT-IN DELAY CIRCUIT (EXTERNAL DELAY TIME SETTING) HIGH-ACCURACY VOLTAGE DETECTOR

www.sii-ic.com



Rev.1.0_02

The S-1003 Series is a high-accuracy voltage detector developed using CMOS technology. The detection voltage is fixed internally with an accuracy of ±1.0% ($-V_{DET} \geq 2.2$ V). It operates with current consumption of 500 nA typ.
The release signal can be delayed by setting a capacitor externally. Delay time accuracy is ±15%.
Moreover, since the S-1003 Series includes the manual reset function, the reset signal can be also output forcibly.
Two output forms Nch open-drain output and CMOS output are available.

## ■ Features

| | |
|---|---|
| • Detection voltage: | 1.2 V to 5.0 V (0.1 V step) |
| • Detection voltage accuracy: | ±1.0% ($2.2 \text{ V} \leq -V_{DET} \leq 5.0$ V) |
| | ±22 mV ($1.2 \text{ V} \leq -V_{DET} < 2.2$ V) |
| • Current consumption: | 500 nA typ. |
| • Operation voltage range: | 0.95 V to 10.0 V |
| • Hysteresis width: | 5% ± 2% |
| • Manual reset function: | MR pin logic active "L", active "H" |
| • Delay time accuracy: | ±15% ($C_D$ = 4.7 nF) |
| • Output form: | Nch open-drain output (Active "L") |
| | CMOS output (Active "L") |
| • Operation temperature range: | Ta = −40°C to +85°C |
| • Lead-free (Sn 100%), halogen-free | |

## ■ Applications

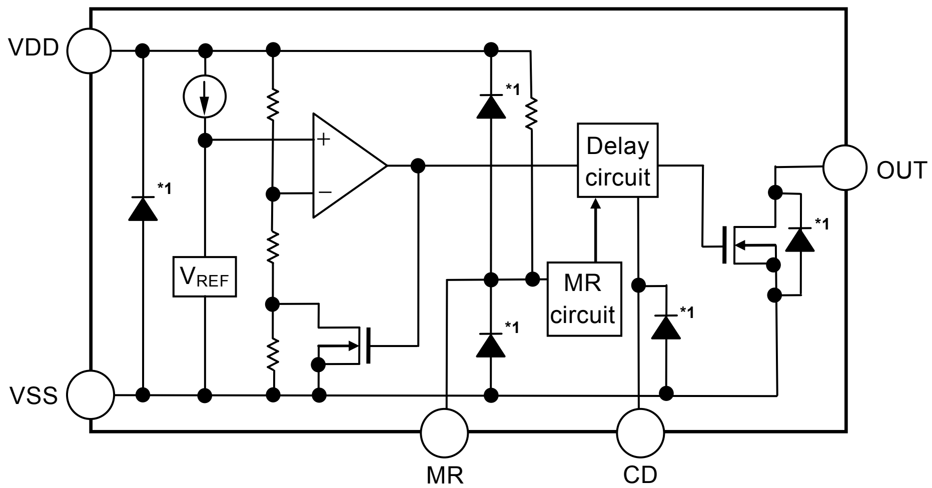
- Power supply monitor for microcomputer and reset for CPU
- Constant voltage power supply monitor for TV, Blu-ray recorder and home appliance
- Power supply monitor for portable devices such as notebook PC, digital still camera and mobile phone

## ■ Packages

- SOT-23-5
- SNT-6A

## ■ Block Diagrams

### 1. Nch open-drain output product (S-1003NAxxI)

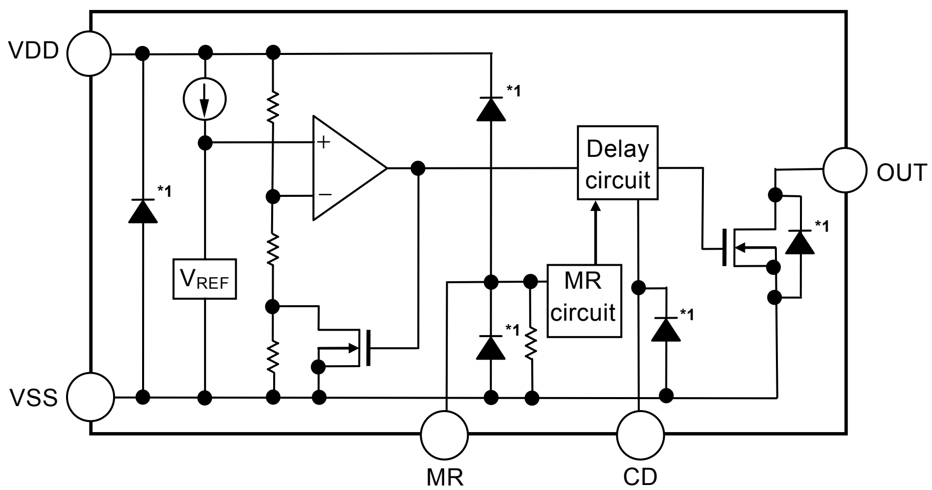



| Function | Status |
|---|---|
| Output logic | Active "L" |
| MR pin logic | Active "L" |

***1.** Parasitic diode

**Figure 1**

### 2. Nch open-drain output product (S-1003NBxxI)

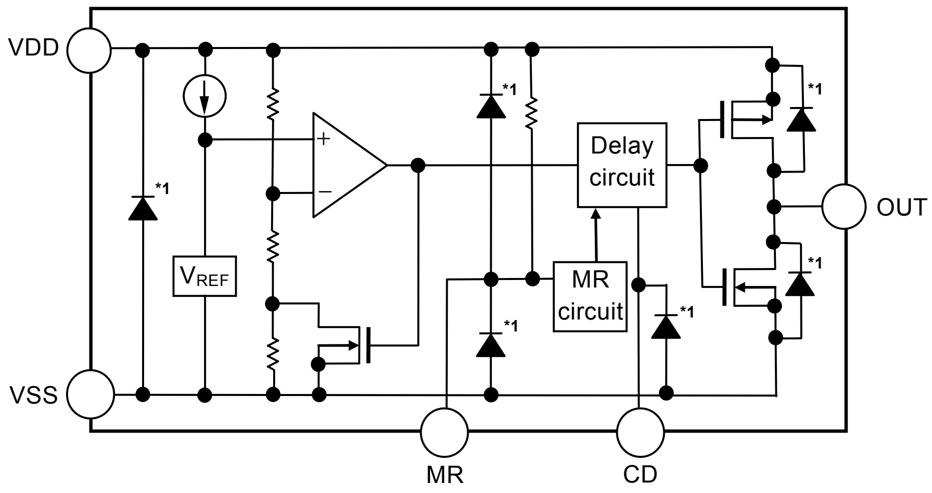



| Function | Status |
|---|---|
| Output logic | Active "L" |
| MR pin logic | Active "H" |

***1.** Parasitic diode

**Figure 2**

### 3. CMOS output product (S-1003CAxxl)

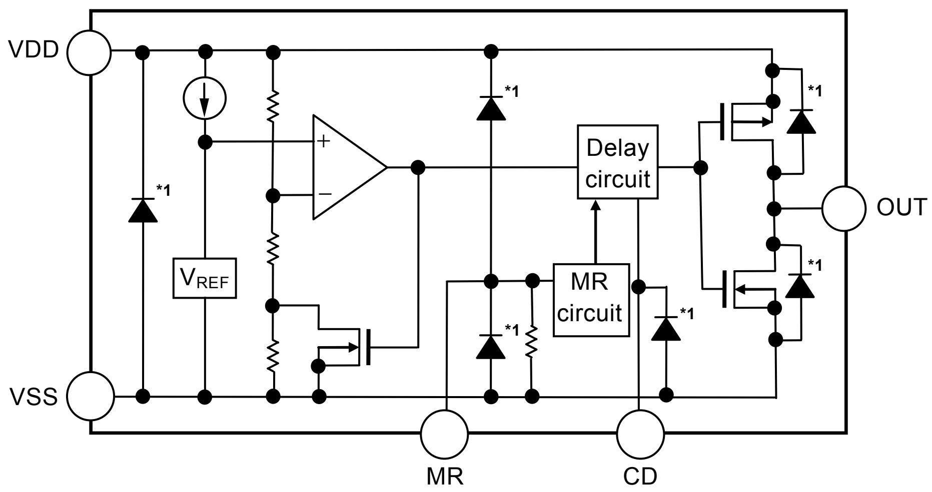



| Function | Status |
|---|---|
| Output logic | Active "L" |
| MR pin logic | Active "L" |

***1.** Parasitic diode

**Figure 3**

### 4. CMOS output product (S-1003CBxxl)




| Function | Status |
|---|---|
| Output logic | Active "L" |
| MR pin logic | Active "H" |

***1.** Parasitic diode

**Figure 4**

## ■ Product Name Structure

Users can select the output form, MR pin logic, detection voltage value, and package type for the S-1003 Series. Refer to "**1. Product name**" regarding the contents of product name, "**2. Product type list**" regarding the product types, "**3. Packages**" regarding the package drawings and "**4. Product name list**" regarding details of product name.

### 1. Product name

**S-1003 x x xx I - xxxx U**

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications[*1]
  - M5T1: SOT-23-5, Tape
  - I6T1: SNT-6A, Tape
- Operation temperature
  - I: Ta = –40°C to +85°C
- Detection voltage value
  - 12 to 50
  - (e.g., when the detection voltage is 1.2 V, it is expressed as 12.)
- MR pin logic[*2]
  - A: Active "L"
  - B: Active "H"
- Output form[*2]
  - N: Nch open-drain output (Active "L")[*3]
  - C: CMOS output (Active "L")[*3]

***1.** Refer to the tape drawing.
***2.** Refer to "**2. Product type list**".
***3.** If you request the product with output logic active "H", contact our sales office.

### 2. Product type list

**Table 1**

| Product Type | Output Form | MR Pin Logic | Output Logic |
|---|---|---|---|
| NA | Nch open-drain output | Active "L" | Active "L" |
| NB | | Active "H" | Active "L" |
| CA | CMOS output | Active "L" | Active "L" |
| CB | | Active "H" | Active "L" |

### 3. Packages

**Table 2 Package Drawing Codes**

| Package Name | Dimension | Tape | Reel | Land |
|---|---|---|---|---|
| SOT-23-5 | MP005-A-P-SD | MP005-A-C-SD | MP005-A-R-SD | – |
| SNT-6A | PG006-A-P-SD | PG006-A-C-SD | PG006-A-R-SD | PG006-A-L-SD |

## 4. Product name list

### 4. 1 S-1003 Series NA type

Output form: Nch open-drain output (Active "L")
MR pin logic: Active "L"

**Table 3**

| Detection Voltage | SOT-23-5 | SNT-6A |
|---|---|---|
| 1.2 V ± 22 mV | S-1003NA12I-M5T1U | S-1003NA12I-I6T1U |
| 1.3 V ± 22 mV | S-1003NA13I-M5T1U | S-1003NA13I-I6T1U |
| 1.4 V ± 22 mV | S-1003NA14I-M5T1U | S-1003NA14I-I6T1U |
| 1.5 V ± 22 mV | S-1003NA15I-M5T1U | S-1003NA15I-I6T1U |
| 1.6 V ± 22 mV | S-1003NA16I-M5T1U | S-1003NA16I-I6T1U |
| 1.7 V ± 22 mV | S-1003NA17I-M5T1U | S-1003NA17I-I6T1U |
| 1.8 V ± 22 mV | S-1003NA18I-M5T1U | S-1003NA18I-I6T1U |
| 1.9 V ± 22 mV | S-1003NA19I-M5T1U | S-1003NA19I-I6T1U |
| 2.0 V ± 22 mV | S-1003NA20I-M5T1U | S-1003NA20I-I6T1U |
| 2.1 V ± 22 mV | S-1003NA21I-M5T1U | S-1003NA21I-I6T1U |
| 2.2 V ± 1.0% | S-1003NA22I-M5T1U | S-1003NA22I-I6T1U |
| 2.3 V ± 1.0% | S-1003NA23I-M5T1U | S-1003NA23I-I6T1U |
| 2.4 V ± 1.0% | S-1003NA24I-M5T1U | S-1003NA24I-I6T1U |
| 2.5 V ± 1.0% | S-1003NA25I-M5T1U | S-1003NA25I-I6T1U |
| 2.6 V ± 1.0% | S-1003NA26I-M5T1U | S-1003NA26I-I6T1U |
| 2.7 V ± 1.0% | S-1003NA27I-M5T1U | S-1003NA27I-I6T1U |
| 2.8 V ± 1.0% | S-1003NA28I-M5T1U | S-1003NA28I-I6T1U |
| 2.9 V ± 1.0% | S-1003NA29I-M5T1U | S-1003NA29I-I6T1U |
| 3.0 V ± 1.0% | S-1003NA30I-M5T1U | S-1003NA30I-I6T1U |
| 3.1 V ± 1.0% | S-1003NA31I-M5T1U | S-1003NA31I-I6T1U |
| 3.2 V ± 1.0% | S-1003NA32I-M5T1U | S-1003NA32I-I6T1U |
| 3.3 V ± 1.0% | S-1003NA33I-M5T1U | S-1003NA33I-I6T1U |
| 3.4 V ± 1.0% | S-1003NA34I-M5T1U | S-1003NA34I-I6T1U |
| 3.5 V ± 1.0% | S-1003NA35I-M5T1U | S-1003NA35I-I6T1U |
| 3.6 V ± 1.0% | S-1003NA36I-M5T1U | S-1003NA36I-I6T1U |
| 3.7 V ± 1.0% | S-1003NA37I-M5T1U | S-1003NA37I-I6T1U |
| 3.8 V ± 1.0% | S-1003NA38I-M5T1U | S-1003NA38I-I6T1U |
| 3.9 V ± 1.0% | S-1003NA39I-M5T1U | S-1003NA39I-I6T1U |
| 4.0 V ± 1.0% | S-1003NA40I-M5T1U | S-1003NA40I-I6T1U |
| 4.1 V ± 1.0% | S-1003NA41I-M5T1U | S-1003NA41I-I6T1U |
| 4.2 V ± 1.0% | S-1003NA42I-M5T1U | S-1003NA42I-I6T1U |
| 4.3 V ± 1.0% | S-1003NA43I-M5T1U | S-1003NA43I-I6T1U |
| 4.4 V ± 1.0% | S-1003NA44I-M5T1U | S-1003NA44I-I6T1U |
| 4.5 V ± 1.0% | S-1003NA45I-M5T1U | S-1003NA45I-I6T1U |
| 4.6 V ± 1.0% | S-1003NA46I-M5T1U | S-1003NA46I-I6T1U |
| 4.7 V ± 1.0% | S-1003NA47I-M5T1U | S-1003NA47I-I6T1U |
| 4.8 V ± 1.0% | S-1003NA48I-M5T1U | S-1003NA48I-I6T1U |
| 4.9 V ± 1.0% | S-1003NA49I-M5T1U | S-1003NA49I-I6T1U |
| 5.0 V ± 1.0% | S-1003NA50I-M5T1U | S-1003NA50I-I6T1U |

### 4. 2 S-1003 Series NB type

Output form: Nch open-drain output (Active "L")
MR pin logic: Active "H"

**Table 4**

| Detection Voltage | SOT-23-5 | SNT-6A |
|---|---|---|
| 1.2 V ± 22 mV | S-1003NB12I-M5T1U | S-1003NB12I-I6T1U |
| 1.3 V ± 22 mV | S-1003NB13I-M5T1U | S-1003NB13I-I6T1U |
| 1.4 V ± 22 mV | S-1003NB14I-M5T1U | S-1003NB14I-I6T1U |
| 1.5 V ± 22 mV | S-1003NB15I-M5T1U | S-1003NB15I-I6T1U |
| 1.6 V ± 22 mV | S-1003NB16I-M5T1U | S-1003NB16I-I6T1U |
| 1.7 V ± 22 mV | S-1003NB17I-M5T1U | S-1003NB17I-I6T1U |
| 1.8 V ± 22 mV | S-1003NB18I-M5T1U | S-1003NB18I-I6T1U |
| 1.9 V ± 22 mV | S-1003NB19I-M5T1U | S-1003NB19I-I6T1U |
| 2.0 V ± 22 mV | S-1003NB20I-M5T1U | S-1003NB20I-I6T1U |
| 2.1 V ± 22 mV | S-1003NB21I-M5T1U | S-1003NB21I-I6T1U |
| 2.2 V ± 1.0% | S-1003NB22I-M5T1U | S-1003NB22I-I6T1U |
| 2.3 V ± 1.0% | S-1003NB23I-M5T1U | S-1003NB23I-I6T1U |
| 2.4 V ± 1.0% | S-1003NB24I-M5T1U | S-1003NB24I-I6T1U |
| 2.5 V ± 1.0% | S-1003NB25I-M5T1U | S-1003NB25I-I6T1U |
| 2.6 V ± 1.0% | S-1003NB26I-M5T1U | S-1003NB26I-I6T1U |
| 2.7 V ± 1.0% | S-1003NB27I-M5T1U | S-1003NB27I-I6T1U |
| 2.8 V ± 1.0% | S-1003NB28I-M5T1U | S-1003NB28I-I6T1U |
| 2.9 V ± 1.0% | S-1003NB29I-M5T1U | S-1003NB29I-I6T1U |
| 3.0 V ± 1.0% | S-1003NB30I-M5T1U | S-1003NB30I-I6T1U |
| 3.1 V ± 1.0% | S-1003NB31I-M5T1U | S-1003NB31I-I6T1U |
| 3.2 V ± 1.0% | S-1003NB32I-M5T1U | S-1003NB32I-I6T1U |
| 3.3 V ± 1.0% | S-1003NB33I-M5T1U | S-1003NB33I-I6T1U |
| 3.4 V ± 1.0% | S-1003NB34I-M5T1U | S-1003NB34I-I6T1U |
| 3.5 V ± 1.0% | S-1003NB35I-M5T1U | S-1003NB35I-I6T1U |
| 3.6 V ± 1.0% | S-1003NB36I-M5T1U | S-1003NB36I-I6T1U |
| 3.7 V ± 1.0% | S-1003NB37I-M5T1U | S-1003NB37I-I6T1U |
| 3.8 V ± 1.0% | S-1003NB38I-M5T1U | S-1003NB38I-I6T1U |
| 3.9 V ± 1.0% | S-1003NB39I-M5T1U | S-1003NB39I-I6T1U |
| 4.0 V ± 1.0% | S-1003NB40I-M5T1U | S-1003NB40I-I6T1U |
| 4.1 V ± 1.0% | S-1003NB41I-M5T1U | S-1003NB41I-I6T1U |
| 4.2 V ± 1.0% | S-1003NB42I-M5T1U | S-1003NB42I-I6T1U |
| 4.3 V ± 1.0% | S-1003NB43I-M5T1U | S-1003NB43I-I6T1U |
| 4.4 V ± 1.0% | S-1003NB44I-M5T1U | S-1003NB44I-I6T1U |
| 4.5 V ± 1.0% | S-1003NB45I-M5T1U | S-1003NB45I-I6T1U |
| 4.6 V ± 1.0% | S-1003NB46I-M5T1U | S-1003NB46I-I6T1U |
| 4.7 V ± 1.0% | S-1003NB47I-M5T1U | S-1003NB47I-I6T1U |
| 4.8 V ± 1.0% | S-1003NB48I-M5T1U | S-1003NB48I-I6T1U |
| 4.9 V ± 1.0% | S-1003NB49I-M5T1U | S-1003NB49I-I6T1U |
| 5.0 V ± 1.0% | S-1003NB50I-M5T1U | S-1003NB50I-I6T1U |

### 4. 3 S-1003 Series CA type

Output form: CMOS output (Active "L")
MR pin logic: Active "L"

**Table 5**

| Detection Voltage | SOT-23-5 | SNT-6A |
|---|---|---|
| 1.2 V ± 22 mV | S-1003CA12I-M5T1U | S-1003CA12I-I6T1U |
| 1.3 V ± 22 mV | S-1003CA13I-M5T1U | S-1003CA13I-I6T1U |
| 1.4 V ± 22 mV | S-1003CA14I-M5T1U | S-1003CA14I-I6T1U |
| 1.5 V ± 22 mV | S-1003CA15I-M5T1U | S-1003CA15I-I6T1U |
| 1.6 V ± 22 mV | S-1003CA16I-M5T1U | S-1003CA16I-I6T1U |
| 1.7 V ± 22 mV | S-1003CA17I-M5T1U | S-1003CA17I-I6T1U |
| 1.8 V ± 22 mV | S-1003CA18I-M5T1U | S-1003CA18I-I6T1U |
| 1.9 V ± 22 mV | S-1003CA19I-M5T1U | S-1003CA19I-I6T1U |
| 2.0 V ± 22 mV | S-1003CA20I-M5T1U | S-1003CA20I-I6T1U |
| 2.1 V ± 22 mV | S-1003CA21I-M5T1U | S-1003CA21I-I6T1U |
| 2.2 V ± 1.0% | S-1003CA22I-M5T1U | S-1003CA22I-I6T1U |
| 2.3 V ± 1.0% | S-1003CA23I-M5T1U | S-1003CA23I-I6T1U |
| 2.4 V ± 1.0% | S-1003CA24I-M5T1U | S-1003CA24I-I6T1U |
| 2.5 V ± 1.0% | S-1003CA25I-M5T1U | S-1003CA25I-I6T1U |
| 2.6 V ± 1.0% | S-1003CA26I-M5T1U | S-1003CA26I-I6T1U |
| 2.7 V ± 1.0% | S-1003CA27I-M5T1U | S-1003CA27I-I6T1U |
| 2.8 V ± 1.0% | S-1003CA28I-M5T1U | S-1003CA28I-I6T1U |
| 2.9 V ± 1.0% | S-1003CA29I-M5T1U | S-1003CA29I-I6T1U |
| 3.0 V ± 1.0% | S-1003CA30I-M5T1U | S-1003CA30I-I6T1U |
| 3.1 V ± 1.0% | S-1003CA31I-M5T1U | S-1003CA31I-I6T1U |
| 3.2 V ± 1.0% | S-1003CA32I-M5T1U | S-1003CA32I-I6T1U |
| 3.3 V ± 1.0% | S-1003CA33I-M5T1U | S-1003CA33I-I6T1U |
| 3.4 V ± 1.0% | S-1003CA34I-M5T1U | S-1003CA34I-I6T1U |
| 3.5 V ± 1.0% | S-1003CA35I-M5T1U | S-1003CA35I-I6T1U |
| 3.6 V ± 1.0% | S-1003CA36I-M5T1U | S-1003CA36I-I6T1U |
| 3.7 V ± 1.0% | S-1003CA37I-M5T1U | S-1003CA37I-I6T1U |
| 3.8 V ± 1.0% | S-1003CA38I-M5T1U | S-1003CA38I-I6T1U |
| 3.9 V ± 1.0% | S-1003CA39I-M5T1U | S-1003CA39I-I6T1U |
| 4.0 V ± 1.0% | S-1003CA40I-M5T1U | S-1003CA40I-I6T1U |
| 4.1 V ± 1.0% | S-1003CA41I-M5T1U | S-1003CA41I-I6T1U |
| 4.2 V ± 1.0% | S-1003CA42I-M5T1U | S-1003CA42I-I6T1U |
| 4.3 V ± 1.0% | S-1003CA43I-M5T1U | S-1003CA43I-I6T1U |
| 4.4 V ± 1.0% | S-1003CA44I-M5T1U | S-1003CA44I-I6T1U |
| 4.5 V ± 1.0% | S-1003CA45I-M5T1U | S-1003CA45I-I6T1U |
| 4.6 V ± 1.0% | S-1003CA46I-M5T1U | S-1003CA46I-I6T1U |
| 4.7 V ± 1.0% | S-1003CA47I-M5T1U | S-1003CA47I-I6T1U |
| 4.8 V ± 1.0% | S-1003CA48I-M5T1U | S-1003CA48I-I6T1U |
| 4.9 V ± 1.0% | S-1003CA49I-M5T1U | S-1003CA49I-I6T1U |
| 5.0 V ± 1.0% | S-1003CA50I-M5T1U | S-1003CA50I-I6T1U |

### 4. 4 S-1003 Series CB type

Output form: CMOS output (Active "L")
MR pin logic: Active "H"

**Table 6**

| Detection Voltage | SOT-23-5 | SNT-6A |
|---|---|---|
| 1.2 V ± 22 mV | S-1003CB12I-M5T1U | S-1003CB12I-I6T1U |
| 1.3 V ± 22 mV | S-1003CB13I-M5T1U | S-1003CB13I-I6T1U |
| 1.4 V ± 22 mV | S-1003CB14I-M5T1U | S-1003CB14I-I6T1U |
| 1.5 V ± 22 mV | S-1003CB15I-M5T1U | S-1003CB15I-I6T1U |
| 1.6 V ± 22 mV | S-1003CB16I-M5T1U | S-1003CB16I-I6T1U |
| 1.7 V ± 22 mV | S-1003CB17I-M5T1U | S-1003CB17I-I6T1U |
| 1.8 V ± 22 mV | S-1003CB18I-M5T1U | S-1003CB18I-I6T1U |
| 1.9 V ± 22 mV | S-1003CB19I-M5T1U | S-1003CB19I-I6T1U |
| 2.0 V ± 22 mV | S-1003CB20I-M5T1U | S-1003CB20I-I6T1U |
| 2.1 V ± 22 mV | S-1003CB21I-M5T1U | S-1003CB21I-I6T1U |
| 2.2 V ± 1.0% | S-1003CB22I-M5T1U | S-1003CB22I-I6T1U |
| 2.3 V ± 1.0% | S-1003CB23I-M5T1U | S-1003CB23I-I6T1U |
| 2.4 V ± 1.0% | S-1003CB24I-M5T1U | S-1003CB24I-I6T1U |
| 2.5 V ± 1.0% | S-1003CB25I-M5T1U | S-1003CB25I-I6T1U |
| 2.6 V ± 1.0% | S-1003CB26I-M5T1U | S-1003CB26I-I6T1U |
| 2.7 V ± 1.0% | S-1003CB27I-M5T1U | S-1003CB27I-I6T1U |
| 2.8 V ± 1.0% | S-1003CB28I-M5T1U | S-1003CB28I-I6T1U |
| 2.9 V ± 1.0% | S-1003CB29I-M5T1U | S-1003CB29I-I6T1U |
| 3.0 V ± 1.0% | S-1003CB30I-M5T1U | S-1003CB30I-I6T1U |
| 3.1 V ± 1.0% | S-1003CB31I-M5T1U | S-1003CB31I-I6T1U |
| 3.2 V ± 1.0% | S-1003CB32I-M5T1U | S-1003CB32I-I6T1U |
| 3.3 V ± 1.0% | S-1003CB33I-M5T1U | S-1003CB33I-I6T1U |
| 3.4 V ± 1.0% | S-1003CB34I-M5T1U | S-1003CB34I-I6T1U |
| 3.5 V ± 1.0% | S-1003CB35I-M5T1U | S-1003CB35I-I6T1U |
| 3.6 V ± 1.0% | S-1003CB36I-M5T1U | S-1003CB36I-I6T1U |
| 3.7 V ± 1.0% | S-1003CB37I-M5T1U | S-1003CB37I-I6T1U |
| 3.8 V ± 1.0% | S-1003CB38I-M5T1U | S-1003CB38I-I6T1U |
| 3.9 V ± 1.0% | S-1003CB39I-M5T1U | S-1003CB39I-I6T1U |
| 4.0 V ± 1.0% | S-1003CB40I-M5T1U | S-1003CB40I-I6T1U |
| 4.1 V ± 1.0% | S-1003CB41I-M5T1U | S-1003CB41I-I6T1U |
| 4.2 V ± 1.0% | S-1003CB42I-M5T1U | S-1003CB42I-I6T1U |
| 4.3 V ± 1.0% | S-1003CB43I-M5T1U | S-1003CB43I-I6T1U |
| 4.4 V ± 1.0% | S-1003CB44I-M5T1U | S-1003CB44I-I6T1U |
| 4.5 V ± 1.0% | S-1003CB45I-M5T1U | S-1003CB45I-I6T1U |
| 4.6 V ± 1.0% | S-1003CB46I-M5T1U | S-1003CB46I-I6T1U |
| 4.7 V ± 1.0% | S-1003CB47I-M5T1U | S-1003CB47I-I6T1U |
| 4.8 V ± 1.0% | S-1003CB48I-M5T1U | S-1003CB48I-I6T1U |
| 4.9 V ± 1.0% | S-1003CB49I-M5T1U | S-1003CB49I-I6T1U |
| 5.0 V ± 1.0% | S-1003CB50I-M5T1U | S-1003CB50I-I6T1U |

## ■ Pin Configurations

### 1. SOT-23-5

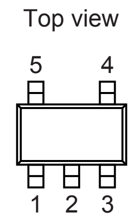



**Figure 5**

**Table 7**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | CD | Connection pin for delay capacitor |
| 2 | VSS | GND pin |
| 3 | MR | Manual reset pin |
| 4 | OUT | Voltage detection output pin |
| 5 | VDD | Voltage input pin |

### 2. SNT-6A

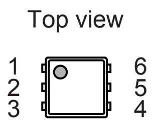



**Figure 6**

**Table 8**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | CD | Connection pin for delay capacitor |
| 2 | VDD | Voltage input pin |
| 3 | OUT | Voltage detection output pin |
| 4 | MR | Manual reset pin |
| 5 | NC[*1] | No connection |
| 6 | VSS | GND pin |

***1.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

## ■ Absolute Maximum Ratings

**Table 9**

(Ta = +25°C unless otherwise specified)

| Item | | Symbol | Absolute Maximum Rating | Unit |
|---|---|---|---|---|
| Power supply voltage | | $V_{DD} - V_{SS}$ | 12.0 | V |
| CD pin input voltage | | $V_{CD}$ | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |
| MR pin input voltage | | $V_{MR}$ | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |
| Output voltage | Nch open-drain output product | $V_{OUT}$ | $V_{SS} - 0.3$ to 12.0 | V |
| | CMOS output product | | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V |
| Output current | | $I_{OUT}$ | 50 | mA |
| Power dissipation | SOT-23-5 | $P_D$ | 600*1 | mW |
| | SNT-6A | | 400*1 | mW |
| Operation ambient temperature | | $T_{opr}$ | −40 to +85 | °C |
| Storage temperature | | $T_{stg}$ | −40 to +125 | °C |

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Name: JEDEC STANDARD51-7

**Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

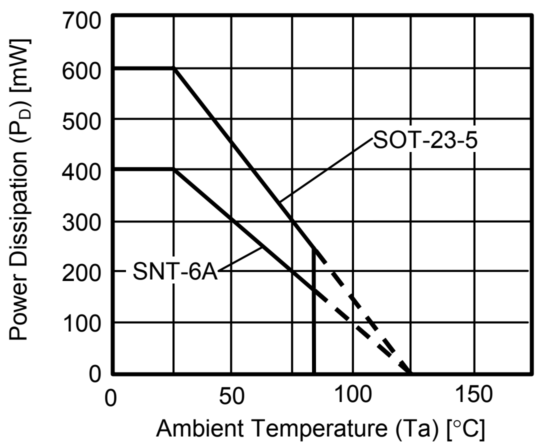



**Figure 7 Power Dissipation of Package (When Mounted on Board)**

## ■ Electrical Characteristics

### 1. Nch open-drain output product

**Table 10**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Detection voltage*1 | $-V_{DET}$ | $1.2\ V \le -V_{DET} < 2.2\ V$ | | $-V_{DET(S)} - 0.022$ | $-V_{DET(S)}$ | $-V_{DET(S)} + 0.022$ | V | 1 |
| | | $2.2\ V \le -V_{DET} \le 5.0\ V$ | | $-V_{DET(S)} \times 0.99$ | $-V_{DET(S)}$ | $-V_{DET(S)} \times 1.01$ | V | 1 |
| Hysteresis width | $V_{HYS}$ | – | | $-V_{DET} \times 0.03$ | $-V_{DET} \times 0.05$ | $-V_{DET} \times 0.07$ | V | 1 |
| Current consumption | $I_{SS}$ | $V_{DD} = -V_{DET(S)} + 1.0\ V$ | | – | 0.50 | 0.90 | μA | 2 |
| Operation voltage | $V_{DD}$ | – | | 0.95 | – | 10.0 | V | 1 |
| Output current | $I_{OUT}$ | Output transistor<br>Nch<br>$V_{DS}$*2 = 0.5 V<br>MR pin active | $V_{DD} = 0.95\ V$ | 0.59 | 1.00 | – | mA | 3 |
| | | | $V_{DD} = 1.2\ V$ | 0.73 | 1.33 | – | mA | 3 |
| | | | $V_{DD} = 2.4\ V$ | 1.47 | 2.39 | – | mA | 3 |
| | | | $V_{DD} = 4.8\ V$ | 1.86 | 2.50 | – | mA | 3 |
| Leakage current | $I_{LEAK}$ | Output transistor<br>Nch<br>$V_{DD} = 10.0\ V$, $V_{OUT} = 10.0\ V$<br>MR pin non-active | | – | – | 0.08 | μA | 3 |
| Delay time*3 | $t_D$ | $C_D = 4.7\ nF$ | | 8.5 | 10.0 | 11.5 | ms | 4 |
| Detection voltage temperature coefficient*4 | $\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$ | Ta = −40°C to +85°C | | – | ±100 | ±350 | ppm/°C | 1 |
| MR pin input voltage "H" | $V_{MRH}$ | NA type<br>(MR pin logic active "L") | | $V_{DD} - 0.3$ | – | – | V | 6 |
| | | NB type<br>(MR pin logic active "H") | | 1.2 | – | – | V | 6 |
| MR pin input voltage "L" | $V_{MRL}$ | NA type<br>(MR pin logic active "L") | | – | – | $V_{DD} - 1.2$ | V | 6 |
| | | NB type<br>(MR pin logic active "H") | | – | – | 0.3 | V | 6 |
| MR pin input resistance | $R_{MR}$ | – | | 0.5 | 1.0 | 1.6 | MΩ | 6 |

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (the center value of the detection voltage range in **Table 3** or **Table 4**.)

***2.** $V_{DS}$: Drain-to-source voltage of the output transistor

***3.** The time period from when the pulse voltage of 0.95 V → $-V_{DET(S)} + 1.0$ V is applied to the VDD pin to when $V_{OUT}$ reaches $V_{DD} \times 0.9$, after the output pin is pulled up to $V_{DD}$ by the resistance of 100 kΩ.

***4.** The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta}\ [mV/°C]^{*1} = -V_{DET(S)}\,(typ.)[V]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}\ [ppm/°C]^{*3} \div 1000$$

***1.** Temperature change of the detection voltage
***2.** Set detection voltage
***3.** Detection voltage temperature coefficient

### 2. CMOS output product

**Table 11**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|---|
| Detection voltage*1 | $-V_{DET}$ | $1.2\ V \le -V_{DET} < 2.2\ V$ | | $-V_{DET(S)} - 0.022$ | $-V_{DET(S)}$ | $-V_{DET(S)} + 0.022$ | V | 1 |
| | | $2.2\ V \le -V_{DET} \le 5.0\ V$ | | $-V_{DET(S)} \times 0.99$ | $-V_{DET(S)}$ | $-V_{DET(S)} \times 1.01$ | V | 1 |
| Hysteresis width | $V_{HYS}$ | – | | $-V_{DET} \times 0.03$ | $-V_{DET} \times 0.05$ | $-V_{DET} \times 0.07$ | V | 1 |
| Current consumption | $I_{SS}$ | $V_{DD} = -V_{DET(S)} + 1.0\ V$ | | – | 0.50 | 0.90 | μA | 2 |
| Operation voltage | $V_{DD}$ | – | | 0.95 | – | 10.0 | V | 1 |
| Output current | $I_{OUT}$ | Output transistor Nch $V_{DS}$*2 = 0.5 V MR pin active | $V_{DD}$ = 0.95 V | 0.59 | 1.00 | – | mA | 3 |
| | | | $V_{DD}$ = 1.2 V | 0.73 | 1.33 | – | mA | 3 |
| | | | $V_{DD}$ = 2.4 V | 1.47 | 2.39 | – | mA | 3 |
| | | | $V_{DD}$ = 4.8 V | 1.86 | 2.50 | – | mA | 3 |
| | | Output transistor Pch $V_{DS}$*2 = 0.5 V | $V_{DD}$ = 4.8 V S-1003Cx12 to 43 | 1.62 | 2.60 | – | mA | 5 |
| | | | $V_{DD}$ = 6.0 V | 1.78 | 2.86 | – | mA | 5 |
| Delay time*3 | $t_D$ | $C_D$ = 4.7 nF | | 8.5 | 10.0 | 11.5 | ms | 4 |
| Detection voltage temperature coefficient*4 | $\frac{\Delta -V_{DET}}{\Delta Ta \bullet -V_{DET}}$ | Ta = −40°C to +85°C | | – | ±100 | ±350 | ppm/°C | 1 |
| MR pin input voltage "H" | $V_{MRH}$ | CA type (MR pin logic active "L") | | $V_{DD} - 0.3$ | – | – | V | 6 |
| | | CB type (MR pin logic active "H") | | 1.2 | – | – | V | 6 |
| MR pin input voltage "L" | $V_{MRL}$ | CA type (MR pin logic active "L") | | – | – | $V_{DD} - 1.2$ | V | 6 |
| | | CB type (MR pin logic active "H") | | – | – | 0.3 | V | 6 |
| MR pin input resistance | $R_{MR}$ | – | | 0.5 | 1.0 | 1.6 | MΩ | 6 |

***1.** $-V_{DET}$: Actual detection voltage value, $-V_{DET(S)}$: Set detection voltage value (the center value of the detection voltage range in **Table 5** or **Table 6**.)

***2.** $V_{DS}$: Drain-to-source voltage of the output transistor

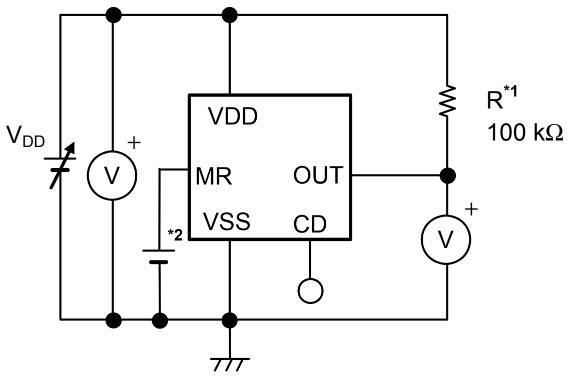
***3.** The time period from when the pulse voltage of 0.95 V → $-V_{DET(S)}$ + 1.0 V is applied to the VDD pin to when $V_{OUT}$ reaches $V_{DD} \times 0.9$.

***4.** The temperature change of the detection voltage [mV/°C] is calculated by using the following equation.

$$\frac{\Delta - V_{DET}}{\Delta Ta}\ [\text{mV/°C}]^{*1} = -V_{DET(S)}\ (\text{typ.})[\text{V}]^{*2} \times \frac{\Delta - V_{DET}}{\Delta Ta \bullet -V_{DET}}\ [\text{ppm/°C}]^{*3} \div 1000$$

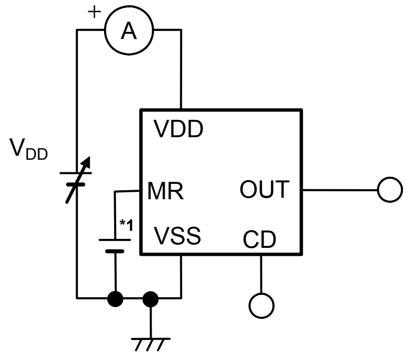
***1.** Temperature change of the detection voltage
***2.** Set detection voltage
***3.** Detection voltage temperature coefficient

## ■ Test Circuits



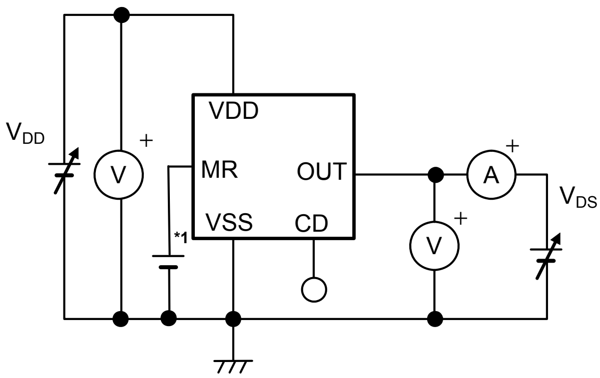

*1. R is unnecessary for CMOS output product.
*2. Set to $V_{DD}$ or GND (MR pin non-active).

**Figure 8 Test Circuit 1**



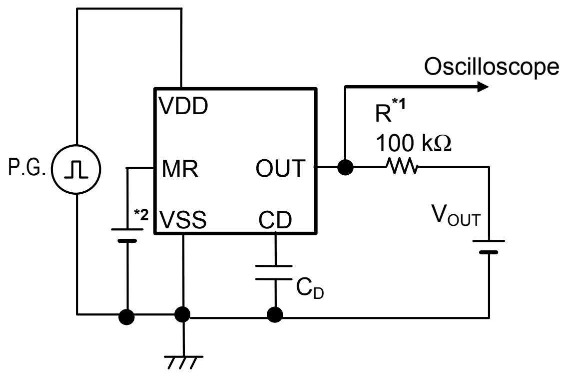

*1. Set to $V_{DD}$ or GND (MR pin non-active).

**Figure 9 Test Circuit 2**



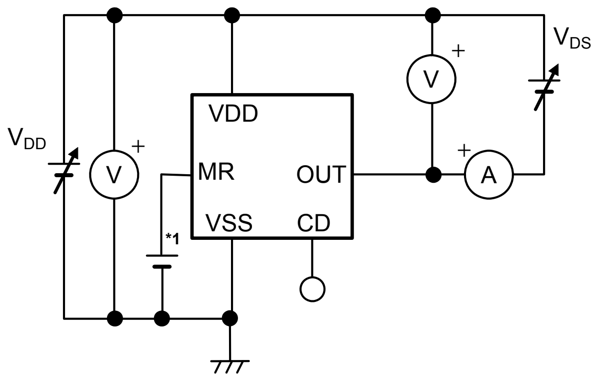

*1. Set to $V_{DD}$ or GND.

**Figure 10 Test Circuit 3**



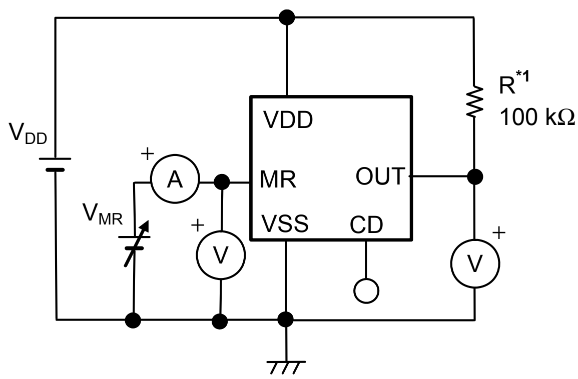

*1. R is unnecessary for CMOS output product.
*2. Set to $V_{DD}$ or GND (MR pin non-active).

**Figure 11 Test Circuit 4**




*1. Set to $V_{DD}$ or GND (MR pin non-active).

**Figure 12 Test Circuit 5**

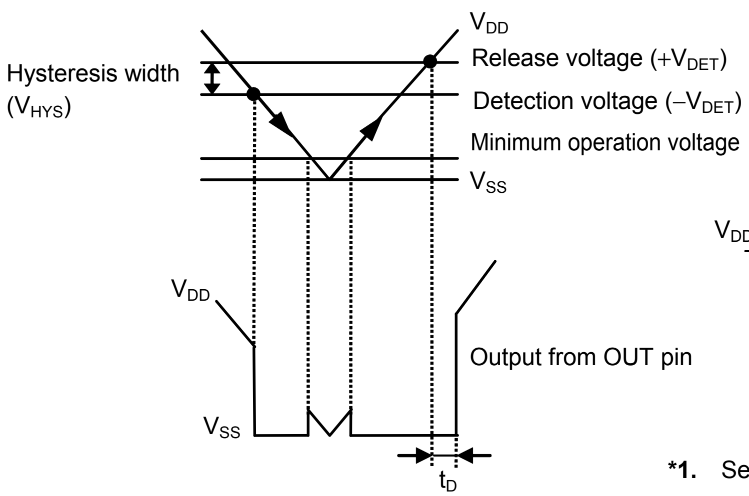


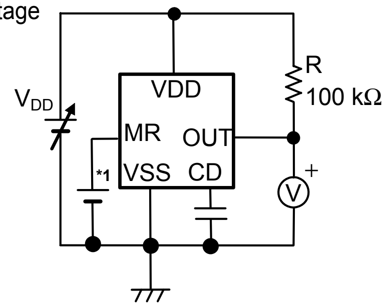

*1. R is unnecessary for CMOS output product.

**Figure 13 Test Circuit 6**

## ■ Timing Charts

### 1. Nch open-drain output product

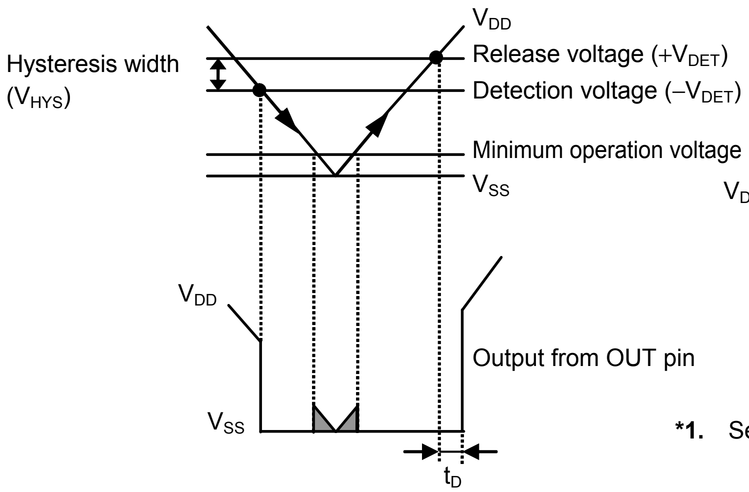


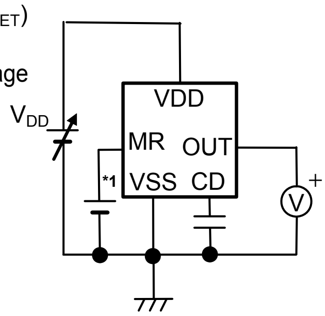




***1.** Set to $V_{DD}$ or GND (MR pin non-active).

**Figure 14**

### 2. CMOS output product




***1.** Set to $V_{DD}$ or GND (MR pin non-active).

**Remark** When $V_{DD}$ is the minimum operation voltage or less, the output voltage from the OUT pin is indefinite in the shaded area.

**Figure 15**

## ■ Operation

### 1. Basic operation: CMOS output (active "L") product

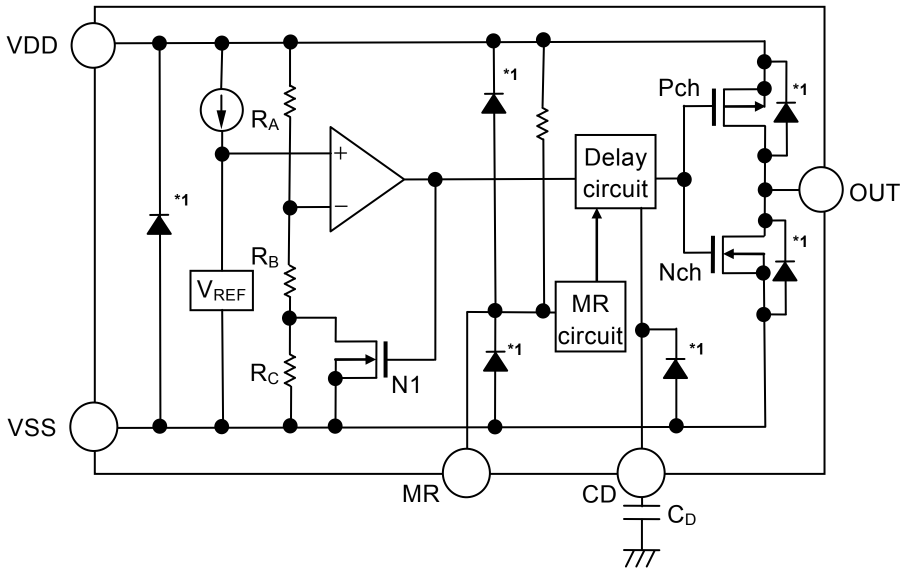
(1) When the power supply voltage ($V_{DD}$) is the release voltage ($+V_{DET}$) or more, the Nch transistor is OFF and the Pch transistor is ON to output $V_{DD}$ ("H"). Since the Nch transistor N1 in **Figure 16** is OFF, the comparator input voltage is $\frac{(R_B + R_C) \bullet V_{DD}}{R_A + R_B + R_C}$.

(2) Although $V_{DD}$ decreases to $+V_{DET}$ or less, $V_{DD}$ is output when $V_{DD}$ is higher than the detection voltage ($-V_{DET}$). When $V_{DD}$ decreases to $-V_{DET}$ or less (point A in **Figure 17**), the Nch transistor is ON and the Pch transistor is OFF so that $V_{SS}$ ("L") is output. At this time, the Nch transistor N1 in **Figure 16** is turned on, and the input voltage to the comparator is $\frac{R_B \bullet V_{DD}}{R_A + R_B}$.

(3) The output is indefinite by decreasing $V_{DD}$ to the IC's minimum operation voltage or less. If the output is pulled up, it will be $V_{DD}$.

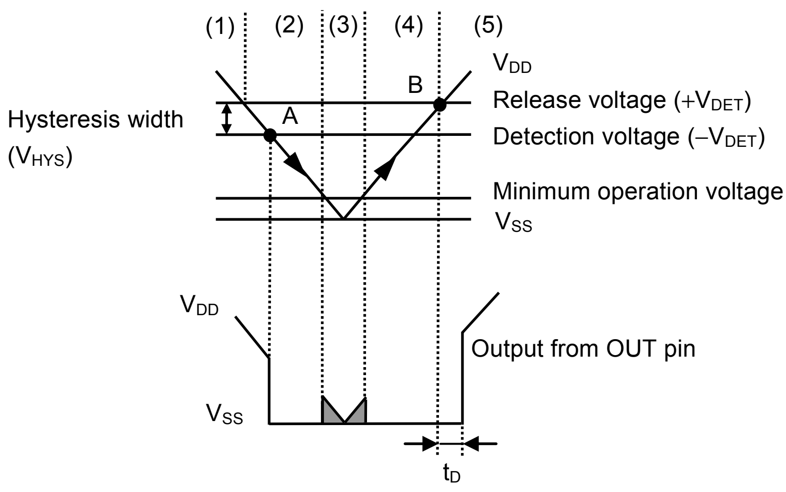
(4) $V_{SS}$ is output by increasing $V_{DD}$ to the minimum operation voltage or more. Although $V_{DD}$ exceeds $-V_{DET}$ and $V_{DD}$ is less than $+V_{DET}$, the output is $V_{SS}$.

(5) When increasing $V_{DD}$ to $+V_{DET}$ or more (point B in **Figure 17**), the Nch transistor is OFF and the Pch transistor is ON so that $V_{DD}$ is output. At this time, $V_{DD}$ is output from the OUT pin after the passage of the delay time ($t_D$).




***1.** Parasitic diode

**Figure 16 Operation 1**




**Remark** When $V_{DD}$ is the minimum operation voltage or less, the output voltage from the OUT pin is indefinite in the shaded area.

**Figure 17 Operation 2**

## 2. Manual reset function

The OUT pin voltage can be changed to detection status forcibly by the MR pin input voltage ($V_{MR}$).
When not using the manual reset function, set $V_{MR} = V_{DD}$ in the S-1003 Series xA type, and $V_{MR} = V_{SS}$ in the S-1003 Series xB type.

**Caution Perform thorough evaluation in the actual application when using the MR pin in open. Due to the parasitic capacitance of the MR pin, the manual reset function may malfunction when the power supply fluctuates.**

### 2. 1 S-1003 Series xA type (MR pin logic active "L")

(1) MR pin = "L"
When the VDD pin voltage is the release voltage ($+V_{DET}$) or more, the OUT pin changes to the detection status from the release status immediately if a voltage of the MR pin input voltage "L" ($V_{MRL}$) or less is applied to the MR pin.

(2) MR pin = "H"
If a voltage of the MR pin input voltage "H" ($V_{MRH}$) or more is applied to the MR pin, output from the OUT pin is determined to be "H" or "L" depending on the VDD pin voltage.
After the passage of the delay time ($t_D$), the OUT pin changes to the release status from the detection status.

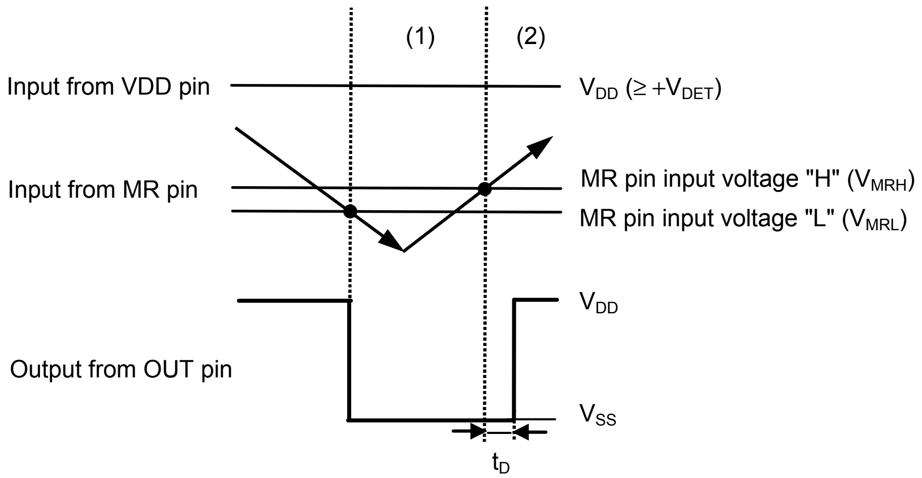
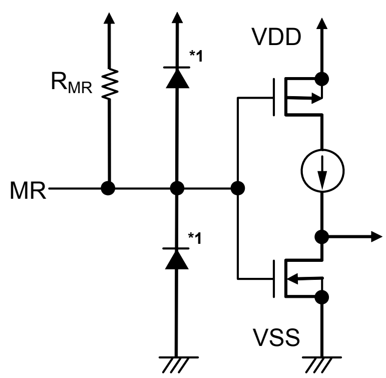



**Figure 18 Timing Chart of MR Pin Logic Active "L"**

**Remark** Since the MR pin is pulled up to the VDD pin internally, output from the OUT pin is determined to be "H" or "L" in the floating status depending on the VDD pin voltage (Refer to **Figure 19**).




***1.** Parasitic diode

**Figure 19**

### 2. 2 S-1003 Series xB type (MR pin logic active "H")

(1) MR pin = "H"
When the VDD pin voltage is the release voltage ($+V_{DET}$) or more, the OUT pin changes to the detection status from the release status immediately if a voltage of the MR pin input voltage "H" ($V_{MRH}$) or more is applied to the MR pin.

(2) MR pin = "L"
If a voltage of the MR pin input voltage "L" ($V_{MRL}$) or less is applied to the MR pin, output from the OUT pin is determined to be "H" or "L" depending on the VDD pin voltage.
After the passage of the delay time ($t_D$), the OUT pin changes to the release status from the detection status.

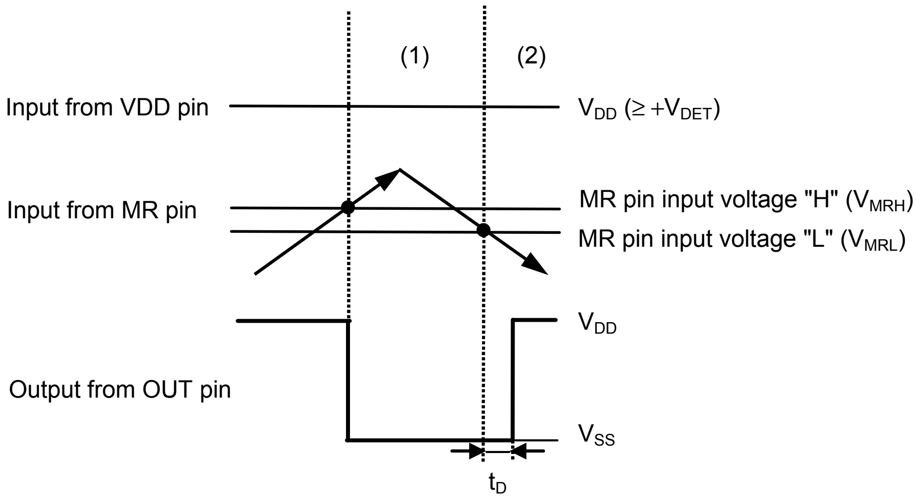
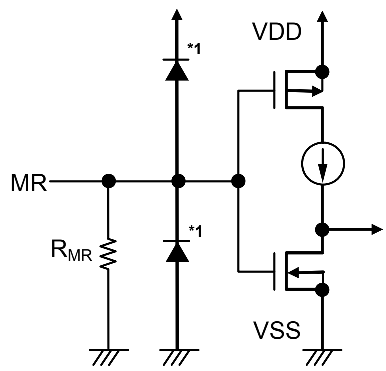



**Figure 20 Timing Chart of MR Pin Logic Active "H"**

**Remark** Since the MR pin is pulled down to the VSS pin internally, output from the OUT pin is determined to be "H" or "L" in the floating status depending on the VDD pin voltage (Refer to **Figure 21**).




***1.** Parasitic diode

**Figure 21**

### 2. 3 Cautions of manual reset function

#### 2. 3. 1 Slew rate when switching manual reset function

Although there is a hysteresis width between the MR pin input voltage "L" ($V_{MRL}$) and the MR pin input voltage "H" ($V_{MRH}$), note that the IC may malfunction if the slew rate (Refer to **Figure 22**, **Figure 23**) is low when the MR pin voltage is changed.
The slew rate is calculated by using the following equation.

$$\text{Slew rate} = \frac{V_{MRH} - V_{MRL}}{\Delta t}$$

**(1) When MR pin logic is active "L"**

The OUT pin voltage may oscillate if the parasitic resistance ($R_P$) between the power supply and the VDD pin is high.

- In case of $R_P \geq 8$ kΩ: Connect a capacitor of 1 nF or more between the VDD pin and the VSS pin.
- In case of 5 kΩ $\leq R_P <$ 8 kΩ: Capacitors are unnecessary if the slew rate is 100 V/s or higher.
- In case of $R_P <$ 5 kΩ: Capacitors are unnecessary if the slew rate is 1 V/s or higher.

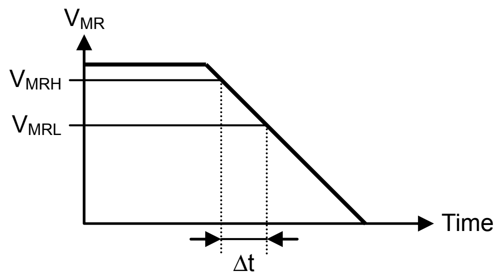



**Figure 22**

**(2) When MR pin logic is active "H"**

Connect a capacitor of 100 pF or more to the CD pin, and set the slew rate 20 V/s or higher.

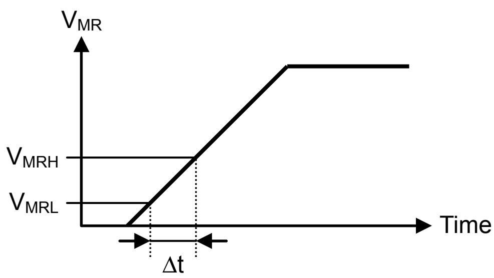



**Figure 23**

### 2. 4 When connecting resistance ($R_A$) between power supply voltage ($V_{DD}$) and VDD pin

When the MR pin voltage ($V_{MR}$) is an intermediate voltage (especially $V_{MRL} < V_{MR} < V_{MRH}$), the current consumption increases by 25 μA max. A voltage drop occurs since this current flows through $R_A$. If the VDD pin voltage ($V_{IN}$) becomes the detection voltage ($-V_{DET}$) or less for that reason, the OUT pin changes to the detection status, and the detection status or the release status are not controlled by $V_{MR}$. The OUT pin may not be able to change to the release status unless $V_{DD}$ is raised (Refer to **Figure 24**).

**(1) When MR pin logic is active "L"**

In case of $V_{IN} > V_{MR}$, a current also flows through the MR pin input resistance ($R_{MR}$). For example, when $V_{IN}$ = 10 V, $V_{MR}$ = 1 V, $R_{MR}$ = 0.5 MΩ (min.), a current of 18 μA flows from the VDD pin to the MR pin. Therefore, set $R_A$ so as to satisfy the following equation.

$R_A \leq (V_{DD} - (-V_{DET})) / (25\ \mu A + \text{MR pin current})$

**(2) When MR pin logic is active "H"**

Set $R_A$ so as to satisfy the following equation.

$R_A \leq (V_{DD} - (-V_{DET})) / 25\ \mu A$

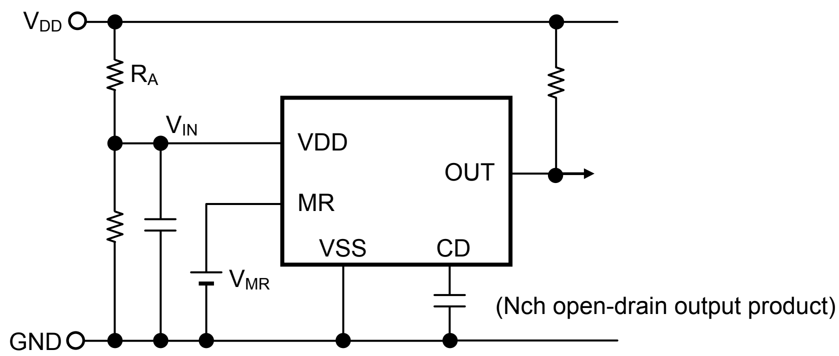



**Figure 24**

### 3. Delay circuit

The delay circuit delays the output signal to the OUT pin from the time at which the power supply voltage ($V_{DD}$) exceeds the release voltage ($+V_{DET}$) when $V_{DD}$ is turned on. The output signal is not delayed when $V_{DD}$ decreases to the detection voltage ($-V_{DET}$) or less (refer to "**Figure 17 Operation 2**").
The delay time ($t_D$) is determined by the time constant of the built-in constant current (approx. 100 nA) and the attached delay capacitor ($C_D$), or the delay time ($t_{D0}$) when the CD pin is open, and calculated from the following equation. When the $C_D$ value is sufficiently large, the $t_{D0}$ value can be disregarded.

$$t_D\ [\text{ms}] = \text{Delay coefficient} \times C_D\ [\text{nF}] + t_{D0}\ [\text{ms}]$$

**Table 12 Delay Coefficient**

| Operation Temperature | Delay Coefficient | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| Ta = +85°C | 1.60 | 1.89 | 2.13 |
| Ta = +25°C | 1.78 | 2.05 | 2.30 |
| Ta = −40°C | 2.01 | 2.31 | 2.71 |

**Table 13 Delay Time**

| Operation Temperature | Delay Time ($t_{D0}$) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| Ta = −40°C to +85°C | 0.021 ms | 0.044 ms | 0.147 ms |

**Caution 1. When the CD pin is open, a double pulse shown in Figure 25 may appear at release.**
**To avoid the double pulse, attach a 100 pF or larger capacitor to the CD pin. Do not apply voltage to the CD pin from the exterior.**

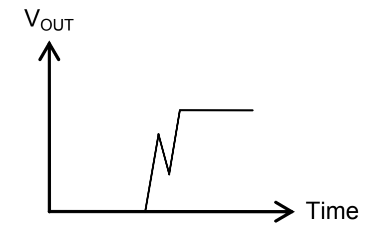



**Figure 25**

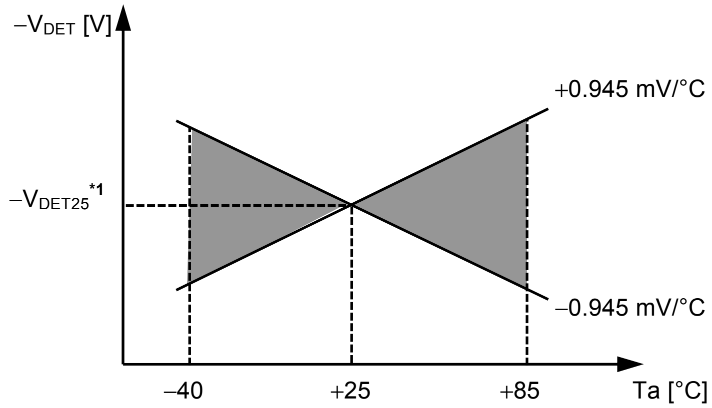
**2. Mounted board layout should be made in such a way that no current flows into or flows from the CD pin since the impedance of the CD pin is high, otherwise correct delay time cannot be provided.**

**3. There is no limit for the capacitance of $C_D$ as long as the leakage current of the capacitor can be ignored against the built-in constant current value. Leakage current causes deviation in delay time. When the leakage current is larger than the built-in constant current, no release takes place.**

## 4. Other characteristics

### 4. 1 Temperature characteristics of detection voltage

The shaded area in **Figure 26** shows the temperature characteristics of detection voltage in the operation temperature range.




***1.** $-V_{DET25}$ is an actual detection voltage value at Ta = +25°C.

**Figure 26 Temperature Characteristics of Detection Voltage (Example for $-V_{DET}$ = 2.7 V)**

### 4. 2 Temperature characteristics of release voltage

The temperature change $\frac{\Delta + V_{DET}}{\Delta Ta}$ of the release voltage is calculated by using the temperature change $\frac{\Delta - V_{DET}}{\Delta Ta}$ of the detection voltage as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

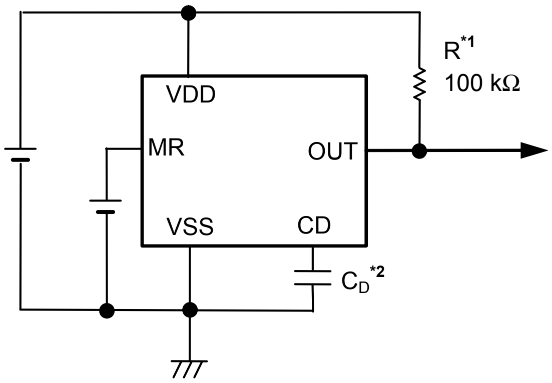
The temperature change of the release voltage and the detection voltage has the same sign consequently.

### 4. 3 Temperature characteristics of hysteresis voltage

The temperature change of the hysteresis voltage is expressed as $\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta}$ and is calculated as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} - \frac{\Delta - V_{DET}}{\Delta Ta} = \frac{V_{HYS}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

## ■ Standard Circuit




***1.** R is unnecessary for CMOS output product.
***2.** The delay capacitor ($C_D$) should be connected directly to the CD pin and the VSS pin.

**Figure 27**

**Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**

## ■ Explanation of Terms

### 1. Detection voltage ($-V_{DET}$)

The detection voltage is a voltage at which the output in **Figure 30** turns to "L". The detection voltage varies slightly among products of the same specification. The variation of detection voltage between the specified minimum ($-V_{DET}$ min.) and the maximum ($-V_{DET}$ max.) is called the detection voltage range (Refer to **Figure 28**).

Example: In the S-1003Cx15, the detection voltage is either one in the range of 1.478 V $\leq -V_{DET} \leq$ 1.522 V.
This means that some S-1003Cx15 have $-V_{DET}$ = 1.478 V and some have $-V_{DET}$ = 1.522 V.

### 2. Release voltage ($+V_{DET}$)

The release voltage is a voltage at which the output in **Figure 30** turns to "H". The release voltage varies slightly among products of the same specification. The variation of release voltage between the specified minimum ($+V_{DET}$ min.) and the maximum ($+V_{DET}$ max.) is called the release voltage range (Refer to **Figure 29**). The range is calculated from the actual detection voltage ($-V_{DET}$) of a product and is in the range of $-V_{DET} \times 1.03 \leq +V_{DET} \leq -V_{DET} \times 1.07$.

Example: For the S-1003Cx15, the release voltage is either one in the range of 1.522 V $\leq +V_{DET} \leq$ 1.629 V.
This means that some S-1003Cx15 have $+V_{DET}$ = 1.522 V and some have $+V_{DET}$ = 1.629 V.

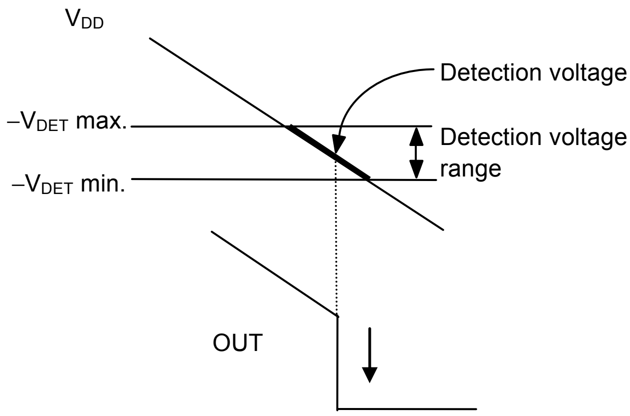



**Figure 28 Detection Voltage**

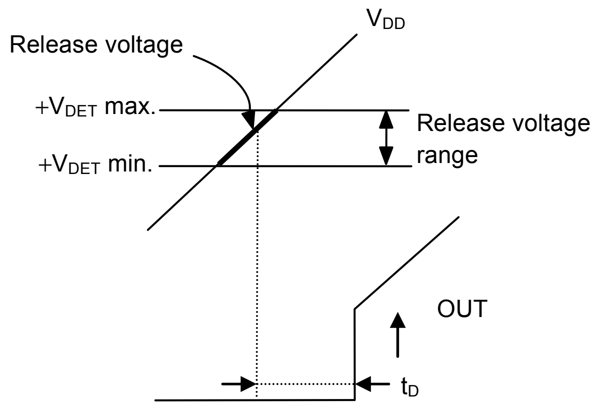
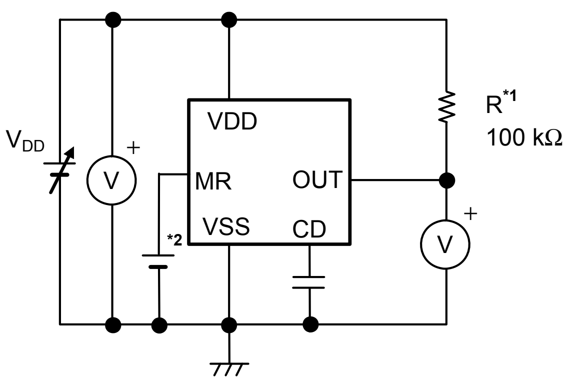



**Figure 29 Release Voltage**




***1.** R is unnecessary for CMOS output product.
***2.** Set to $V_{DD}$ or GND (MR pin non-active).

**Figure 30 Test Circuit of Detection Voltage and Release Voltage**

### 3. Hysteresis width ($V_{HYS}$)

The hysteresis width is the voltage difference between the detection voltage and the release voltage (the voltage at point B – the voltage at point A = $V_{HYS}$ in "**Figure 17 Operation 2**"). Setting the hysteresis width between the detection voltage and the release voltage, prevents malfunction caused by noise on the input voltage.

### 4. Delay time ($t_D$)

The delay time in the S-1003 Series is a period from the input voltage to the VDD pin exceeding the release voltage ($+V_{DET}$) until the output from the OUT pin inverts. The delay time changes according to the delay capacitor ($C_D$).

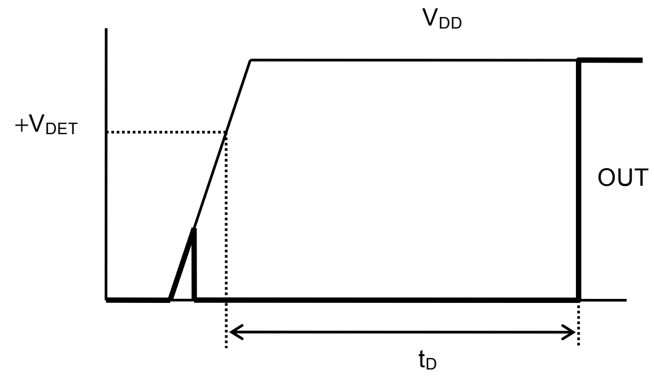



**Figure 31 Delay Time**

### 5. Feed-through current

Feed-through current is a current that flows instantaneously at the time of detection and release of a voltage detector. The feed-through current is large in CMOS output product, small in Nch open-drain output product.

### 6. Oscillation

In applications where a resistor is connected to the voltage detector input (**Figure 32**), taking a CMOS active "L" product for example, the feed-through current which is generated when the output goes from "L" to "H" (release) causes a voltage drop equal to [feed-through current] × [input resistance] across the resistor. When the input voltage drops below the detection voltage ($-V_{DET}$) as a result, the output voltage goes to "L". In this status, the feed-through current stops and its resultant voltage drop disappears, and the output goes from "L" to "H". The feed-through current is then generated again, a voltage drop appears, and repeating the process finally induces oscillation.

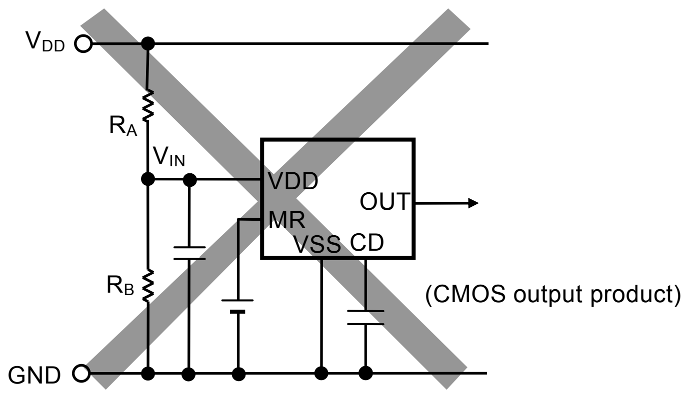



**Figure 32 Example for Bad Implementation Due to Detection Voltage Change**

## ■ Precautions

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- In CMOS output product of the S-1003 Series, the feed-through current flows at the detection and the release. If the input impedance is high, oscillation may occur due to the voltage drop by the feed-through current when releasing.

- In CMOS output product oscillation may occur when a pull-down resistor is used, and falling speed of the power supply voltage ($V_{DD}$) is slow near the detection voltage.

- When designing for mass production using an application circuit described herein, the product deviation and temperature characteristics of the external parts should be taken into consideration. SII Semiconductor Corporation shall not bear any responsibility for patent infringements related to products using the circuits described herein.

- SII Semiconductor Corporation claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

- As seen in **Figure 33**, when connecting an input resistance ($R_A$) in Nch open-drain output product of the S-1003 Series, $R_A$ should be 100 kΩ or less to prevent oscillation. Moreover, note that the hysteresis width may be larger as the following equation.

$$\text{Maximum hysteresis width} = V_{HYS} + R_A \bullet 20\ \mu A$$

- When using the manual reset function, refer to **"2. 4 When connecting resistance ($R_A$) between power supply voltage ($V_{DD}$) and VDD pin"** in **"■ Operation"** to set the constant.

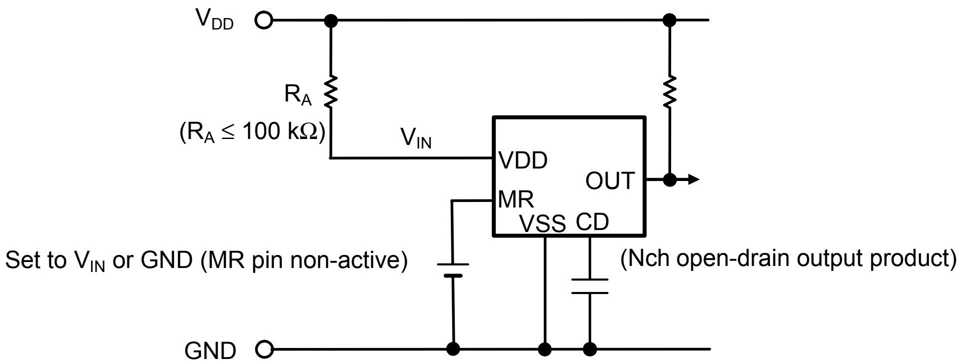



**Figure 33**

**Caution The above connection diagram and constant will not guarantee successful operation.
Perform thorough evaluation using the actual application to set the constant.**