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S-1410/1411 Series

105°C OPERATION, 3.8 μA CURRENT CONSUMPTION WATCHDOG TIMER WITH RESET FUNCTION

The S-1410/1411 Series is a watchdog timer developed using CMOS technology, which can operate with low current consumption of 3.8 μA typ. The reset function and the low voltage detection function are available.

■ Features

- Detection voltage: 2.0 V to 5.0 V, selectable in 0.1 V step
- Detection voltage accuracy: ±1.5%
- Input voltage: V_{DD} = 0.9 V to 6.0 V
- Hysteresis width: 5% typ.
- Current consumption: 3.8 μA typ.
- Reset time-out period: 14.5 ms typ. (C_{POR} = 2200 pF)
- Watchdog operation is switchable: Enable, Disable
- Watchdog operation voltage range: V_{DD} = 2.5 V to 6.0 V
- Watchdog mode switching function*1: Time-out mode, window mode
- Watchdog input edge is selectable: Rising edge, falling edge, both rising and falling edges
- Product type is selectable: S-1410 Series (Product with $\overline{W}$ / T pin (Output: $\overline{WDO}$ pin)) S-1411 Series (Product without $\overline{W}$ / T pin (Output: $\overline{RST}$ pin, $\overline{WDO}$ pin))
- Operation temperature range: Ta = −40°C to +105°C
- Lead-free (Sn 100%), halogen-free

***1.** The S-1411 Series is fixed to the window mode.

■ Application

- Power supply monitoring and system monitoring in microcontroller mounted apparatus

■ Packages

- TMSOP-8
- HSNT-8(2030)

■ Block Diagrams

1. S-1410 Series A / B / C Type

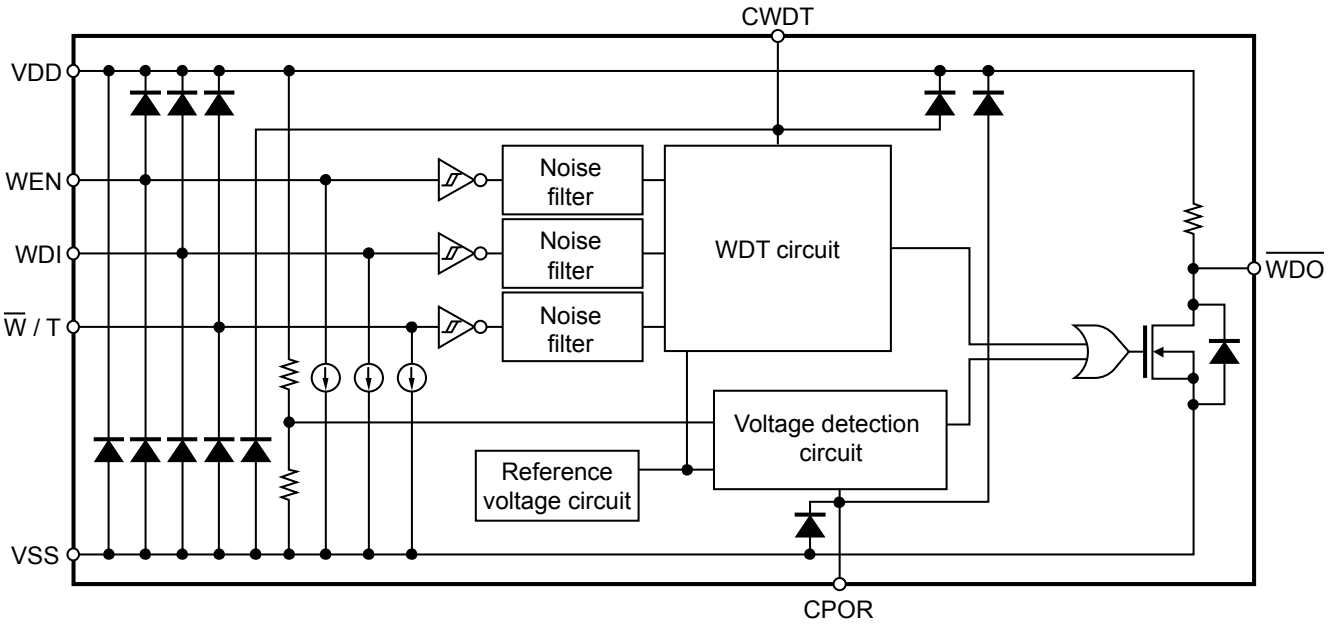


Figure 1

2. S-1410 Series D / E / F Type

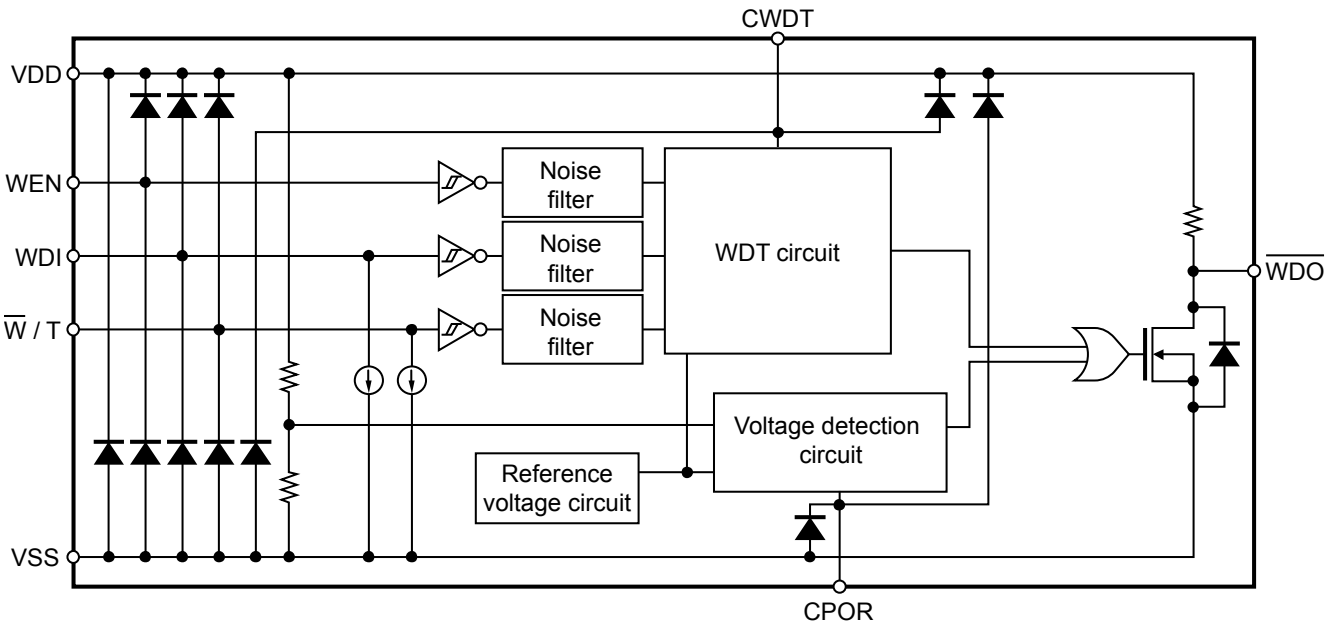


Figure 2

3. S-1410 Series G / H / I Type

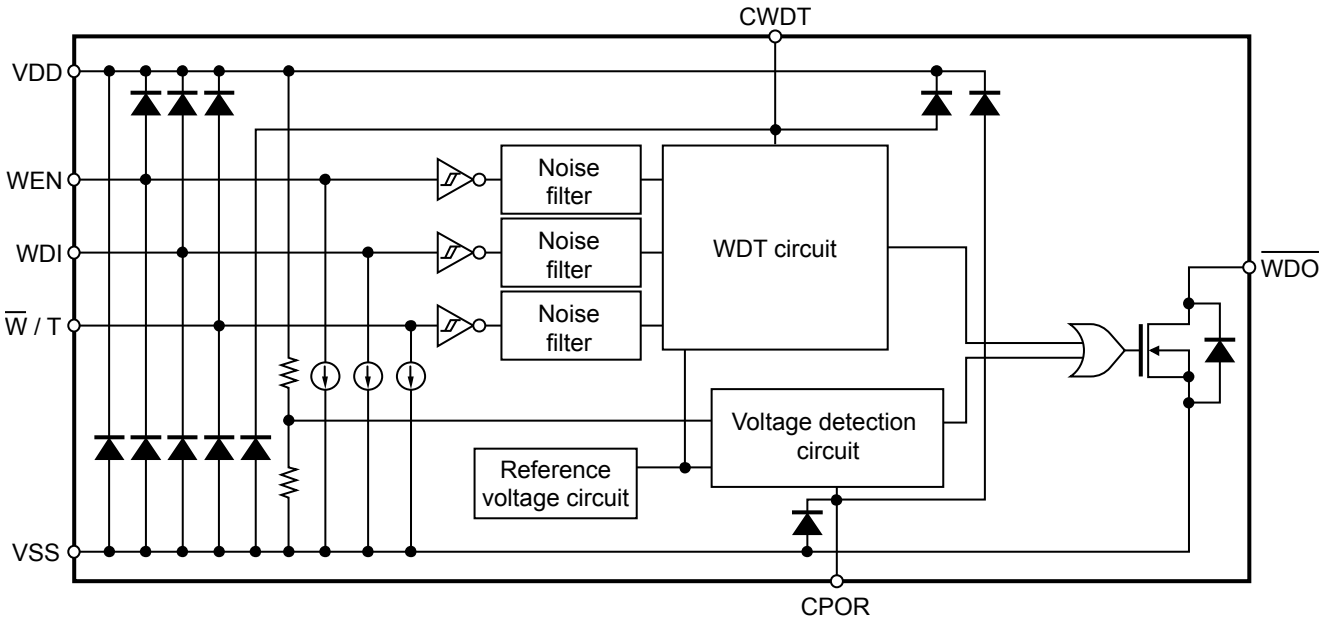


Figure 3

4. S-1410 Series J / K / L Type

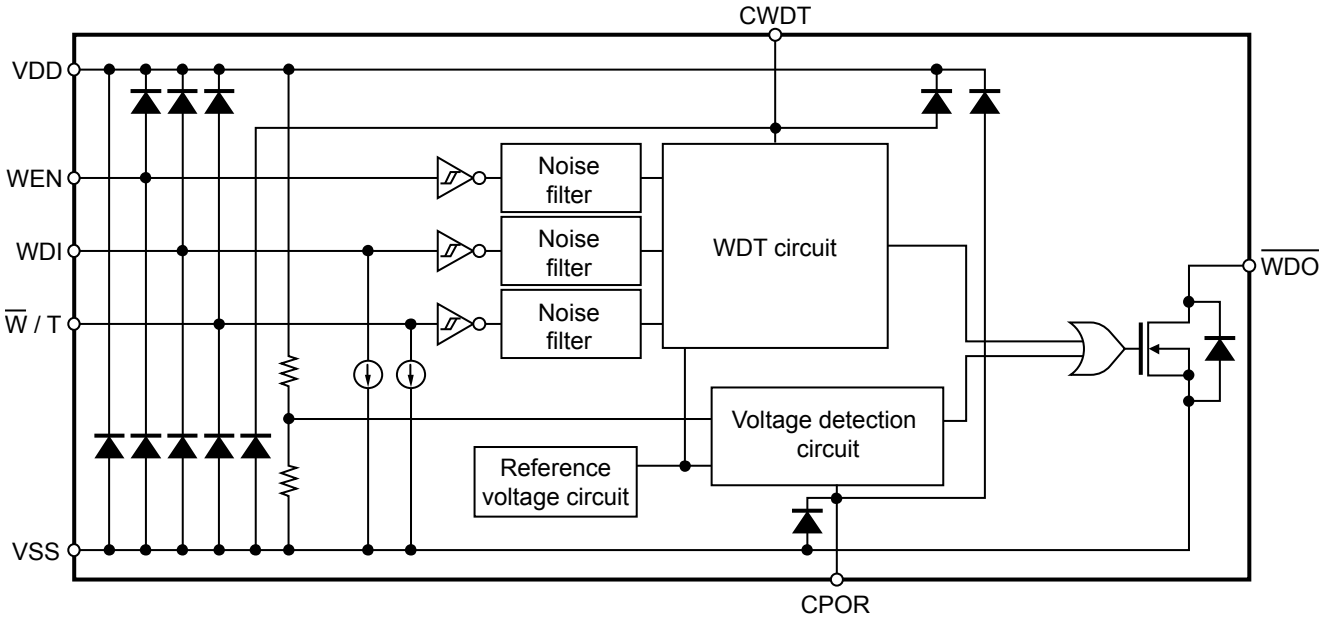


Figure 4

5. S-1411 Series A / B / C Type

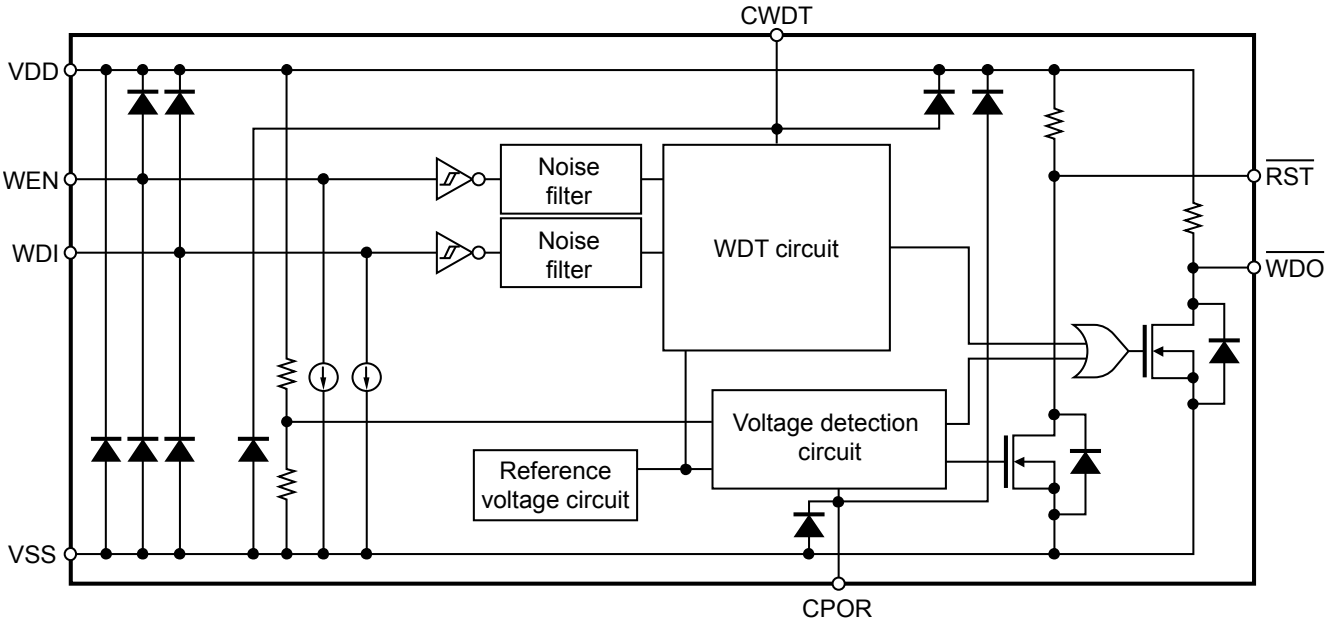


Figure 5

6. S-1411 Series D / E / F Type

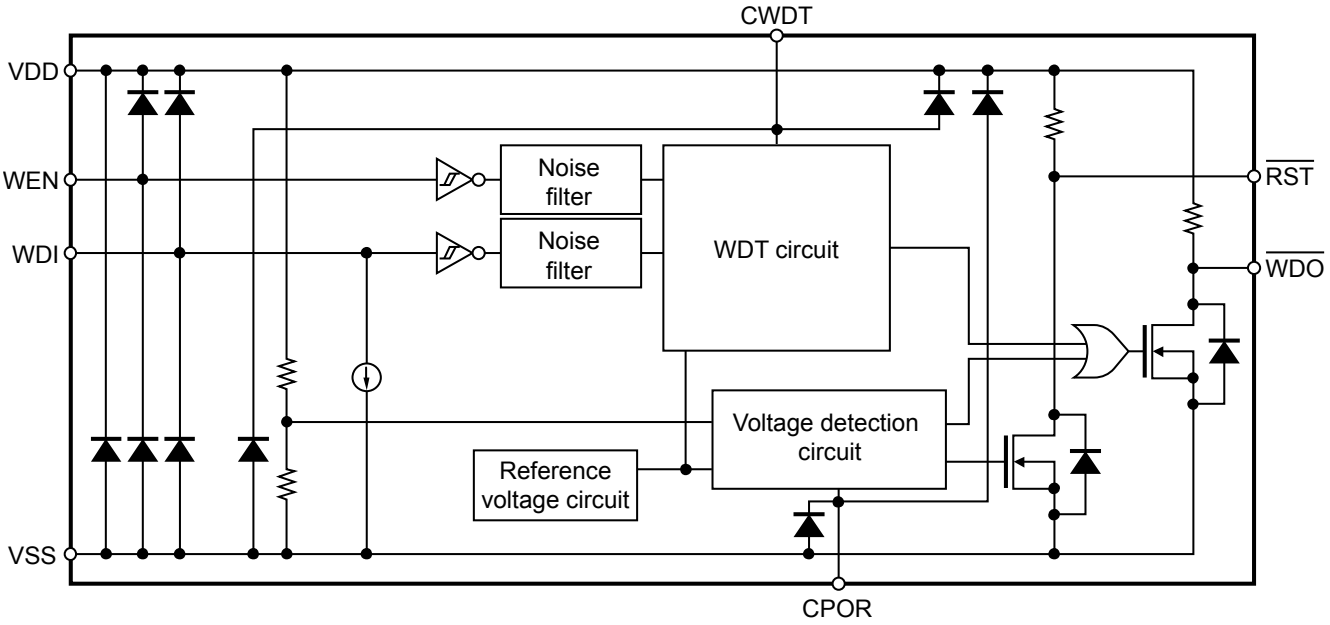


Figure 6

7. S-1411 Series G / H / I Type

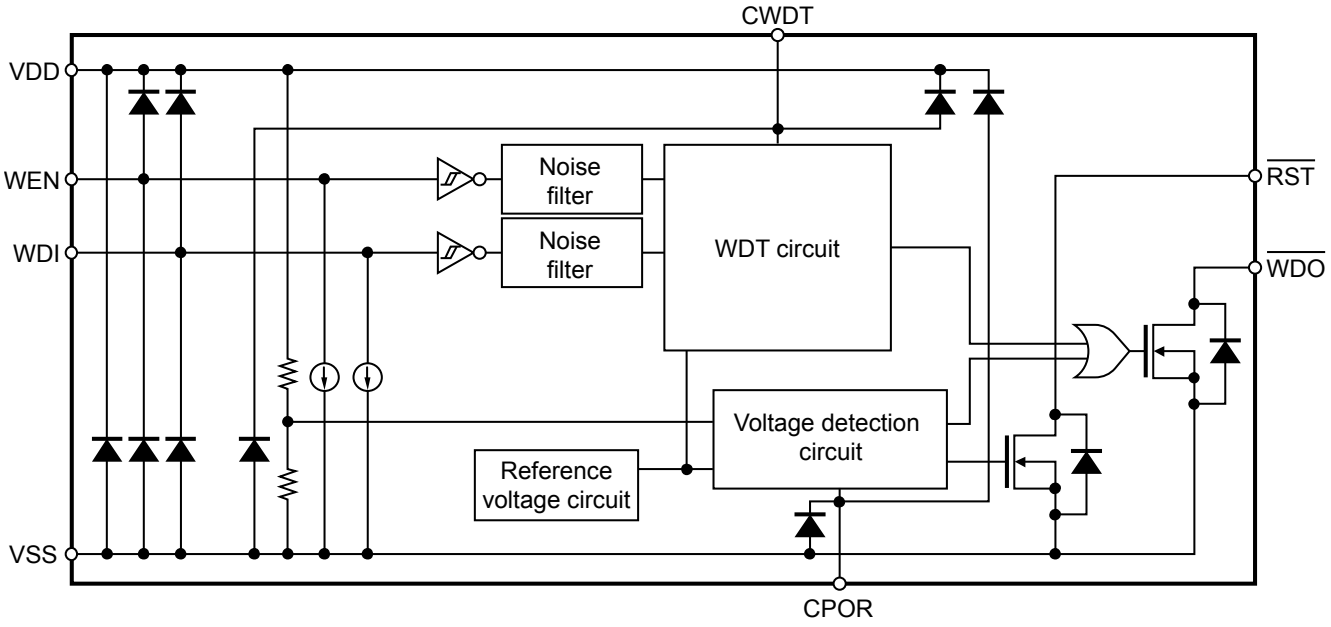


Figure 7

8. S-1411 Series J / K / L Type

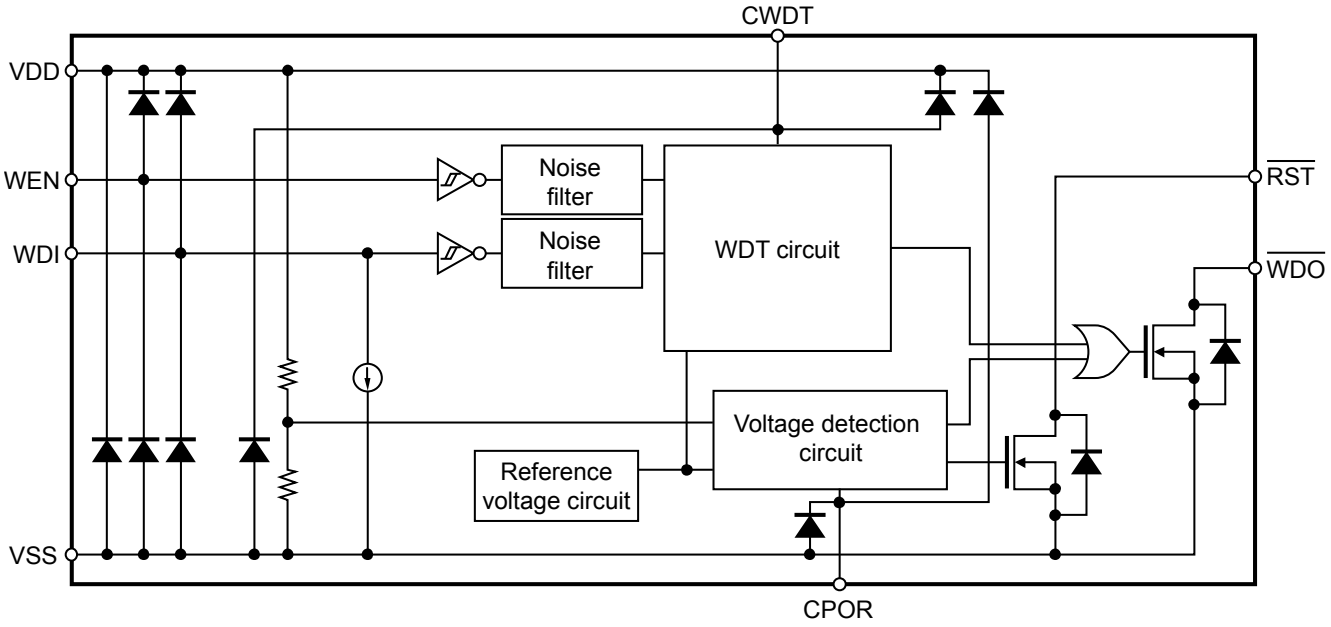


Figure 8

■ Product Name Structure

Users can select the product type, detection voltage, and package type for the S-1410/1411 Series. Refer to "**1. Product name**" regarding the contents of product name, "**2. Product type list**" regarding the product types, "**3. Packages**" regarding the package drawings.

1. Product name

S-141 x x xx - xxxx U 4

- Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- Package abbreviation and IC packing specifications*1
  - K8T2: TMSOP-8, Tape
  - A8T1: HSNT-8(2030), Tape
- Detection voltage
  - 20 to 50
  - (e.g., when the detection voltage is 2.0 V, it is expressed as 20.)
- Product type 1*2
  - A to L
- Product type 2*3
  - 0, 1

***1.** Refer to the tape drawing.

***2.** Refer to "**2. Product type list**".

***3.** 0: S-1410 Series (Product with $\overline{W}$ / T pin)
The $\overline{WDO}$ pin outputs the signals which are from the watchdog timer circuit and the voltage detection circuit.
1: S-1411 Series (Product without $\overline{W}$ / T pin)
The $\overline{WDO}$ pin outputs the signals which are from the watchdog timer circuit and the voltage detection circuit.
The $\overline{RST}$ pin outputs the signal which is from the voltage detection circuit.
The watchdog mode is fixed to the window mode.

2. Product type list

Table 1

Product Type	WEN Pin Logic	Constant Current Source Pull-down for WEN Pin	Input Edge	Output Pull-up Resistor
A	Active "H"	Available	Rising edge	Available
B	Active "H"	Available	Falling edge	Available
C	Active "H"	Available	Both rising and falling edges	Available
D	Active "L"	Unavailable	Rising edge	Available
E	Active "L"	Unavailable	Falling edge	Available
F	Active "L"	Unavailable	Both rising and falling edges	Available
G	Active "H"	Available	Rising edge	Unavailable
H	Active "H"	Available	Falling edge	Unavailable
I	Active "H"	Available	Both rising and falling edges	Unavailable
J	Active "L"	Unavailable	Rising edge	Unavailable
K	Active "L"	Unavailable	Falling edge	Unavailable
L	Active "L"	Unavailable	Both rising and falling edges	Unavailable

3. Packages

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	–
HSNT-8(2030)	PP008-A-P-SD	PP008-A-C-SD	PP008-A-R-SD	PP008-A-L-SD

■ Pin Configurations

1. TMSOP-8

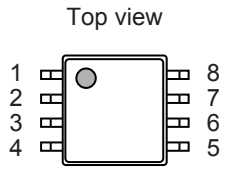


Figure 9

Table 3 S-1410 Series

Pin No.	Symbol	Description
1	$\overline{W}$ / T*1	Watchdog mode switching pin
2	CPOR	Reset time-out period adjustment pin
3	CWDT	Watchdog time adjustment pin
4	VSS	GND pin
5	WEN	Watchdog enable pin
6	$\overline{WDO}$	Watchdog output and reset output pin
7	WDI	Watchdog input pin
8	VDD	Voltage input pin

Table 4 S-1411 Series

Pin No.	Symbol	Description
1	$\overline{RST}$	Reset output pin
2	CPOR	Reset time-out period adjustment pin
3	CWDT	Watchdog time adjustment pin
4	VSS	GND pin
5	WEN	Watchdog enable pin
6	$\overline{WDO}$	Watchdog output pin
7	WDI	Watchdog input pin
8	VDD	Voltage input pin

***1.** $\overline{W}$ / T pin = "H": Time-out mode
$\overline{W}$ / T pin = "L": Window mode

2. HSNT-8(2030)

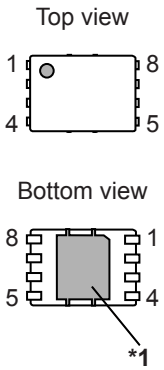


Figure 10

Table 5 S-1410 Series

Pin No.	Symbol	Description
1	$\overline{W}$ / T*2	Watchdog mode switching pin
2	CPOR	Reset time-out period adjustment pin
3	CWDT	Watchdog time adjustment pin
4	VSS	GND pin
5	WEN	Watchdog enable pin
6	$\overline{WDO}$	Watchdog output and reset output pin
7	WDI	Watchdog input pin
8	VDD	Voltage input pin

Table 6 S-1411 Series

Pin No.	Symbol	Description
1	$\overline{RST}$	Reset output pin
2	CPOR	Reset time-out period adjustment pin
3	CWDT	Watchdog time adjustment pin
4	VSS	GND pin
5	WEN	Watchdog enable pin
6	$\overline{WDO}$	Watchdog output pin
7	WDI	Watchdog input pin
8	VDD	Voltage input pin

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND.
However, do not use it as the function of electrode.

***2.** $\overline{W}$ / T pin = "H": Time-out mode
$\overline{W}$ / T pin = "L": Window mode

■ Pin Functions

Refer to "■ **Operations**" for details.

1. $\overline{W}$ / T pin (S-1410 Series only)

This is a pin to switch the watchdog mode.
The S-1410 Series changes to the time-out mode when the $\overline{W}$ / T pin is "H", and changes to the window mode when the $\overline{W}$ / T pin is "L". Switching the mode is prohibited during the operation.
The $\overline{W}$ / T pin is connected to a constant current source (0.3 μA typ.) and is pulled down internally.

1. 1 Time-out mode ($\overline{W}$ / T pin = "H")

The S-1410 Series detects an abnormality when not inputting an edge to the WDI pin during the watchdog time-out period (t_{WDU}). And then "L" is output from the $\overline{WDO}$ pin.

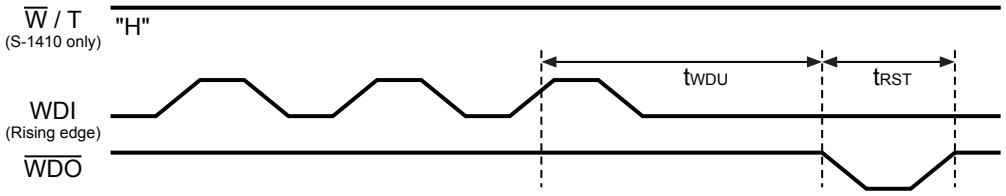


Figure 11 Abnormality Detection in Time-out Mode

1. 2 Window mode ($\overline{W}$ / T pin = "L")

When not inputting an edge to the WDI pin during t_{WDU}, or when an edge is input to the WDI pin again within a specific period of time (the discharge time due to an edge detection + 1 charge-discharge time (t_{WDL})) after inputting an edge to the WDI pin, the $\overline{WDO}$ pin output changes from "H" to "L".

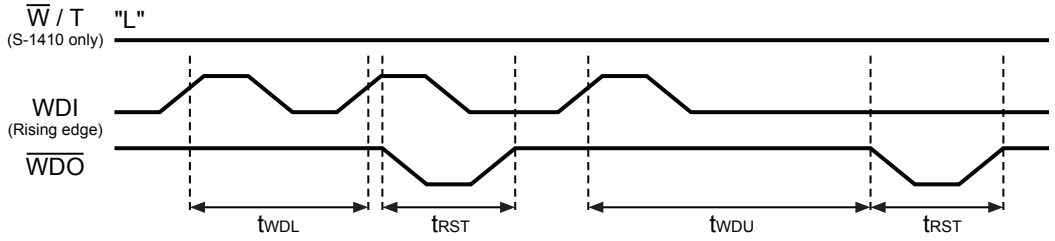


Figure 12 Abnormality Detection in Window Mode

2. $\overline{\text{RST}}$ pin (S-1411 Series only)

This is a reset output pin. It outputs "L" when detecting a low voltage.
Be sure to connect an external pull-up resistor (R_{extR}) to the $\overline{\text{RST}}$ pin in the product without an output pull-up resistor.

3. $\overline{\text{WDO}}$ pin

3. 1 S-1410 Series

This pin combines the reset output and the watchdog output (time-out detection, double pulse detection).
Be sure to connect an external pull-up resistor (R_{extW}) to the $\overline{\text{WDO}}$ pin in the product without an output pull-up resistor. **Table 7** shows the $\overline{\text{WDO}}$ pin output status.

Table 7

Operation Status	$\overline{\text{WDO}}$ Pin	
	$\overline{\text{W}}$ / T Pin = "H"	$\overline{\text{W}}$ / T Pin = "L"
Normal operation	"H"	"H"
Low voltage detection	"L"	"L"
Time-out detection	"L"	"L"
Double pulse detection	"H"	"L"
When watchdog timer is Disable	"H"	"H"

3. 2 S-1411 Series

This is the watchdog output (time-out detection, double pulse detection) pin.
Be sure to connect an external pull-up resistor (R_{extW}) to the $\overline{\text{WDO}}$ pin in the product without an output pull-up resistor. **Table 8** shows the $\overline{\text{WDO}}$ pin and $\overline{\text{RST}}$ pin output statuses.

Table 8

Operation Status	$\overline{\text{WDO}}$ Pin	$\overline{\text{RST}}$ Pin
Normal operation	"H"	"H"
Low voltage detection	"L"	"L"
Time-out detection	"L"	"H"
Double pulse detection	"L"	"H"
When watchdog timer is Disable	"H"	"H"

4. CPOR pin

This is a pin to connect an adjustment capacitor for reset output delay time (C_{POR}) in order to generate the reset time-out period (t_{RST}). C_{POR} is charged and discharged by an internal constant current circuit, and the charge-discharge duration is t_{RST}.
t_{RST} is calculated by using the following equation. Take into consideration C_{POR} variation.

$$t_{RST} = 6{,}500{,}000 \times C_{POR}\ [F] + 0.0002$$

5. CWDT pin

This is a pin to connect an adjustment capacitor for watchdog output delay time (C_{WDT}) in order to generate the watchdog time-out period (t_{WDU}) and the watchdog double pulse detection time (t_{WDL}). C_{WDT} is charged and discharged by an internal constant current circuit.
t_{WDU} is calculated by using the following equation. Take into consideration C_{WDT} variation.

$$t_{WDU} = 50{,}000{,}000 \times C_{WDT}\ [F] + 0.0011$$

Moreover, t_{WDL} is calculated by using the following equation.

$$t_{WDL} = \frac{t_{WDU}}{32}$$

6. WEN pin

This is a pin to switch Enable / Disable of the watchdog timer.
The voltage detection circuit independently operates at all times regardless of the watchdog timer operation.

6. 1 S-1410/1411 Series A / B / C / G / H / I type (WEN pin logic active "H" product)

The watchdog timer becomes Enable if the input is "H", and the charge-discharge operation is performed at the CWDT pin.
The WEN pin is connected to a constant current source (0.3 μA typ.) and is pulled down internally.

6. 2 S-1410/1411 Series D / E / F / J / K / L type (WEN pin logic active "L" product)

The watchdog timer becomes Enable if the input is "L", and the charge-discharge operation is performed at the CWDT pin.
The WEN pin is not pulled down internally.

7. WDI pin

This is an input pin to receive a signal from the monitored object. By inputting an edge at an appropriate timing, the WDI pin confirms the normal operation of the monitored object.
The WDI pin is connected to a constant current source (0.3 μA typ.) and is pulled down internally.

■ Absolute Maximum Ratings

Table 9

(Ta = +25°C unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
VDD pin voltage		V_{DD}	V_{SS} – 0.3 to V_{SS} + 7.0	V
WDI pin voltage		V_{WDI}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
WEN pin voltage		V_{WEN}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
$\overline{W}$ / T pin voltage		$V_{\overline{W}/T}$	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
CPOR pin voltage		V_{CPOR}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
CWDT pin voltage		V_{CWDT}	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
$\overline{RST}$ pin voltage	A / B / C / D / E / F type	$V_{\overline{RST}}$	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
	G / H / I / J / K / L type		V_{SS} – 0.3 to V_{SS} + 7.0	V
$\overline{WDO}$ pin voltage	A / B / C / D / E / F type	$V_{\overline{WDO}}$	V_{SS} – 0.3 to V_{DD} + 0.3 ≤ V_{SS} + 7.0	V
	G / H / I / J / K / L type		V_{SS} – 0.3 to V_{SS} + 7.0	V
Operation ambient temperature		T_{opr}	–40 to +105	°C
Storage temperature		T_{stg}	–40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 10

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	TMSOP-8	Board A	–	160	–	°C/W
			Board B	–	133	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W
		HSNT-8(2030)	Board A	–	181	–	°C/W
			Board B	–	135	–	°C/W
			Board C	–	40	–	°C/W
			Board D	–	42	–	°C/W
			Board E	–	32	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Recommended Operation Conditions

Table 11

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
VDD pin voltage	V_{DD}	Detector block	0.9	–	6.0	V
		Watchdog timer block	2.5	–	6.0	V
Set detection voltage	$-V_{DET(S)}$	0.1 V step	2.0	–	5.0	V
External pull-up resistor for $\overline{RST}$ pin	R_{extR}	S-1411 Series G / H / I / J / K / L type	10	100	–	kΩ
External pull-up resistor for $\overline{WDO}$ pin	R_{extW}	S-1410/1411 Series G / H / I / J / K / L type	10	100	–	kΩ
Adjustment capacitor for reset output delay time	C_{POR}	–	0.1	2.2	1000	nF
Adjustment capacitor for watchdog output delay time	C_{WDT}	–	0.1	0.47	1000	nF

■ Electrical Characteristics

1. S-1410 Series

Table 12 (1 / 2)

(WEN pin logic active "H" product, V_{DD} = 5.0 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	–		$-V_{DET(S)} \times 0.985$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.015$	V	1
Hysteresis width	V_{HYS}	–		$-V_{DET} \times 0.03$	$-V_{DET} \times 0.05$	$-V_{DET} \times 0.07$	V	1
Current consumption during operation	I_{SS1}	When watchdog timer operates		–	3.8	7.8	μA	2
Reset time-out period	t_{RST}	C_{POR} = 2200 pF		8.7	14.5	20	ms	3
Watchdog time-out period	t_{WDU}	C_{WDT} = 470 pF		15	24.6	34	ms	3
Watchdog double pulse detection time	t_{WDL}	C_{WDT} = 470 pF		461	769	1077	μs	4
Watchdog output voltage "H"	V_{WOH}	A / B / C / D / E / F type only		V_{DD} – 1.0	–	–	V	5
Watchdog output voltage "L"	V_{WOL}	External pull-up resistor of 100 kΩ is connected for G / H / I / J / K / L type		–	–	0.4	V	6
Watchdog output pull-up current	I_{WUP}	$V_{\overline{WDO}}$ = 0 V, A / B / C / D / E / F type only		–	–0.85	–0.4	μA	7
Watchdog output current	I_{WOUT}	V_{DS} = 0.4 V	V_{DD} = 1.5 V	0.6	1.1	–	mA	8
			V_{DD} = 1.8 V	1.1	1.6	–	mA	8
			V_{DD} = 2.5 V	2.1	2.6	–	mA	8
			V_{DD} = 3.0 V	2.8	3.3	–	mA	8
Watchdog output leakage current	I_{WLEAK}	V_{DS} = 6.0 V, V_{DD} = 6.0 V		–	–	0.096	μA	9
Input pin voltage 1 "H"	V_{SH1}	WEN pin		$0.7 \times V_{DD}$	–	–	V	10
Input pin voltage 1 "L"	V_{SL1}	WEN pin		–	–	$0.3 \times V_{DD}$	V	10
Input pin voltage 2 "H"	V_{SH2}	$\overline{W}$ / T pin		$0.7 \times V_{DD}$	–	–	V	10
Input pin voltage 2 "L"	V_{SL2}	$\overline{W}$ / T pin		–	–	$0.3 \times V_{DD}$	V	10
Input pin voltage 3 "H"	V_{SH3}	WDI pin		$0.7 \times V_{DD}$	–	–	V	10
Input pin voltage 3 "L"	V_{SL3}	WDI pin		–	–	$0.3 \times V_{DD}$	V	10

Table 12 (2 / 2)

(WEN pin logic active "H" product, V_{DD} = 5.0 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Input pin current 1 "H"	I_{SH1}	WEN pin, V_{DD} = 6.0 V, Input pin voltage = 6.0 V	A / B / C / G / H / I type	–	0.3	1.0	μA	10
			D / E / F / J / K / L type	–0.1	–	0.1	μA	10
Input pin current 1 "L"	I_{SL1}	WEN pin, V_{DD} = 6.0 V, Input pin voltage = 0 V		–0.1	–	0.1	μA	10
Input pin current 2 "H"	I_{SH2}	$\overline{W}$ / T pin, V_{DD} = 6.0 V, Input pin voltage = 6.0 V		–	0.3	1.0	μA	10
Input pin current 2 "L"	I_{SL2}	$\overline{W}$ / T pin, V_{DD} = 6.0 V, Input pin voltage = 0 V		–0.1	–	0.1	μA	10
Input pin current 3 "H"	I_{SH3}	WDI pin, V_{DD} = 6.0 V, Input pin voltage = 6.0 V		–	0.3	1.0	μA	10
Input pin current 3 "L"	I_{SL3}	WDI pin, V_{DD} = 6.0 V, Input pin voltage = 0 V		–0.1	–	0.1	μA	10
Input pulse width "H"*2	t_{high1}	–		1.5	–	–	μs	10
Input pulse width "L"*2	t_{low1}	–		1.5	–	–	μs	10
Watchdog output delay time	t_{WOUT}	–		–	25	40	μs	3
Reset output delay time	t_{ROUT}	–		–	25	40	μs	3
Input setup time	t_{iset}	–		1.0	–	–	μs	3

***1.** $-V_{DET}$: Actual detection voltage, $-V_{DET(S)}$: Set detection voltage

***2.** The input pulse width "H" (t_{high1}) and the input pulse width "L" (t_{low1}) are defined as shown in **Figure 13**.
Inputs to the WEN pin and the WDI pin should be greater than or equal to the min. value specified in "■ **Electrical Characteristics**".

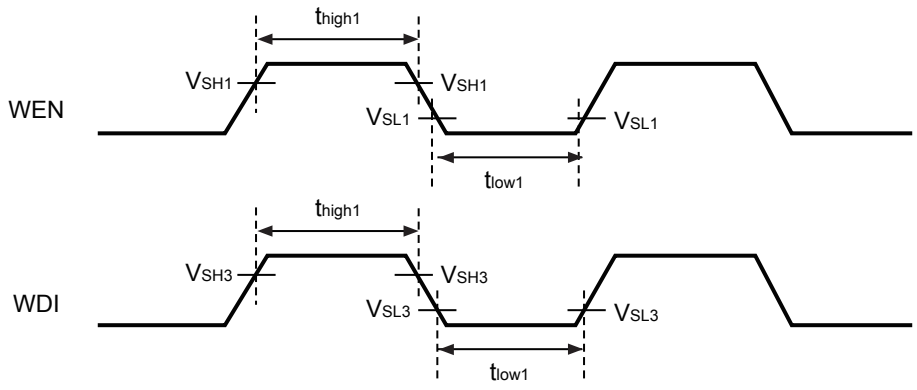


Figure 13

2. S-1411 Series

Table 13 (1 / 2)

(WEN pin logic active "H" product, V_{DD} = 5.0 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage*1	$-V_{DET}$	–		$-V_{DET(S)} \times 0.985$	$-V_{DET(S)}$	$-V_{DET(S)} \times 1.015$	V	11
Hysteresis width	V_{HYS}	–		$-V_{DET} \times 0.03$	$-V_{DET} \times 0.05$	$-V_{DET} \times 0.07$	V	11
Current consumption during operation	I_{SS1}	When watchdog timer operates		–	3.8	7.8	μA	12
Reset time-out period	t_{RST}	C_{POR} = 2200 pF		8.7	14.5	20	ms	13
Watchdog time-out period	t_{WDU}	C_{WDT} = 470 pF		15	24.6	34	ms	13
Watchdog double pulse detection time	t_{WDL}	C_{WDT} = 470 pF		461	769	1077	μs	14
Reset output voltage "H"	V_{ROH}	A / B / C / D / E / F type only		V_{DD} – 1.0	–	–	V	15
Reset output voltage "L"	V_{ROL}	External pull-up resistor of 100 kΩ is connected for G / H / I / J / K / L type		–	–	0.4	V	16
Reset output pull-up current	I_{RUP}	$V_{\overline{RST}}$ = 0 V, A / B / C / D / E / F type only		–	–0.85	–0.4	μA	17
Reset output current	I_{ROUT}	V_{DS} = 0.4 V	V_{DD} = 1.5 V	0.6	1.1	–	mA	18
			V_{DD} = 1.8 V	1.1	1.6	–	mA	18
			V_{DD} = 2.5 V	2.1	2.6	–	mA	18
			V_{DD} = 3.0 V	2.8	3.3	–	mA	18
Reset output leakage current	I_{RLEAK}	V_{DS} = 6.0 V, V_{DD} = 6.0 V		–	–	0.096	μA	19
Watchdog output voltage "H"	V_{WOH}	A / B / C / D / E / F type only		V_{DD} – 1.0	–	–	V	20
Watchdog output voltage "L"	V_{WOL}	External pull-up resistor of 100 kΩ is connected for G / H / I / J / K / L type		–	–	0.4	V	21
Watchdog output pull-up current	I_{WUP}	$V_{\overline{WDO}}$ = 0 V, A / B / C / D / E / F type only		–	–0.85	–0.4	μA	22
Watchdog output current	I_{WOUT}	V_{DS} = 0.4 V	V_{DD} = 1.5 V	0.6	1.1	–	mA	23
			V_{DD} = 1.8 V	1.1	1.6	–	mA	23
			V_{DD} = 2.5 V	2.1	2.6	–	mA	23
			V_{DD} = 3.0 V	2.8	3.3	–	mA	23
Watchdog output leakage current	I_{WLEAK}	V_{DS} = 6.0 V, V_{DD} = 6.0 V		–	–	0.096	μA	24
Input pin voltage 1 "H"	V_{SH1}	WEN pin		$0.7 \times V_{DD}$	–	–	V	25
Input pin voltage 1 "L"	V_{SL1}	WEN pin		–	–	$0.3 \times V_{DD}$	V	25
Input pin voltage 3 "H"	V_{SH3}	WDI pin		$0.7 \times V_{DD}$	–	–	V	25
Input pin voltage 3 "L"	V_{SL3}	WDI pin		–	–	$0.3 \times V_{DD}$	V	25

Table 13 (2 / 2)

(WEN pin logic active "H" product, V_{DD} = 5.0 V, Ta = +25°C unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Input pin current 1 "H"	I_{SH1}	WEN pin, V_{DD} = 6.0 V, Input pin voltage = 6.0 V	A / B / C / G / H / I type	–	0.3	1.0	μA	25
			D / E / F / J / K / L type	–0.1	–	0.1	μA	25
Input pin current 1 "L"	I_{SL1}	WEN pin, V_{DD} = 6.0 V, Input pin voltage = 0 V		–0.1	–	0.1	μA	25
Input pin current 3 "H"	I_{SH3}	WDI pin, V_{DD} = 6.0 V, Input pin voltage = 6.0 V		–	0.3	1.0	μA	25
Input pin current 3 "L"	I_{SL3}	WDI pin, V_{DD} = 6.0 V, Input pin voltage = 0 V		–0.1	–	0.1	μA	25
Input pulse width "H"*2	t_{high1}	–		1.5	–	–	μs	25
Input pulse width "L"*2	t_{low1}	–		1.5	–	–	μs	25
Watchdog output delay time	t_{WOUT}	–		–	25	40	μs	13
Reset output delay time	t_{ROUT}	–		–	25	40	μs	13
Input setup time	t_{iset}	–		1.0	–	–	μs	13

***1.** $-V_{DET}$: Actual detection voltage, $-V_{DET(S)}$: Set detection voltage

***2.** The input pulse width "H" (t_{high1}) and the input pulse width "L" (t_{low1}) are defined as shown in **Figure 14**.
Inputs to the WEN pin and the WDI pin should be greater than or equal to the min. value specified in "■ **Electrical Characteristics**".

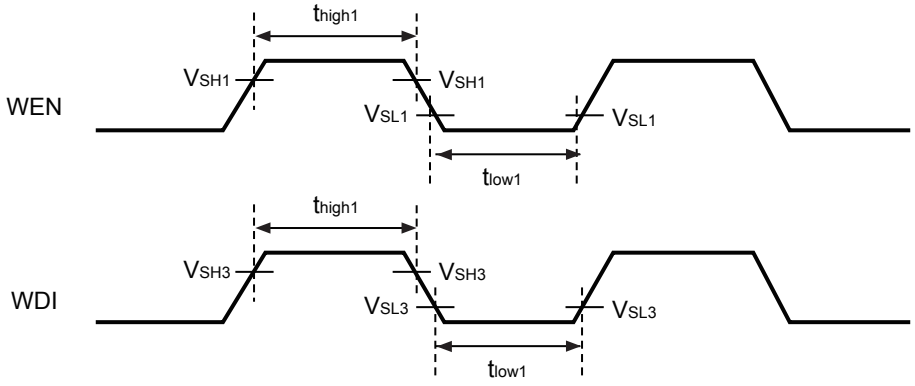


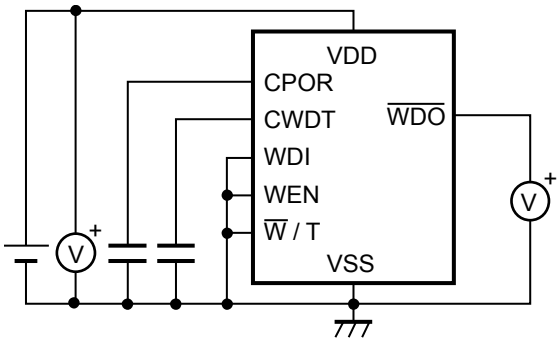
Figure 14

■ Test Circuits

Refer to "■ **Recommended Operation Conditions**" when setting constants of external pull-up resistors (R_{extR}, R_{extW}) and external capacitors (C_{POR}, C_{WDT}).

1. S-1410 Series

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

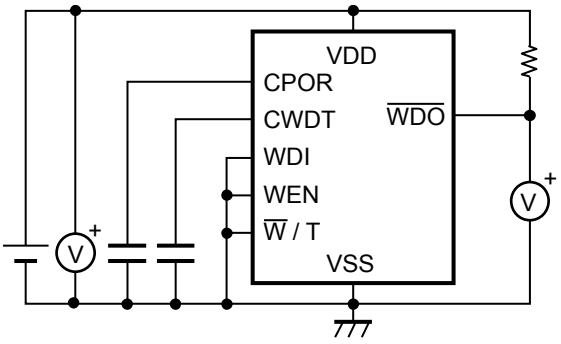


Figure 15 Test Circuit 1

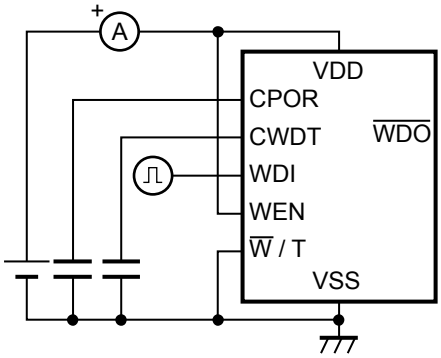
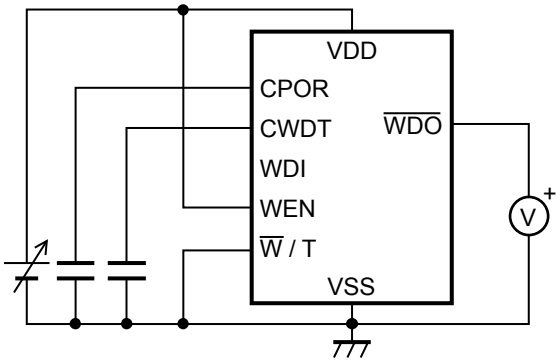


Figure 16 Test Circuit 2

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

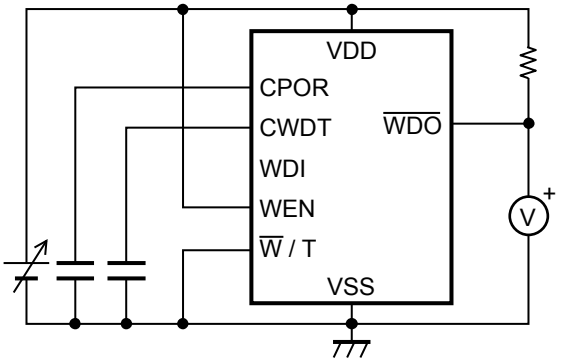
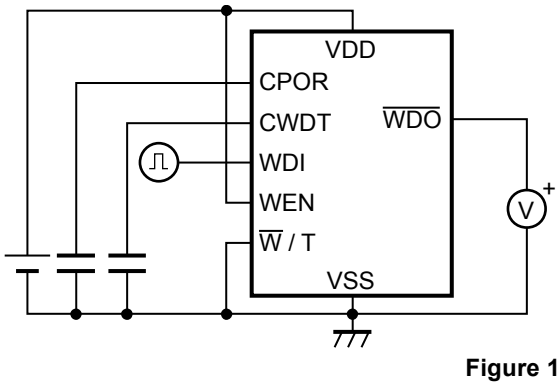


Figure 17 Test Circuit 3

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

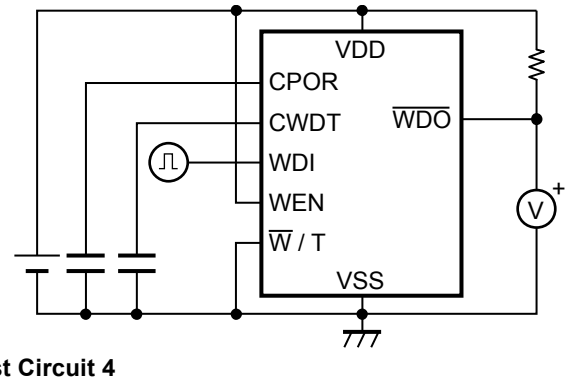


Figure 18 Test Circuit 4

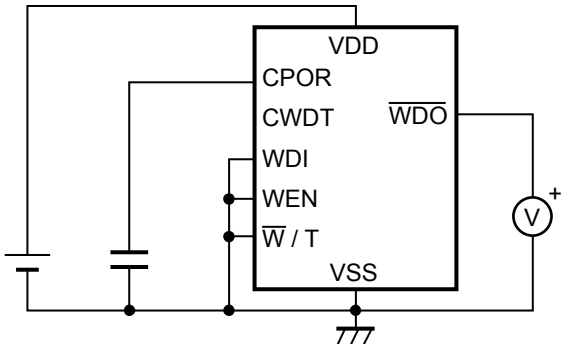
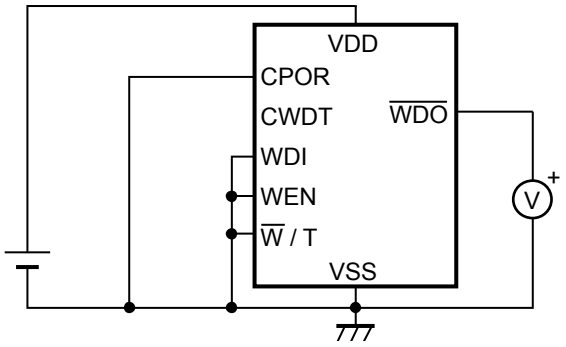


Figure 19 Test Circuit 5

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

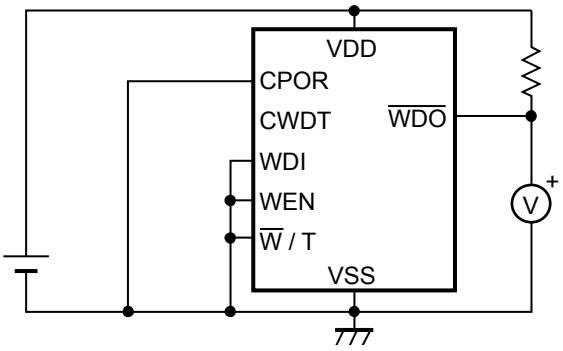


Figure 20 Test Circuit 6

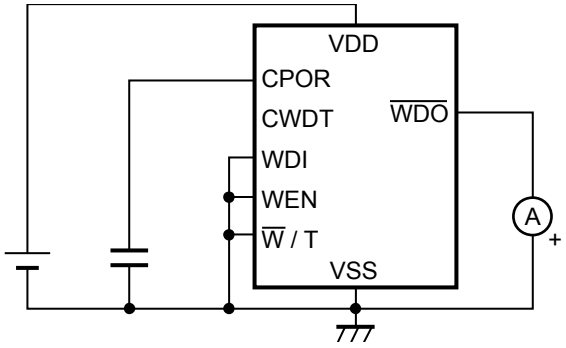


Figure 21 Test Circuit 7

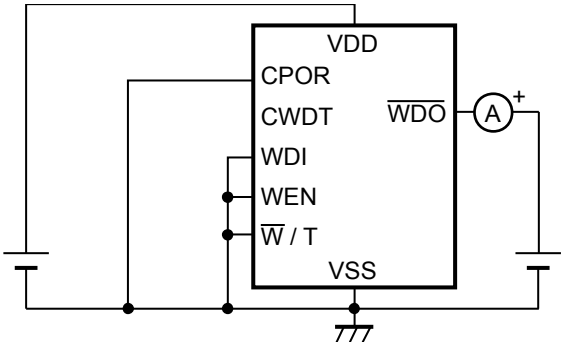


Figure 22 Test Circuit 8

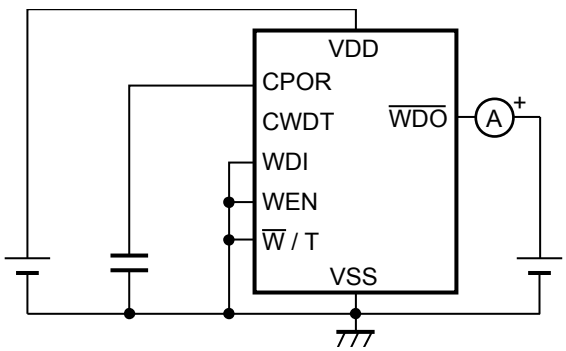


Figure 23 Test Circuit 9

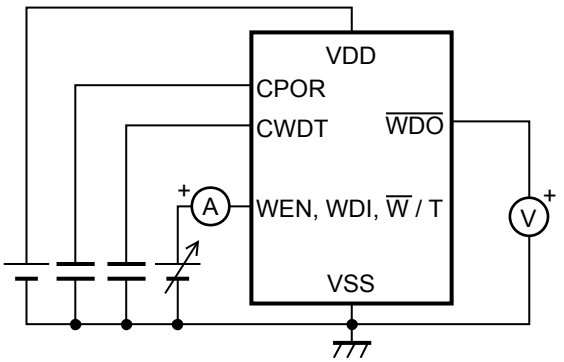
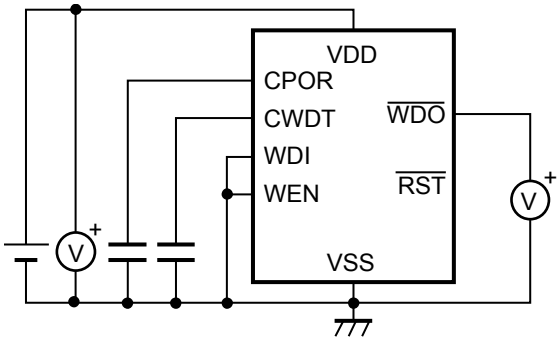


Figure 24 Test Circuit 10

2. S-1411 Series

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

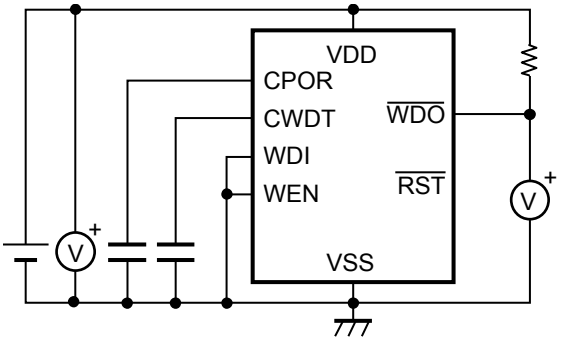


Figure 25 Test Circuit 11

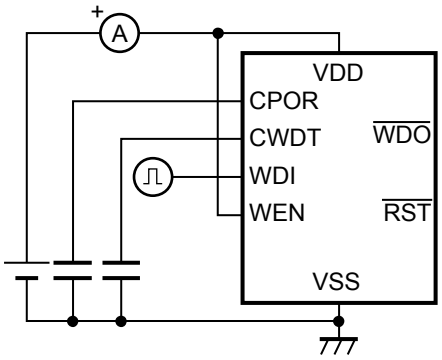
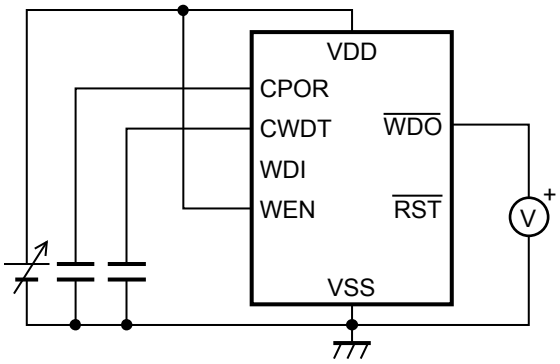


Figure 26 Test Circuit 12

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

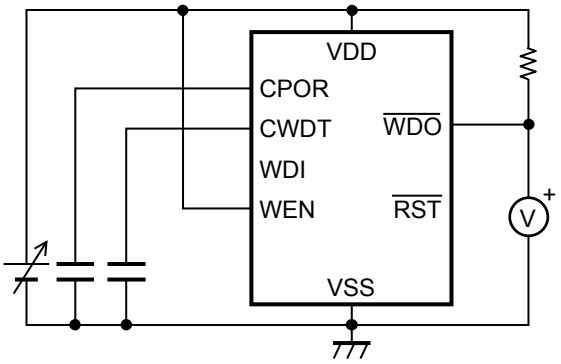
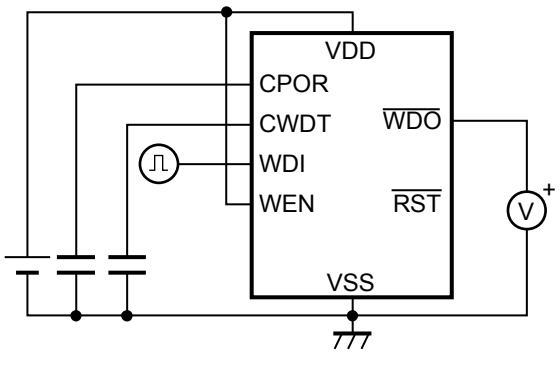


Figure 27 Test Circuit 13

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

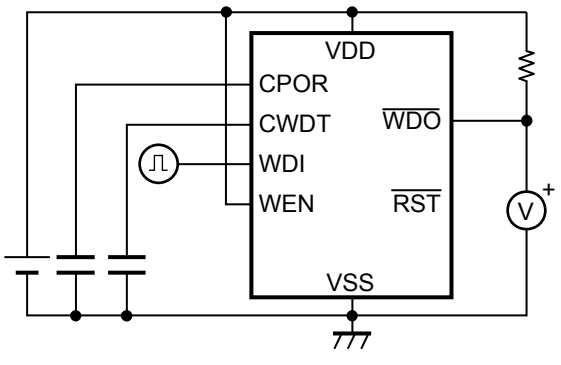


Figure 28 Test Circuit 14

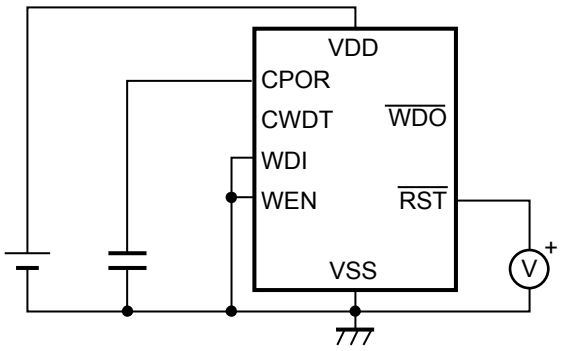
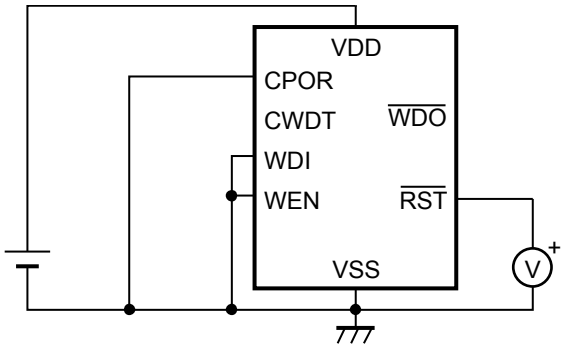


Figure 29 Test Circuit 15

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

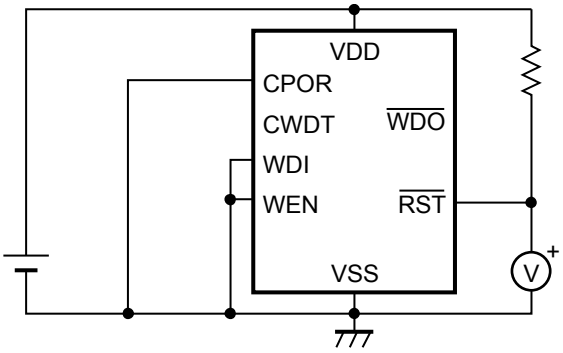


Figure 30 Test Circuit 16

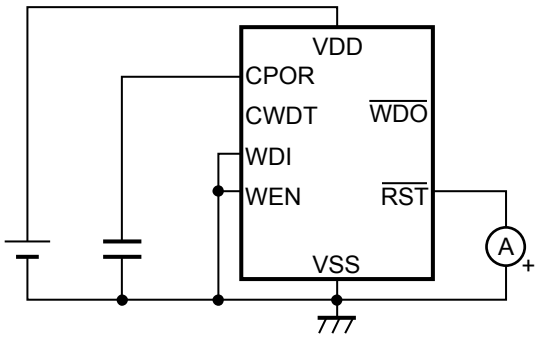


Figure 31 Test Circuit 17

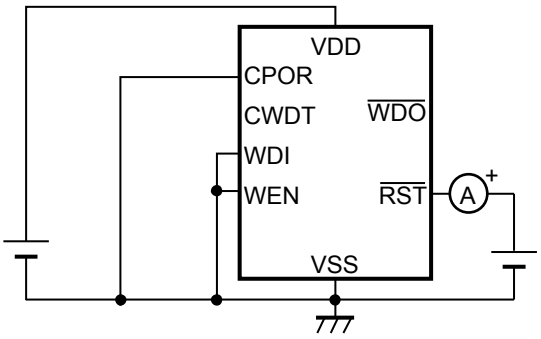


Figure 32 Test Circuit 18

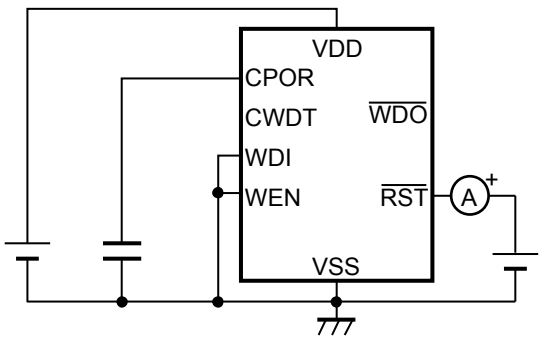


Figure 33 Test Circuit 19

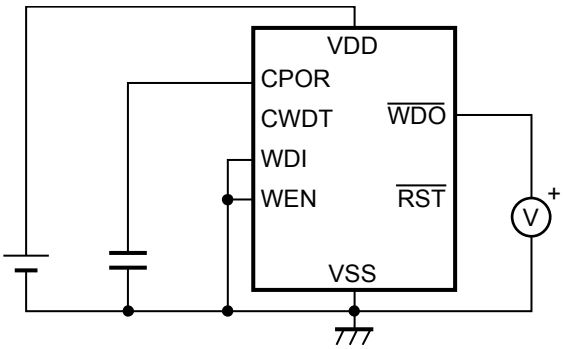
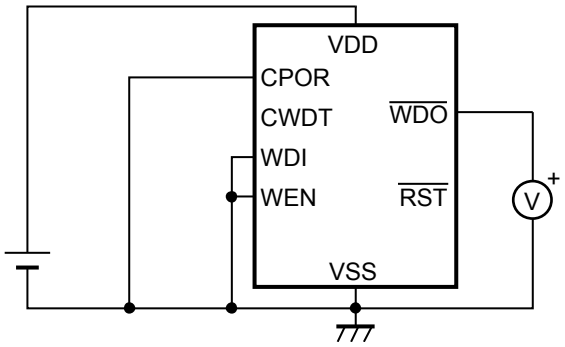


Figure 34 Test Circuit 20

(1) A / B / C / D / E / F type



(2) G / H / I / J / K / L type

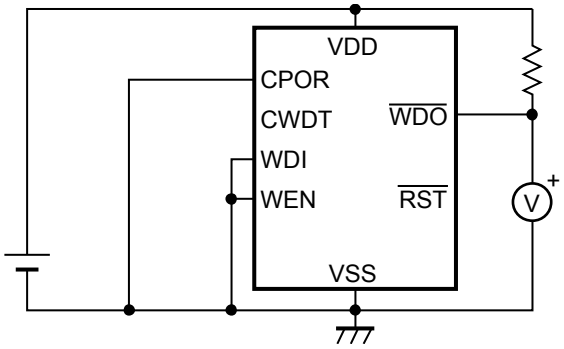


Figure 35 Test Circuit 21

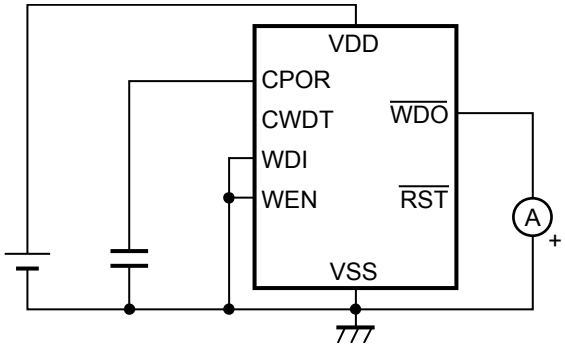


Figure 36 Test Circuit 22

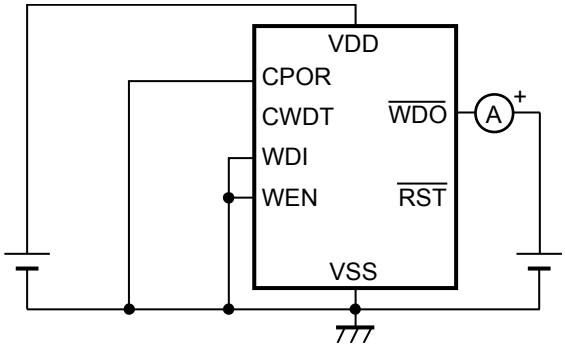


Figure 37 Test Circuit 23

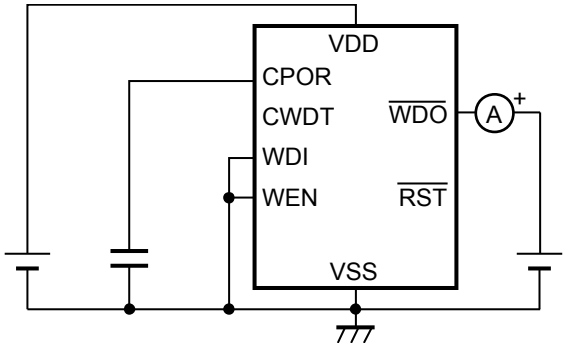


Figure 38 Test Circuit 24

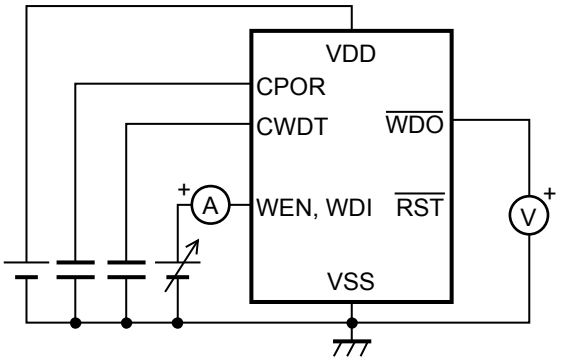
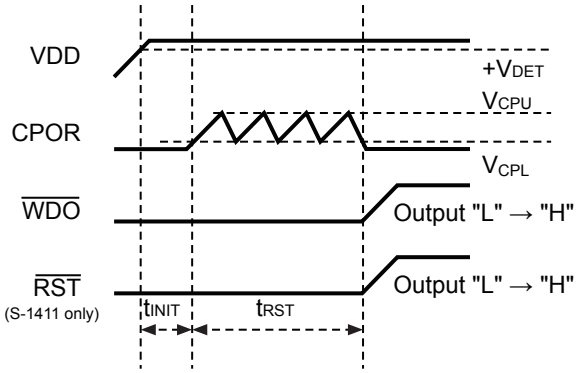


Figure 39 Test Circuit 25

■ Operations

1. From power-on to reset release

The S-1410/1411 Series initiates the initialization if the VDD pin voltage exceeds the release voltage ($+V_{DET}$).
The charge-discharge operation to the CPOR pin is initiated after the passage of the initialization time (t_{INIT}), and the $\overline{WDO}$ pin output and the $\overline{RST}$ pin output change from "L" to "H" after the operation is performed 4 times.



Remark V_{CPU}: CPOR charge upper limit threshold (1.25 V typ.)
V_{CPL}: CPOR charge lower limit threshold (0.20 V typ.)

Figure 40

t_{INIT} changes according to the power supply rising time. Refer to **Figure 41** for the relation between t_{INIT} and the power supply rising time.

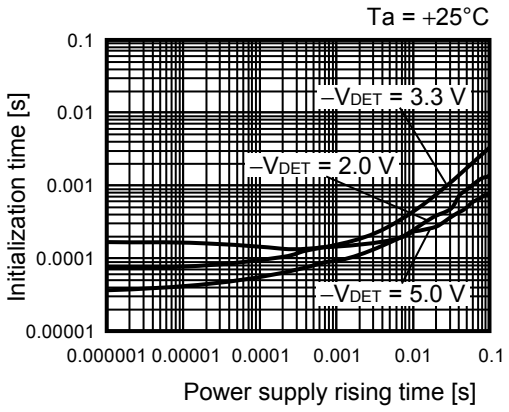
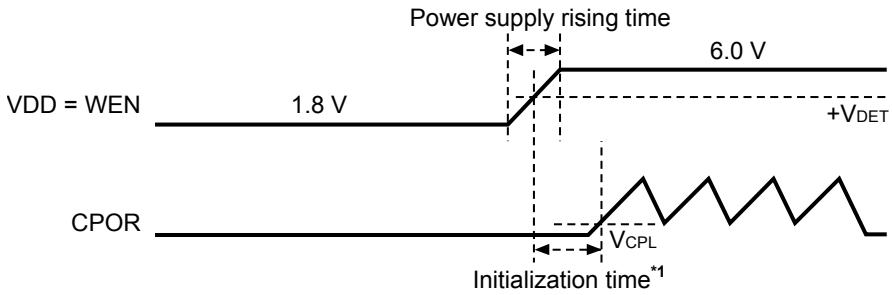


Figure 41 Power Supply Rising Time Dependency of Initialization Time



***1.** The initialization time is the time period from when the VDD pin voltage reaches $+V_{DET}$ to when C_{POR} rises.

Figure 42 Initialization Time

2. From reset release to initiation of charge-discharge operation to CWDT pin

The charge-discharge operation to the CWDT pin differs depending on the status of the WEN pin at the reset release.

2. 1 When WEN pin is "H" at reset release (Active "H")

Since the watchdog timer is Enable, the S-1410/1411 Series initiates the charge-discharge operation to the CWDT pin.

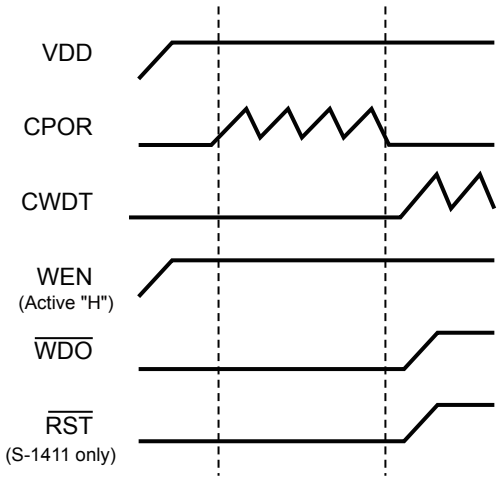


Figure 43 WEN Pin = "H"

2. 2 When WEN pin is "L" at reset release (Active "H")

Since the watchdog timer is Disable after the CPOR pin performs the charge-discharge operation 4 times, the S-1410/1411 Series does not initiate the charge-discharge operation to the CWDT pin. If the input to the WEN pin changes to "H" in this status, the S-1410/1411 Series initiates the charge-discharge operation to the CWDT pin.

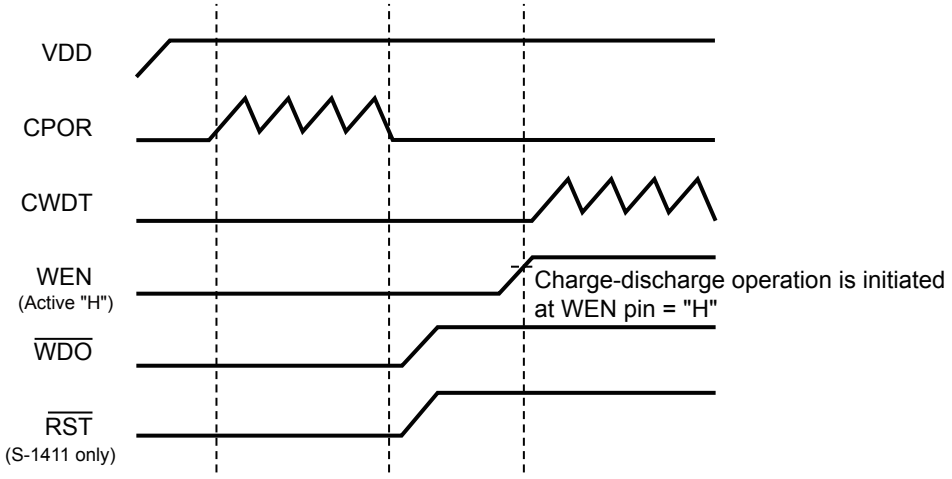


Figure 44 WEN Pin = "L" → "H"

3. Watchdog time-out detection

The watchdog timer detects a time-out after the charge-discharge operation to the CWDT pin is performed 32 times, then the $\overline{WDO}$ pin output changes from "H" to "L".

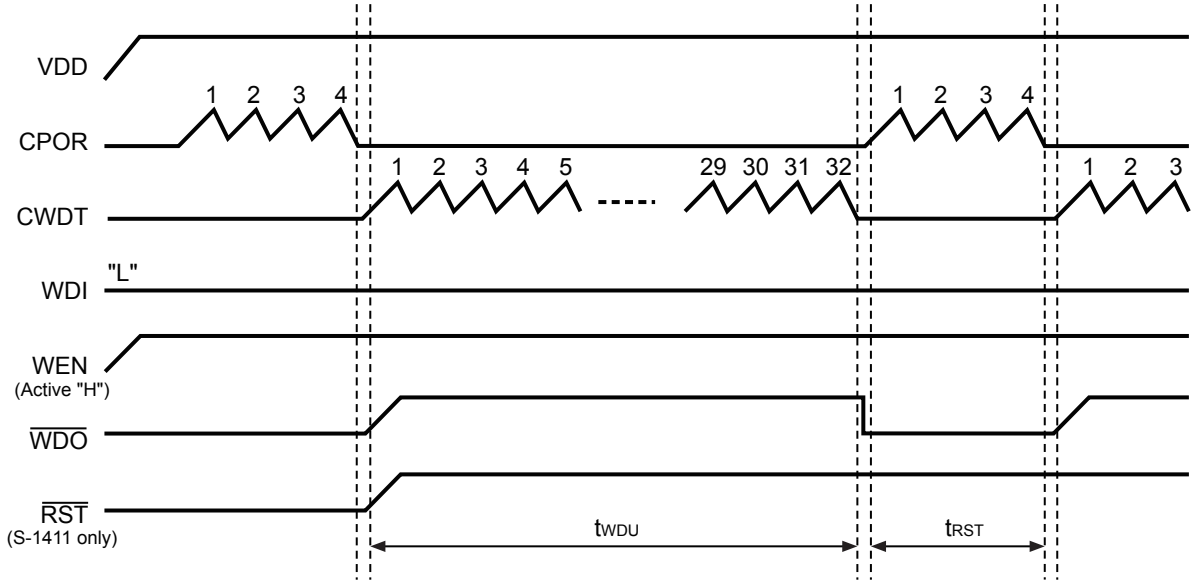


Figure 45

4. Internal counter reset due to edge detection

When the WDI pin detects an edge during the charge-discharge operation to the CWDT pin, the internal counter which counts the number of times of the charge-discharge operation is reset. The CWDT pin initiates the discharge operation when an edge is detected, and initiates the charge-discharge operation again after the discharge operation is completed.

4. 1 Counter reset due to rising edge detection (S-141xAxx, S-141xDxx, S-141xGxx, S-141xJxx)

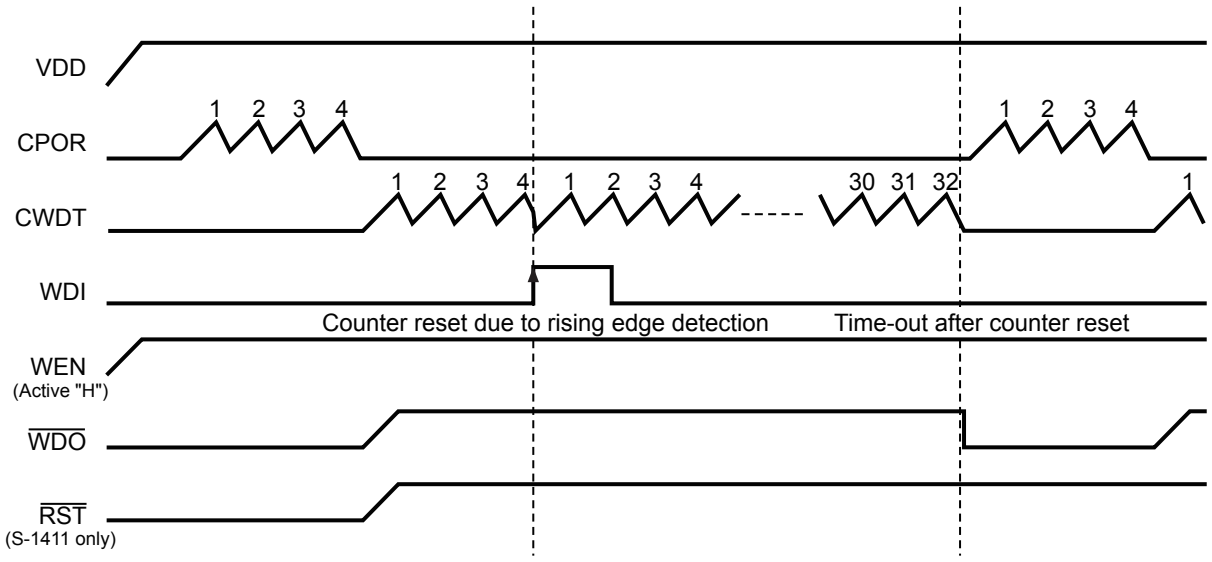


Figure 46