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S-1702 Series

SUPER-LOW CURRENT CONSUMPTION 150 mA VOLTAGE REGULATOR WITH BUILT-IN HIGH-ACCURACY VOLTAGE DETECTOR AND RESET INPUT FUNCTION

www.sii-ic.com

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The S-1702 Series, developed based on CMOS technology, is a 150 mA output positive voltage regulator with a low dropout voltage, a high-accuracy output voltage, and low current consumption.

The S-1702 Series includes a voltage regulator with high-accuracy output voltage of $\pm 1.0\%$ allowing to use a ceramic capacitor of 1.0 μ F or more, and a voltage detector that monitors the output/input voltage of the regulator. It also includes an overcurrent protection circuit that prevents the output current from exceeding the current capacitance of the output transistor and an output forcible discharge circuit for the regulator operation off.

Small SNT-6A package is available for the S-1702 Series. And an external small capacitor can be used, enabling high-density mounting. Its super-low current consumption makes the S-1702 Series ideal for mobile devices.

Features

Regulator block

 Output voltage: Output voltage accuracy: Current consumption: Output current: Built-in overcurrent protection circuit: Built-in ON / OFF forcible discharge circuit: Ripple rejection: Detector block	1.5 V to 5.5 V, selectable in 0.05 V step $\pm 1.0\%$ Current consumption of regulator block: 9 µA typ., 16 µA max. Possible to output 150 mA (V _{IN} \ge V _{OUT(S)} + 1.0 V) ^{*1} Limits overcurrent of output transistor. Ensures long battery life, discharges output load instantaneously. 70 dB typ. (f = 1.0 kHz)
 Detection voltage: Built-in high-accuracy voltage detection circuit: External reset input: 	 1.3 V to 5.2 V, selectable in 0.05 V step ±1.0% Monitoring output/input or monitoring external input by option (detector output) Forcible assertion of detector output by external reset pin (RESX) input

Overall

- Correlation temperature gradient in the regulator and the detector blocks
- Current consumption: During operation^{*2}: 10 μA typ., 18 μA max.
- Operation temperature range: $Ta = -40^{\circ}C \text{ to } +85^{\circ}C$
- Lead-free (Sn 100%), halogen-free
- *1. Attention should be paid to the power dissipation of the package when the output current is large.
- *2. Excluding current flowing in pull-up and pull-down resistors connected to the ON / OFF or RESX pins

Applications

- Wireless power supply circuit block for cellular phone
- Power supply circuit block for health care product
- Power supply circuit block for various mobile device

Package

SNT-6A

1

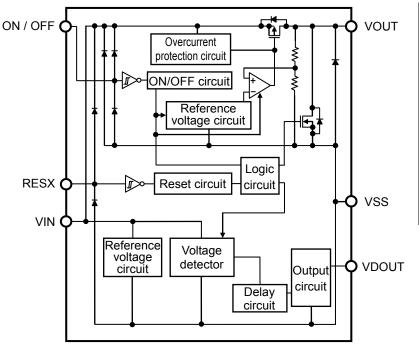
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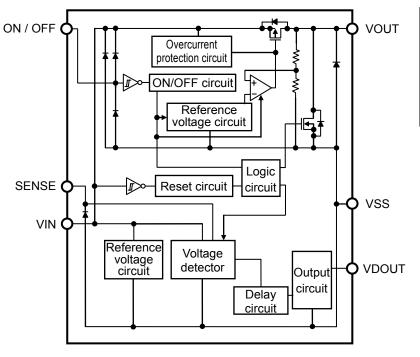
Block Diagrams

1. S-1702 Series A type to H type



Product Type	Detector Monitor Voltage	Discharge Shunt Function by ON / OFF and RESX Pins Control by Control by	
		ON / OFF Pin	RESX Pin
A	Vout	0	0
В	Vout	0	×
С	Vout	×	0
D	Vout	×	×
Е	VIN	0	0
F	VIN	0	×
G	VIN	×	0
Н	VIN	×	×

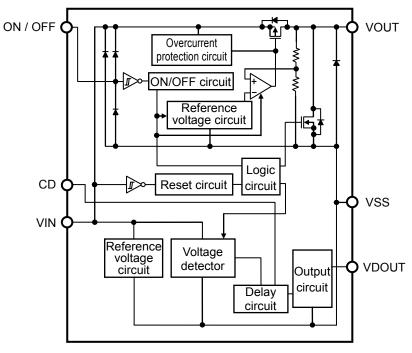
Figure 1



2.	S-1702 Series J type and K type (external input detection type)	
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Product Type	Detector Monitor Voltage	Discharge Shunt Function by ON / OFF Pin
J	External input	0
к	External input	×

Figure 2



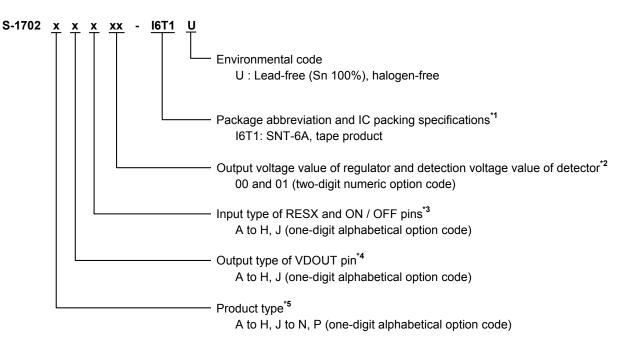
3. S-1702 Series L type to N type, P type (external delay type)

Product Type	Detector Monitor Voltage	Discharge Shunt Function by ON / OFF Pin
L	Vout	0
М	Vout	×
Ν	VIN	0
Р	VIN	×

Figure 3

Product Name Structure

1. Product name



- ***1.** Refer to the tape drawing.
- *2. Refer to Table 4 of "2. Function list according to product type".
- *3. Refer to Table 3 of "2. Function list according to product type".
- *4. Refer to Table 2 of "2. Function list according to product type".
- *5. Refer to Table 1 of "2. Function list according to product type".

2. Function list according to product type

Option	ON / OFF Pin	RESX Pin		Detector Monitor	Discharge Sh	unt Function
Code	Application	Application	Delay Type	Voltage	Control by ON / OFF Pin	Control by RESX Pin
А	ON / OFF	RESX	Internal	Vout	0	0
В	ON / OFF	RESX	Internal	Vout	0	×
С	ON / OFF	RESX	Internal	Vout	×	0
D	ON / OFF	RESX	Internal	Vout	×	×
Е	ON / OFF	RESX	Internal	VIN	0	0
F	ON / OFF	RESX	Internal	VIN	0	×
G	ON / OFF	RESX	Internal	VIN	×	0
Н	ON / OFF	RESX	Internal	VIN	×	×
J	ON / OFF	SENSE	Internal	VSENSE	0	-
K	ON / OFF	SENSE	Internal	VSENSE	×	-
L	ON / OFF	CD	External	Vout	0	-
М	ON / OFF	CD	External	Vout	×	_
N	ON / OFF	CD	External	VIN	0	_
Р	ON / OFF	CD	External	VIN	×	-

Table 1 Product Types

Table 2 Output Types of VDOUT Pin

Option Code	Output Type	Hysteresis
А	Nch open drain output	5.0%
В	CMOS output (VOUT drive)	5.0%
С	CMOS output (VIN drive)	5.0%
D	Nch open drain output	2.5%
E	CMOS output (VOUT drive)	2.5%
F	CMOS output (V _{IN} drive)	2.5%
G	Nch open drain output	None
Н	CMOS output (VOUT drive)	None
J	CMOS output (V _{IN} drive)	None

Option Code	RESX Pin	ON / OFF Pin
А	No pull-up/pull-down resistor	No pull-up/pull-down resistor
В	No pull-up/pull-down resistor	Pull-up
С	No pull-up/pull-down resistor	Pull-down
D	Pull-up	No pull-up/pull-down resistor
Е	Pull-up	Pull-up
F	Pull-up	Pull-down
G	Pull-down	No pull-up/pull-down resistor
Н	Pull-down	Pull-up
J	Pull-down	Pull-down

Table 3 Input Types of RESX and ON / OFF Pins

Table 4 Output Voltage Values of Regulator and Detection Voltage Values of Detector

Option Code	Output Voltage	Detection Voltage
00	3.1 V ±1.0%	2.75 V ±1.0%
01	3.1 V ±1.0%	2.60 V ±1.0%

Remark Please contact our sales office for products with an output voltage or detection voltage other than those specified above.

3. Package

Deekere Neme		Drawing Code		
Package Name	Package	Таре	Reel	Land
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD

Pin Configuration

1. SNT-6A



Figure 4

14510 0			
Pin No.	Symbol	Description	
1	VIN	Input voltage pin	
2	ON / OFF	ON / OFF pin	
	RESX	External reset pin (S-1702Axx to Hxx)	
3	CD	External delay capacitor connection pin (S-1702Lxx to Nxx, Pxx)	
	SENSE	Detector SENSE pin (S-1702Jxx, Kxx)	
4	VSS	GND pin	
5	VDOUT	Detector output voltage pin	
6	VOUT	Regulator output voltage pin	

Table 5

Absolute Maximum Ratings

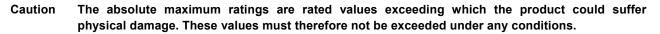
		Table 6		
			(Ta = +25°C unless otherw	vise specified)
	Item	Symbol	Absolute Maximum Rating	Unit
		VIN	$V_{\text{SS}}-0.3$ to $V_{\text{SS}}+7.0$	V
		Von / OFF	$V_{\text{SS}} - 0.3$ to $V_{\text{IN}} + 0.3$	V
Input voltage		VRESX	$V_{\text{SS}} - 0.3$ to $V_{\text{IN}} + 0.3$	V
			$V_{\text{SS}} - 0.3$ to $V_{\text{IN}} + 0.3$	V
		VSENSE	$V_{\text{SS}}-0.3$ to $V_{\text{SS}}+7.0$	V
Regulator output vo	Itage	Vout	$V_{\text{SS}} - 0.3$ to $V_{\text{IN}} + 0.3$	V
Detector output	Nch open drain output	. v	$V_{SS} - 0.3$ to $V_{SS} + 7.0$	V
voltage	CMOS output	VDOUT	$V_{SS} - 0.3$ to $V_{IN} + 0.3$	V
Power dissipation		PD	400 ^{*1}	mW
Operation ambient temperature		Topr	-40 to +85	°C
Storage temperature		T _{stg}	-40 to +125	°C

***1.** When mounted on board

[Mounted board]

(1) Board size : 114.3 mm \times 76.2 mm \times t1.6 mm

(2) Board name : JEDEC STANDARD51-7



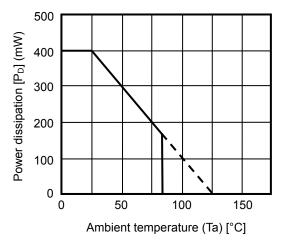


Figure 5 Power Dissipation of Package

Electrical Characteristics

1. Common to series (S-1702Axx to Hxx, Jxx to Nxx, Pxx)

Table 7 (1 / 2) Entire circuit

Entire circuit		, , , , , , , , , , , , , , , , , , ,	(Ta = +2	5°C unles	s otherw	vise spec	ified)
Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Test Circuit
Current consumption during operation ^{*1}	lss	$V_{IN} = V_{OUT(S)} + 1.0 V$	_	10	18	μA	2

Regulator block

Item	Symbol	Co	ondition		Min.	Тур.	Max.	Unit	Test Circuit
Output voltage*2	Vout(e)	V_{IN} = $V_{OUT(S)}$ + 1.0 V	ν, Ι _{Ουτ} = 3	0 mA	V _{OUT(S)} ×0.99	Vout(s)	V _{OUT(S)} ×1.01	V	1
Output current*3	lout	$V_{IN} > V_{OUT(S)} + 1.0 V$	/		150* ⁸	-	_	mA	3
			1.5 V < V	$OUT(S) \le 2.0 V$	_	0.54	0.58	V	1
			2.0 V < V	$OUT(S) \le 2.5 V$	_	0.23	0.35	V	1
Dropout voltage*4	Vdrop	Iout = 100 mA	2.5 V < V	$OUT(S) \leq 3.0 V$	_	0.2	0.3	V	1
			3.0 V < V	$OUT(S) \leq 3.3 V$	_	0.15	0.23	V	1
			3.3 V < V	$OUT(S) \le 5.5 V$	_	0.14	0.21	V	1
Line regulation	$\frac{\Delta V_{OUT1}}{\Delta V_{IN} \bullet V_{OUT}}$	V _{OUT(S)} + 0.5 V < V _{IN} I _{OUT} = 30 mA	₁ < 6.5 V,		-	0.05	0.2	%/V	1
Load regulation		$V_{IN} = V_{OUT(S)} + 1.0 V_{OUT(S)} + 1.0 V_{OUT(S)}$	•		_	20	40	mV	1
Output voltage temperature coefficient *5	ΔV _{OUT} ΔTa • V _{OUT}	$V_{IN} = V_{OUT(S)} + 1.0 V$ $I_{OUT} = 30 \text{ mA},$ $-40^{\circ}\text{C} \le \text{Ta} \le +85^{\circ}\text{C}$	Ι,		_	±100	±300	ppm/ °C	1
Current consumption during operation*1	Iss1	$V_{IN} = V_{OUT(S)} + 1.0 V$ RESX and ON / OF operation, no load		abled for	_	9	16	μA	2
Input voltage	VIN		_		2	_	6.5	V	-
ON / OFF pin input voltage "H"	V _{SH1}	$V_{IN} = V_{OUT(S)} + 1.0 V$	∕, R∟ = 1.0	kΩ	1.2	_	_	V	4
ON / OFF pin input voltage "L"	V _{SL1}	$V_{IN} = V_{OUT(S)} + 1.0 V$	∕, R∟ = 1.0	kΩ	_	-	0.3	V	4
				S-1702xxA	-0.1	_	0.1	μA	4
ON / OFF pin input current "H"	I _{SH1}	VIN = 6.5 V, VON / OFF	= = 6.5 V	S-1702xxD	-0.1	_	0.1	μA	4
				S-1702xxG	-0.1	_	0.1	μA	4
ON / OFF pin				S-1702xxA	-0.1	_	0.1	μA	4
input current "L"	I _{SL1}	VIN = 6.5 V, VON / OFF	= = 0 V	S-1702xxD	-0.1	-	0.1	μA	4
				S-1702xxG	-0.1	-	0.1	μA	4
Ripple rejection	RR	$V_{IN} = V_{OUT(S)} + 1.0 V$ f = 1.0 kHz,	^{/,} 1.5 V :	\leq V _{OUT(S)} < 3.1 V	_	70	-	dB	5
		ΔV_{rip} = 0.5 Vrms, I _{OUT} = 30 mA		$\leq V_{OUT(S)} \leq 5.5 V$	_	65	-	dB	5
Short-circuit current	ISHORT	$V_{IN} = V_{OUT(S)} + 1.0 V$ ON / OFF pin enabl $V_{OUT} = 0 V$		eration,	_	300	_	mA	5

Detector block			ne (2 / 2)	(Ta = +25	5°C unles	s otherwis	se spec	cified)
Item	Symbol	Condi	tion	Min.	Тур.	Max.	Unit	Test Circuit
Detection voltage*6	-Vdet	-		-V _{DET(S)} ×0.99	-VDET(S)	-V _{DET(S)} ×1.01	V	6
		S-1702xAx, S-1702xBx,	S-1702xCx	–V _{DET} ×0.035	-V _{DET} ×0.05	-V _{DET} ×0.065	V	6
Hysteresis width	V _{HYS}	S-1702xDx, S-1702xEx,	S-1702xFx	–V _{DET} ×0.01	-V _{DET} ×0.025	–V _{DET} ×0.04	V	6
		S-1702xGx, S-1702xHx	S-1702xJx	Ι	0	–V _{DET} ×0.015	V	6
		$1.3 \text{ V} \le -V_{\text{DET}(S)} \le 2.3 \text{ V}$	V_{IN} = $-V_{\text{DET}(S)}$ + 1.5 V	-	2.4	4.0	μA	2
Current consumption	ISS2	$1.3 V \leq -V DEI(S) \leq 2.3 V$	V _{IN} = 5.5 V	_	2.6	4.5	μA	2
during operation*1	1882	$2.3 V \le -V_{DET(S)} < 5.2 V$	$V_{\text{IN}} = -V_{\text{DET}(S)} + 1.5 \text{ V}$	_	2.2	3.5	μA	2
		$2.3 \text{ V} \leq -\text{V} \text{DET(S)} \leq 5.2 \text{ V}$	V _{IN} = 5.5 V	_	2.3	4.0	μA	2
Input voltage	VIN	_		0.8	_	6.5	V	-
Detection voltage temperature coefficient * ⁷	Δ-V _{DET} ΔTa • -V _{DET}	Ta = –40°C to +85°C ^{*9}		-	±100	±400	ppm/ °C	6

Table 7 (2 / 2)

*1. Excluding current flowing in pull-up and pull-down resistors connected to the ON / OFF or RESX pins

*2. VOUT(S): Set output voltage VOUT(E): Actual output voltage

Output voltage when fixing IOUT (= 30 mA) and inputting VOUT(S) + 1.0 V

- The output current at which the output voltage becomes 95% of V_{OUT(E)} after gradually increasing the output current. *3.
- *4. $V_{drop} = V_{IN1} - (V_{OUT3} \times 0.98)$

 V_{OUT3} is the output voltage when $V_{IN} = V_{OUT(S)} + 1.0 V$ and $I_{OUT} = 100 mA$.

....

VIN1 is the input voltage at which the output voltage becomes 98% of Vout3 after gradually decreasing the input voltage.

*5. A change in the temperature of the regulator output voltage [mV/°C] is calculated using the following equation.

$$\frac{\Delta V_{OUT}}{\Delta Ta} [mV/^{\circ}C]^{*1} = V_{OUT(S)} [V]^{*2} \times \frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}} [ppm/^{\circ}C]^{*3} \div 1000$$

- *1. Change in temperature of output voltage
- *2. Set output voltage
- *3. Output voltage temperature coefficient
- *6. –V_{DET(S)} : Set detection voltage
 - -VDET : Actual detection voltage
- *7. A change in the temperature of the detector detection voltage [mV/°C] is calculated using the following equation.

$$\frac{\Delta - V_{\text{DET}}}{\Delta \text{Ta}} [\text{mV/}^{\circ}\text{C}]^{*1} = -V_{\text{DET}(S)} (\text{Typ.}) [\text{V}]^{*2} \times \frac{\Delta - V_{\text{DET}}}{\Delta \text{Ta} \bullet - V_{\text{DET}}} [\text{ppm/}^{\circ}\text{C}]^{*3} \div 1000$$

- *1. Change in temperature of detection voltage
- *2. Set detection voltage
- *3. Detection voltage temperature coefficient
- *8. The output current can be at least this value. Due to restrictions on the package power dissipation, this value may not be satisfied. Attention should be paid to the power dissipation of the package when the output current is large. This specification is guaranteed by design.
- *9. Since products are not screened at high and low temperatures, the specification for this temperature range is guaranteed by design, not tested in production.

2. Discharge shunt circuit (discharge shunt function) (S-1702Axx, Bxx, Cxx, Exx, Fxx, Gxx, Jxx, Lxx, Nxx)

Table 8

			(Ta = +2	5°C unles	s otherwis	se spec	ified)
Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Test Circuit
"L" output, Nch on resistor	RLOW	V_{DS} = 0.5 V, V_{GS} = 6.5 V	_	100	_	Ω	3

3. Detector output circuit (VDOUT pin)

Table 9

Nch open drain output (S-	1702xAx, x	Dx, xGx)	(Ta = +2	5°C unles	s otherwis	se spec	ified)
Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Test Circuit
Output current	Idout1	Output transistor: Nch, V _{DS} = 0.5 V, V _{DD} = 1.2 V	1.36	2.55	_	mA	7
Leakage current	I _{LEAK}	Output transistor: Nch, V _{DS} = 5.5 V, V _{DD} = 5.5 V	-	_	100	nA	7
CMOS output (S-1702xBx,	xCx, xEx, x	(Fx, xHx, xJx)					
Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Test Circuit
	Idout2	Output transistor: Nch, V _{DS} = 0.5 V, V _{IN} = 1.2 V	1.36	2.55	_	mA	7
Output current	Idout3	Output transistor: Pch, V _{DS} = 0.5 V, V _{IN} = 5.5 V	1.71	2.76	_	mA	8

4. RESX pin (S-1702Axx, Bxx, Cxx, Dxx, Exx, Fxx, Gxx, Hxx)

Table 10

(Ta = +25°C unless otherwise specified) Test Symbol Condition Item Min. Typ. Max. Unit Circuit RESX pin input voltage "H"*1 V_{SH2} $V_{IN} = V_{OUT(S)} + 1.0 V, R_L = 1.0 k\Omega$ 1.2 _ V 4 RESX pin input voltage "L" V_{SL2} $V_{\text{IN}} = V_{\text{OUT}(S)} + 1.0 \text{ V}, \text{ R}_{\text{L}} = 1.0 \text{ k}\Omega$ 0.3 V 4 _ _ S-1702xxA -0.1 0.1 μΑ 4 _ VIN = 6.5 V, VRESX = 6.5 V S-1702xxB -0.1 4 RESX pin input current "H" 0.1 ISH2 _ μΑ S-1702xxC -0.1 4 _ 0.1 μA S-1702xxA -0.1 0.1 μΑ 4 _ RESX pin input current "L" $V_{IN} = 6.5 V, V_{RESX} = 0 V$ 4 ISL2 S-1702xxB -0.10.1 μΑ — S-1702xxC -0.1 0.1 μΑ 4 _

*1. VOUT(S): set output voltage value

5. Pull-up / pull-down resistor value of ON / OFF pin and RESX pin (S-1702xxB, xxC, xxD, xxE, xxF xxG, xxH, xxJ) Table 11

(Ta = $+25^{\circ}$ C unless otherwise specified)

Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Test Circuit
Pull-up / pull-down resistor	R _{PULL}	-	_	2.0	-	MΩ	4

6. Response time

Table 12

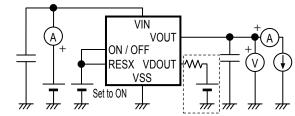
Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Test Circuit
Response time	T _{PLH1}	_	_	—	90	μs	6
External delay type (S-1	I702Lxx, Mxx,	Nxx, Pxx)					
Item	Symbol	Condition	Min.	Тур.	Max.	Unit	Test Circuit
Response time	T _{PLH2}	C _D = 4.7 nF	_	30	_	ms	9

4.

6.

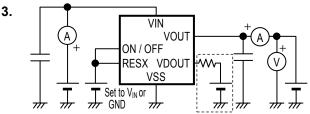
Test Circuits

1.



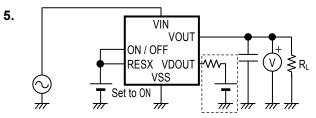
The portion enclosed by dotted lines is not required for CMOS output products.





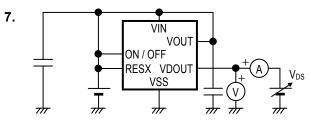
The portion enclosed by dotted lines is not required for CMOS output products.



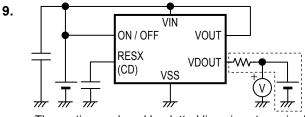


The portion enclosed by dotted lines is not required for CMOS output products.



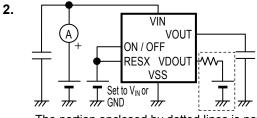






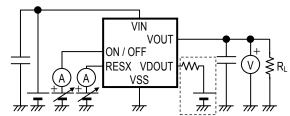
The portion enclosed by dotted lines is not required for CMOS output products.

Figure 14



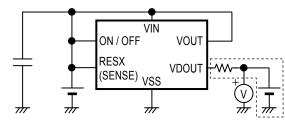
The portion enclosed by dotted lines is not required for CMOS output products.

Figure 7



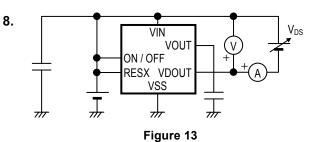
The portion enclosed by dotted lines is not required for CMOS output products.

Figure 9



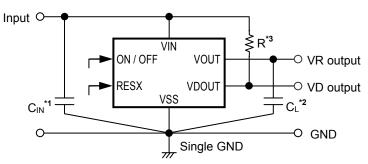
The portion enclosed by dotted lines is not required for CMOS output products.

Figure 11



Standard Circuits

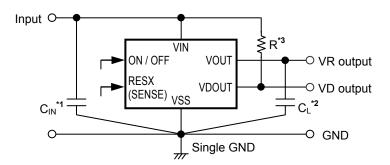
1. S-1702Axx, Bxx, Cxx, Dxx, Exx, Fxx, Gxx, Hxx



- ***1.** C_{IN} is a capacitor for stabilizing the input.
- *2. A ceramic capacitor of 1.0 μ F or more can be used for C_L.
- ***3.** R is not required for a CMOS output product.



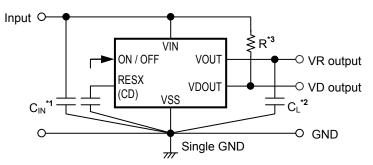
2. S-1702Jxx, Kxx



- *1. C_{IN} is a capacitor for stabilizing the input.
- *2. A ceramic capacitor of 1.0 μ F or more can be used for C_L.
- *3. R is not required for a CMOS output product.

Figure 16

3. S-1702Lxx, Mxx, Nxx, Pxx



- *1. C_{IN} is a capacitor for stabilizing the input.
- *2. A ceramic capacitor of 1.0 μF or more can be used for $C_L.$
- ***3.** R is not required for a CMOS output product.

Figure 17

Caution The above connection diagrams and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

Condition of Application

Input capacitor (CIN):	1.0 μF or more
Output capacitor (CL):	1.0 µF or more
ESR of output capacitor:	10 Ω or less

Caution Generally a series regulator may cause oscillation, depending on the selection of external parts. Confirm that no oscillation occurs in the application for which the above capacitors are used.

■ Selection of VIN Input and VOUT Output Capacitors (C_{IN}, C_L)

The S-1702 Series requires an output capacitor (C_L) between the VOUT and VSS pins for phase compensation. A ceramic capacitor with a capacitance of 1.0 μ F or more provides a stable operation in all temperature ranges. When using an OS capacitor, a tantalum capacitor, or an aluminum electrolytic capacitor, a capacitance must be 1.0 μ F or more, and the ESR must be 10 Ω or less.

The output overshoot and undershoot values, which are transient response characteristics, vary depending on the output capacitor value. The required capacitance value for the input capacitor differs depending on the application.

The recommended application values are $C_{IN} \ge 1.0 \ \mu\text{F}$ and $C_L \ge 1.0 \ \mu\text{F}$; however, perform thorough evaluation using the actual device, including evaluation of temperature characteristics.

Explanation of Terms

1. Regulator block

1.1 Low dropout voltage regulator

This voltage regulator has the low dropout voltage due to its built-in low on-resistance transistor.

1.2 Low ESR

A capacitor whose ESR (Equivalent Series Resistance) is low. The S-1702 Series enables use of a low ESR capacitor, such as a ceramic capacitor, for the output-side capacitor (C_L). A capacitor whose ESR is 10 Ω or less can be used.

1.3 Output voltage (VOUT)

The accuracy of the output voltage is ensured at $\pm 1.0\%$ under the specified conditions of fixed input voltage^{*1}, fixed output current, and fixed temperature.

- ***1.** Differs depending on the product.
- Caution If the above conditions change, the output voltage value may vary and exceed the accuracy range of the output voltage. Refer to "■ Electrical Characteristics" and "■ Characteristics (Typical Data)" for details.

1.4 Line regulation
$$\left(\frac{\Delta V_{\text{OUT1}}}{\Delta V_{\text{IN}} \bullet V_{\text{OUT}}}\right)$$

Indicates the dependency of the output voltage on the input voltage. That is, the values show how much the output voltage changes due to a change in the input voltage with the output current remaining unchanged.

1. 5 Load regulation (ΔV_{OUT2})

Indicates the dependency of the output voltage on the output current. That is, the values show how much the output voltage changes due to a change in the output current with the input voltage remaining unchanged.

1. 6 Dropout voltage (Vdrop)

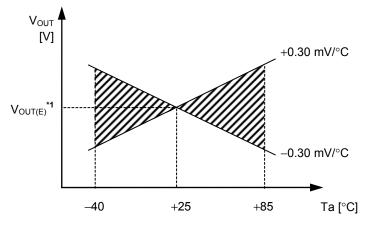
Indicates the difference between input voltage (V_{IN1}) and the output voltage when; decreasing input voltage (V_{IN}) gradually until the output voltage has dropped out to the value of 98% of output voltage (V_{OUT3}), which is at V_{IN} = $V_{OUT(S)} + 1.0 \text{ V}$.

 V_{drop} = $V_{IN1} - (V_{OUT3} \times 0.98)$

Output voltage temperature coefficient $\left(\frac{\Delta V_{\text{out}}}{\Delta T a \bullet V_{\text{out}}}\right)$ 1.7

The shaded area in Figure 18 is the range where V_{OUT} varies in the operation temperature range when the output voltage temperature coefficient is ±100 ppm/°C (Refer to *5 of Table 7 for how to calculate the temperature change of the output voltage [mV/°C]).

Example of V_{OUT} = 3.0 V typ. product



*1. $V_{OUT(E)}$ is the value of the output voltage measured at Ta = +25°C.

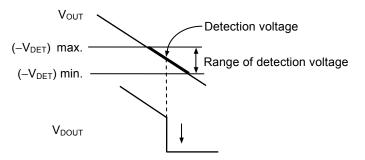


2. Detector block

2.1 Detection voltage (-VDET)

The detection voltage $(-V_{DET})$ is a voltage when the detector output voltage (V_{DOUT}) switches to low. This detection voltage varies slightly depending on products even having the same specification. The range between the minimum $(-V_{DET})$ value and the maximum $(-V_{DET})$ value due to variation is called the range of detection voltage (refer to **Figure 19**).

e.g. In a product with $-V_{DET}$ = 3.0 V, the detection voltage is a value in the range of 2.97 V \leq ($-V_{DET}$) \leq 3.03 V. This means that some products have 2.97 V for $-V_{DET}$ and some have 3.03 V.



Remark This is the case when the regulator output voltage (V_{OUT}) is monitored by the detector.

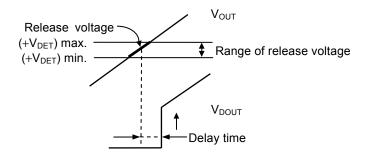
Figure 19 Detection Voltage (-V_{DET})

2. 2 Release voltage (+V_{DET})

The release voltage ($+V_{DET}$) is a voltage when the detector output voltage (V_{DOUT}) switches to high. This release voltage varies slightly depending on products even having the same specification. The range between the minimum ($+V_{DET}$) value and the maximum ($+V_{DET}$) value due to variation is called the range of release voltage (refer to **Figure 20**).

e.g. In a product with $-V_{DET}$ = 3.0 V and hysteresis width of 5%, the release voltage is a value in the range of 3.074 V \leq (+V_{DET}) \leq 3.227 V.

This means that some products have 3.074 V for +V_{DET} and some have 3.227 V.



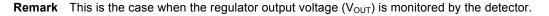


Figure 20 Release Voltage (+V_{DET})

2.3 Hysteresis width (V_{HYS})

The hysteresis width is the difference between the detection voltage and the release voltage. Setting the hysteresis width prevents malfunction caused by noise on the input voltage. The hysteresis width is internally fixed and varies depending on the product type for details, refer to **"Table 2 Output Types of VDOUT Pin"**.

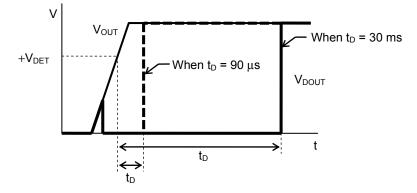
2.4 Delay time (t_D)

The delay time (t_D) is a period from the input voltage flowing to the detector block has exceeded the release voltage ($+V_{DET}$), until the detector output voltage (V_{DOUT}) inverts.

The internal delay type products (S-1702Axx, Bxx, Cxx, Dxx, Exx, Fxx, Gxx, Hxx, Jxx, Kxx) have delay time which is internally fixed.

In external delay type products (S-1702Lxx, Mxx, Nxx, Pxx), the delay time (t_D) can be changed by controlling the capacitance value of the capacitor (C_D) connected between the CD (RESX) and VSS pins.

For how to set the delay time (t_D), refer to "3. 2 Delay circuit" in "3. Detector block" in "■ Operation".



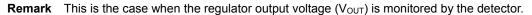


Figure 21

2.5 Through-type current

This is the current that flows instantaneously when the voltage detector detects and releases a voltage. A large through-type current flows in CMOS output products (S-1702xBx, xCx, xEx, xFx, xHx, xJx). A small through-type current flows in Nch open drain products (S-1702xAx, xDx, xGx).

2.6 Oscillation

In applications where a resistor is connected to the input side (**Figure 22**), the through-type current which is generated when the detector output voltage (V_{DOUT}) goes from low to high (release) causes a voltage drop equal to Through-type current × Input resistance across the resistor. When the input voltage drops below the detection voltage as a result, the detector output voltage (V_{DOUT}) goes from high to low. In this state, the through-type current stops, its resultant voltage drop disappears, and the detector output voltage (V_{DOUT}) goes from low to high. The through-type current is then generated again, a voltage drop appears, and repeating the process finally induces oscillation.

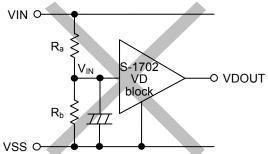
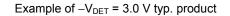
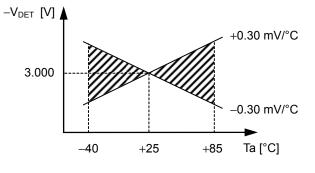


Figure 22 Example of Bad Implementation of Detection Voltage Changer

2.7 Detection voltage temperature characteristics

The shaded area in **Figure 23** is the range where $-V_{DET}$ varies within the operation temperature range when the detection voltage temperature coefficient is ± 100 ppm/°C (Refer to ***7** of **Table 7** for how to calculate the temperature change of the detection voltage [mV/°C]).







2.8 Release voltage temperature characteristics

The temperature change $\frac{\Delta + V_{DET}}{\Delta Ta}$ of the release voltage is calculated by the temperature change $\frac{\Delta - V_{DET}}{\Delta Ta}$ of the detection voltage as follows:

$$\frac{\Delta + V_{DET}}{\Delta Ta} = \frac{+V_{DET}}{-V_{DET}} \times \frac{\Delta - V_{DET}}{\Delta Ta}$$

The temperature changes of the release voltage and the detection voltage consequently have the same sign.

2.9 Hysteresis voltage temperature characteristics

The temperature change of the hysteresis voltage is expressed as $\frac{\Delta + V_{\text{DET}}}{\Delta \text{Ta}} - \frac{\Delta - V_{\text{DET}}}{\Delta \text{Ta}}$ and is calculated as follows:

$$\frac{\Delta + V_{\text{DET}}}{\Delta \text{Ta}} - \frac{\Delta - V_{\text{DET}}}{\Delta \text{Ta}} = \frac{V_{\text{HYS}}}{-V_{\text{DET}}} \times \frac{\Delta - V_{\text{DET}}}{\Delta \text{Ta}}$$
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Operation

1. Control of S-1702 Series by using ON / OFF and RESX pins

1.1 Starting and stopping regulator block

The regulator block can be started and stopped according to the combination of the ON / OFF and RESX pins. The regulator block switches off the output transistor between the VIN pin and VOUT pin and reduces current consumption significantly.

The detector block is operating during this period, so only the amount of current consumed by the detector block flows in the S-1702 Series.

1. 2 Regulator output (V_{OUT}) control: discharge shunt function *1

The regulator output (V_{OUT}) can be controlled by combining the ON / OFF and RESX pins.

In the product types having a discharge shunt circuit^{*1} (Axx, Bxx, Cxx, Exx, Fxx, Gxx, Jxx, Lxx, Nxx), this circuit forcibly sets the regulator output (V_{OUT}) the V_{SS} level^{*1}.

In the product types that do not have a discharge shunt circuit^{*1} (Dxx, Hxx, Kxx, Mxx, Pxx), the regulator output (V_{OUT}) is set at the V_{SS} level by a division resistor of several M Ω between the VOUT pin and VSS pin.

*1. For details of a discharge shunt circuit, refer to "2. 2. 2 Discharge shunt function" in "2. Regulator Block".

1.3 Detector output voltage (VDOUT) control: forcible assertion function

The detector output voltage (V_{DOUT}) is forcibly asserted to the V_{SS} level by combining the ON / OFF and RESX pins.

When the forcible assertion function is not being used, the result of detection by the detector (release status: "H", detection status: "L") is output from the VDOUT pin.

1.4 Operation of each function according to ON / OFF and RESX pins

The following shows the operation of each function according to the combination of the ON / OFF and RESX pin.

1702Axx, Exx				
ON / OFF Pin	RESX Pin	Regulator Block	Regulator Output (Vout)	Detector Outpu (VDOUT)
"L"	"L"	Stops	Forcibly discharged	Vss potential
"L"	"H"	Stops	Forcibly discharged	Vss potential
"H"	"L"	Stops	Forcibly discharged	Vss potential
"H"	"H"	Starts	Set value	"H" or "L"
702Bxx, Fxx				
ON / OFF Pin	RESX Pin	Regulator Block	Regulator Output (Vout)	Detector Outpu (Vроит)
"L"	"L"	Stops	Forcibly discharged	Vss potential
"L"	"H"	Stops	Forcibly discharged	Vss potential
"H"	"L"	Starts	Set value	Vss potential
"H"	"H"	Starts	Set value	"H" or "L"
702Cxx, Gxx				
ON / OFF Pin	RESX Pin	Regulator Block	Regulator Output (Vout)	Detector Outpu (Vроит)
"L"	"L"	Stops	Forcibly discharged	Vss potential
"L"	"H"	Stops	Not forcibly discharged	"H" or "L"
"H"	"L"	Stops	Forcibly discharged	Vss potential
"H"	"H"	Storto		"
		Starts	Set value	"H" or "L"
0N / OFF Pin	RESX Pin	Regulator Block	Regulator Output (Vout)	
1702Dxx, Hxx			Regulator Output	Detector Outpu
0N / OFF Pin	RESX Pin	Regulator Block	Regulator Output (Vоит) Not forcibly	Detector Outpu (VDOUT)
I 702Dxx, Hxx ON / OFF Pin "L"	RESX Pin "L"	Regulator Block Stops	Regulator Output (Vout) Not forcibly discharged Not forcibly	Detector Outpu (V _{DOUT}) V _{SS} potential
I 702Dxx, Hxx ON / OFF Pin "L" "L"	RESX Pin "L" "H"	Regulator Block Stops Stops	Regulator Output (Vour) Not forcibly discharged Not forcibly discharged	Detector Outpu (V _{DOUT}) V _{SS} potential "H" or "L"
I702Dxx, Hxx ON / OFF Pin "L" "L" "H" "H"	RESX Pin "L" "H" "L" "H"	Regulator Block Stops Stops Starts	Regulator Output (Vout) Not forcibly discharged Not forcibly discharged Set value	Detector Outpu (V _{DOUT}) V _{SS} potential "H" or "L" V _{SS} potential
I 702Dxx, Hxx ON / OFF Pin "L" "L" "H"	RESX Pin "L" "H" "H"	Regulator Block Stops Stops Starts	Regulator Output (Vout) Not forcibly discharged Not forcibly discharged Set value	Detector Outpu (V _{DOUT}) V _{SS} potential "H" or "L" V _{SS} potential "H" or "L"
I702Dxx, Hxx ON / OFF Pin "L" "L" "H" "H"	RESX Pin "L" "H" "H" K FF Pin	Regulator Block Stops Stops Starts Starts	Regulator Output (V _{OUT}) Not forcibly discharged Not forcibly discharged Set value Set value Regulator Output	Detector Outpu (V _{DOUT}) V _{SS} potential "H" or "L" V _{SS} potential "H" or "L" Detector Outpu
I702Dxx, Hxx ON / OFF Pin "L" "L" "H" "H" I702Jxx, Lxx, Nxx ON / O	RESX Pin "L" "H" "H"	Regulator Block Stops Stops Starts Starts Regulator Block	Regulator Output (Vout) Not forcibly discharged Not forcibly discharged Set value Set value Regulator Output (Vout)	Detector Outpu (V _{DOUT}) V _{SS} potential "H" or "L" V _{SS} potential "H" or "L" Detector Outpu (V _{DOUT})
I702Dxx, Hxx ON / OFF Pin "L" "L" "H" "H" I702Jxx, Lxx, Nxx ON / O "L	RESX Pin "L" "H" "H"	Regulator Block Stops Stops Starts Starts Regulator Block Stops	Regulator Output (VouT) Not forcibly discharged Not forcibly discharged Set value Set value Regulator Output (VouT) Forcibly discharged	Detector Outpu (V _{DOUT}) V _{SS} potential "H" or "L" V _{SS} potential "H" or "L" Detector Outpu (V _{DOUT}) V _{SS} potential
I702Dxx, Hxx ON / OFF Pin "L" "L" "H" "H" I702Jxx, Lxx, Nxx ON / O	RESX Pin "L" "H" "H" c FF Pin " t" x	Regulator Block Stops Stops Starts Starts Regulator Block Stops	Regulator Output (VouT) Not forcibly discharged Not forcibly discharged Set value Set value Regulator Output (VouT) Forcibly discharged	Detector Outpu (V _{DOUT}) V _{SS} potential "H" or "L" V _{SS} potential "H" or "L" Detector Outpu (V _{DOUT}) V _{SS} potential
I702Dxx, Hxx ON / OFF Pin "L" "L" "H" I702Jxx, Lxx, Nxx ON / O "L "H	RESX Pin "L" "H" "L" "H" C FF Pin " X FF Pin FF Pin	Regulator Block Stops Stops Starts Starts Regulator Block Stops Starts	Regulator Output (VouT) Not forcibly discharged Not forcibly discharged Set value Set value Regulator Output (VouT) Forcibly discharged Set value Regulator Output	Detector Outpu (V _{DOUT}) Vss potential "H" or "L" Vss potential "H" or "L" Detector Outpu (V _{DOUT}) Vss potential "H" or "L"

Table 13

1.5 Equivalent circuits of ON / OFF and RESX pins

The ON / OFF and RESX pins are internally fixed to any one of three states; pulled-up (via a pull-up resistor), pulled-down (via a pull-down resistor), or neither pulled-up nor pulled-down (no down pull-up / pull-down resistor). For details, refer to "**Table 3** Input Types of RESX and ON / OFF Pins". The equivalent circuits are shown below.

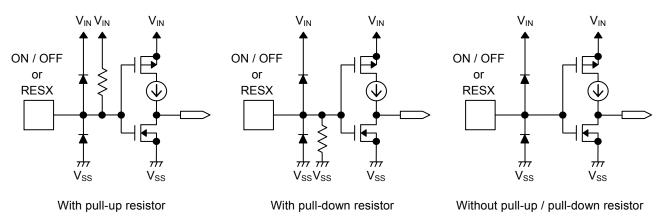


Figure 24 Equivalent Circuits of ON / OFF and RESX Pins

Caution In product without pull-up / pull-down resistor, do not use the ON / OFF and RESX pins in a floating status.

Note that applying voltage of 0.3 V to 1.2 V may increase current consumption.

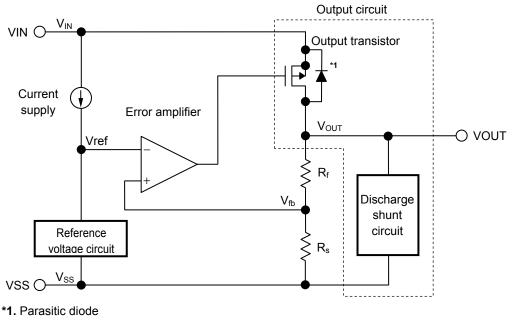
2. Regulator block

2.1 Basic operation

Figure 25 shows a block diagram of the regulator block.

The error amplifier compares the reference voltage (V_{ref}) with feedback voltage (V_{fb}), which is the output voltage resistance-divided by feedback resistors (R_s and R_f). It supplies the gate voltage necessary to maintain the constant output voltage which is not influenced by the input voltage and temperature change, to the output transistor.

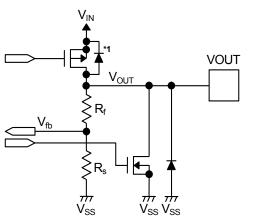
The regulator output voltage (V_{OUT}) of the S-1702 Series can be selected from a value between 1.5 V and 5.5 V.

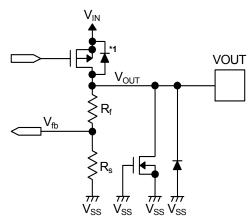




2.2 Output circuit

The output circuit of the regulator block consists of an output transistor and a discharge shunt circuit. The discharge shunt function is enabled or disabled for the VOUT pin. Refer to **"Table 1 Product Types"** for details. The equivalent circuits are shown below.





Discharge shunt function: disabled

Discharge shunt function: enabled

*1. Parasitic diode

Figure 26 Equivalent Circuits of VOUT Pin

2. 2. 1 Output transistor

The S-1702 Series regulator block uses a low on-resistance Pch MOS FET transistor as the output transistor.

Caution Be sure that V_{OUT} does not exceed V_{IN} + 0.3 V to prevent the voltage regulator from being damaged due to inverse current flowing from the VOUT pin through a parasitic diode to the VIN pin, when the potential of V_{OUT} became higher than V_{IN} .

2. 2. 2 Discharge shunt function

The discharge shunt function is enabled in the S-1702Axx, Bxx, Cxx, Exx, Fxx, Gxx, Jxx, Lxx, and Nxx.

When the regulator block is stopped, the output transistor is turned off and the discharge shunt circuit is turned on according to the combination of the ON / OFF and the RESX pins.

This operation causes the charge in the output capacitor (C_L) to be discharged, and forcibly sets the VOUT pin the V_{SS} level.

The VOUT pin is set at the V_{SS} level in a shorter time than the S-1702Dxx, Hxx, Kxx, Mxx, and Pxx, because they disable the discharge shunt function.

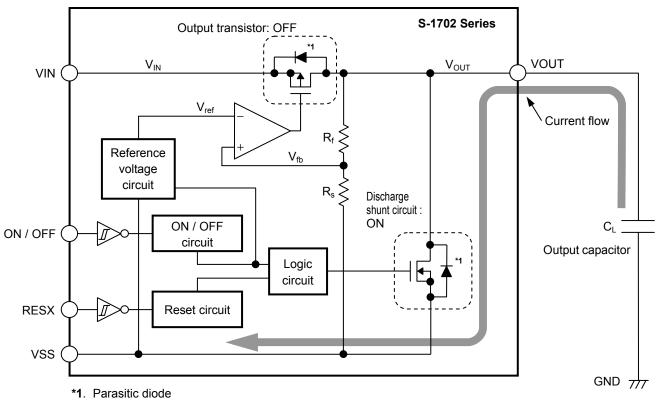


Figure 27 Discharge Shunt Function