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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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S-24CM01C

2-WIRE SERIAL E^{2}PROM

www.sii-ic.com

The S-24CM01C is a 2-wire, low current consumption and wide range operation serial E^{2}PROM. The S-24CM01C has the capacity of 1 M-bit, and the organization is 131072 words × 8-bit. Page write and sequential read are available.

■ Features

- Operating voltage range Read: 1.6 V to 5.5 V
  Write: 1.7 V to 5.5 V
- Page write: 256 bytes / page
- Sequential read
- Operation frequency: 1.0 MHz (V_{CC} = 2.5 V to 5.5 V)
  400 kHz (V_{CC} = 1.6 V to 2.5 V)
- Write time: 5.0 ms max.
- Noise suppression: Schmitt trigger and noise filter on input pins (SCL, SDA)
- Write protect function during the low power supply voltage
- Endurance: 10^6cycles / unit*1 (Ta = +25°C)
- Data retention: 100 years (Ta = +25°C)
- Memory capacity: 1 M-bit
- Write protect: 100%
- Initial shipment data: FFh
- Lead-free (Sn 100%), halogen-free*2

***1.** For each unit (unit: the 4 bytes with the same address of P0, W15 to W2)
***2.** Refer to "■ **Product Name Structure**" for details.

■ Package

- 8-Pin SOP (JEDEC)

Caution **This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to SII Semiconductor Corporation is indispensable.**

■ Pin Configuration

1. 8-Pin SOP (JEDEC)

8-Pin SOP (JEDEC)
Top view

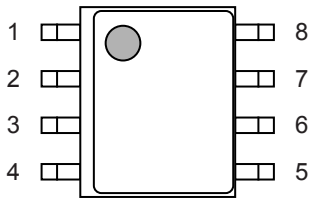


Figure 1

S-24CM01CI-J8T1U4

Table 1

Pin No	Symbol	Description
1	NC*1	No connection
2	A1	Slave address input
3	A2	Slave address input
4	GND	Ground
5	SDA*2	Serial data I/O
6	SCL*2	Serial clock input
7	WP	Write protect input Connected to V_{CC}: Protection valid Open or connected to GND: Protection invalid
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.
***2.** Do not use it in high impedance.

Remark Refer to the "**Package drawings**" for the details.

■ Block Diagram

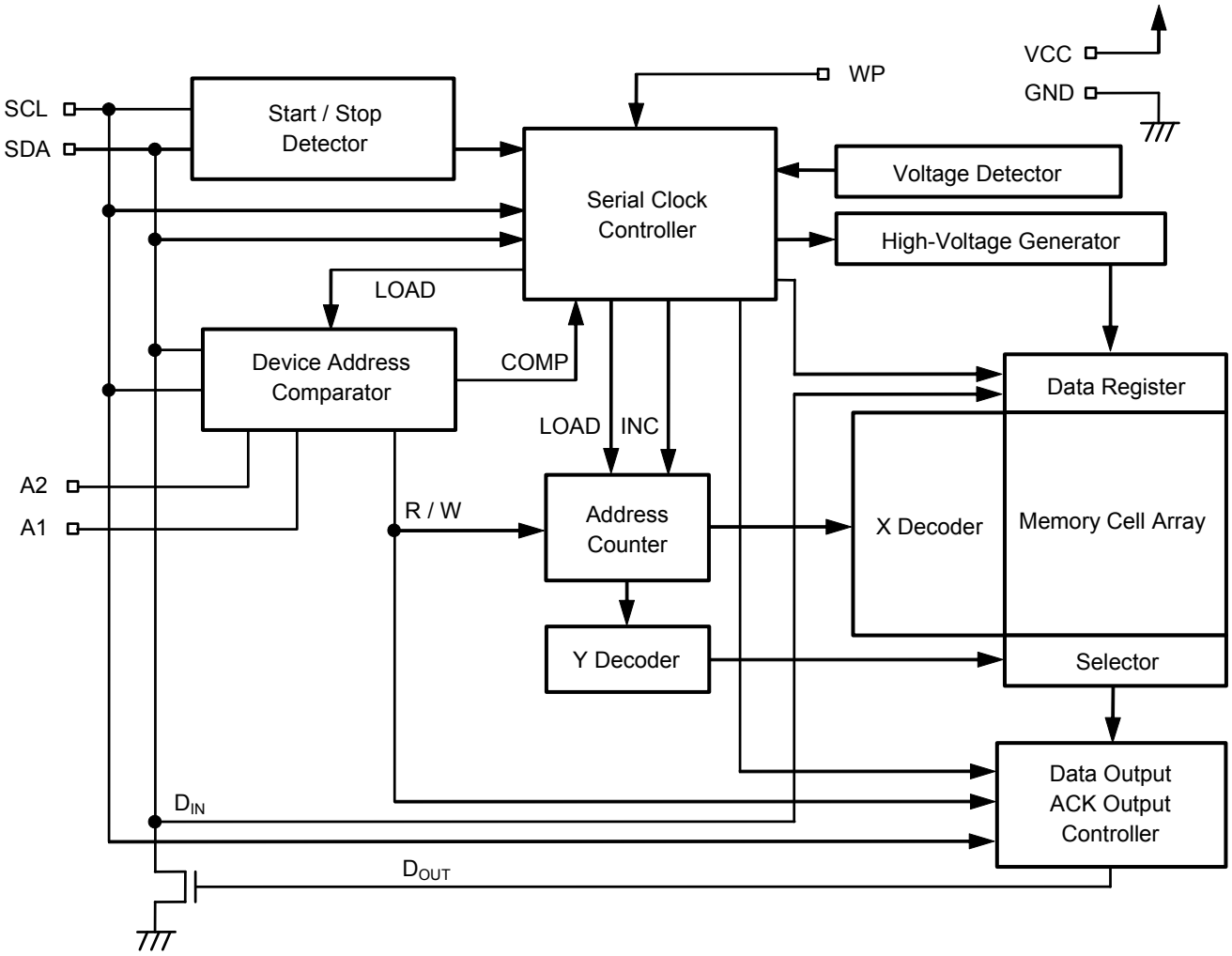


Figure 2

■ Absolute Maximum Ratings

Table 2

Item	Symbol	Absolute Maximum Ratings	Unit
Power supply voltage	V_{CC}	−0.3 to +6.5	V
Input voltage	V_{IN}	−0.3 to +6.5	V
Output voltage	V_{OUT}	−0.3 to +6.5	V
Operation ambient temperature	T_{opr}	−40 to +85	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 3

Item	Symbol	Condition	Ta = −40°C to +85°C		Unit
			Min.	Max.	
Power supply voltage	V_{CC}	Read Operation	1.6	5.5	V
		Write Operation	1.7	5.5	V
High level input voltage	V_{IH}	V_{CC} = 1.8 V to 5.5 V	0.7 × V_{CC}	5.5	V
		V_{CC} = 1.6 V to 1.8 V	0.8 × V_{CC}	5.5	V
Low level input voltage	V_{IL}	V_{CC} = 1.8 V to 5.5 V	−0.3	0.3 × V_{CC}	V
		V_{CC} = 1.6 V to 1.8 V	−0.3	0.2 × V_{CC}	V

■ Pin Capacitance

Table 4

(Ta = +25°C, f = 1.0 MHz, V_{CC} = 5.0 V)

Item	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V (SCL, A1, A2, WP)	−	10	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V (SDA)	−	10	pF

■ Endurance

Table 5

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Endurance	N_W	Ta = +25°C	10^6	−	cycles / unit*1

***1.** For each unit (unit: the 4 bytes with the same address of P0, W15 to W2)

■ Data Retention

Table 6

Item	Symbol	Operation Ambient Temperature	Min.	Max.	Unit
Data retention	−	Ta = +25°C	100	−	year

■ DC Electrical Characteristics

Table 7

Item	Symbol	Condition	Ta = –40°C to +85°C				Unit
			V_{CC} = 2.5 V to 5.5 V f_{SCL} = 1.0 MHz		V_{CC} = 1.6 V to 2.5 V f_{SCL} = 400 kHz		
			Min.	Max.	Min.	Max.	
Current consumption (READ)	I_{CC1}	–	–	2.0	–	1.5	mA

Table 8

Item	Symbol	Condition	Ta = –40°C to +85°C				Unit
			V_{CC} = 2.5 V to 5.5 V f_{SCL} = 1.0 MHz		V_{CC} = 1.7 V to 2.5 V f_{SCL} = 400 kHz		
			Min.	Max.	Min.	Max.	
Current consumption (WRITE)	I_{CC2}	–	–	4.0	–	4.0	mA

Table 9

Item	Symbol	Condition	Ta = –40°C to +85°C				Unit
			V_{CC} = 2.5 V to 5.5 V		V_{CC} = 1.6 V to 2.5 V		
			Min.	Max.	Min.	Max.	
Standby current consumption	I_{SB}	V_{IN} = V_{CC} or GND	–	10.0	–	4.0	µA
Input leakage current 1	I_{LI1}	SCL, SDA, V_{IN} = GND to V_{CC}	–	1.0	–	1.0	µA
Input leakage current 2	I_{LI2}	A1, A2 V_{IN} > 0.7 × V_{CC} At standby mode	–	1.0	–	1.0	µA
Output leakage current	I_{LO}	SDA V_{OUT} = GND to V_{CC}	–	1.0	–	1.0	µA
Input current 1	I_{IL}	WP V_{IN} < 0.3 × V_{CC}	–	50.0	–	50.0	µA
Input current 2	I_{IH}	WP V_{IN} > 0.7 × V_{CC}	–	2.0	–	2.0	µA
Input Impedance 1	Z_{IL}	WP V_{IN} = 0.3 × V_{CC}	30	–	30	–	kΩ
Input Impedance 2	Z_{IH}	WP V_{IN} = 0.7 × V_{CC}	500	–	500	–	kΩ
Low level output voltage	V_{OL}	I_{OL} = 3.2 mA	–	0.4	–	–	V
		I_{OL} = 1.5 mA	–	0.3	–	0.3	V
		I_{OL} = 0.7 mA	–	0.2	–	0.2	V

■ AC Electrical Characteristics

Table 10 Measurement Conditions

Input pulse voltage	$0.2 \times V_{CC}$ to $0.8 \times V_{CC}$
Input pulse rising / falling time	20 ns or less
Output reference voltage	$0.3 \times V_{CC}$ to $0.7 \times V_{CC}$
Output load	100 pF

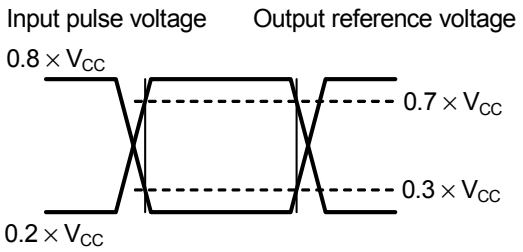


Figure 3 I/O Waveform during AC Measurement

Table 11

Item	Symbol	Ta = –40°C to +85°C				Unit
		V_{CC} = 2.5 V to 5.5 V		V_{CC} = 1.6 V to 2.5 V		
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	1000	0	400	kHz
SCL clock time “L”	t_{LOW}	0.4	–	1.3	–	µs
SCL clock time “H”	t_{HIGH}	0.3	–	0.6	–	µs
SDA output delay time	t_{AA}	0.1	0.5	0.1	0.9	µs
SDA output hold time	t_{DH}	50	–	50	–	ns
Start condition setup time	$t_{SU.STA}$	0.25	–	0.6	–	µs
Start condition hold time	$t_{HD.STA}$	0.25	–	0.6	–	µs
Data input setup time	$t_{SU.DAT}$	80	–	100	–	ns
Data input hold time	$t_{HD.DAT}$	0	–	0	–	ns
Stop condition setup time	$t_{SU.STO}$	0.25	–	0.6	–	µs
SCL, SDA rising time	t_R	–	0.3	–	0.3	µs
SCL, SDA falling time	t_F	–	0.3	–	0.3	µs
WP setup time	t_{WS1}	0	–	0	–	µs
WP hold time	t_{WH1}	0	–	0	–	µs
WP release setup time	t_{WS2}	0	–	0	–	µs
WP release hold time	t_{WH2}	0	–	0	–	µs
Bus release time	t_{BUF}	0.5	–	1.3	–	µs
Noise suppression time	t_I	–	50	–	50	ns

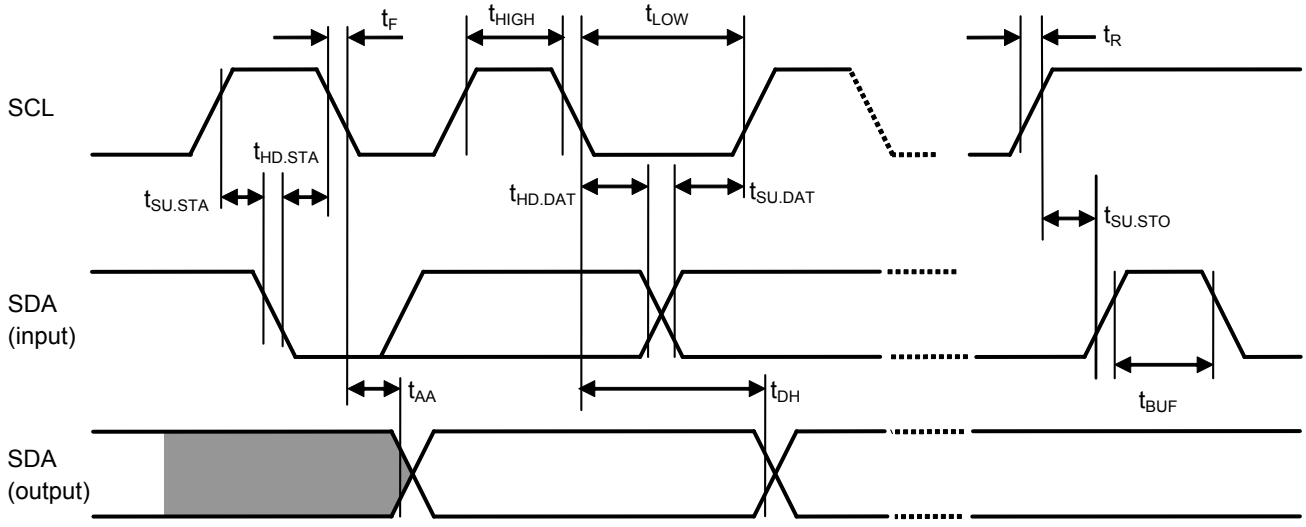


Figure 4 Bus Timing

Table 12

Item	Symbol	Ta = –40°C to +85°C V_{CC} = 1.7 V to 5.5 V		Unit
		Min.	Max.	
Write time	t_{WR}	–	5.0	ms

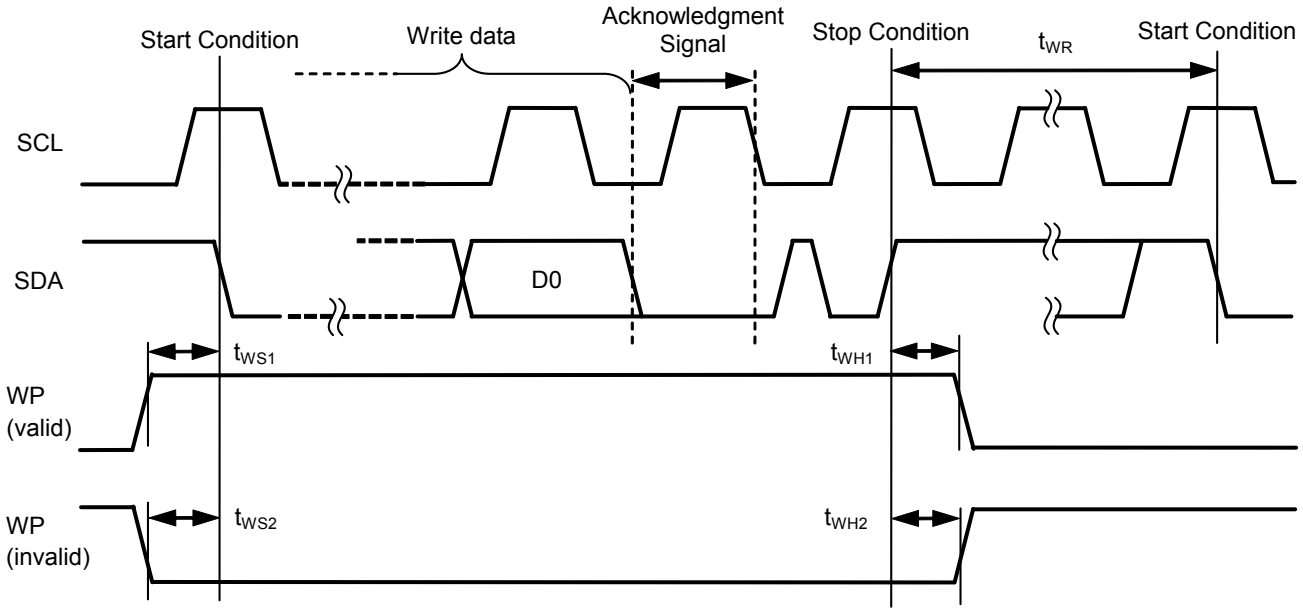


Figure 5 Write Cycle Timing

■ Pin Functions

1. A1 and A2 (Slave address input) pins

In the S-24CM01C, to set the slave address, connect each pin of A1, A2 to GND or V_{CC}. Therefore the users can set 4 types of slave address by a combination of A1, A2 pins.

Comparing the slave address transmitted from the master device and one that you set, makes possible to select the S-24CM01C from other devices connected onto the bus.
Each A1 and A2 pin has a pull-down resistor. In open, these pins have the status when they are connected to GND.

2. SDA (Serial data input / output) pin

The SDA pin is used for the bi-directional transmission of serial data. This pin is a signal input pin, and an Nch open drain output pin.
In use, generally, connect the SDA line to any other device which has the open-drain or open-collector output with Wired-OR connection by pulling up to V_{CC} by a resistor (**Figure 6** shows the relation with an output load).

3. SCL (Serial clock input) pin

The SCL pin is used for the serial clock input. Since the signals are processed at a rising or falling edge of the SCL clock, pay attention to the rising and falling time and comply with the specification.

4. WP (Write protect input) pin

The write protect is enabled by connecting the WP pin to V_{CC}. When not using the write protect, connect this pin to GND or set in open.

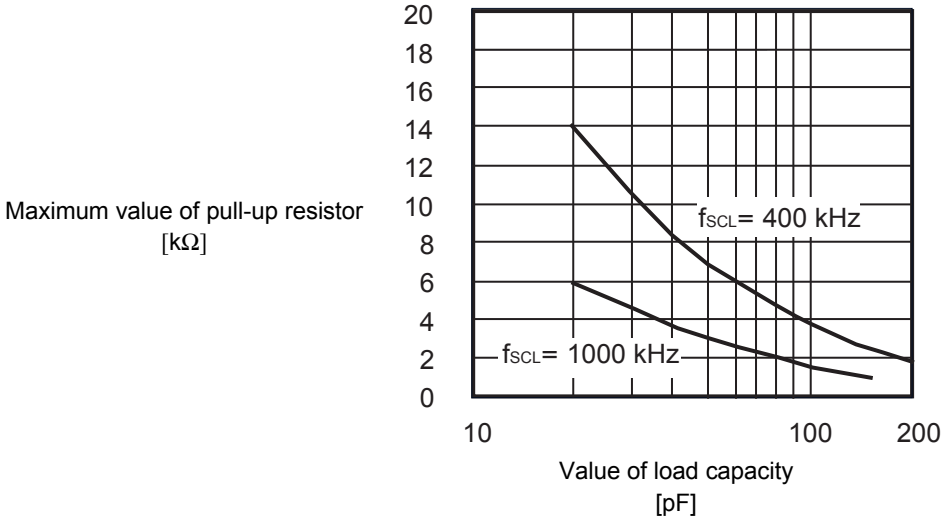


Figure 6 Output Load

■ Initial Shipment Data

Initial shipment data of all addresses is “FFh”.

■ ECC Function (Error correction function)

S-24CM01C Series adds 6 ECC bits for error correction to each 4 bytes with the same address of P0, W15 to W2. The ECC function can make correction and output correct data even if wrong data of 1 bit is in the 4 bytes when reading.
In addition, the S-24CM01C Series rewrites the 4 bytes used as the rewriting minimum unit and 6 ECC bits if only 1 byte data is input.
Therefore, it is recommended to rewrite data of each 4 bytes with the same address of P0, W15 to W2 in order to get the maximum endurance in the application in which the data is rewritten frequently.

■ Operation

1. Start condition

Start is identified by a high to low transition of the SDA line while the SCL line is stable at high.
Every operation begins from a start condition.

2. Stop condition

Stop is identified by a low to high transition of the SDA line while the SCL line is stable at high.
When a device receives a stop condition during a read sequence, the read operation is interrupted, and the device enters standby mode.
When a device receives a stop condition during a write sequence, the reception of the write data is halted, and the S-24CM01C initiates a write cycle.

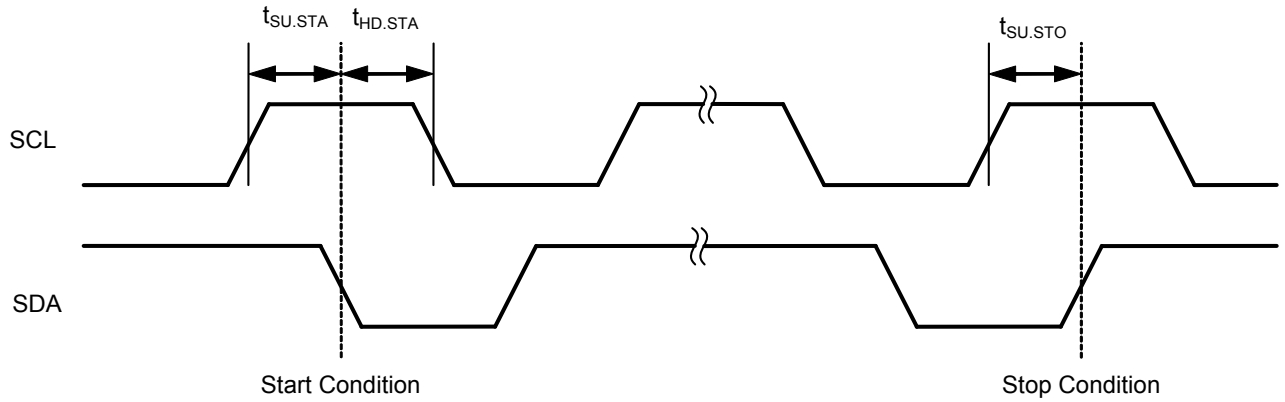


Figure 7 Start / Stop Conditions

3. Data transmission

Changing the SDA line while the SCL line is low, data is transmitted.
Changing the SDA line while the SCL line is high, a start or stop condition is recognized.

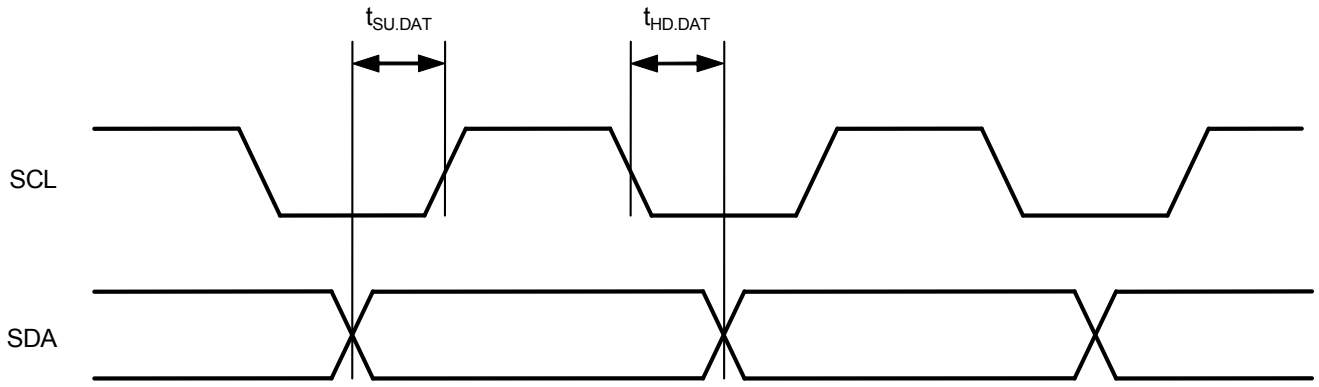


Figure 8 Data Transmission Timing

4. Acknowledge

The unit of data transmission is 8 bits. During the 9th clock cycle period the receiver on the bus pulls down the SDA line to acknowledge the receipt of the 8-bit data.
When an internal write cycle is in progress, the S-24CM01C does not generate an acknowledge.

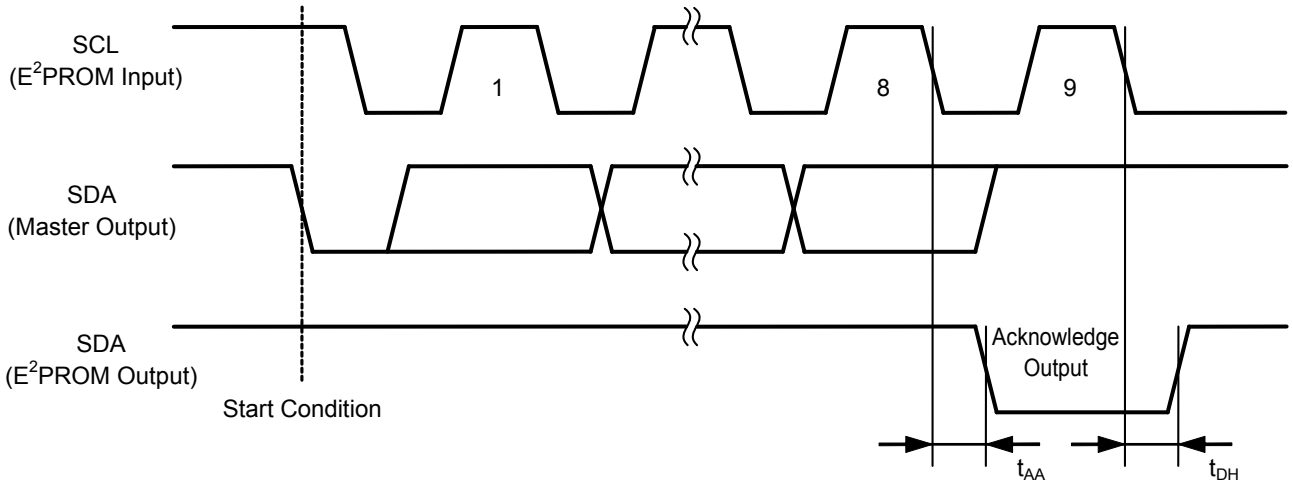


Figure 9 Acknowledge Output Timing

5. Device addressing

To start communication, the master device on the system sends a start condition to the bus line. Next, the master device sends a 7-bit device address and a 1-bit read / write instruction code to the SDA bus.
The upper 4 bits of the device address are the “Device Code”, and are fixed to “1010”.

In the S-24CM01C, 2 bits with successive values are called the “Slave Address”. These bits are used to identify a device on the system bus and are compared with a predetermined value defined by the address input pins (A2 and A1). If the comparison result is a match, the slave device responds with an acknowlede during the 9th clock cycle.
The bit that follows the slave address (P0) is the "Page Address". This bit is used to select one of two 64 K-byte memory blocks (addresses 00000h to 0FFFFh, and addresses 10000h to 1FFFFh).

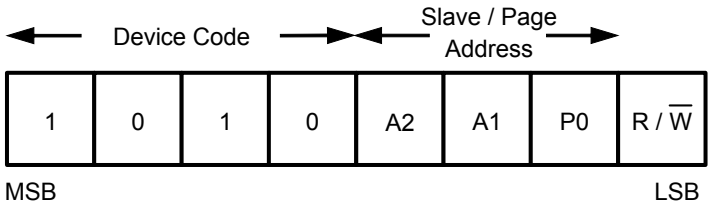


Figure 10 Device Address

6. Write

6. 1 Byte write

When the master sends a 7-bit device address and a 1-bit read / write instruction code set to “0” following a start condition, the S-24CM01C acknowledges it. The S-24CM01C then receives the upper 8-bit word address and responds with an acknowledge. The S-24CM01C then receives the lower 8-bit word address and responds with an acknowledge. After the S-24CM01C receives 8-bit write data and responds with an acknowledge, it receives a stop condition and that initiates the write cycle at the addressed memory.
During the write cycle, all operations are forbidden and no acknowledge is generated.

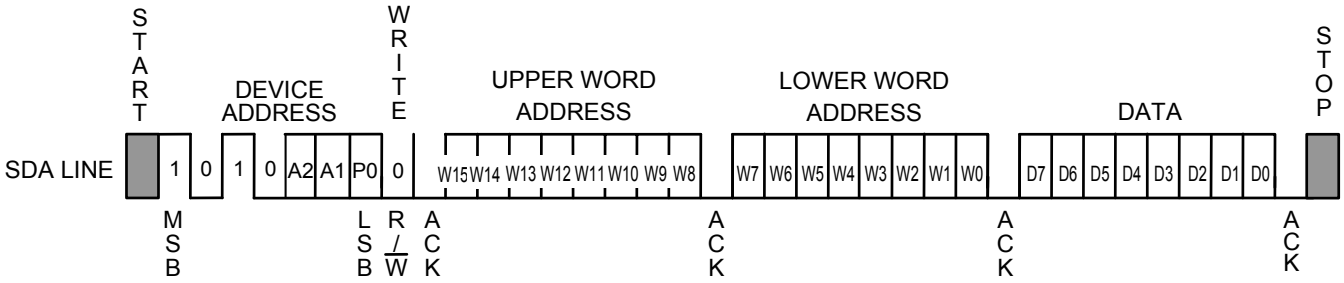


Figure 11 Byte Write

6. 2 Page write

The page write mode allows up to 256 bytes to be written in a single write operation in the S-24CM01C.
The basic process used to transmit data is the same as byte write, but page write involves sequentially receiving as much 8-bit write data as the size of the page.
When the S-24CM01C receives a 7-bit device address and a 1-bit read / write instruction code set to “0” following a start condition, it generates an acknowledge. The S-24CM01C then receives the upper 8-bit word address, and responds with an acknowledge. The S-24CM01C then receives the lower 8-bit word address, and responds with an acknowledge. After the S-24CM01C receives 8-bit write data and responds with an acknowledge, it receives 8-bit write data corresponding to the next word address, and generates an acknowledge. The S-24CM01C repeats reception of 8-bit write data and generation of acknowledges in succession. The S-24CM01C can receive as much write data as the maximum page size.
Receiving a stop condition initiates a write cycle of the area starting from the designated memory address and with a page size equal to the received write data.

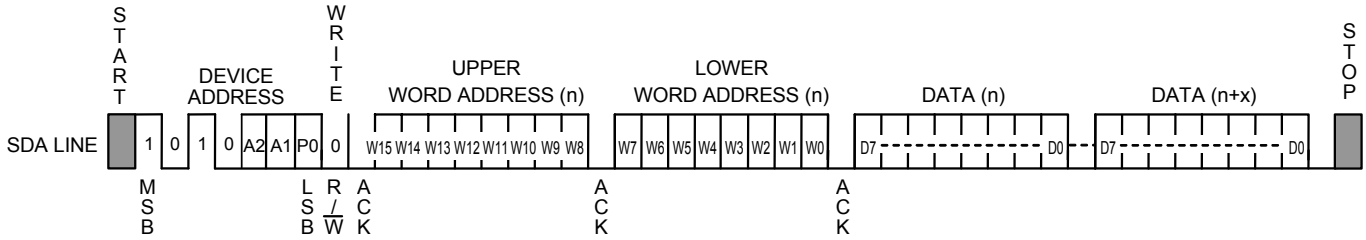


Figure 12 Page Write

In the S-24CM01C, the lower 8 bits of the word address are automatically incremented every time the S-24CM01C receives 8-bit write data. If the size of the write data exceeds 256 bytes, the upper 8 bits of the word address and the page address (P0) remain unchanged, and the lower 8 bits are rolled over so that the last 256-byte data that the S-24CM01C received is overwritten.

6. 3 Write protect

Write protect is available in the S-24CM01C. When the WP pin is connected to the V_{CC}, write operation to memory area is inhibited.
When the WP pin is connected to GND or set in open, the write protect is invalid, and write operation in all memory area is available.
Fix the level of the WP pin from start condition in the write operation (byte write, page write) until stop condition. If the WP pin changes during this time, the address data being written at this time is not guaranteed. Regarding the timing of write protect, refer to **Figure 5**.
In not using the write protect, connect the WP pin to GND or set it open. The write protect is valid in the range of operation power supply voltage.
As seen in **Figure 13** when the write protect is valid, the S-24CM01C does not generate an acknowledgment signal after data input.

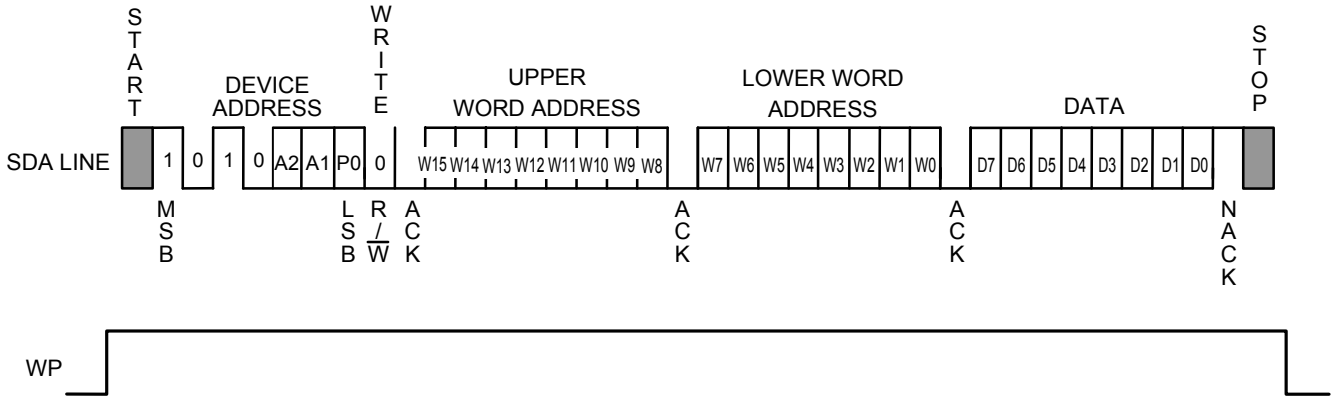
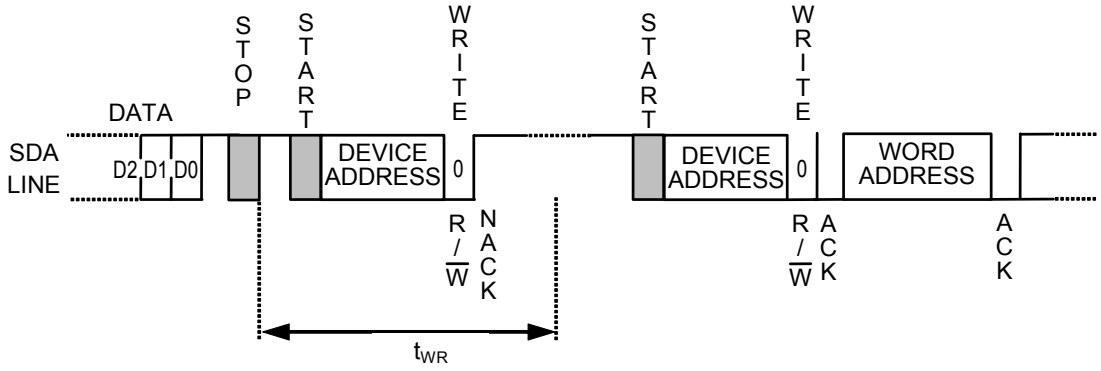


Figure 13 Write Protect

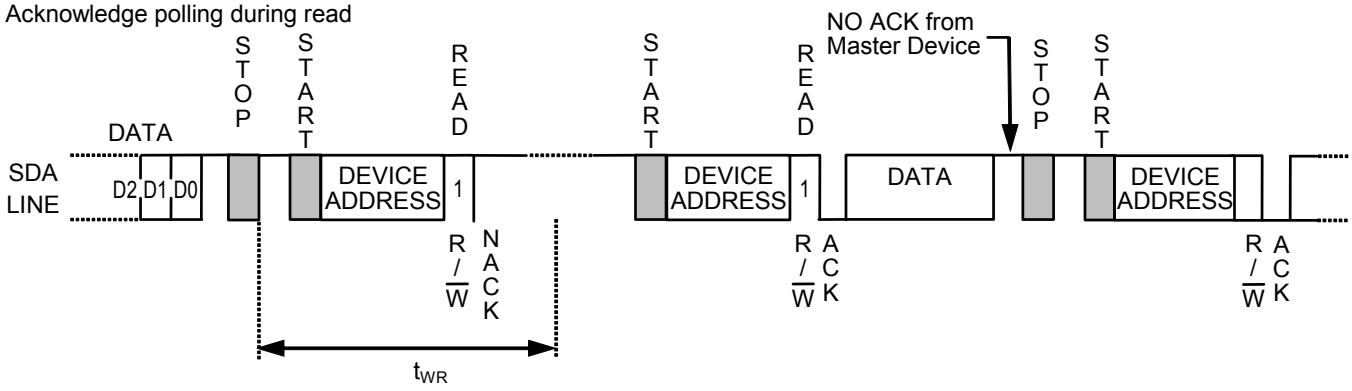
6. 4 Acknowledge polling

Acknowledge polling is used to know the completion of the write cycle in the S-24CM01C.
After the S-24CM01C receives a stop condition and once the write cycle starts, all operations are inhibited and no response is made to the signal transmitted by the master device.
Accordingly the master device can recognize the completion of the write cycle in the S-24CM01C by detecting a response from the slave device after transmitting the start condition, the device address and the read / write instruction code to the S-24CM01C (slave device).
That is, if the S-24CM01C does not generate an acknowledgment signal, the write cycle is in progress and if the S-24CM01C generates an acknowledgment signal, the write cycle has been completed.
It is recommended to use the read instruction "1" as the read / write instruction code transmitted by the master device.

Acknowledge polling during write



Acknowledge polling during read



Remark Users are able to input word address and data after ACK output in acknowledge polling during write.
Users are able to read data after ACK output in acknowledge polling during read. However, after that users input the write instruction, a start condition may not be input during data output. Input a stop condition and the next instruction after data output and ACK output.

Figure 14 Usage Example of Acknowledge Polling

7. Read

7. 1 Current address read

Either in writing or in reading, the S-24CM01C holds the last accessed memory address. The memory address is maintained as long as the power voltage does not decrease less than the operating voltage.
The master device can read the data at the memory address of the current address pointer without assigning the word address as a result, when it recognizes the position of the address pointer in the S-24CM01C. This is called "Current Address Read".
In the following, the address counter in the S-24CM01C is assumed to be "n".
When the S-24CM01C receives a 7-bit device address and a 1-bit read / write instruction code set to "1" following a start condition, it responds with an acknowledge.
Next, an 8-bit data at the address "n" is sent from the S-24CM01C synchronous to the SCL clock. The address counter is incremented and the content of the address counter becomes n + 1.
The master device outputs stop condition not an acknowledge, the reading of S-24CM01C is ended.

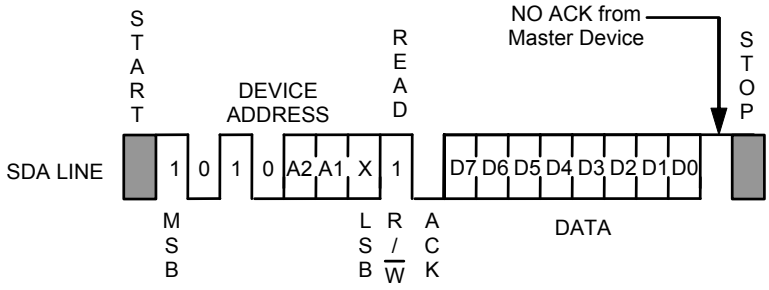


Figure 15 Current Address Read

Attention should be paid to the following point on the recognition of the address pointer in the S-24CM01C.
When reading, the memory address counter in the S-24CM01C is automatically incremented after the 8th bit of data is output. When writing, on the other hand, the upper bits of the memory address (the upper bits of the word address and the page address*1) are left unchanged and are not incremented.

***1.** The upper 8 bits of the word address and the page address (P0)

7. 2 Random read

Random read is used to read the data at an arbitrary memory address.
A dummy write is performed to load the memory address into the address counter.
When the S-24CM01C receives a 7-bit device address and a 1-bit read / write instruction code set to “0” following a start condition, it responds with an acknowledge.
The S-24CM01C then receives a upper 8-bit word address and responds with an acknowledge. And the S-24CM01C receives a lower 8-bit word address and responds with an acknowledge. The memory address is loaded to the address counter in the S-24CM01C by these operations. Reception of write data does not follow in a dummy write whereas reception of write data follows in byte write and in page write.
Since the memory address is loaded into the memory address counter by dummy write, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition and performing the same operation in the current address read.
That is, when the S-24CM01C receives a 7-bit device address and a 1-bit read / write instruction code set to “1”, following a start condition signal, it responds with an acknowledge. Next, 8-bit data is transmitted from the S-24CM01C in synchronous to the SCL clock. The master device outputs stop condition not an acknowledge, the reading of S-24CM01C is ended.

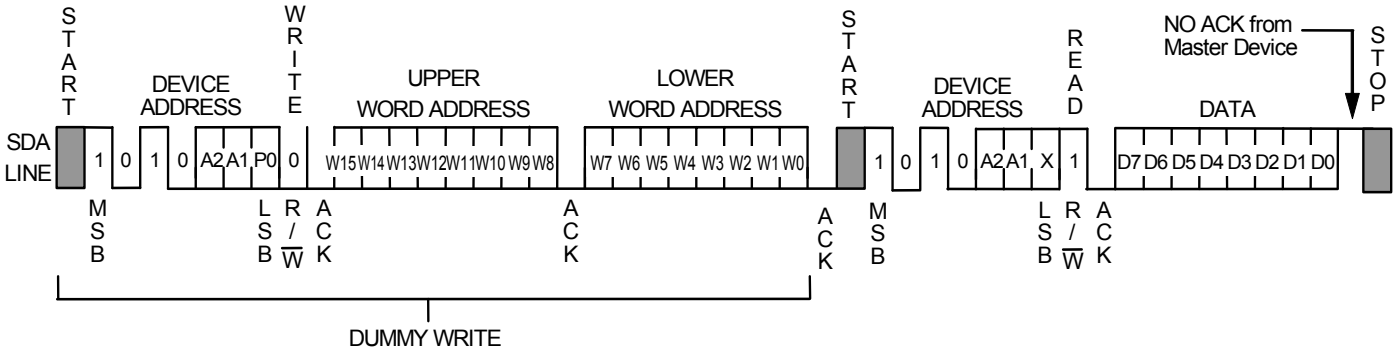


Figure 16 Random Read

7. 3 Sequential read

When the S-24CM01C receives a 7-bit device address and a 1-bit read / write instruction code set to “1” following a start condition both in current address read and random read, it responds with an acknowledge.
When an 8-bit data is output from the S-24CM01C synchronous to the SCL clock, the address counter is automatically incremented.
When the master device responds with an acknowledge, the data at the next memory address is transmitted. Response with an acknowledge by the master device has the memory address counter in the S-24CM01C incremented and makes it possible to read data in succession. This is called “Sequential Read”.
The master device outputs stop condition not an acknowledge, the reading of S-24CM01C is ended.
Data can be read in succession in the sequential read mode. When the memory address counter reaches the last word address, it rolls over to the first word address.

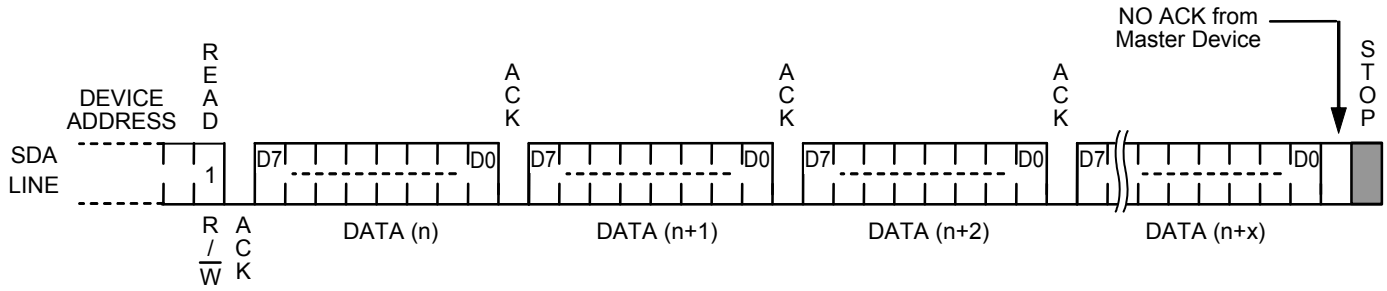


Figure 17 Sequential Read

■ Write Protect Function during the Low Power Supply Voltage

The S-24CM01C has a built-in detection circuit which operates with the low power supply voltage, cancels Write when the power supply voltage drops and power-on. Its detection and release voltages are 1.50 V typ. (Refer to **Figure 18**).
The S-24CM01C cancels Write by detecting a low power supply voltage when it receives a stop condition.
In the data trasmission and the Write operation, data in the address written during the low power supply voltage is not assurable.

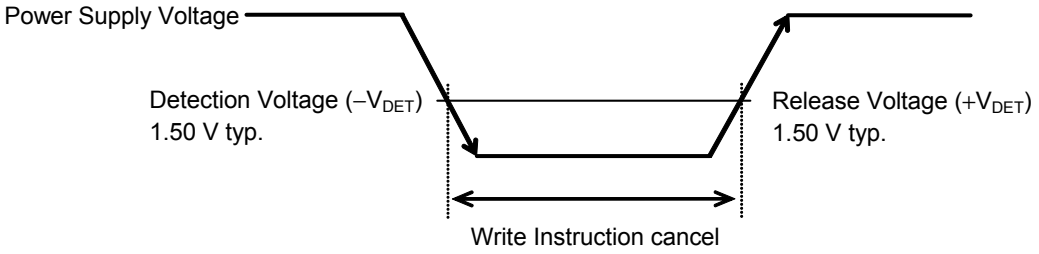


Figure 18 Operation during Low Power Supply Voltage

■ Using S-24CM01C

1. Adding a pull-up resistor to SDA I/O pin and SCL input pin

In consideration of I²C-bus protocol function, the SDA I/O pins should be connected with a pull-up resistor. The S-24CM01C cannot transmit normally without using a pull-up resistor.

In case that the SCL input pin of the S-24CM01C is connected to the Nch open drain output pin of the master device, connect the SCL pin with a pull-up resistor. As well, in case the SCL input pin of the S-24CM01C is connected to the tri-state output pin of the master device, connect the SCL pin with a pull-up resistor in order not to set it in high impedance. This prevents the S-24CM01C from error caused by an uncertain output (high impedance) from the tri-state pin when resetting the master device during the voltage drop.

2. Equivalent circuit of input and I/O pin

The S-24CM01C does not have a built-in pull-down or pull-up resistor for the SCL and SDA pins. The WP, A2, and A1 pins have a pull-down resistor. The SDA pin has an open-drain output. The following are equivalent circuits of the pins.

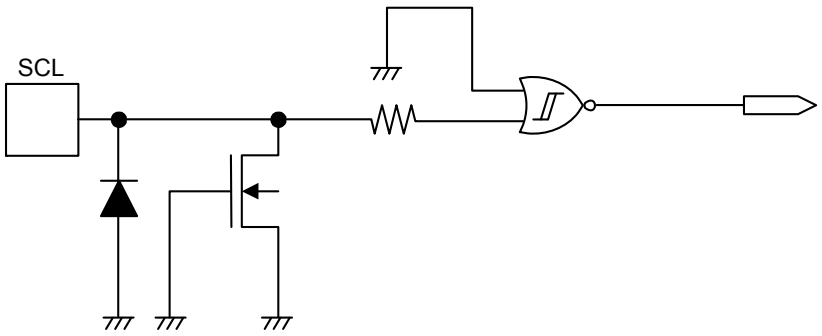


Figure 19 SCL Pin

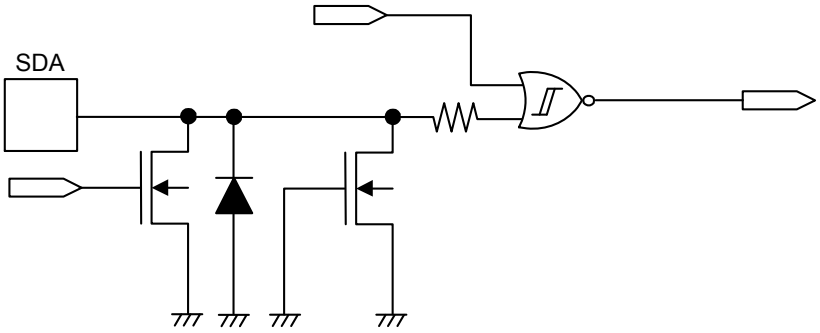


Figure 20 SDA Pin

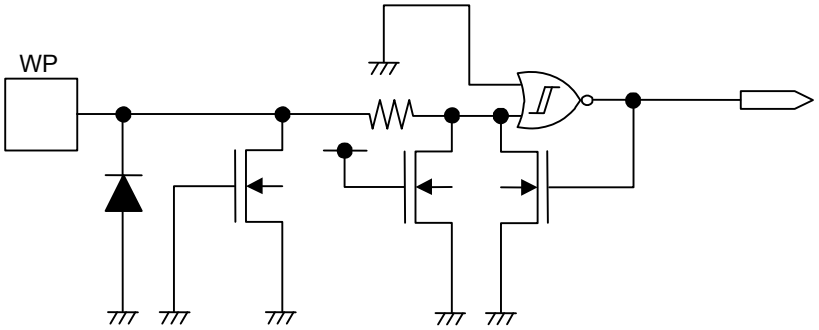


Figure 21 WP Pin

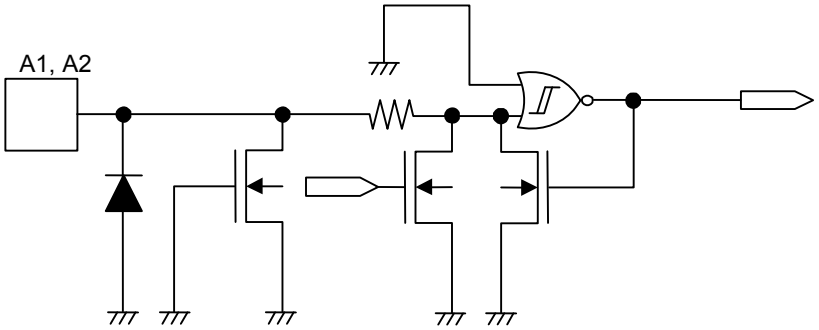


Figure 22 A1, A2 Pins

3. Phase adjustment during S-24CM01C access

The S-24CM01C does not have a pin to reset (the internal circuit). The users cannot forcibly reset it externally. If the communication to the S-24CM01C interrupted, the users need to handle it as you do for software.
In the S-24CM01C, users are able to reset the internal circuit by inputting a start condition and a stop condition.
Although the reset signal is input to the master device, the S-24CM01C's internal circuit does not go in reset, but it does by inputting a stop condition to the S-24CM01C. The S-24CM01C keeps the same status thus cannot do the next operation. Especially, this case corresponds to that only the master device is reset when the power supply voltage drops.
If the power supply voltage restored in this status, input the instruction after resetting (adjusting the phase with the master device) the S-24CM01C. How to reset is shown below.

[How to reset S-24CM01C]

The S-24CM01C is able to be reset by a start and stop instructions. When the S-24CM01C is reading data "0" or is outputting the acknowledgment signal, outputs "0" to the SDA line. In this status, the master device cannot output an instruction to the SDA line. In this case, terminate the acknowledgment output operation or the Read operation, and then input a start instruction. **Figure 23** shows this procedure.
First, input a start condition. Then transmit 9 clocks (dummy clock) of SCL. During this time, the master device sets the SDA line to "H". By this operation, the S-24CM01C interrupts the acknowledgment output operation or data output, so input a start condition*1. When a start condition is input, the S-24CM01C is reset. To make doubly sure, input the stop condition to the S-24CM01C. The normal operation is then possible.

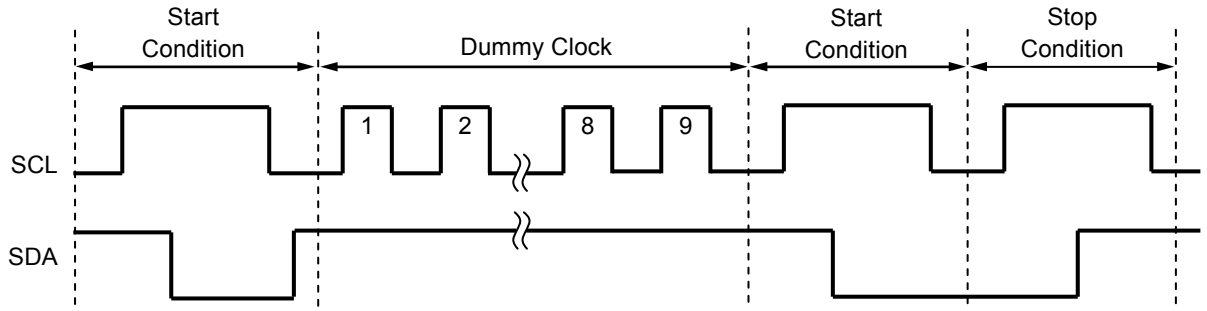


Figure 23 Resetting S-24CM01C

***1.** After 9 clocks (dummy clock), if the SCL clock continues to being output without inputting a start condition, S-24CM01C may go in the write operation when it receives a stop condition. To prevent this, input a start condition after 9 clocks (dummy clock).

Remark Regarding this reset procedure with dummy clock, it is recommended to perform at the system initialization after applying the power supply voltage.

4. Acknowledge check

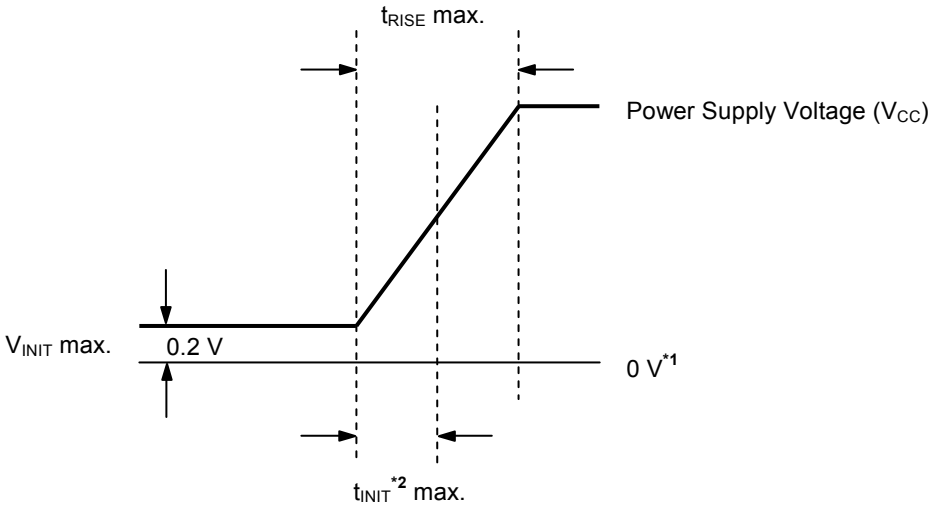
The I²C-bus protocol includes an acknowledge check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the master device and S-24CM01C. This function is effective to prevent malfunction, so it is recommended to perform an acknowledge check with the master device.

5. Built-in power-on-clear circuit

The S-24CM01C has a built-in power-on-clear circuit that initializes itself at the same time during power-on. Unsuccessful initialization may cause a malfunction. To operate the power-on-clear circuit normally, the following conditions must be satisfied to raise the power supply voltage.

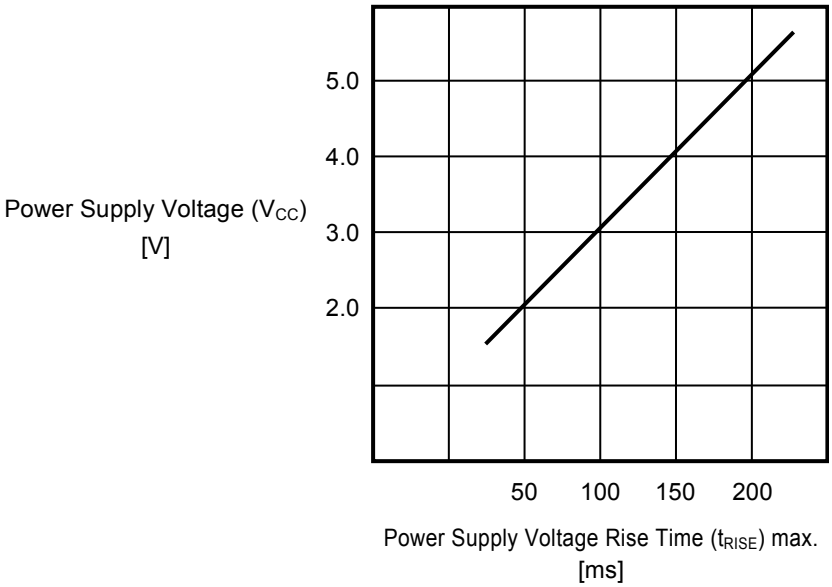
5. 1 Raising power supply voltage

Shown in **Figure 24**, raise the power supply voltage from 0.2 V max., within the time defined as t_{RISE} which is the time required to reach the power supply voltage to be set.
For example, if the power supply voltage is 5.0 V, t_{RISE} = 200 ms seen in **Figure 25**. The power supply voltage must be raised within 200 ms.



***1.** 0 V means there is no difference in potential between the VCC pin and the GND pin of the S-24CM01C.
***2.** t_{INIT} is the time required to initialize the S-24CM01C. No instructions are accepted during this time.

Figure 24 Raising Power Supply Voltage



For example: If the power supply voltage = 5.0 V, raise the power supply voltage to 5.0 V within 200 ms.

Figure 25 Power Supply Voltage Rise Time

When initialization is successfully completed by the power-on-clear circuit, the S-24CM01C enters the standby status.
If the power-on-clear circuit does not operate;
The S-24CM01C has not completed initialization, an instruction previously input is still valid or an instruction may be inappropriately recognized. In this case, S-24CM01C may perform the Write operation.
The voltage drops due to power off while the S-24CM01C is being accessed. Even if the master device is reset due to the low power voltage, the S-24CM01C may malfunction unless the power-on-clear operation conditions of S-24CM01C are satisfied.

When not keeping to the power supply voltage rise time seen in **Figure 25**, adjust the phase (reset) to reset the internal circuit in the S-24CM01C normally.

5. 2 Initialization time

The S-24CM01C initializes at the same time when the power supply voltage is raised. Input instructions to the S-24CM01C after initialization. S-24CM01C does not accept any instruction during initialization. **Figure 26** shows the initialization time of the S-24CM01C.

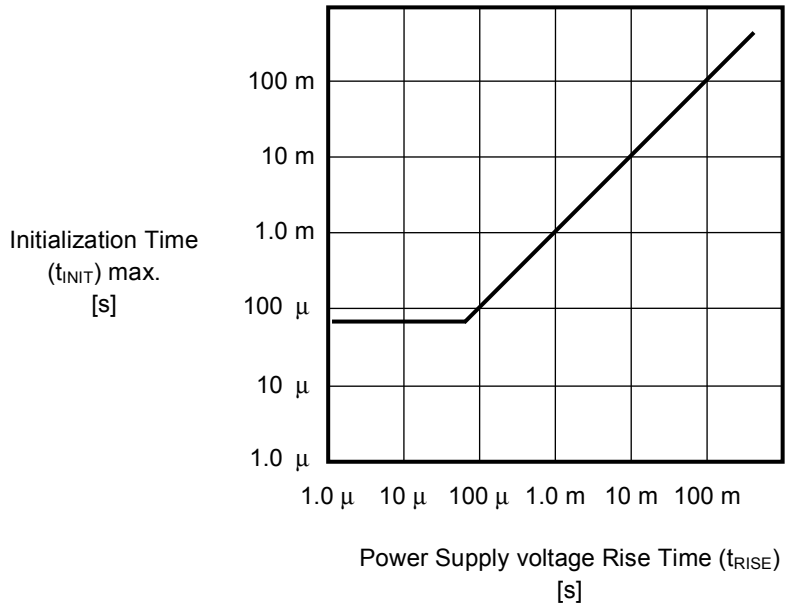


Figure 26 Initialization Time of S-24CM01C