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2-WIRE CMOS SERIAL E^{2}PROM S-24CS01A/02A/04A/08A

The S-24CS01A/02A/04A/08A is a 2-wired, low power and wide range operation 1-Kbit, 2-Kbit, 4-Kbit and 8-Kbit E^{2}PROM organized as 128 words × 8 bits, 256 words × 8 bits, 512 words × 8 bits and 1024 words × 8 bits in each.
Page write and sequential read are available.

■ Features

- Low power consumption Standby : 2.0 μA Max. (V_{CC}=5.5 V)
  Read : 0.8 mA Max. (V_{CC}=5.5 V)
- Operating voltage range Read : 1.8 to 5.5 V (at −40 to +85°C)
  Write : 2.55 to 5.5 V (at −40 to +85°C)
- Page write : 8 bytes / page (S-24CS01A/02A)
  16 bytes / page (S-24CS04A/08A)
- Sequential read
- Operating Frequency : 400 kHz (V_{CC} = 2.55 to 5.5 V, at −40 to +85°C)
- Write disable function when power supply voltage is low
- Endurance: 10^7 cycles/word*1 (at +25°C) write capable,
  10^6 cycles/word*1 (at +85°C)
  3×10^5 cycles/word*1 (at +105°C)
  ***1.** For each address (Word: 8 bits)
- Data retention: 10 years (after rewriting 10^6 cycles/word at +85°C)
- S-24CS01A : 1 Kbit
- S-24CS02A : 2 Kbit
- S-24CS04A : 4 Kbit
- S-24CS08A : 8 Kbit
- High-temperature operation : +105°C Max. supported
  (Only S-24CS0xAFJ-TBH-G, S-24CS0xAFT-TBH-G)
- Write protection : 100%
- Lead-free product

■ Packages

Package name	Drawing code			
	Package	Tape	Reel	Land
8-Pin DIP	DP008-F	—	—	—
8-Pin SOP(JEDEC)	FJ008-A	FJ008-D	FJ008-D	—
8-Pin TSSOP	FT008-A	FT008-E	FT008-E	—
SNT-8A	PH008-A	PH008-A	PH008-A	PH008-A

Caution This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to SII is indispensable.

■ Pin Configurations

8-Pin DIP
Top view

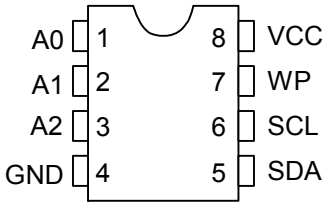


Figure 1

S-24CS01ADP-G
S-24CS02ADP-G
S-24CS04ADP-G
S-24CS08ADP-1G

Table 1

Pin No.	Symbol	Description
1	A0	Address input (No connection in S-24CS04A/08A*1)
2	A1	Address input (No connection in S-24CS08A*1)
3	A2	Address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.

Remark See Dimensions for details of the package drawings.

8-Pin SOP(JEDEC)
Top view

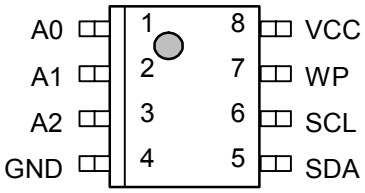


Figure 2

S-24CS01AFJ-TB-G
S-24CS01AFJ-TBH-G
S-24CS02AFJ-TB-G
S-24CS02AFJ-TBH-G
S-24CS04AFJ-TB-G
S-24CS04AFJ-TBH-G
S-24CS08AFJ-TB-1G
S-24CS08AFJ-TBH-1G

Table 2

Pin No.	Symbol	Description
1	A0	Address input (No connection in S-24CS04A/08A*1)
2	A1	Address input (No connection in S-24CS08A*1)
3	A2	Address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.

Remark See Dimensions for details of the package drawings.

8-Pin TSSOP
Top view

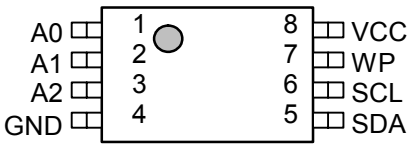


Figure 3

S-24CS01AFT-TB-G
S-24CS01AFT-TBH-G
S-24CS02AFT-TB-G
S-24CS02AFT-TBH-G
S-24CS04AFT-TB-G
S-24CS04AFT-TBH-G
S-24CS08AFT-TB-1G
S-24CS08AFT-TBH-1G

Table 3

Pin No.	Symbol	Description
1	A0	Address input (No connection in S-24CS04A/08A*1)
2	A1	Address input (No connection in S-24CS08A*1)
3	A2	Address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.

Remark See Dimensions for details of the package drawings.

SNT-8A
Top view

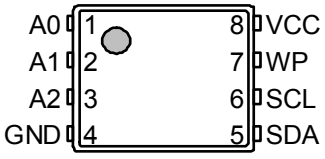


Figure 4

S-24CS01APH-TF-G
S-24CS02APH-TF-G
S-24CS04APH-TF-G

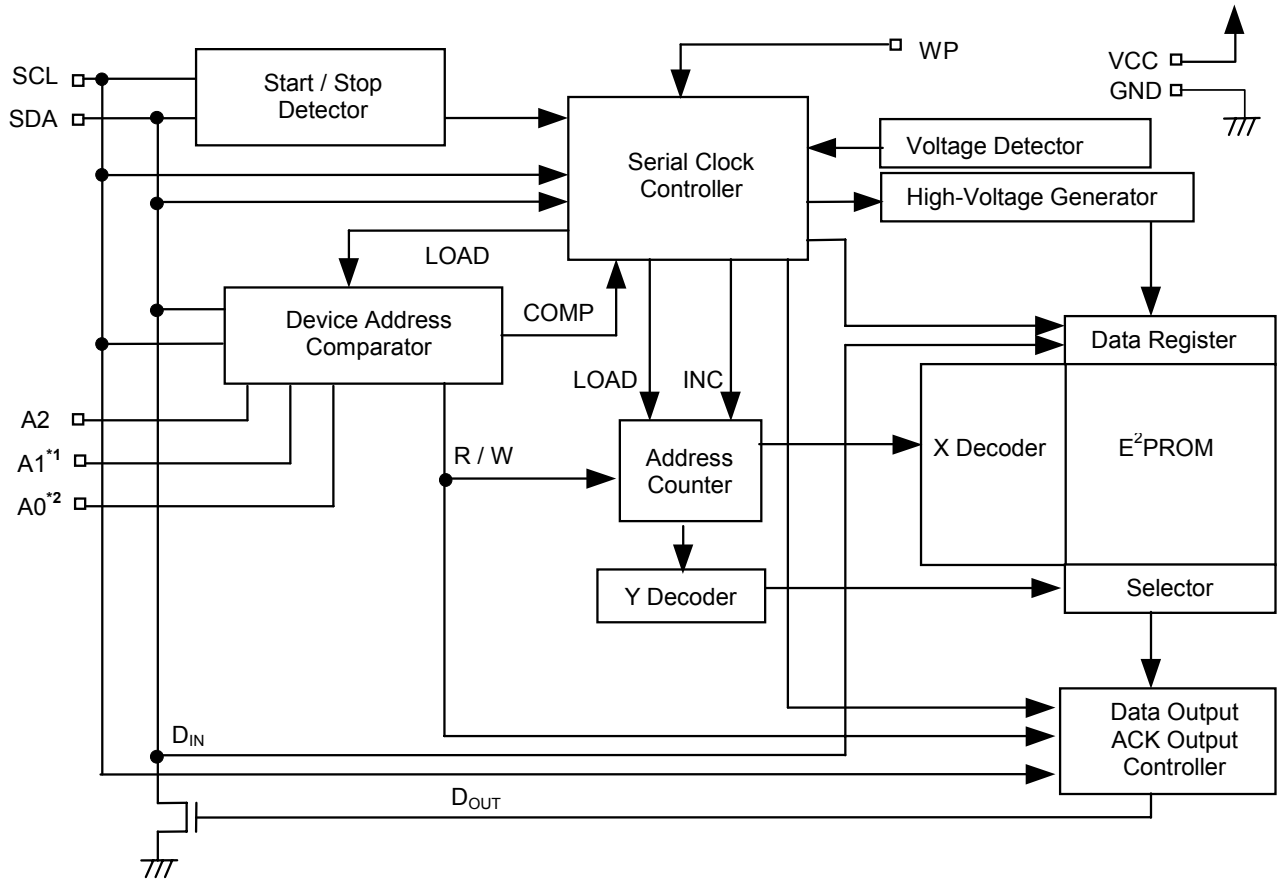
Table 4

Pin No.	Symbol	Description
1	A0	Address input (No connection in S-24CS04A*1)
2	A1	Address input
3	A2	Address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.

Remark See Dimensions for details of the package drawings.

■ Block diagram



***1.** This pin is not available for S-24CS08A.
***2.** This pin is not available for S-24CS04A/08A.

Figure 5

■ Absolute Maximum Ratings

Table 5

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC}	V
Operating ambient temperature	T_{opr}	−40 to +105	°C
Storage temperature	T_{stg}	−65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 6

Item	Symbol	Conditions	−40 to +85°C			+85 to +105°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Power supply voltage	V_{CC}	Read Operation	1.8	—	5.5	4.5	—	5.5	V
		Write Operation	2.55	—	5.5	4.5	—	5.5	V
High level input voltage	V_{IH}	V_{CC}=4.5 to 5.5 V	0.7×V_{CC}	—	V_{CC}	0.7×V_{CC}	—	V_{CC}	V
		V_{CC}=2.55 to 4.5 V	0.7×V_{CC}	—	V_{CC}	—	—	—	V
		V_{CC}=1.8 to 2.55 V	0.8×V_{CC}	—	V_{CC}	—	—	—	V
Low level input voltage	V_{IL}	V_{CC}=4.5 to 5.5 V	0.0	—	0.3×V_{CC}	0.0	—	0.3×V_{CC}	V
		V_{CC}=2.55 to 4.5 V	0.0	—	0.3×V_{CC}	—	—	—	V
		V_{CC}=1.8 to 2.55 V	0.0	—	0.2×V_{CC}	—	—	—	V

■ Pin Capacitance

Table 7

(Ta=25°C, f=1.0 MHz, V_{CC}=5 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0 V (S-24CS01A/02A: SCL, A0, A1, A2, WP)	—	—	10	pF
		V_{IN}=0 V (S-24CS04A: SCL, A1, A2, WP)	—	—	10	pF
		V_{IN}=0 V (S-24CS08A: SCL, A2, WP)	—	—	10	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$=0 V (SDA)	—	—	10	pF

■ Endurance

Table 8

Item	Symbol	Operation temperature	Min.	Typ.	Max.	Unit
Endurance	N_W	−40 to +85°C	10^6	—	—	cycles / word*1
		+85 to +105°C	3×10^5	—	—	cycles / word*1

***1.** For each address (Word: 8 bits)

■ DC Electrical Characteristics

Table 9

Item	Symbol	Conditions	–40 to +85°C									+85 to +105°C			Unit
			V_{CC}=4.5 to 5.5 V f = 400 kHz			V_{CC}=2.7 to 4.5 V*1 f = 100 kHz			V_{CC}=1.8 to 2.7 V f = 100 kHz			V_{CC}=4.5 to 5.5 V f = 350 kHz			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	—	—	—	0.8	—	—	0.3	—	—	0.2	—	—	0.8	mA
Current consumption (WRITE)	I_{CC2}	—	—	—	4.0	—	—	1.5	—	—	—	—	—	4.0	mA

***1.** V_{CC}=2.55 to 4.5 V in Write

Table 10

Item	Symbol	Conditions	–40 to +85°C									+85 to +105°C			Unit
			V_{CC}=4.5 to 5.5 V			V_{CC}=2.55 to 4.5 V			V_{CC}=1.8 to 2.55 V			V_{CC}=4.5 to 5.5 V			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	V_{IN}=V_{CC} or GND	—	—	2.0	—	—	2.0	—	—	2.0	—	—	2.0	µA
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	µA
Output leakage current	I_{LO}	V_{OUT}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	µA
Low level output voltage	V_{OL}	I_{OL}=3.2 mA	—	—	0.4	—	—	0.4	—	—	—	—	—	0.4	V
		I_{OL}=1.5 mA	—	—	0.3	—	—	0.3	—	—	0.5	—	—	0.3	V
Current address hold voltage	V_{AH}	—	1.5	—	5.5	1.5	—	4.5	1.5	—	2.55	1.5	—	5.5	V

■ AC Electrical Characteristics

Table 11 Measurement Conditions

Input pulse voltage	$0.1\times V_{CC}$ to $0.9\times V_{CC}$
Input pulse rising / falling time	20 ns
Output judgment voltage	$0.5\times V_{CC}$
Output load	100 pF+ Pull-up resistor 1.0 kΩ

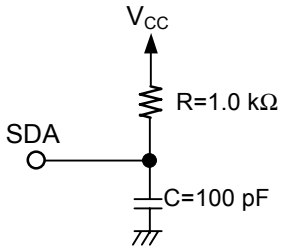


Figure 6 Output Load Circuit

Table 12

Item	Symbol	−40 to +85°C									+85 to +105°C			Unit
		V_{CC}=4.5 to 5.5 V			V_{CC}=2.55 to 4.5 V			V_{CC}=1.8 to 2.55 V			V_{CC}=4.5 to 5.5 V			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	0	—	400	0	—	400	0	—	100	0	—	350	kHz
SCL clock time "L"	t_{LOW}	1.0	—	—	1.0	—	—	4.7	—	—	1.1	—	—	µs
SCL clock time "H"	t_{HIGH}	0.9	—	—	0.9	—	—	4.0	—	—	1.0	—	—	µs
SDA output delay time	t_{AA}	0.1	—	0.9	0.1	—	0.9	0.1	—	3.5	0.1	—	1.0	µs
SDA output hold time	t_{DH}	50	—	—	50	—	—	100	—	—	50	—	—	ns
Start condition setup time	$t_{SU.STA}$	0.6	—	—	0.6	—	—	4.7	—	—	0.6	—	—	µs
Start condition hold time	$t_{HD.STA}$	0.6	—	—	0.6	—	—	4.0	—	—	0.6	—	—	µs
Data input setup time	$t_{SU.DAT}$	100	—	—	100	—	—	200	—	—	100	—	—	ns
Data input hold time	$t_{HD.DAT}$	0	—	—	0	—	—	0	—	—	0	—	—	ns
Stop condition setup time	$t_{SU.STO}$	0.6	—	—	0.6	—	—	4.0	—	—	0.6	—	—	µs
SCL, SDA rising time	t_R	—	—	0.3	—	—	0.3	—	—	1.0	—	—	0.3	µs
SCL, SDA falling time	t_F	—	—	0.3	—	—	0.3	—	—	0.3	—	—	0.3	µs
Bus release time	t_{BUF}	1.3	—	—	1.3	—	—	4.7	—	—	1.3	—	—	µs
Noise suppression time	t_I	—	—	50	—	—	100	—	—	100	—	—	50	ns

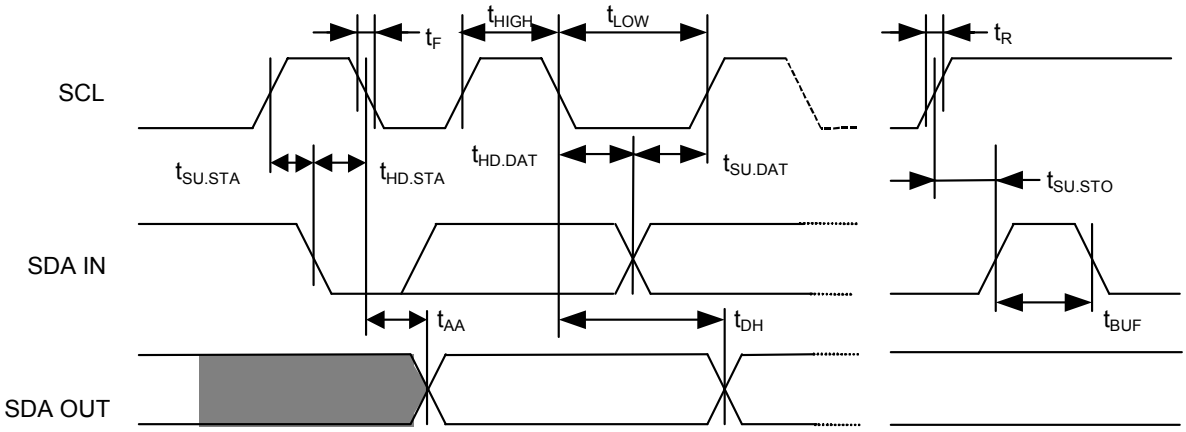


Figure 7 Bus Timing

Table 13

Item	Symbol	−40 to +85°C			+85 to +105°C			Unit
		V_{CC}=2.55 to 5.5 V			V_{CC}=4.5 to 5.5 V			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Write time	t_{WR}	—	4.0	10.0	—	4.0	10.0	ms

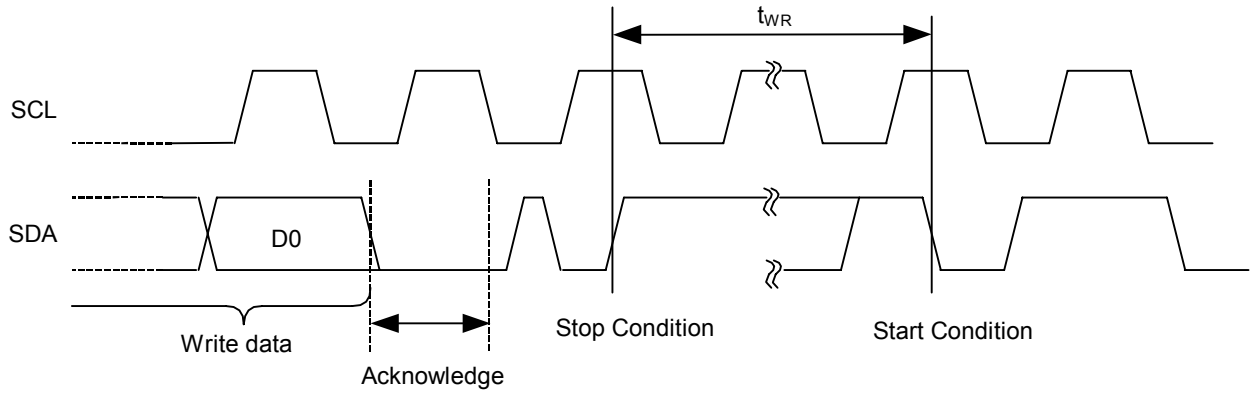


Figure 8 Write Cycle Timing

■ Pin Functions

1. Address Input Pins (A0, A1 and A2)

The slave address is assigned by connecting pins A0, A1 and A2 to the GND or to the V_{CC} respectively. One of the eight different slave address can be assigned to the S-24CS01A/02A by the combination of pins A0, A1 and A2.

The slave address is assigned by connecting pins A1 and A2 to the GND or to the V_{CC} respectively. One of the four different slave address can be assigned to the S-24CS04A by the combination of pins A1 and A2.

The slave address is assigned by connecting the A2 pin to the GND or to the V_{CC} respectively. The two different slave address can be assigned to the S-24CS08A by A2 pin.

The given slave address, which is compared with the slave address transmitted from the master device, is used to select the one among the multiple devices connected to the bus. The address input pin should be connected to the GND or to the V_{CC}.

2. SDA (Serial Data Input / Output) Pin

The SDA pin is used for bi-directional transmission of serial data. It consists of a signal input pin and an Nch open-drain output pin.
The SDA line is usually pulled up to the V_{CC}, and OR-wired with other open-drain or open-collector output devices.

3. SCL (Serial Clock Input) Pin

The SCL pin is used for serial clock input. Since signals are processed at the rising or falling edge of the SCL clock input signal, attention should be paid to the rising time and falling time to conform to the specifications.

4. WP Pin

The write protection is enabled by connecting the WP pin to the V_{CC}. When there is no need for write protection, connect the pin to the GND.

■ Operation

1. Start Condition

Start is identified by a high to low transition of the SDA line while the SCL line is stable at high.
Every operation begins from a start condition.

2. Stop Condition

Stop is identified by a low to high transition of the SDA line while the SCL line is stable at high.
When a device receives a stop condition during a read sequence, the read operation is interrupted, and the device enters standby mode.
When a device receives a stop condition during a write sequence, the reception of the write data is halted, and the E^{2}PROM initiates a write cycle.

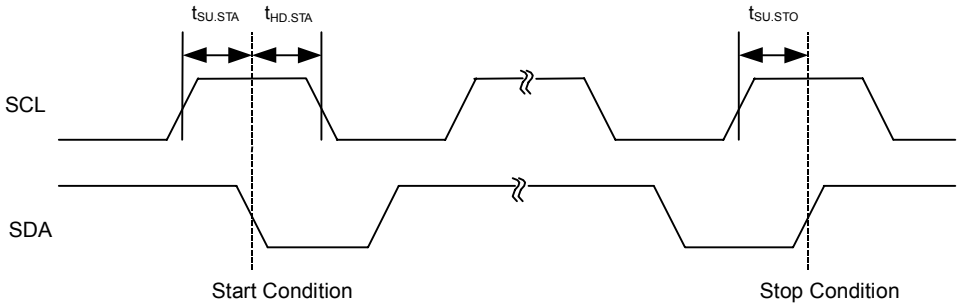


Figure 9 Start / Stop Conditions

3. Data Transmission

Changing the SDA line while the SCL line is low, data is transmitted.
Changing the SDA line while the SCL line is high, a start or stop condition is recognized.

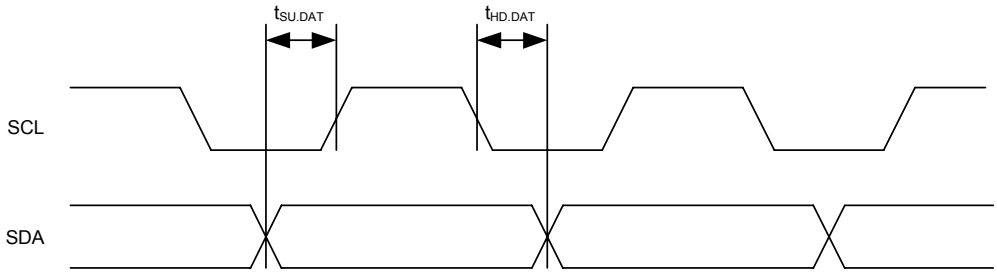


Figure 10 Data Transmission Timing

4. Acknowledge

The unit of data transmission is 8 bits. During the 9th clock cycle period the receiver on the bus pulls down the SDA line to acknowledge the receipt of the 8-bit data.
When an internal write cycle is in progress, the device does not generate an acknowledge.

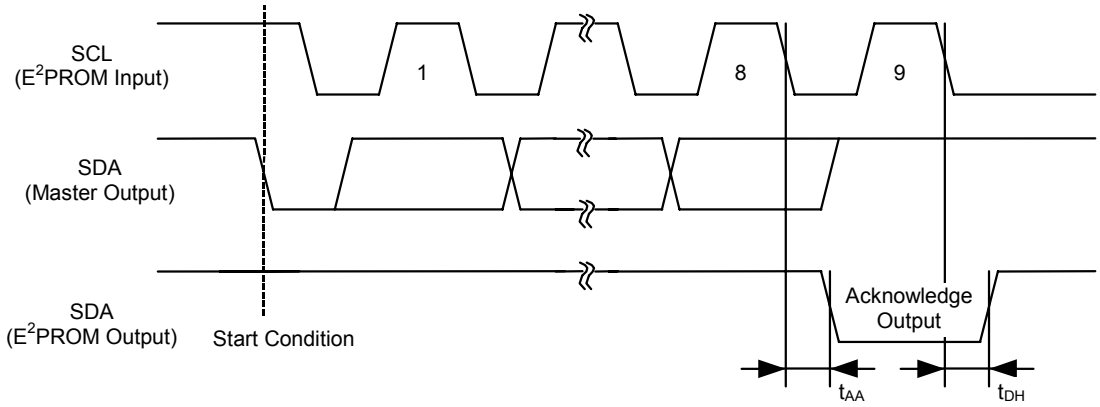


Figure 11 Acknowledge Output Timing

5. Device Addressing

To start communication, the master device on the system generates a start condition to the bus line. Next, the master device sends 7-bit device address and a 1-bit read / write instruction code on to the SDA bus. The 4 most significant bits of the device address are called the "Device Code", and are fixed to "1010".

In S-24CS01A/02A, successive 3 bits are called the “Slave Address”. These 3 bits are used to identify a device on the system bus and are compared with the predetermined value which is defined by the address input pins (A0, A1 and A2). When the comparison result matches, the slave device responds with an acknowledge during the 9th clock cycle.

In S-24CS04A, successive 2 bits are called the "Slave Address". These 2 bits are used to identify a device on the system bus and are compared with the predetermined value which is defined by the address input pins (A1 and A2). When the comparison result matches, the slave device responds with an acknowledge during the 9th clock cycle.
The successive 1 bit (P0) is used to define a page address and choose the two 256-byte memory blocks (Address 000h to 0FFh and 100h to 1FFh).

In S-24CS08A, successive 1 bit is called the “Slave Addrdess”. This 1 bit is used to identify a device on the system bus and is compared with the predetermined value which is defined by the address input pin (A2). When the comparison result matches, the slave device responds with an acknowledge during the 9th clocks cycle.
The successive 2 bits (P1 and P0) are used to define a page address and choose the four 256-byte memory blocks (Address 000h to 0FFh, 100h to 1FFh, 200h to 2FFh and 300h to 3FFh).

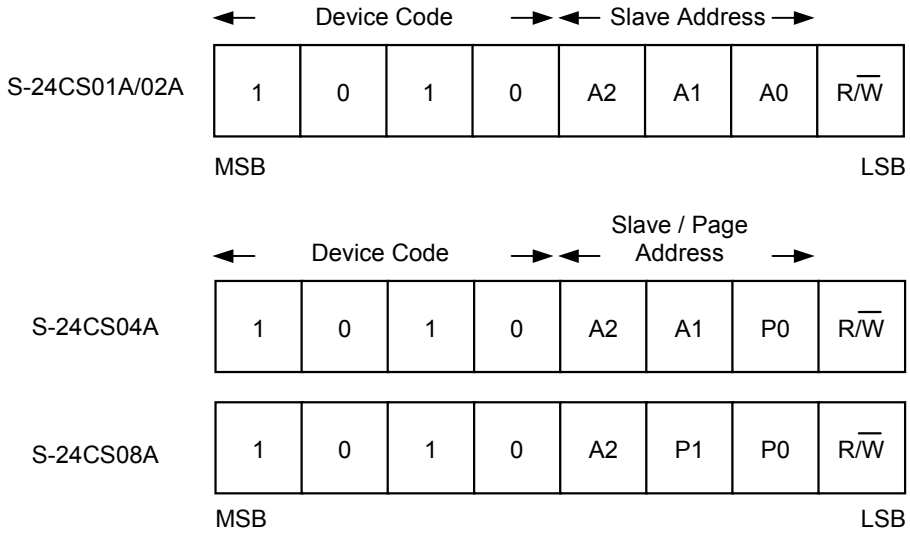
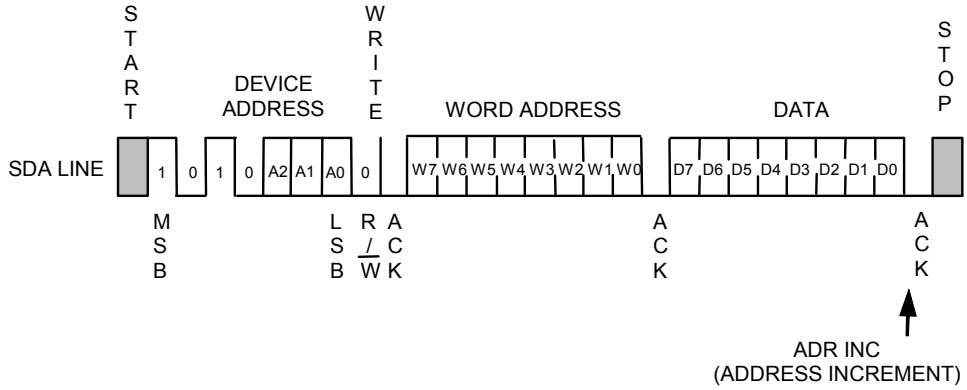


Figure 12 Device Address

6. Write

6. 1 Byte Write

When the master sends a 7-bit device address and a 1-bit read / write instruction code set to "0", following a start condition, the E^{2}PROM acknowledges it. The E^{2}PROM then receives an 8-bit word address and responds with an acknowledge. After the E^{2}PROM receives 8-bit write data and responds with an acknowledge, it receives a stop condition and that initiates the write cycle at the addressed memory.
During the write cycle all operations are forbidden and no acknowledge is generated.

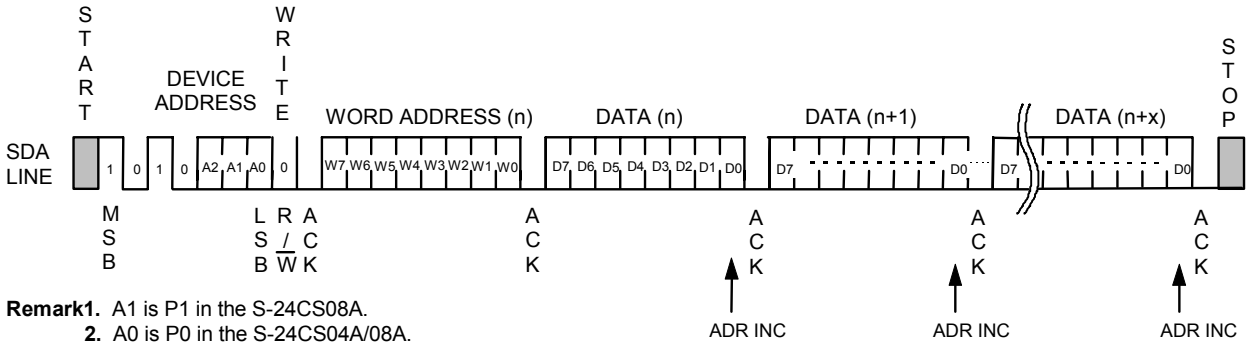


Remark1. A1 is P1 in the S-24CS08A.
2. A0 is P0 in the S-24CS04A/08A.
3. W7 is optional in the S-24CS01A.

Figure 13 Byte Write

6. 2 Page Write

The page write mode allows up to 8 bytes to be written in a single write operation in the S-24CS01A/02A and 16 bytes to be written in a single write operation in the S-24CS04A/08A.
Basic data transmission procedure is the same as that in the "Byte Write". But instead of generating a stop condition, the master transmits 8-bit write data up to 8 bytes before the page write.
When the E²PROM receives a 7-bit device address and a 1-bit read / write instruction code set to "0", following a start condition, it generates an acknowledge. Then the E²PROM receives an 8-bit word address, and responds with an acknowledge. After the E²PROM receives 8-bit write data and responds with an acknowledge, it receives 8-bit write data corresponding to the next word address, and generates an acknowledge. The E²PROM repeats reception of 8-bit write data and generation of acknowledge in succession. The E²PROM can receive as many write data as the maximum page size.
Receiving a stop condition initiates a write cycle of the area starting from the designated memory address and having the page size equal to the received write data.



Remark1. A1 is P1 in the S-24CS08A.
2. A0 is P0 in the S-24CS04A/08A.
3. W7 is optional in the S-24CS01A.

Figure 14 Page Write

In S-24CS01A/02A, the lower 3 bits of the word address are automatically incremented every time when the E²PROM receives 8-bit write data. If the size of the write data exceeds 8 bytes, the upper 5 bits of the word address remain unchanged, and the lower 3 bits are rolled over and previously received data will be overwritten.

In S-24CS04A, the lower 4 bits of the word address are automatically incremented every time when the E²PROM receives 8-bit write data. If the size of the write data exceeds 16 bytes, the upper 4 bits of the word address and page address (P0) remain unchanged, and the lower 4 bits are rolled over and previously received data will be overwritten.

In S-24CS08A, the lower 4 bits of the word address are automatically incremented every time when the E²PROM receives 8-bit write data. If the size of the write data exceeds 16 bytes, the upper 4 bits of the word address and page address (P1 and P0) remain unchanged, and the lower 4 bits are rolled over and previously received data will be overwritten.

6. 3 Write Protection

Write protection is available in the S-24CS01A/02A/04A/08A. When the WP pin is connected to the V_{CC}, write operation to memory area is forbidden at all.
When the WP pin is connected to the GND, the write protection is invalid, and write operation in all memory area is available.
Fix the level of the WP pin from the rising edge of SCL for loading the last write data (D0) until the end of the write time (10 ms max.). If the WP pin changes during this time, the address data being written at this time is not guaranteed.
There is no need for using write protection, the WP pin should be connected to the GND. The write protection is valid in the operating voltage range.

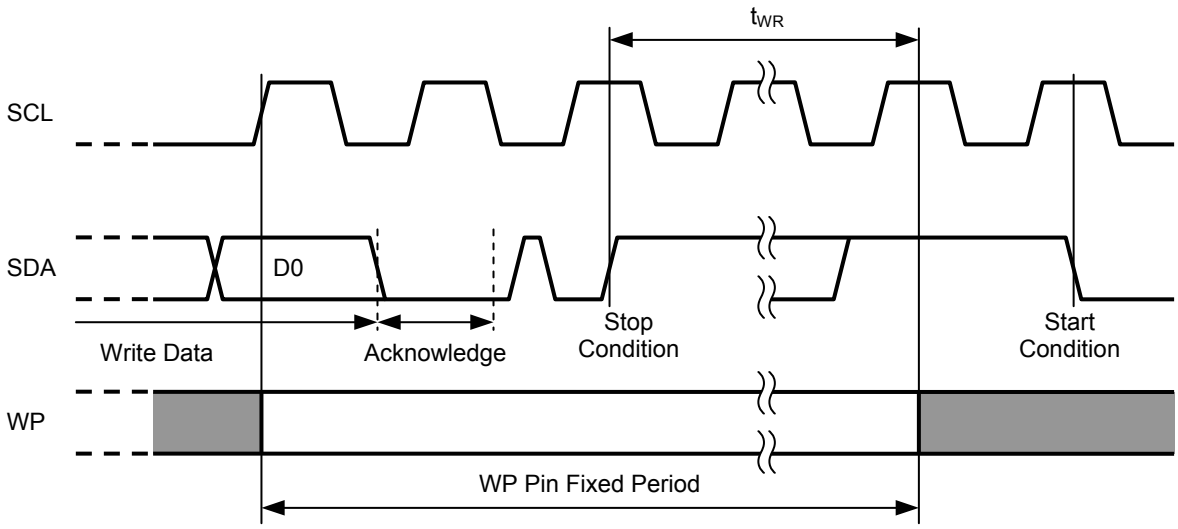


Figure 15 WP Pin Fixed Period

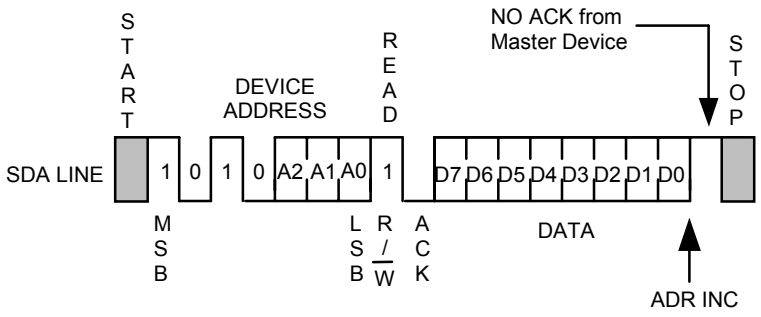
6. 4 Acknowledge Polling

Acknowledge polling is used to know the completion of the write cycle in the E^{2}PROM.
After the E^{2}PROM receives a stop condition and once starts the write cycle, all operations are forbidden and no response is made to the signal transmitted by the master device.
Accordingly the master device can recognize the completion of the write cycle in the E^{2}PROM by detecting a response from the slave device after transmitting the start condition, the device address and the read/write instruction code to the E^{2}PROM, namely to the slave devices.
That is, if the E^{2}PROM does not generate an acknowledge, the write cycle is in progress and if the E^{2}PROM generates an acknowledge, the write cycle has been completed.
Keep the level of the WP pin fixed until acknowledge is confirmed.
It is recommended to use the read instruction "1" as the read/write instruction code transmitted by the master device.

7. Read

7. 1 Current Address Read

Either in writing or in reading the E^{2}PROM holds the last accessed memory address, internally incremented by one. The memory address is maintained as long as the power voltage is higher than the current address hold voltage V_{AH}.
The master device can read the data at the memory address of the current address pointer without assigning the word address as a result, when it recognizes the position of the address pointer in the E^{2}PROM. This is called "Current Address Read".
In the following the address counter in the E^{2}PROM is assumed to be “n”.
When the E^{2}PROM receives a 7-bit device address and a 1-bit read / write instruction code set to “1” following a start condition, it responds with an acknowledge. However, the page address (P0) in S-24CS04A and the page address (P1 and P0) in S-24CS08A become invalid and the memory address of the current address pointer becomes valid.
Next an 8-bit data at the address "n" is sent from the E^{2}PROM synchronous to the SCL clock. The address counter is incremented at the falling edge of the SCL clock for the 8th bit data, and the content of the address counter becomes n+1.
The master device outputs stop condition not an acknowledge ,the reading of E^{2}PROM is ended.



Remark1. A1 is P1 in S-24CS08A.
2. A0 is P0 in S-24CS04A/08A.

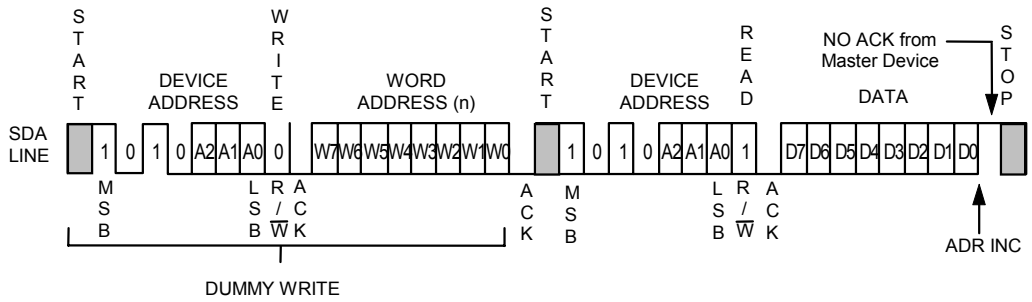
Figure 16 Current Address Read

Attention should be paid to the following point on the recognition of the address pointer in the E^{2}PROM.
In the read operation the memory address counter in the E^{2}PROM is automatically incremented at every falling edge of the SCL clock for the 8th bit of the output data. In the write operation, on the other hand, the upper bits of the memory address (the upper bits of the word address and page address)[*1] are left unchanged and are not incremented at the falling edge of the SCL clock for the 8th bit of the received data.

***1.** S-24CS01A/02A is the upper 5 bits of the word address.
S-24CS04A is the upper 4 bits of the word address and the page address P0.
S-24CS08A is the upper 4 bits of the word address and the page address P1 and P0.

7. 2 Random Read

Random read is used to read the data at an arbitrary memory address.
A dummy write is performed to load the memory address into the address counter.
When the E^{2}PROM receives a 7-bit device address and a 1-bit read / write instruction code set to "0" following a start condition, it responds with an acknowledge. The E^{2}PROM then receives an 8-bit word address and responds with an acknowledge. The memory address is loaded to the address counter in the E^{2}PROM by these operations. Reception of write data does not follow in a dummy write whereas reception of write data follows in a byte write and in a page write.
Since the memory address is loaded into the memory address counter by dummy write, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition and performing the same operation in the current address read.
That is, when the E^{2}PROM receives a 7-bit device address and a 1-bit read / write instruction code set to "1", following a start condition signal, it responds with an acknowledge. Next, 8-bit data is transmitted from the E^{2}PROM in synchronous to the SCL clock. The master device outputs stop condition not an acknowledge , the reading of E^{2}PROM is ended.



Remark1. A1 is P1 in the S-24CS08A.
2. A0 is P0 in the S-24CS04A/08A.
3. W7 is optional in the S-24CS01A.

Figure 17 Random Read

7. 3 Sequential Read

When the E^{2}PROM receives a 7-bit device address and a 1-bit read / write instruction code set to "1" following a start condition both in current and random read operations, it responds with an acknowledge.
An 8-bit data is then sent from the E^{2}PROM synchronous to the SCL clock and the address counter is automatically incremented at the falling edge of the SCL clock for the 8th bit data.
When the master device responds with an acknowledge, the data at the next memory address is transmitted. Response with an acknowledge by the master device has the memory address counter in the E^{2}PROM incremented and makes it possible to read data in succession. This is called "Sequential Read".
The master device outputs stop condition not an acknowledge , the reading of E^{2}PROM is ended.
Data can be read in succession in the sequential read mode. When the memory address counter reaches the last word address, it rolls over to the first memory address.

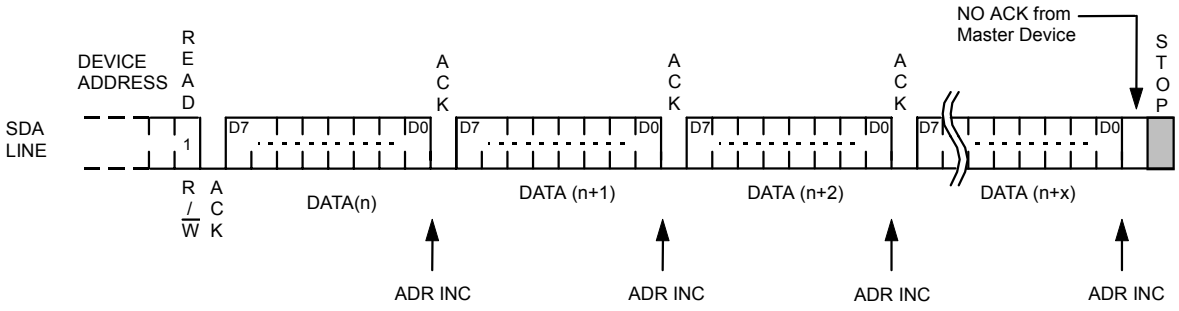


Figure 18 Sequential Read

8. Address Increment Timing

The timing for the automatic address increment is the falling edge of the SCL clock for the 8th bit of the read data in read operation and the falling edge of the SCL clock for the 8th bit of the received data in write operation.

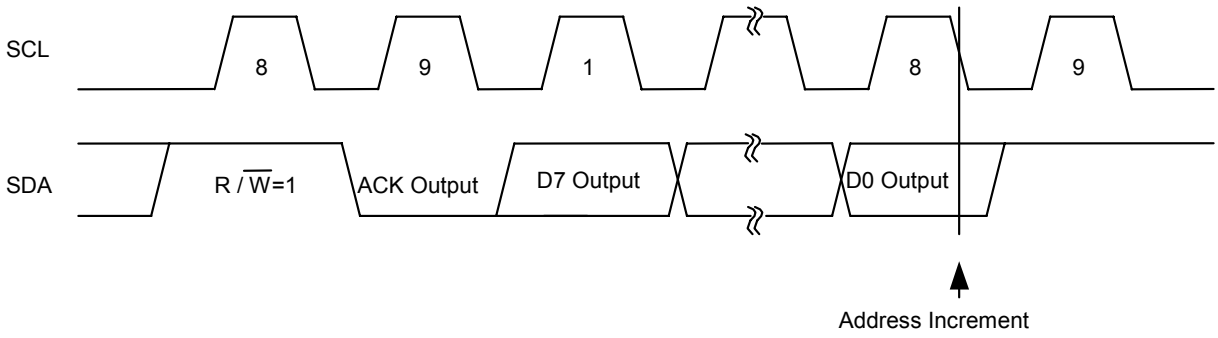


Figure 19 Address Increment Timing in Reading

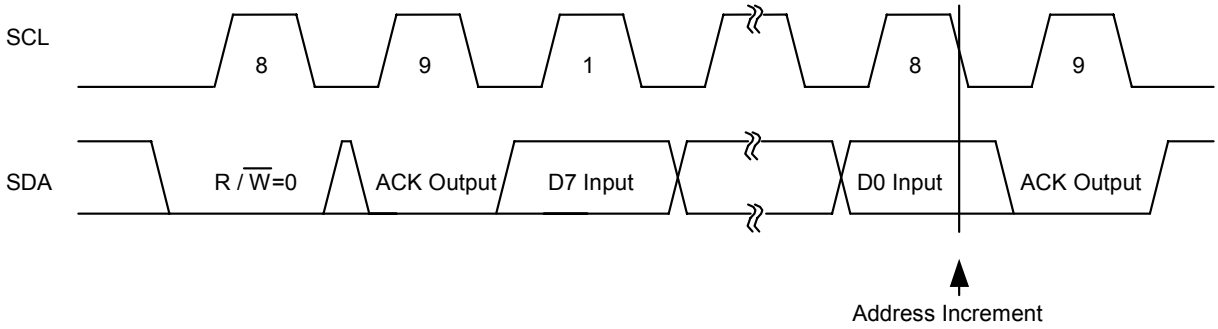


Figure 20 Address Increment Timing in Writing

■ Write Inhibition Function at Low Power Voltage

The S-24CS01A/02A/04A/08A have a detection circuit for low power voltage. The detection circuit cancels a write instruction when the power voltage is low or the power switch is on. The detection voltage is 1.75 V typically and the release voltage is 2.05 V typically, the hysteresis of approximate 0.3 V thus exists. (See **Figure 21**.)
When a low power voltage is detected, a write instruction is canceled at the reception of a stop condition.
When the power voltage lowers during a data transmission or a write operation, the data at the address of the operation is not assured.

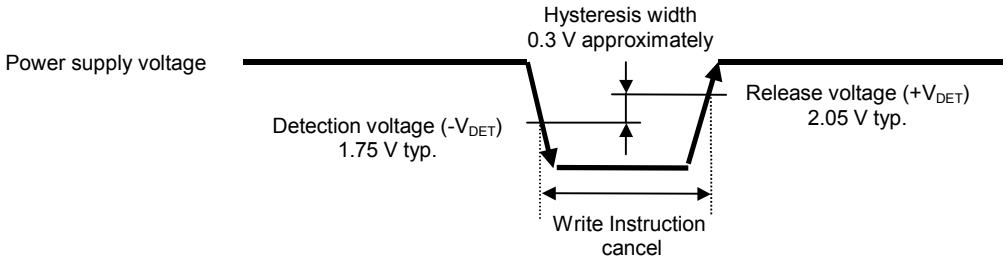


Figure 21 Operation at low power voltage

■ Using S-24CS01A/02A/04A/08A

1. Adding a pull-up resistor to SDA I/O pin and SCL input pin

Add a 1 to 5 kΩ pull-up resistor to the SCL input pin[*1] and the SDA I/O pin in order to enable the functions of the I^{2}C-bus protocol. Normal communication cannot be provided without a pull-up resistor.

***1.** When the SCL input pin of the E^{2}PROM is connected to a tri-state output pin of the microprocessor, connect the same pull-up resistor to prevent a high impedance status from being input to the SCL input pin.
This protects the E^{2}PROM from malfunction due to an undefined output (high impedance) from the tri-state pin when the microprocessor is reset when the voltage drops.

2. I/O pin equivalent circuit

The I/O pins of this IC do not include pull-up and pull-down resistors. The SDA pin is an open-drain output. The following shows the equivalent circuits.

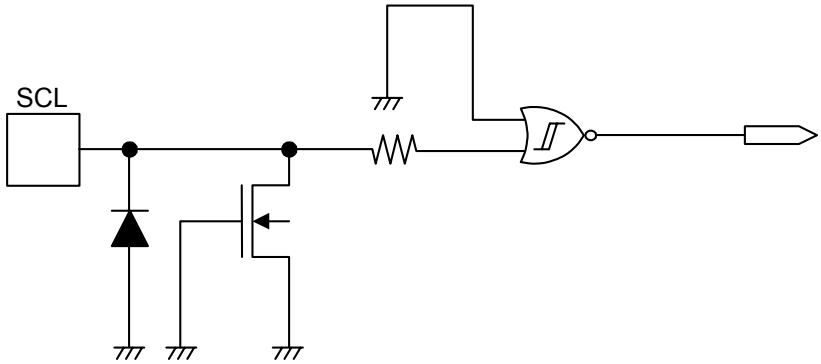


Figure 22 SCL Pin

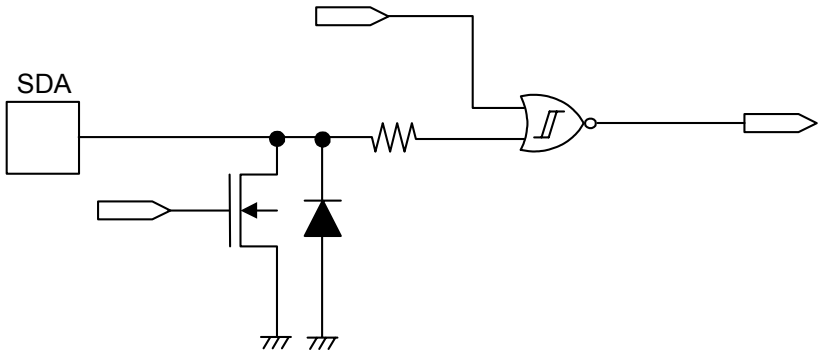


Figure 23 SDA Pin

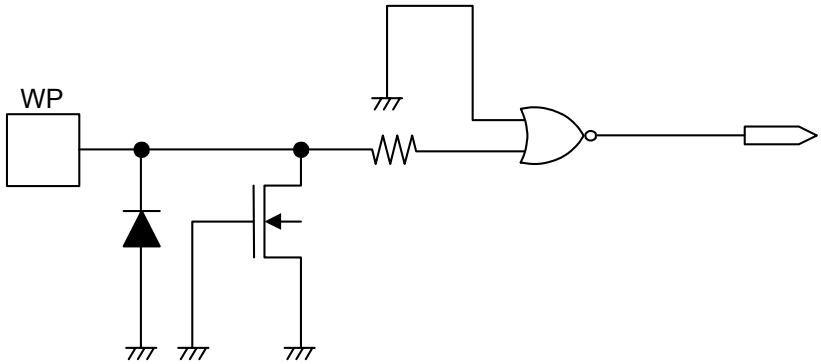


Figure 24 WP Pin

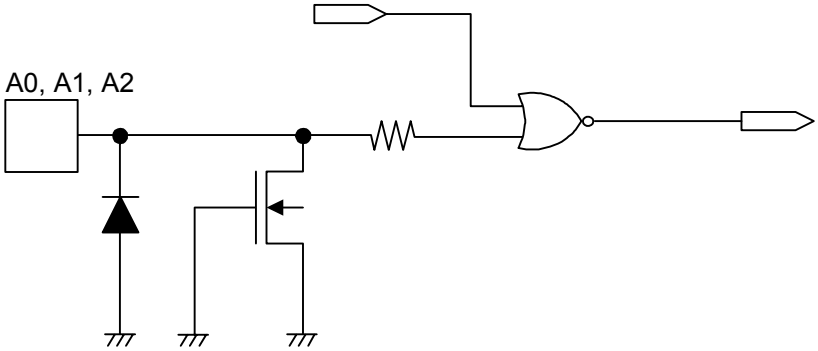


Figure 25 A0, A1, A2 Pin

3. Matching phases while E^{2}PROM is accessed

The S-24CS01A/02A/04A/08A does not have a pin for resetting (the internal circuit), therefore, the E^{2}PROM cannot be forcibly reset externally. If a communication interruption occurs in the E^{2}PROM, it must be reset by software.
For example, even if a reset signal is input to the microprocessor, the internal circuit of the E^{2}PROM is not reset as long as the stop condition is not input to the E^{2}PROM. In other words, the E^{2}PROM retains the same status and cannot shift to the next operation. This symptom applies to the case when only the microprocessor is reset when the power supply voltage drops. With this status, if the power supply voltage is restored, reset the E^{2}PROM (after matching the phase with the microprocessor) and input an instruction. The following shows this reset method.

[How to reset E^{2}PROM]

The E^{2}PROM can be reset by the start and stop instructions. When the E^{2}PROM is reading data "0" or is outputting the acknowledge signal, 0 is output to the SDA line. In this status, the microprocessor cannot output an instruction to the SDA line. In this case, terminate the acknowledge output operation or read operation, and then input a start instruction. **Figure 26** shows this procedure.
First, input the start condition. Then transmit 9 clocks (dummy clocks) of SCL. During this time, the microprocessor sets the SDA line to high level. By this operation, the E^{2}PROM interrupts the acknowledge output operation or data output, so input the start condition*1. When a start condition is input, the E^{2}PROM is reset. To make doubly sure, input the stop condition to the E^{2}PROM. Normal operation is then possible.

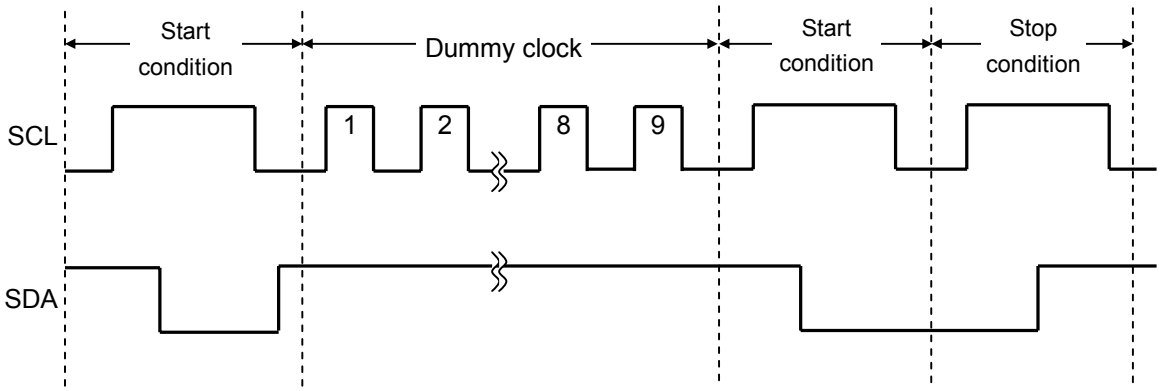


Figure 26 Resetting E^{2}PROM

***1.** After 9 clocks (dummy clocks), if the SCL clock continues to be output without a start condition being input, a write operation may be started upon receipt of a stop condition. To prevent this, input a start condition after 9 clocks (dummy clocks).

Remark It is recommended to perform the above reset using dummy clocks when the system is initialized after the power supply voltage has been raised.

4. Acknowledge check

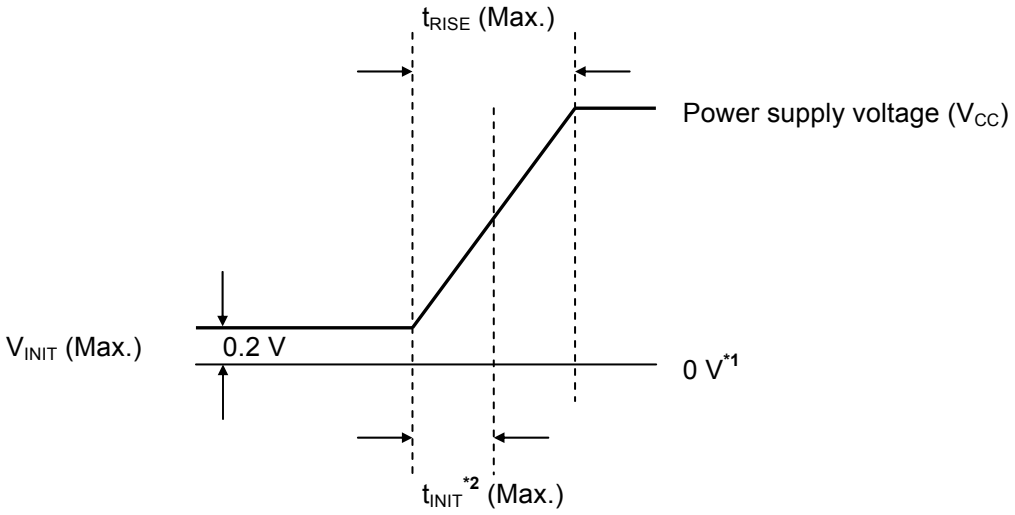
The I²C-bus protocol includes an acknowledge check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the microprocessor and E²PROM. This function is effective to prevent malfunction, so it is recommended to perform an acknowledge check on the microprocessor side.

5. Built-in power-on-clear circuit

E²PROMs have a built-in power-on-clear circuit that initializes the E²PROM. Unsuccessful initialization may cause a malfunction. For the power-on-clear circuit to operate normally, the following conditions must be satisfied for raising the power supply voltage.

5. 1 Raising power supply voltage

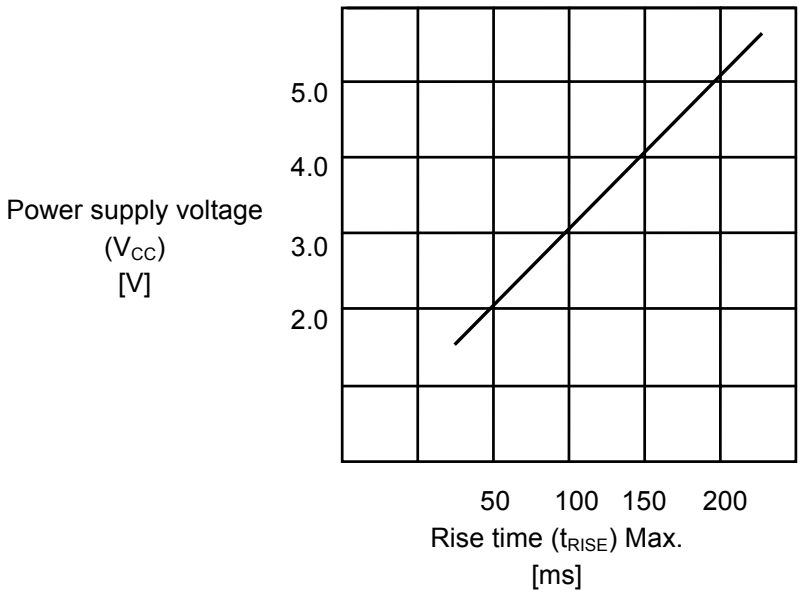
Raise the power supply voltage, starting at 0.2 V maximum, so that the voltage reaches the power supply voltage to be used within the time defined by t_{RISE} as shown in **Figure 27**.
For example, when the power supply voltage to be used is 5.0 V, t_{RISE} is 200 ms as shown in **Figure 28**. The power supply voltage must be raised within 200 ms.



***1.** 0 V means there is no difference in potential between the V_{CC} pin and the GND pin of the E²PROM.

***2.** t_{INIT} is the time required to initialize the E²PROM. No instructions are accepted during this time.

Figure 27 Raising Power Supply Voltage



For example:
If your E^{2}PROM supply voltage = 5.0 V, raise the power supply voltage to 5.0 V within 200 ms.

Figure 28 Raising Time of Power Supply Voltage

When initialization is successfully completed via the power-on-clear circuit, the E^{2}PROM enters the standby status.

If the power-on-clear circuit does not operate, the following are the possible causes.

(1) Because the E^{2}PROM has not been initialized, an instruction formerly input is valid or an instruction may be inappropriately recognized. In this case, writing may be performed.
(2) The voltage may have dropped due to power off while the E^{2}PROM is being accessed. Even if the microprocessor is reset due to the low power voltage, the E^{2}PROM may malfunction unless the power-on-clear operation conditions of E^{2}PROM are satisfied. For the power-on-clear operation conditions of E^{2}PROM, refer to **5. 1 Raising power supply voltage**.

If the power-on-clear circuit does not operate, match the phase (reset) so that the internal E^{2}PROM circuit is normally reset. The statuses of the E^{2}PROM immediately after the power-on-clear circuit operates and when phase is matched (reset) are the same.

5. 2 Wait for the initialization sequence to end

The E^{2}PROM executes initialization during the time that the supply voltage is increasing to its normal value. All instructions must wait until after initialization. The relationship between the initialization time (t_{INIT}) and rise time (t_{RISE}) is shown in **Figure 29**.

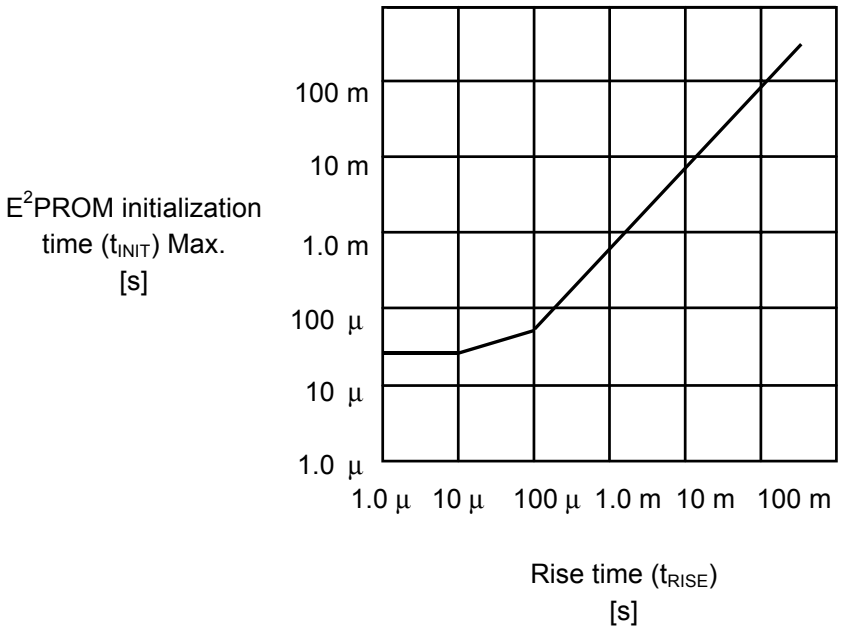


Figure 29 Initialization Time of E^{2}PROM