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■ Pin Configurations

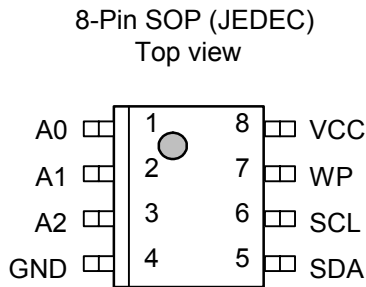


Figure 1

S-24CS64A0I-J8T1G

Table 1

Pin No.	Symbol	Description
1	A0	Slave address input
2	A1	Slave address input
3	A2	Slave address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to V _{CC} : Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

Remark See Dimensions for details of the package drawings.

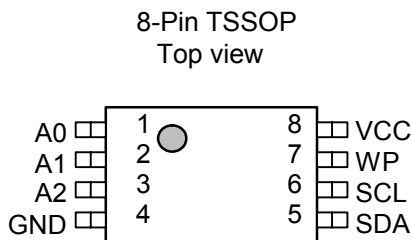


Figure 2

S-24CS64A0I-T8T1G

Table 2

Pin No.	Symbol	Description
1	A0	Slave address input
2	A1	Slave address input
3	A2	Slave address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to V _{CC} : Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

Remark See Dimensions for details of the package drawings.

WLP
Bottom view

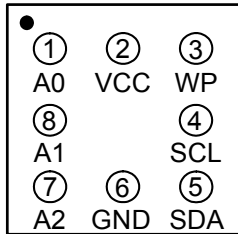


Figure 3

S-24CS64A0I-H8Tx

Table 3

Pin No.	Symbol	Description
1	A0	Slave address input
2	VCC	Power supply
3	WP	Write protection input Connected to V _{CC} : Protection valid Connected to GND: Protection invalid
4	SCL	Serial clock input
5	SDA	Serial data input / output
6	GND	Ground
7	A2	Slave address input
8	A1	Slave address input

Remark Please contact our sales office regarding the product with WLP package.

■ Block Diagram

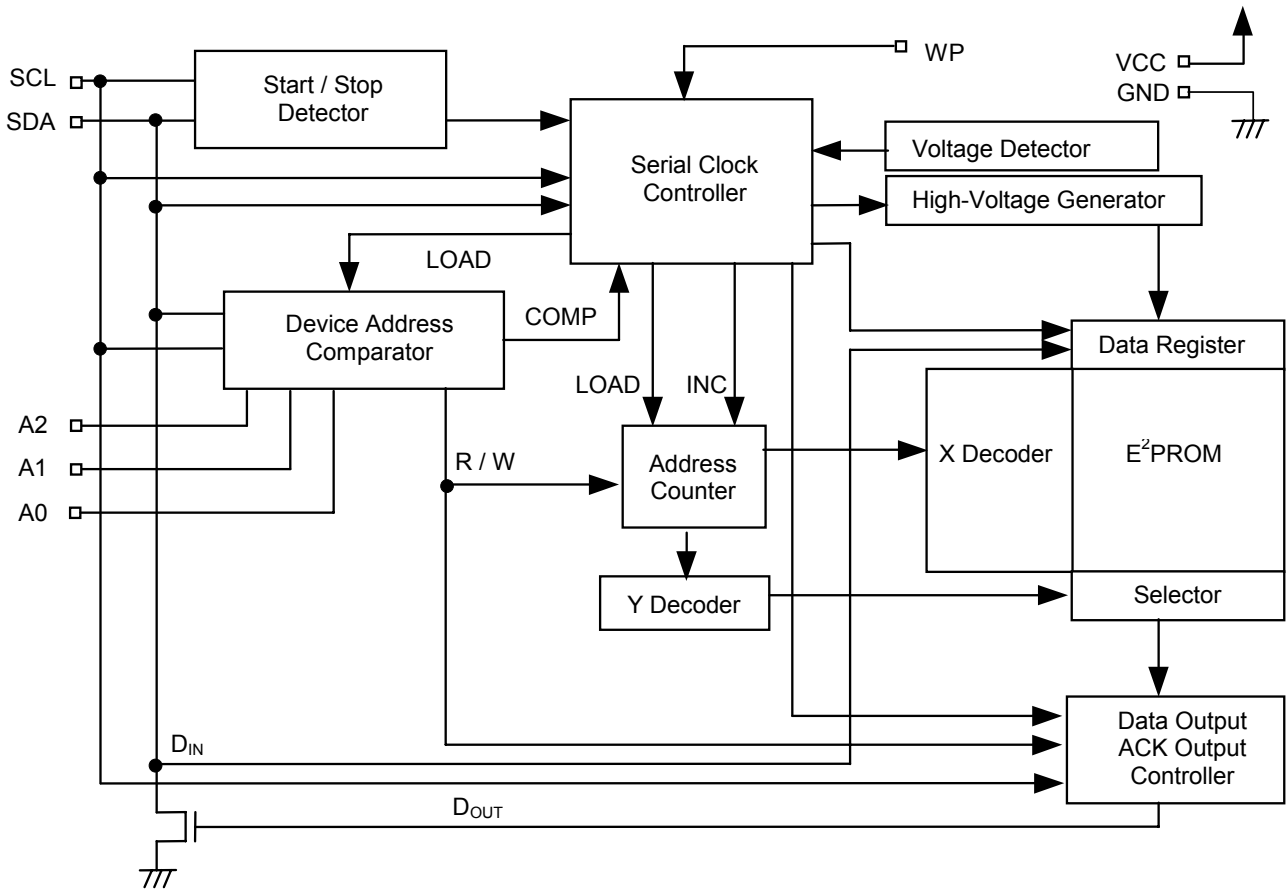


Figure 4

■ Absolute Maximum Ratings

Table 4

Item	Symbol	Ratings	Unit
Power supply voltage	V _{CC}	-0.3 to +7.0	V
Input voltage	V _{IN}	-0.3 to +7.0	V
Output voltage	V _{OUT}	-0.3 to +7.0	V
Operating ambient temperature	T _{opr}	-40 to +85	°C
Storage temperature	T _{stg}	-65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 5

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	V _{CC}	Read Operation	1.8	—	5.5	V
		Write Operation	2.7	—	5.5	V
High level input voltage	V _{IH}	V _{CC} = 2.5 to 5.5 V	0.7×V _{CC}	—	V _{CC}	V
		V _{CC} = 1.8 to 2.5 V	0.8×V _{CC}	—	V _{CC}	V
Low level input voltage	V _{IL}	V _{CC} = 2.5 to 5.5 V	0.0	—	0.3×V _{CC}	V
		V _{CC} = 1.8 to 2.5 V	0.0	—	0.2×V _{CC}	V

■ Pin Capacitance

Table 6

(T_a = 25°C, f = 1.0 MHz, V_{CC} = 5 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0 V (SCL, A0, A1, A2, WP)	—	—	10	pF
Input / output capacitance	C _{I/O}	V _{I/O} = 0 V (SDA)	—	—	10	pF

■ Endurance

Table 7

Item	Symbol	Operation temperature	Min.	Typ.	Max.	Unit
Endurance	N _w	-40 to +85°C	10 ⁵	—	—	cycles / word*1

*1. For each address (Word: 8 bits)

■ DC Electrical Characteristics

Table 8

Item	Symbol	Conditions	V _{CC} = 4.5 to 5.5 V f = 400 kHz			V _{CC} = 2.7 to 4.5 V f = 100 kHz			V _{CC} = 1.8 to 2.7 V f = 100 kHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I _{CC1}	—	—	—	0.8	—	—	0.5	—	—	0.3	mA
Current consumption (WRITE)	I _{CC2}	—	—	—	4.0	—	—	3.0	—	—	—	mA

Table 9

Item	Symbol	Conditions	V _{CC} = 4.5 to 5.5 V			V _{CC} = 2.7 to 4.5 V			V _{CC} = 1.8 to 2.7 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I _{SB}	V _{IN} = V _{CC} or GND	—	—	5.0	—	—	3.0	—	—	3.0	μA
Input leakage current	I _{LI}	V _{IN} = GND to V _{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Output leakage current	I _{LO}	V _{OUT} = GND to V _{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Low level output voltage	V _{OL}	I _{OL} = 3.2 mA	—	—	0.4	—	—	—	—	—	—	V
		I _{OL} = 1.5 mA	—	—	0.3	—	—	0.3	—	—	0.3	V
Current address hold voltage	V _{AH}	—	1.5	—	5.5	1.5	—	4.5	1.5	—	2.7	V

■ AC Electrical Characteristics

Table 10 Measurement Conditions

Input pulse voltage	0.1×V _{CC} to 0.9×V _{CC}
Input pulse rising / falling time	20 ns
Output judgement voltage	0.5×V _{CC}
Output load	100 pF+ Pull-up resistor 1.0 kΩ

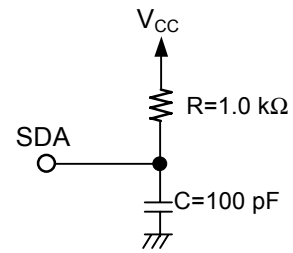


Figure 5 Output Load Circuit

Table 11

Item	Symbol	V _{CC} = 4.5 to 5.5 V			V _{CC} = 2.7 to 4.5 V			V _{CC} = 1.8 to 2.7 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f _{SCL}	0	—	400	0	—	400	0	—	100	kHz
SCL clock time "L"	t _{LOW}	1.0	—	—	1.0	—	—	4.7	—	—	μs
SCL clock time "H"	t _{HIGH}	0.9	—	—	0.9	—	—	4.0	—	—	μs
SDA output delay time	t _{AA}	0.1	—	0.9	0.1	—	0.9	0.1	—	3.5	μs
SDA output hold time	t _{DH}	50	—	—	50	—	—	100	—	—	ns
Start condition setup time	t _{SU.STA}	0.6	—	—	0.6	—	—	4.7	—	—	μs
Start condition hold time	t _{HD.STA}	0.6	—	—	0.6	—	—	4.0	—	—	μs
Data input setup time	t _{SU.DAT}	100	—	—	100	—	—	200	—	—	ns
Data input hold time	t _{HD.DAT}	0	—	—	0	—	—	0	—	—	ns
Stop condition setup time	t _{SU.STO}	0.6	—	—	0.6	—	—	4.0	—	—	μs
SCL, SDA rising time	t _R	—	—	0.3	—	—	0.3	—	—	1.0	μs
SCL, SDA falling time	t _F	—	—	0.3	—	—	0.3	—	—	0.3	μs
Bus release time	t _{BUF}	1.3	—	—	1.3	—	—	4.7	—	—	μs
Noise suppression time	t _i	—	—	50	—	—	100	—	—	100	ns

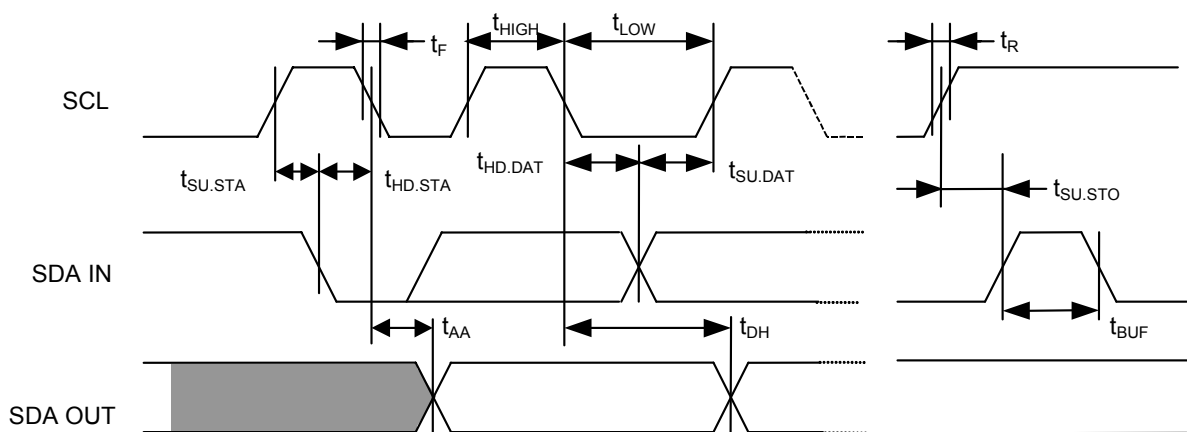


Figure 6 Bus Timing

Table 12

Item	Symbol	V _{CC} = 2.7 to 5.5 V			Unit
		Min.	Typ.	Max.	
Write time	t _{WR}	—	6.0	10.0	ms

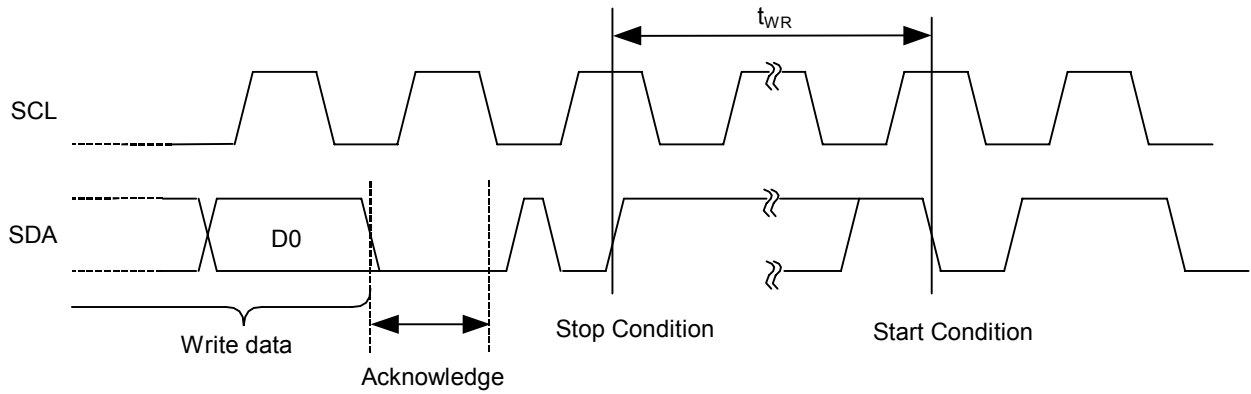


Figure 7 Write Cycle Timing

■ Pin Functions

1. A0, A1 and A2 (Slave Address Input) Pins

The slave address is assigned by connecting pins A0, A1 and A2 to the GND or to the V_{CC} respectively. One of the eight different slave address can be assigned by the combination of pins A0, A1 and A2.

The given slave address, which is compared with the slave address transmitted from the master device, is used to select the one among the multiple devices connected to the bus. The address input pin should be connected to the GND or to the V_{CC} .

2. SDA (Serial Data Input / Output) Pin

The SDA pin is used for bi-directional transmission of serial data. It consists of a signal input pin and an Nch open-drain output pin.

The SDA line is usually pulled up to the V_{CC} , and OR-wired with other open-drain or open-collector output devices.

3. SCL (Serial Clock Input) Pin

The SCL pin is used for serial clock input. Since signals are processed at the rising or falling edge of the SCL clock input signal, attention should be paid to the rising time and falling time to conform to the specifications.

4. WP (Write Protection Input) Pin

The write protection is enabled by connecting the WP pin to the V_{CC} . When there is no need for write protection, connect the pin to the GND.

■ Operation

1. Start Condition

Start is identified by a high to low transition of the SDA line while the SCL line is stable at high. Every operation begins from a start condition.

2. Stop Condition

Stop is identified by a low to high transition of the SDA line while the SCL line is stable at high. When a device receives a stop condition during a read sequence, the read operation is interrupted, and the device enters standby mode. When a device receives a stop condition during a write sequence, the reception of the write data is halted, and the E²PROM initiates a write cycle.

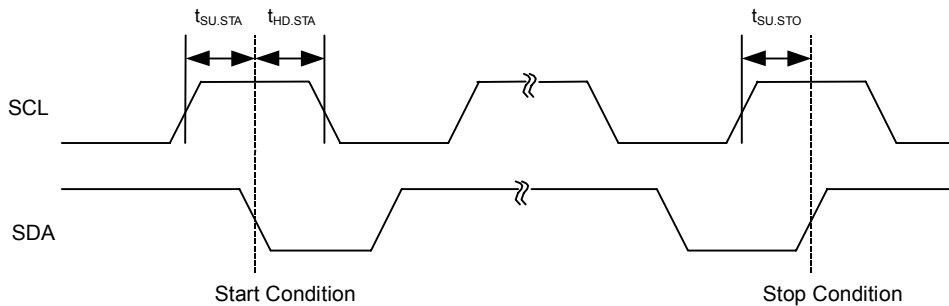


Figure 8 Start / Stop Conditions

3. Data Transmission

Changing the SDA line while the SCL line is low, data is transmitted.
Changing the SDA line while the SCL line is high, a start or stop condition is recognized.

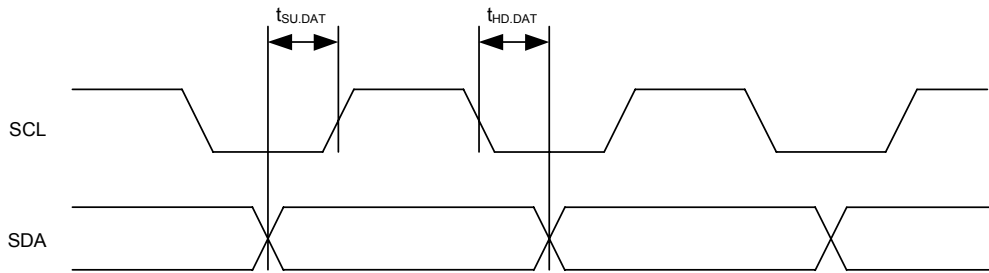


Figure 9 Data Transmission Timing

4. Acknowledge

The unit of data transmission is 8 bits. During the 9th clock cycle period the receiver on the bus pulls down the SDA line to acknowledge the receipt of the 8-bit data.
When a internal write cycle is in progress, the device does not generate an acknowledge.

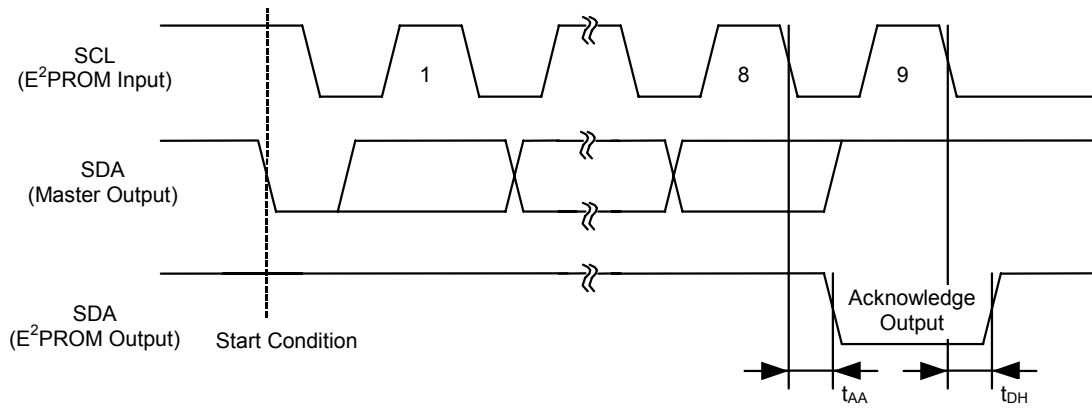


Figure 10 Acknowledge Output Timing

5. Device Addressing

To start communication, the master device on the system generates a start condition to the bus line. Next, the master device sends 7-bit device address and a 1-bit read / write instruction code on to the SDA bus. The 4 most significant bits of the device address are called the "Device Code", and are fixed to "1010". Successive 3 bits are called the "Slave Address". These 3 bits are used to identify a device on the system bus and are compared with the predetermined value which is defined by the address input pins (A0, A1 and A2). When the comparison result matches, the slave device responds with an acknowledge during the 9th clock cycle.

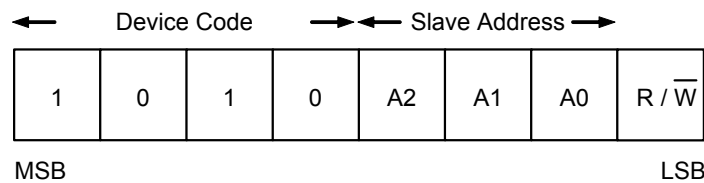


Figure 11 Device Address

6. Write

6.1 Byte Write

When the master sends a 7-bit device address and a 1-bit read / write instruction code set to "0", following a start condition, the E²PROM acknowledges it. The E²PROM then receives the upper 8 bits of the word address and responds with an acknowledge. And the E²PROM receives the lower 8 bits of the word address and responds with an acknowledge. After the E²PROM receives 8-bit write data and responds with an acknowledge, it receives a stop condition and that initiates the write cycle at the addressed memory.

During the write cycle all operations are forbidden and no acknowledge is generated.

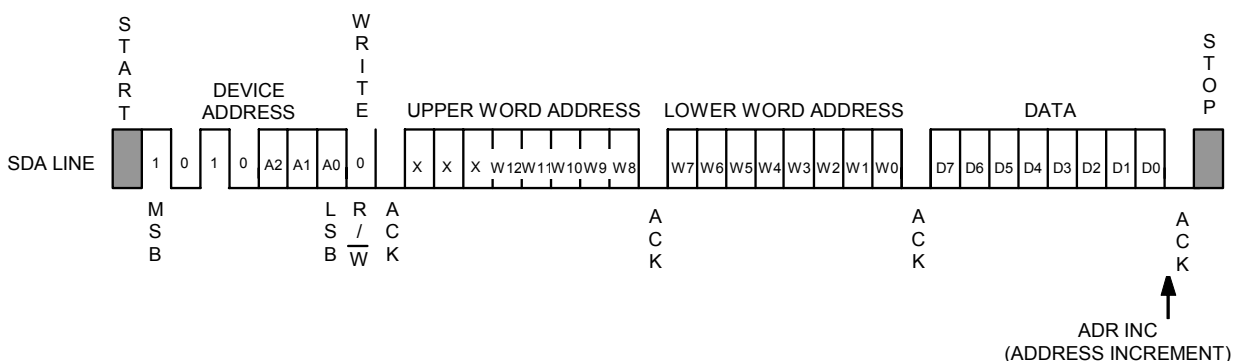


Figure 12 Byte Write

6.2 Page Write

The page write mode allows up to 32 bytes to be written in a single wire operation in the S-24CS64A. Basic data transmission procedure is the same as that in the “Byte Write”. However, when the E²PROM receives 8-bit write data which corresponds to the page size, the page can be written. When the E²PROM receives a 7-bit device address and a 1-bit read / write instruction code set to “0”, following a start condition, it generates an acknowledge. Then the E²PROM receives the upper 8 bits of the word address and responds with an acknowledge. And the E²PROM receives the lower 8 bits of the word address and responds with an acknowledge. After the E²PROM receives 8-bit write data and responds with an acknowledge, it receives 8-bit write data corresponding to the next word address, and generates an acknowledge. The E²PROM repeats reception of 8-bit write data and generation of acknowledge in succession. The E²PROM can receive as many write data as the maximum page size. Receiving a stop condition initiates a write cycle of the area starting from the designated memory address and having the page size equal to the received write data.

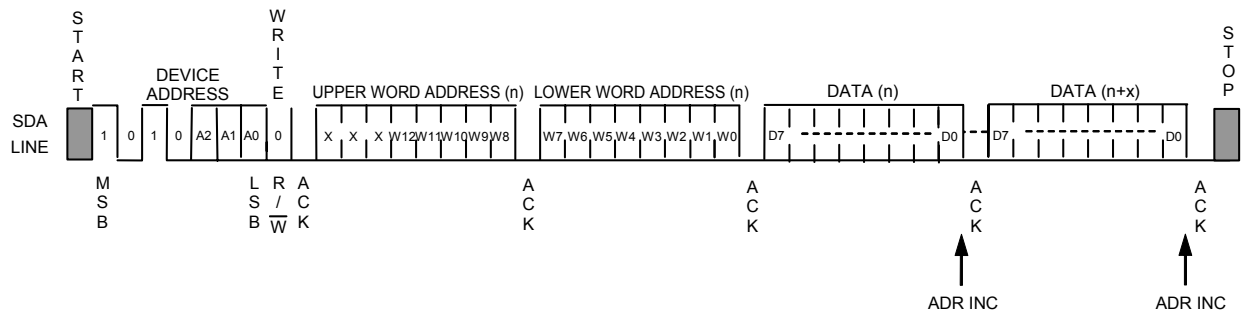


Figure 13 Page Write

The lower 5 bits of the word address are automatically incremented every time when the E²PROM receives 8-bit write data. If the size of the write data exceeds 32 bytes, the upper 8 bits of the word address remain unchanged, and the lower 5 bits are rolled over and previously received data will be overwritten.

6.3 Write Protection

Write protection is available in the S-24CS64A. When the WP pin is connected to the V_{CC}, write operation to memory area is forbidden at all.

When the WP pin is connected to the GND, the write protection is invalid, and write operation in all memory area is available.

Fix the level of the WP pin from the rising edge of SCL for loading the last write data (D0) until the end of the write time (10 ms max.). If the WP pin changes during this time, the address data being written at this time is not guaranteed.

There is no need for using write protection, the WP pin should be connected to the GND. The write protection is valid in the operating voltage range.

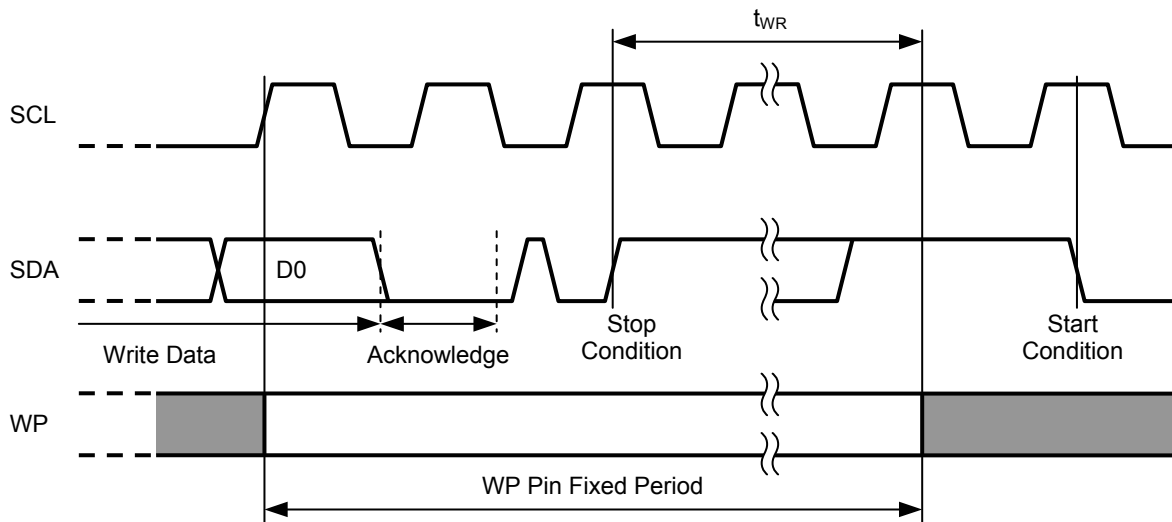


Figure 14 WP Pin Fixed Period

6.4 Acknowledge Polling

Acknowledge polling is used to know the completion of the write cycle in the E²PROM.

After the E²PROM receives a stop condition and once starts the write cycle, all operations are forbidden and no response is made to the signal transmitted by the master device.

Accordingly the master device can recognize the completion of the write cycle in the E²PROM by detecting a response from the slave device after transmitting the start condition, the device address and the read / write instruction code to the E²PROM, namely to the slave devices.

That is, if the E²PROM does not generate an acknowledge, the write cycle is in progress and if the E²PROM generates an acknowledge, the write cycle has been completed.

Keep the level of the WP pin fixed until acknowledge is confirmed.

It is recommended to use the read instruction "1" as the read / write instruction code transmitted by the master device.

7. Read

7.1 Current Address Read

Either in writing or in reading the E²PROM holds the last accessed memory address, internally incremented by one. The memory address is maintained as long as the power voltage is higher than the current address hold voltage V_{AH} .

The master device can read the data at the memory address of the current address pointer without assigning the word address as a result, when it recognizes the position of the address pointer in the E²PROM. This is called "Current Address Read".

In the following the address counter in the E²PROM is assumed to be "n".

When the E²PROM receives a 7-bit device address and a 1-bit read / write instruction code set to "1" following a start condition, it responds with an acknowledge.

Next an 8-bit data at the address "n" is sent from the E²PROM synchronous to the SCL clock. The address counter is incremented at the falling edge of the SCL clock for the 8th bit data, and the content of the address counter becomes n+1.

The master device outputs stop condition not an acknowledge, the reading of E²PROM is ended.

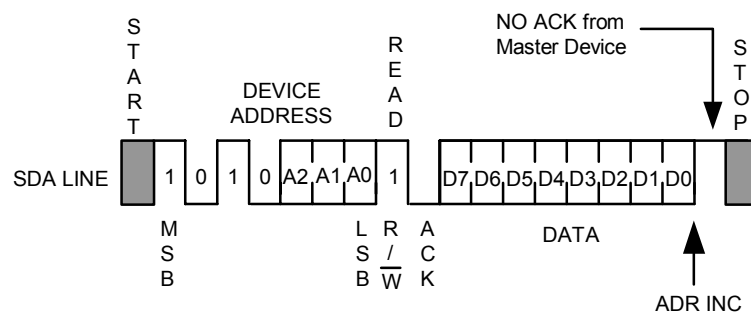


Figure 15 Current Address Read

Attention should be paid to the following point on the recognition of the address pointer in the E²PROM.

In the read operation the memory address counter in the E²PROM is automatically incremented at every falling edge of the SCL clock for the 8th bit of the output data. In the write operation, on the other hand, the upper 8 bits of the memory address are left unchanged and are not incremented at the falling edge of the SCL clock for the 8th bit of the received data.

7.2 Random Read

Random read is used to read the data at an arbitrary memory address.

A dummy write is performed to load the memory address into the address counter.

When the E²PROM receives a 7-bit device address and a 1-bit read / write instruction code set to “0” following a start condition, it responds with an acknowledge. The E²PROM then receives an 8-bit upper word address and responds with an acknowledge. Next the E²PROM then receives an 8-bit lower word address and responds with an acknowledge. The memory address is loaded to the address counter in the E²PROM by these operations. Reception of write data does not follow in a dummy write whereas reception of write data follows in a byte write and in a page write.

Since the memory address is loaded into the memory address counter by dummy write, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition and performing the same operation in the current address read.

That is, when the E²PROM receives a 7-bit device address and a 1-bit read / write instruction code set to “1”, following a start condition signal, it responds with an acknowledge. Next, 8-bit data is transmitted from the E²PROM in synchronous to the SCL clock. The master device outputs stop condition not an acknowledge, the reading of E²PROM is ended.

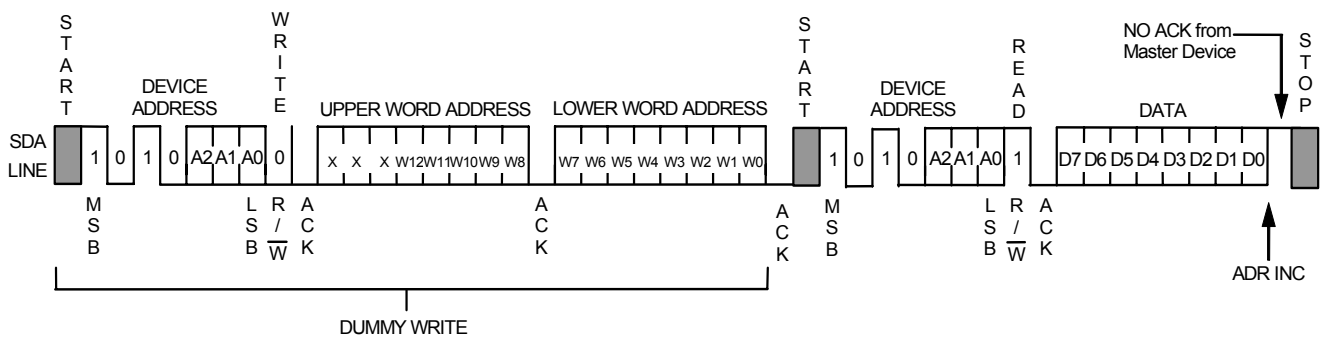


Figure 16 Random Read

7.3 Sequential Read

When the E²PROM receives a 7-bit device address and a 1-bit read / write instruction code set to “1” following a start condition both in current and random read operations, it responds with an acknowledge. An 8-bit data is then sent from the E²PROM synchronous to the SCL clock and the address counter is automatically incremented at the falling edge of the SCL clock for the 8th bit data. When the master device responds with an acknowledge, the data at the next memory address is transmitted. Response with an acknowledge by the master device has the memory address counter in the E²PROM incremented and makes it possible to read data in succession. This is called “Sequential Read”. The master device outputs stop condition not an acknowledge, the reading of E²PROM is ended. Data can be read in succession in the sequential read mode. When the memory address counter reaches the last word address, it rolls over to the first memory address.

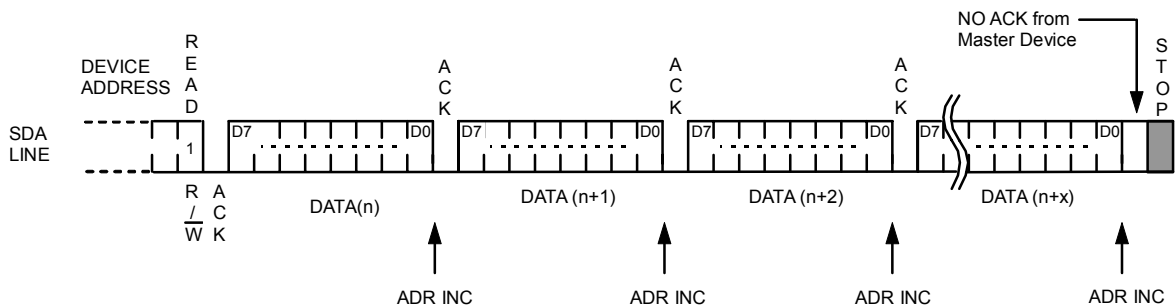


Figure 17 Sequential Read

8. Address Increment Timing

The timing for the automatic address increment is the falling edge of the SCL clock for the 8th bit of the read data in read operation and the the falling edge of the SCL clock for the 8th bit of the received data in write operation.

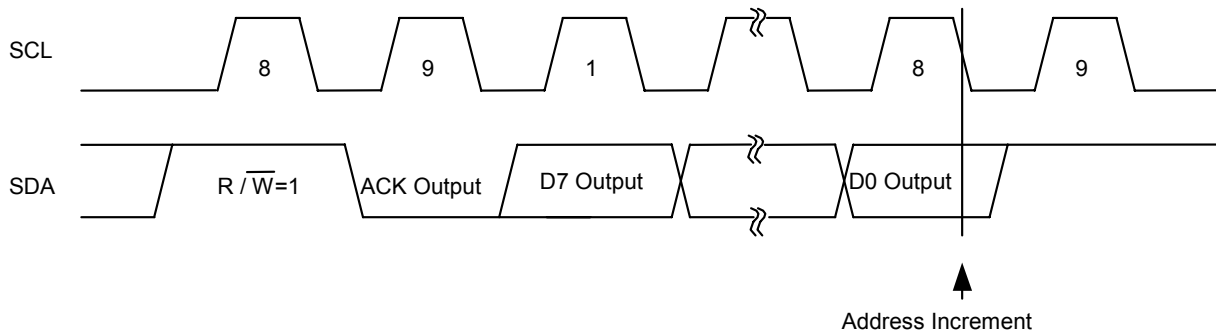


Figure 18 Address Increment Timing in Reading

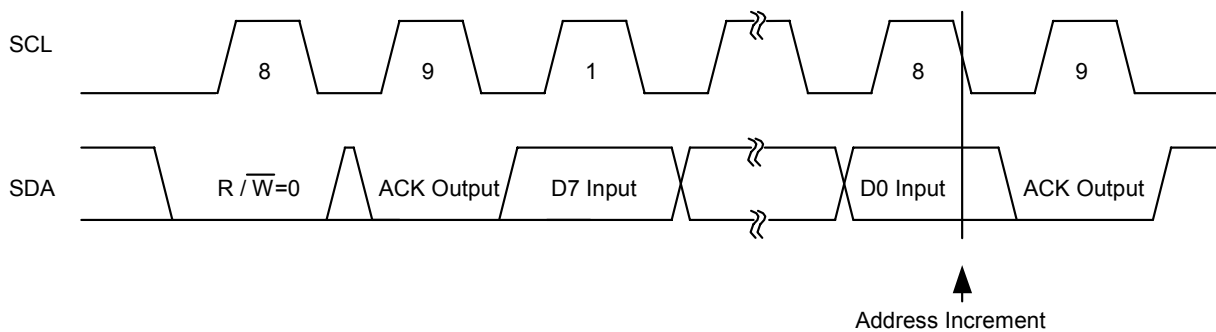


Figure 19 Address Increment Timing in Writing

Write Inhibition Function at Low Power Voltage

The S-24CS64A have a detection circuit for low power voltage. The detection circuit cancels a write instruction when the power voltage is low or the power switch is on. The detection voltage is 1.85 V typically and the release voltage is 1.95 V typically, the hysteresis of approximate 0.1 V thus exists. (See **Figure 20.**)

When a low power voltage is detected, a write instruction is canceled at the reception of a stop condition. When the power voltage lowers during a data transmission or a write operation, the date at the address of the operation is not assured.

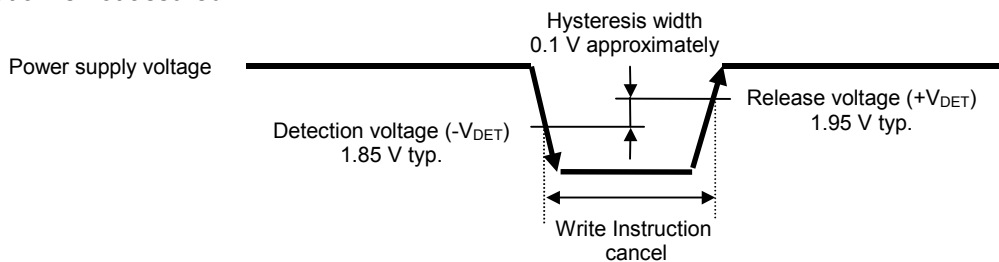


Figure 20 Operation at low power voltage

■ Using S-24CS64A

1. Adding a pull-up resistor to SDA I/O pin and SCL input pin

Add a 1 to 5 k Ω pull-up resistor to the SCL input pin*¹ and the SDA I/O pin in order to enable the functions of the I²C-bus protocol. Normal communication cannot be provided without a pull-up resistor.

*1. When the SCL input pin of the E²PROM is connected to a tri-state output pin of the microprocessor, connect the same pull-up resistor to prevent a high impedance status from being input to the SCL input pin.

This protects the E²PROM from malfunction due to an undefined output (high impedance) from the tri-state pin when the microprocessor is reset when the voltage drops.

2. I/O pin equivalent circuit

The I/O pins of this IC do not include pull-up and pull-down resistors. The SDA pin is an open-drain output. The following shows the equivalent circuits.

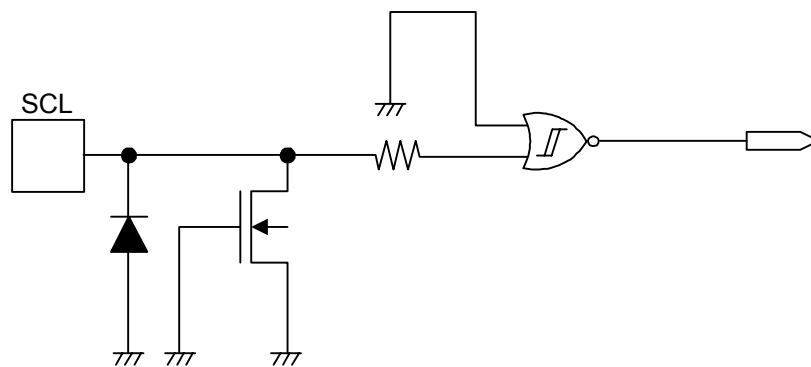


Figure 21 SCL Pin

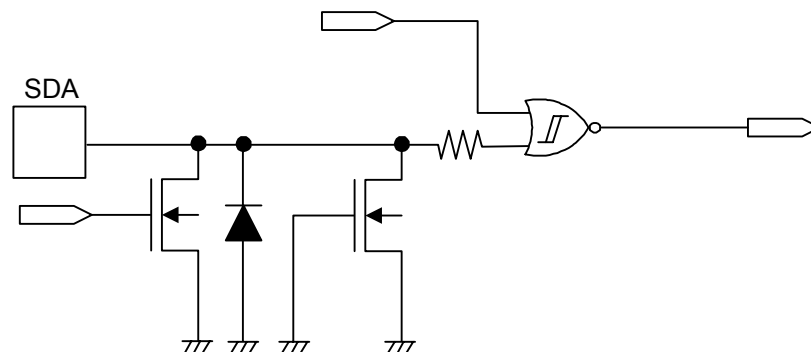


Figure 22 SDA Pin

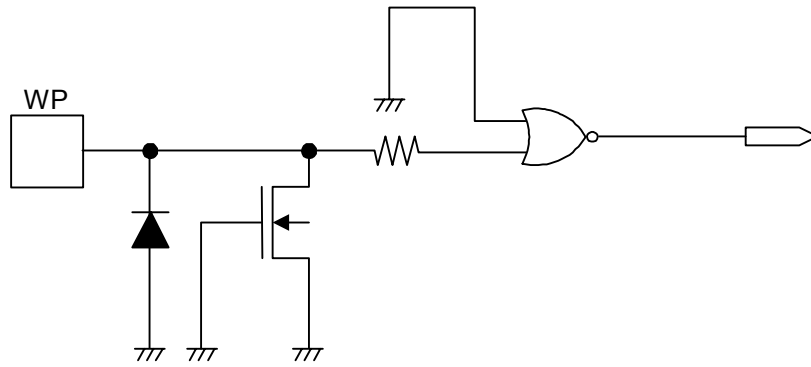


Figure 23 WP Pin

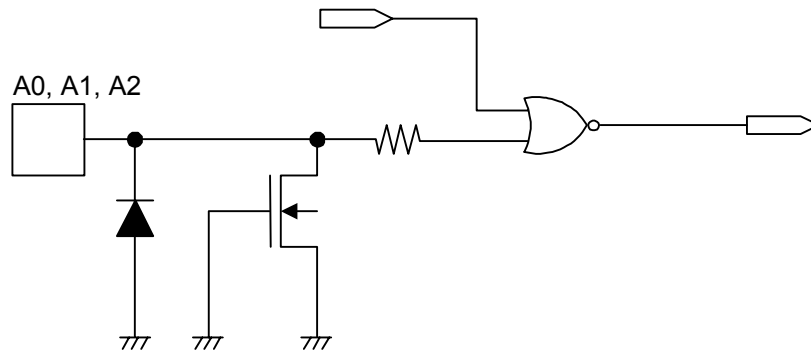


Figure 24 A0, A1, A2 Pin

3. Matching phases while E²PROM is accessed

The S-24CS64A does not have a pin for resetting (the internal circuit), therefore, the E²PROM cannot be forcibly reset externally. If a communication interruption occurs in the E²PROM, it must be reset by software.

For example, even if a reset signal is input to the microprocessor, the internal circuit of the E²PROM is not reset as long as the stop condition is not input to the E²PROM. In other words, the E²PROM retains the same status and cannot shift to the next operation. This symptom applies to the case when only the microprocessor is reset when the power supply voltage drops. With this status, if the power supply voltage is restored, reset the E²PROM (after matching the phase with the microprocessor) and input an instruction. The following shows this reset method.

[How to reset E²PROM]

The E²PROM can be reset by the start and stop instructions. When the E²PROM is reading data "0" or is outputting the acknowledge signal, 0 is output to the SDA line. In this status, the microprocessor cannot output an instruction to the SDA line. In this case, terminate the acknowledge output operation or read operation, and then input a start instruction. **Figure 25** shows this procedure.

First, input the condition. Then transmit 9 clocks (dummy clocks) of SCL. During this time, the microprocessor sets the SDA line to high level. By this operation, the E²PROM interrupts the acknowledge output operation or data output, so input the start condition*¹. When a start condition is input, the E²PROM is reset. To make doubly sure, input the stop condition to the E²PROM. Normal operation is then possible.

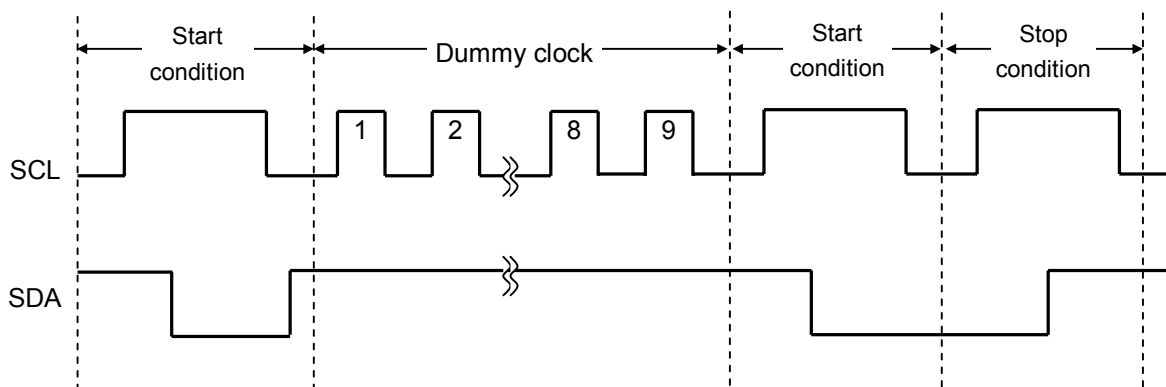


Figure 25 Resetting E²PROM

*1. After 9 clocks (dummy clocks), if the SCL clock continues to be output without a start condition being input, a write operation may be started upon receipt of a stop condition. To prevent this, input a start condition after 9 clocks (dummy clocks).

Remark It is recommended to perform the above reset using dummy clocks when the system is initialized after the power supply voltage has been raised.

4. Acknowledge check

The I²C-bus protocol includes an acknowledge check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the microprocessor and E²PROM. This function is effective to prevent malfunction, so it is recommended to perform an acknowledge check on the microprocessor side.

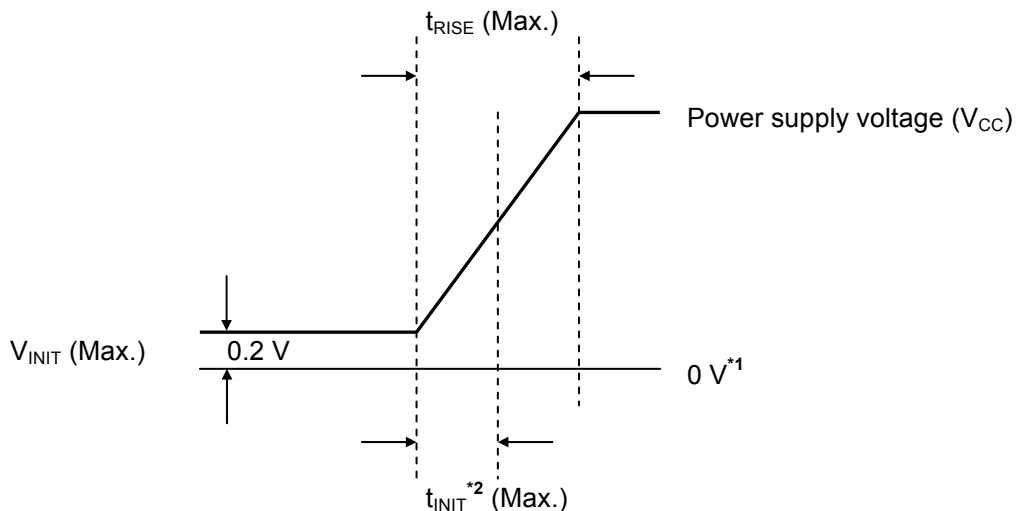
5. Built-in power-on-clear circuit

E²PROMs have a built-in power-on-clear circuit that initializes the E²PROM. Unsuccessful initialization may cause a malfunction. For the power-on-clear circuit to operate normally, the following conditions must be satisfied for raising the power supply voltage.

5.1 Raising power supply voltage

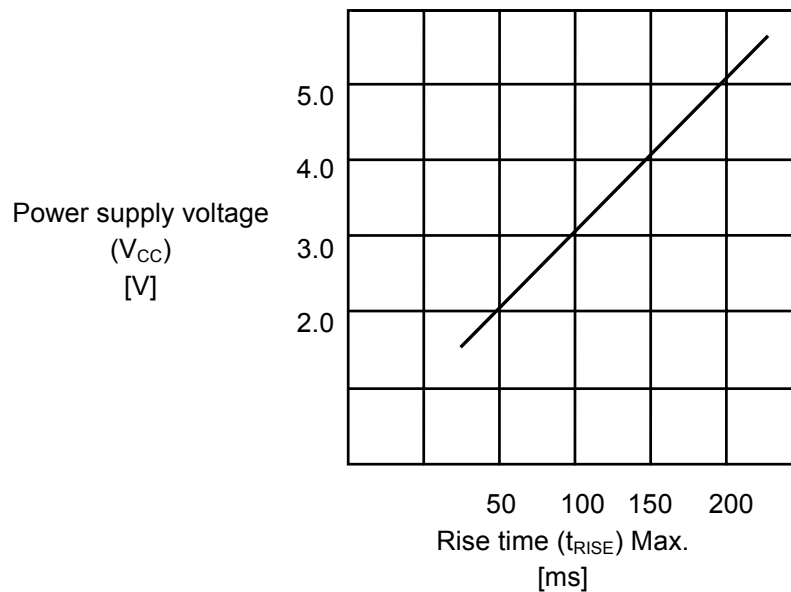
Raise the power supply voltage, starting at 0.2 V maximum, so that the voltage reaches the power supply voltage to be used within the time defined by t_{RISE} as shown in **Figure 26**.

For example, when the power supply voltage to be used is 5.0 V, t_{RISE} is 200 ms as shown in **Figure 27**. The power supply voltage must be raised within 200 ms.



- *1. 0 V means there is no difference in potential between the VCC pin and the GND pin of the E²PROM.
- *2. t_{INIT} is the time required to initialize the E²PROM. No instructions are accepted during this time.

Figure 26 Raising Power Supply Voltage



For example:

If your E²PROM supply voltage = 5.0 V, raise the power supply voltage to 5.0 V within 200 ms.

Figure 27 Raising Time of Power Supply Voltage

When initialization is successfully completed via the power-on-clear circuit, the E²PROM enters the standby status.

If the power-on-clear circuit does not operate, the following are the possible causes.

- (1) Because the E²PROM has not been initialized, an instruction formerly input is valid or an instruction may be inappropriately recognized. In this case, writing may be performed.
- (2) The voltage may have dropped due to power off while the E²PROM is being accessed. Even if the microprocessor is reset due to the low power voltage, the E²PROM may malfunction unless the power-on-clear operation conditions of E²PROM are satisfied. For the power-on-clear operation conditions of E²PROM, refer to **5.1 Raising power supply voltage**.

If the power-on-clear circuit does not operate, match the phase (reset) so that the internal E²PROM circuit is normally reset. The statuses of the E²PROM immediately after the power-on-clear circuit operates and when phase is matched (reset) are the same.

5.2 Wait for the initialization sequence to end

The E²PROM executes initialization during the time that the supply voltage is increasing to its normal value. All instructions must wait until after initialization. The relationship between the initialization time (t_{INIT}) and rise time (t_{RISE}) is shown in **Figure 28**.

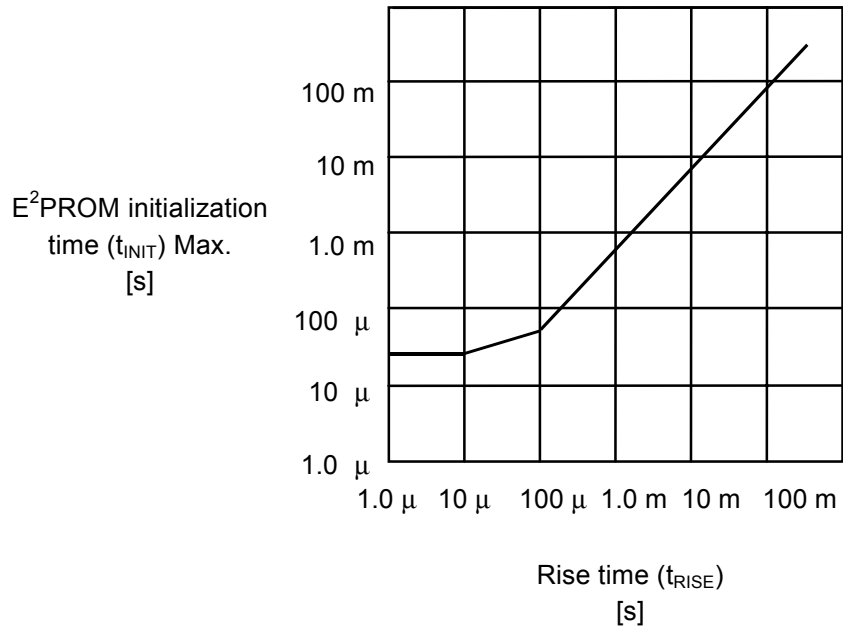


Figure 28 Initialization Time of E²PROM

6. Data hold time ($t_{HD, DAT} = 0 \text{ ns}$)

If SCL and SDA of the E²PROM are changed at the same time, it is necessary to prevent the start / stop condition from being mistakenly recognized due to the effect of noise. If a start / stop condition is mistakenly recognized during communication, the E²PROM enters the standby status. It is recommended that SDA is delayed from the falling edge of SCL by 0.3 μs minimum in the S-24CS64A. This is to prevent time lag caused by the load of the bus line from generating the stop (or start) condition.

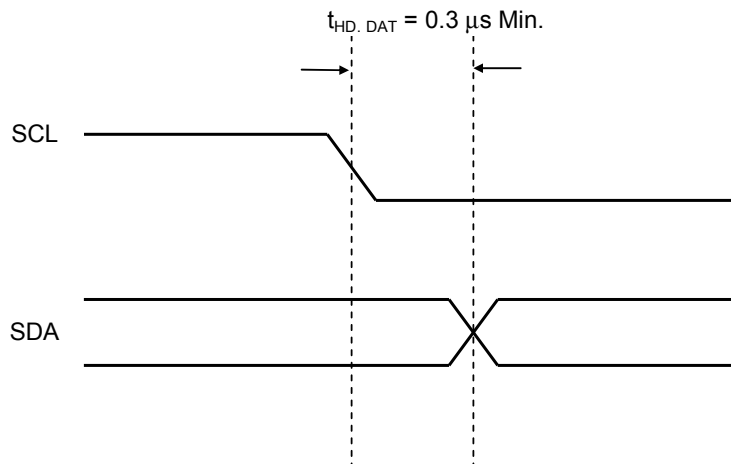


Figure 29 E²PROM Data Hold Time

7. SDA pin and SCL pin noise suppression time

The S-24CS64A includes a built-in low-pass filter to suppress noise at the SDA and SCL pins. This means that if the power supply voltage is 5.0 V, noise with a pulse width of 160 ns or less can be suppressed. The guaranteed for details, refer to noise suppression time (t_i) in **Table 11**.

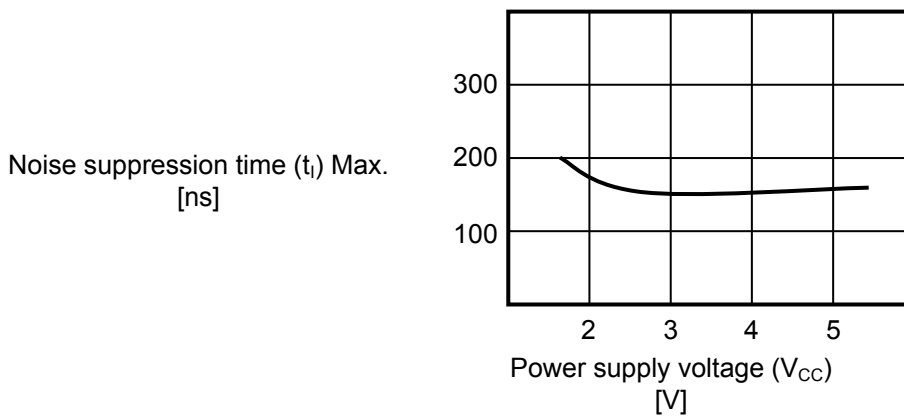


Figure 30 Noise Suppression Time for SDA and SCL Pins