



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



This IC, developed by CMOS technology, is a high-accuracy Hall effect switch IC that operates at a low voltage and low current consumption. The output voltage changes when this IC detects the intensity level of magnetic flux density. Using this IC with a magnet makes it possible to detect the open / close in various devices.

High-density mounting is possible by using the small SOT-23-3 or the super-small SNT-4A package.

Due to its low voltage operation and low current consumption, this IC is suitable for battery-operated portable devices. Also, due to its high-accuracy magnetic characteristics, this IC can make operation's dispersion in the system combined with magnet smaller.

ABLIC Inc. offers a "magnetic simulation service" that provides the ideal combination of magnets and our Hall ICs for customer systems. Our magnetic simulation service will reduce prototype production, development period and development costs. In addition, it will contribute to optimization of parts to realize high cost performance.

For more information regarding our magnetic simulation service, contact our sales office.

■ Features

- Pole detection^{*1}:
• Output logic^{*1}:
• Output form^{*1}:
• Magnetic sensitivity^{*1}:

• Operating cycle (current consumption)^{*1}:

• Power supply voltage range:
• Operation temperature range:
• Lead-free (Sn 100%), halogen-free
- Detection of omnipolar, S pole or N pole
Active "L", active "H"
Nch open-drain output, CMOS output
 $B_{OP} = 1.8 \text{ mT typ.}$
 $B_{OP} = 3.0 \text{ mT typ.}$
 $B_{OP} = 4.5 \text{ mT typ.}$
 $B_{OP} = 7.0 \text{ mT typ.}$
Product with omnipolar detection
 $t_{CYCLE} = 5.70 \text{ ms (} I_{DD} = 12.0 \mu\text{A) typ.}$
 $t_{CYCLE} = 50.50 \text{ ms (} I_{DD} = 2.0 \mu\text{A) typ.}$
 $t_{CYCLE} = 204.10 \text{ ms (} I_{DD} = 1.0 \mu\text{A) typ.}$
Product with S pole or N pole detection
 $t_{CYCLE} = 6.05 \text{ ms (} I_{DD} = 6.0 \mu\text{A) typ.}$
 $t_{CYCLE} = 50.85 \text{ ms (} I_{DD} = 1.4 \mu\text{A) typ.}$
 $t_{CYCLE} = 204.05 \text{ ms (} I_{DD} = 1.0 \mu\text{A) typ.}$
 $V_{DD} = 1.6 \text{ V to } 3.5 \text{ V}$
 $T_a = -40^\circ\text{C to } +85^\circ\text{C}$

*1. The option can be selected.

■ Applications

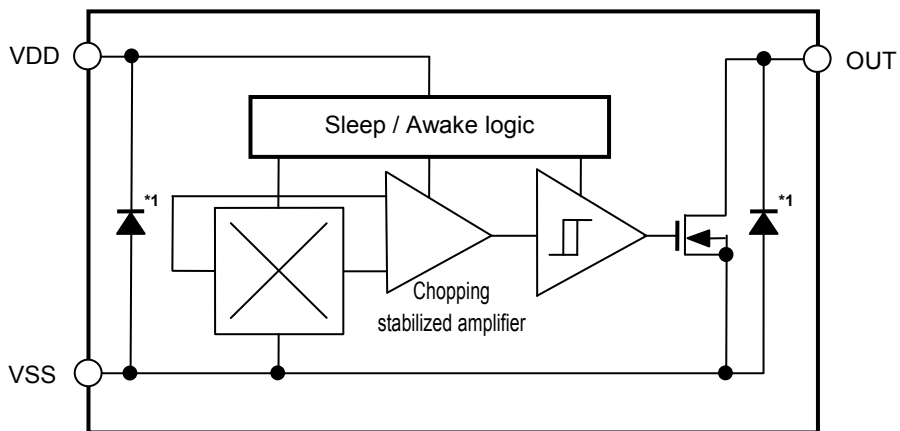
- Mobile phone, smart phone
- Notebook PC, tablet PC
- Digital video camera
- Plaything, portable game
- Home appliance

■ Packages

- SOT-23-3
- SNT-4A

■ Block Diagrams

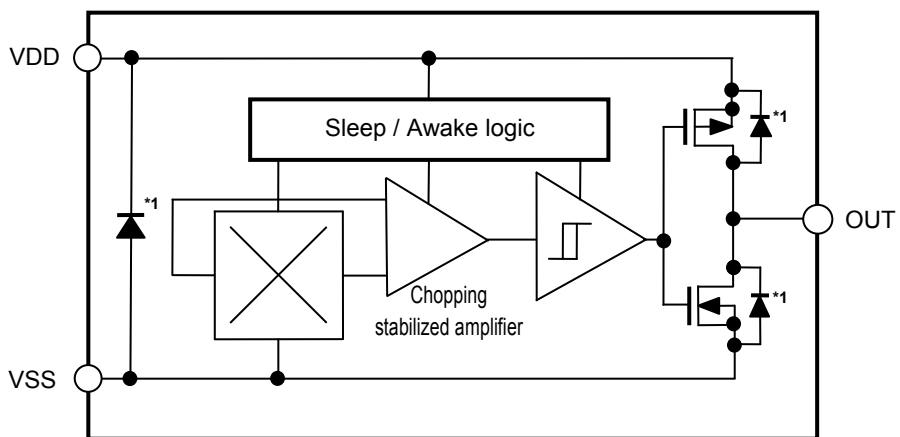
1. Nch open-drain output product



*1. Parasitic diode

Figure 1

2. CMOS output product

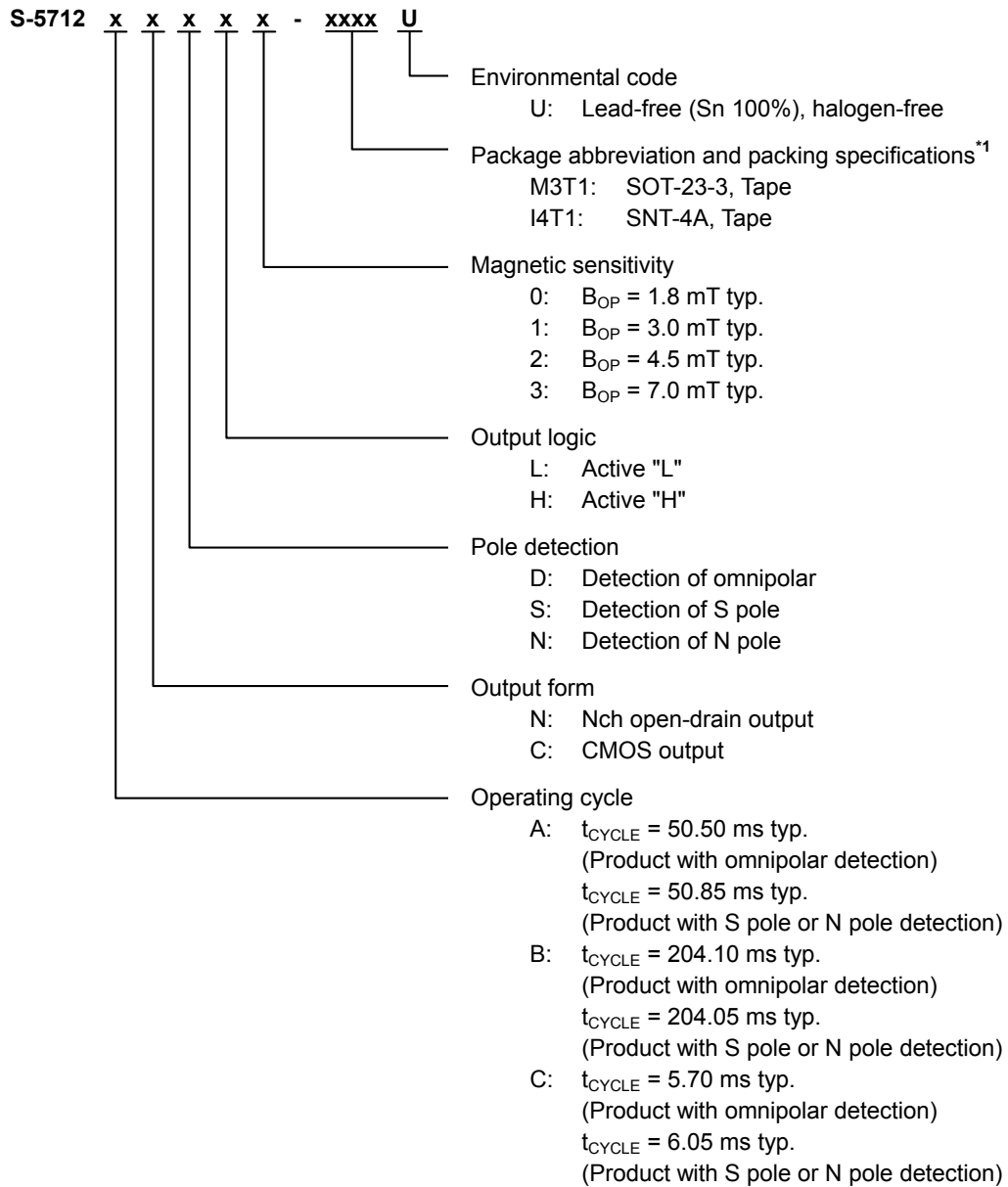


*1. Parasitic diode

Figure 2

■ **Product Name Structure**

1. **Product name**



*1. Refer to the tape drawing.

2. **Packages**

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-23-3	MP003-C-P-SD	MP003-C-C-SD	MP003-Z-R-SD	-
SNT-4A	PF004-A-P-SD	PF004-A-C-SD	PF004-A-R-SD	PF004-A-L-SD

3. Product name list

3.1 SOT-23-3

3.1.1 Nch open-drain output product

Table 2

Product Name	Operating Cycle (t_{CYCLE})	Output Form	Pole Detection	Output Logic	Magnetic Sensitivity (B_{OP})
S-5712ANDL0-M3T1U	50.50 ms typ.	Nch open-drain output	Omnipolar	Active "L"	1.8 mT typ.
S-5712ANDL1-M3T1U	50.50 ms typ.	Nch open-drain output	Omnipolar	Active "L"	3.0 mT typ.
S-5712ANDL2-M3T1U	50.50 ms typ.	Nch open-drain output	Omnipolar	Active "L"	4.5 mT typ.
S-5712ANSL1-M3T1U	50.85 ms typ.	Nch open-drain output	S pole	Active "L"	3.0 mT typ.
S-5712ANSL2-M3T1U	50.85 ms typ.	Nch open-drain output	S pole	Active "L"	4.5 mT typ.
S-5712ANSH1-M3T1U	50.85 ms typ.	Nch open-drain output	S pole	Active "H"	3.0 mT typ.
S-5712BNDL2-M3T1U	204.10 ms typ.	Nch open-drain output	Omnipolar	Active "L"	4.5 mT typ.
S-5712BNDH2-M3T1U	204.10 ms typ.	Nch open-drain output	Omnipolar	Active "H"	4.5 mT typ.

Remark Please contact our sales office for products other than the above.

3.1.2 CMOS output product

Table 3

Product Name	Operating Cycle (t_{CYCLE})	Output Form	Pole Detection	Output Logic	Magnetic Sensitivity (B_{OP})
S-5712ACDL1-M3T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "L"	3.0 mT typ.
S-5712ACDL2-M3T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "L"	4.5 mT typ.
S-5712ACDH1-M3T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "H"	3.0 mT typ.
S-5712ACDH2-M3T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "H"	4.5 mT typ.
S-5712ACSL1-M3T1U	50.85 ms typ.	CMOS output	S pole	Active "L"	3.0 mT typ.
S-5712ACSL2-M3T1U	50.85 ms typ.	CMOS output	S pole	Active "L"	4.5 mT typ.
S-5712ACNL1-M3T1U	50.85 ms typ.	CMOS output	N pole	Active "L"	3.0 mT typ.
S-5712ACNL2-M3T1U	50.85 ms typ.	CMOS output	N pole	Active "L"	4.5 mT typ.
S-5712CCDL1-M3T1U	5.70 ms typ.	CMOS output	Omnipolar	Active "L"	3.0 mT typ.
S-5712CCSL1-M3T1U	6.05 ms typ.	CMOS output	S pole	Active "L"	3.0 mT typ.

Remark Please contact our sales office for products other than the above.

3.2 SNT-4A

3.2.1 Nch open-drain output product

Table 4

Product Name	Operating Cycle (t_{CYCLE})	Output Form	Pole Detection	Output Logic	Magnetic Sensitivity (B_{OP})
S-5712ANDL0-I4T1U	50.50 ms typ.	Nch open-drain output	Omnipolar	Active "L"	1.8 mT typ.
S-5712ANDL1-I4T1U	50.50 ms typ.	Nch open-drain output	Omnipolar	Active "L"	3.0 mT typ.
S-5712ANDL2-I4T1U	50.50 ms typ.	Nch open-drain output	Omnipolar	Active "L"	4.5 mT typ.
S-5712ANSL1-I4T1U	50.85 ms typ.	Nch open-drain output	S pole	Active "L"	3.0 mT typ.
S-5712ANSL2-I4T1U	50.85 ms typ.	Nch open-drain output	S pole	Active "L"	4.5 mT typ.
S-5712BNDL2-I4T1U	204.10 ms typ.	Nch open-drain output	Omnipolar	Active "L"	4.5 mT typ.
S-5712BNDH2-I4T1U	204.10 ms typ.	Nch open-drain output	Omnipolar	Active "H"	4.5 mT typ.

Remark Please contact our sales office for products other than the above.

3.2.2 CMOS output product

Table 5

Product Name	Operating Cycle (t_{CYCLE})	Output Form	Pole Detection	Output Logic	Magnetic Sensitivity (B_{OP})
S-5712ACDL0-I4T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "L"	1.8 mT typ.
S-5712ACDL1-I4T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "L"	3.0 mT typ.
S-5712ACDL2-I4T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "L"	4.5 mT typ.
S-5712ACDL3-I4T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "L"	7.0 mT typ.
S-5712ACDH1-I4T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "H"	3.0 mT typ.
S-5712ACDH2-I4T1U	50.50 ms typ.	CMOS output	Omnipolar	Active "H"	4.5 mT typ.
S-5712ACSL1-I4T1U	50.85 ms typ.	CMOS output	S pole	Active "L"	3.0 mT typ.
S-5712ACSL2-I4T1U	50.85 ms typ.	CMOS output	S pole	Active "L"	4.5 mT typ.
S-5712ACSH1-I4T1U	50.85 ms typ.	CMOS output	S pole	Active "H"	3.0 mT typ.
S-5712ACSH2-I4T1U	50.85 ms typ.	CMOS output	S pole	Active "H"	4.5 mT typ.
S-5712ACNL1-I4T1U	50.85 ms typ.	CMOS output	N pole	Active "L"	3.0 mT typ.
S-5712ACNL2-I4T1U	50.85 ms typ.	CMOS output	N pole	Active "L"	4.5 mT typ.
S-5712ACNL3-I4T1U	50.85 ms typ.	CMOS output	N pole	Active "L"	7.0 mT typ.
S-5712ACNH1-I4T1U	50.85 ms typ.	CMOS output	N pole	Active "H"	3.0 mT typ.
S-5712BCDL1-I4T1U	204.10 ms typ.	CMOS output	Omnipolar	Active "L"	3.0 mT typ.
S-5712BCDL2-I4T1U	204.10 ms typ.	CMOS output	Omnipolar	Active "L"	4.5 mT typ.
S-5712BCDH1-I4T1U	204.10 ms typ.	CMOS output	Omnipolar	Active "H"	3.0 mT typ.
S-5712BCDH2-I4T1U	204.10 ms typ.	CMOS output	Omnipolar	Active "H"	4.5 mT typ.
S-5712BCSL2-I4T1U	204.05 ms typ.	CMOS output	S pole	Active "L"	4.5 mT typ.
S-5712CCDL1-I4T1U	5.70 ms typ.	CMOS output	Omnipolar	Active "L"	3.0 mT typ.
S-5712CCDH1-I4T1U	5.70 ms typ.	CMOS output	Omnipolar	Active "H"	3.0 mT typ.
S-5712CCSL1-I4T1U	6.05 ms typ.	CMOS output	S pole	Active "L"	3.0 mT typ.
S-5712CCNL1-I4T1U	6.05 ms typ.	CMOS output	N pole	Active "L"	3.0 mT typ.

Remark Please contact our sales office for products other than the above.

■ Pin Configurations

1. SOT-23-3

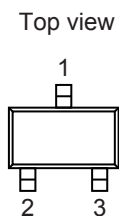


Figure 3

Table 6

Pin No.	Symbol	Pin Description
1	VSS	GND pin
2	VDD	Power supply pin
3	OUT	Output pin

2. SNT-4A

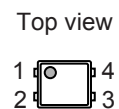


Figure 4

Table 7

Pin No.	Symbol	Pin Description
1	VDD	Power supply pin
2	VSS	GND pin
3	NC*1	No connection
4	OUT	Output pin

*1. The NC pin is electrically open.
 The NC pin can be connected to the VDD pin or the VSS pin.

■ Absolute Maximum Ratings

Table 8

(Ta = +25°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V _{DD}	V _{SS} - 0.3 to V _{SS} + 7.0	V
Output current	I _{OUT}	±1.0	mA
Output voltage	Nch open-drain output product	V _{OUT}	V _{SS} - 0.3 to V _{SS} + 7.0
	CMOS output product		V _{SS} - 0.3 to V _{DD} + 0.3
Operation ambient temperature	T _{opr}	-40 to +85	°C
Storage temperature	T _{stg}	-40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 9

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	
Junction-to-ambient thermal resistance *1	θ _{JA}	SOT-23-3	Board A	-	200	-	°C/W
			Board B	-	165	-	°C/W
			Board C	-	-	-	°C/W
			Board D	-	-	-	°C/W
			Board E	-	-	-	°C/W
		SNT-4A	Board A	-	300	-	°C/W
			Board B	-	242	-	°C/W
			Board C	-	-	-	°C/W
			Board D	-	-	-	°C/W
			Board E	-	-	-	°C/W

*1. Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ Power Dissipation" and "Test Board" for details.

■ Electrical Characteristics

1. Product with omnipolar detection

1.1 S-5712AxDxx

Table 10

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V _{DD}	-		1.60	1.85	3.50	V	-
Current consumption	I _{DD}	Average value		-	2.0	4.0	μA	1
Output voltage	V _{OUT}	Nch open-drain output product	Output transistor Nch, I _{OUT} = 0.5 mA	-	-	0.4	V	2
		CMOS output product	Output transistor Nch, I _{OUT} = 0.5 mA	-	-	0.4	V	2
			Output transistor Pch, I _{OUT} = -0.5 mA	V _{DD} - 0.4	-	-	V	3
Leakage current	I _{LEAK}	Nch open-drain output product Output transistor Nch, V _{OUT} = 3.5 V		-	-	1	μA	4
Awake mode time	t _{AW}	-		-	0.10	-	ms	-
Sleep mode time	t _{SL}	-		-	50.40	-	ms	-
Operating cycle	t _{CYCLE}	t _{AW} + t _{SL}		-	50.50	100.00	ms	-

1.2 S-5712BxDxx

Table 11

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V _{DD}	-		1.60	1.85	3.50	V	-
Current consumption	I _{DD}	Average value		-	1.0	2.0	μA	1
Output voltage	V _{OUT}	Nch open-drain output product	Output transistor Nch, I _{OUT} = 0.5 mA	-	-	0.4	V	2
		CMOS output product	Output transistor Nch, I _{OUT} = 0.5 mA	-	-	0.4	V	2
			Output transistor Pch, I _{OUT} = -0.5 mA	V _{DD} - 0.4	-	-	V	3
Leakage current	I _{LEAK}	Nch open-drain output product Output transistor Nch, V _{OUT} = 3.5 V		-	-	1	μA	4
Awake mode time	t _{AW}	-		-	0.10	-	ms	-
Sleep mode time	t _{SL}	-		-	204.00	-	ms	-
Operating cycle	t _{CYCLE}	t _{AW} + t _{SL}		-	204.10	400.00	ms	-

1.3 S-5712CxDxx

Table 12

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Power supply voltage	V _{DD}	–	1.60	1.85	3.50	V	–	
Current consumption	I _{DD}	Average value	–	12.0	22.0	μA	1	
Output voltage	V _{OUT}	Nch open-drain output product	Output transistor Nch, I _{OUT} = 0.5 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I _{OUT} = 0.5 mA	–	–	0.4	V	2
			Output transistor Pch, I _{OUT} = –0.5 mA	V _{DD} – 0.4	–	–	V	3
Leakage current	I _{LEAK}	Nch open-drain output product Output transistor Nch, V _{OUT} = 3.5 V	–	–	1	μA	4	
Awake mode time	t _{AW}	–	–	0.10	–	ms	–	
Sleep mode time	t _{SL}	–	–	5.60	–	ms	–	
Operating cycle	t _{CYCLE}	t _{AW} + t _{SL}	–	5.70	12.00	ms	–	

2. Product with S pole or N pole detection

2.1 S-5712AxSxx, S-5712AxNxx

Table 13

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Power supply voltage	V _{DD}	–	1.60	1.85	3.50	V	–	
Current consumption	I _{DD}	Average value	–	1.4	3.0	μA	1	
Output voltage	V _{OUT}	Nch open-drain output product	Output transistor Nch, I _{OUT} = 0.5 mA	–	–	0.4	V	2
		CMOS output product	Output transistor Nch, I _{OUT} = 0.5 mA	–	–	0.4	V	2
			Output transistor Pch, I _{OUT} = –0.5 mA	V _{DD} – 0.4	–	–	V	3
Leakage current	I _{LEAK}	Nch open-drain output product Output transistor Nch, V _{OUT} = 3.5 V	–	–	1	μA	4	
Awake mode time	t _{AW}	–	–	0.05	–	ms	–	
Sleep mode time	t _{SL}	–	–	50.80	–	ms	–	
Operating cycle	t _{CYCLE}	t _{AW} + t _{SL}	–	50.85	100.00	ms	–	

2.2 S-5712BxSxx, S-5712BxNxx

Table 14

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V _{DD}	-		1.60	1.85	3.50	V	-
Current consumption	I _{DD}	Average value		-	1.0	2.0	μA	1
Output voltage	V _{OUT}	Nch open-drain output product	Output transistor Nch, I _{OUT} = 0.5 mA	-	-	0.4	V	2
		CMOS output product	Output transistor Nch, I _{OUT} = 0.5 mA	-	-	0.4	V	2
			Output transistor Pch, I _{OUT} = -0.5 mA	V _{DD} - 0.4	-	-	V	3
Leakage current	I _{LEAK}	Nch open-drain output product Output transistor Nch, V _{OUT} = 3.5 V		-	-	1	μA	4
Awake mode time	t _{AW}	-		-	0.05	-	ms	-
Sleep mode time	t _{SL}	-		-	204.00	-	ms	-
Operating cycle	t _{CYCLE}	t _{AW} + t _{SL}		-	204.05	400.00	ms	-

2.3 S-5712CxSxx, S-5712CxNxx

Table 15

(Ta = +25°C, V_{DD} = 1.85 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V _{DD}	-		1.60	1.85	3.50	V	-
Current consumption	I _{DD}	Average value		-	6.0	11.0	μA	1
Output voltage	V _{OUT}	Nch open-drain output product	Output transistor Nch, I _{OUT} = 0.5 mA	-	-	0.4	V	2
		CMOS output product	Output transistor Nch, I _{OUT} = 0.5 mA	-	-	0.4	V	2
			Output transistor Pch, I _{OUT} = -0.5 mA	V _{DD} - 0.4	-	-	V	3
Leakage current	I _{LEAK}	Nch open-drain output product Output transistor Nch, V _{OUT} = 3.5 V		-	-	1	μA	4
Awake mode time	t _{AW}	-		-	0.05	-	ms	-
Sleep mode time	t _{SL}	-		-	6.00	-	ms	-
Operating cycle	t _{CYCLE}	t _{AW} + t _{SL}		-	6.05	12.00	ms	-

■ **Magnetic Characteristics**

1. **Product with omnipolar detection**

1.1 **Product with $B_{OP} = 1.8$ mT typ.**

Table 16

($T_a = +25^\circ\text{C}$, $V_{DD} = 1.85$ V, $V_{SS} = 0$ V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Operation point* ¹	S pole	B_{OPS}	–	0.6	1.8	3.0	mT	5
	N pole	B_{OPN}	–	–3.0	–1.8	–0.6	mT	5
Release point* ²	S pole	B_{RPS}	–	0.1	1.1	2.4	mT	5
	N pole	B_{RPN}	–	–2.4	–1.1	–0.1	mT	5
Hysteresis width* ³	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	0.7	–	mT	5
	N pole	B_{HYSN}	$B_{HYSN} = B_{OPN} - B_{RPN} $	–	0.7	–	mT	5

1.2 **Product with $B_{OP} = 3.0$ mT typ.**

Table 17

($T_a = +25^\circ\text{C}$, $V_{DD} = 1.85$ V, $V_{SS} = 0$ V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Operation point* ¹	S pole	B_{OPS}	–	1.4	3.0	4.0	mT	5
	N pole	B_{OPN}	–	–4.0	–3.0	–1.4	mT	5
Release point* ²	S pole	B_{RPS}	–	1.1	2.2	3.7	mT	5
	N pole	B_{RPN}	–	–3.7	–2.2	–1.1	mT	5
Hysteresis width* ³	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	0.8	–	mT	5
	N pole	B_{HYSN}	$B_{HYSN} = B_{OPN} - B_{RPN} $	–	0.8	–	mT	5

1.3 **Product with $B_{OP} = 4.5$ mT typ.**

Table 18

($T_a = +25^\circ\text{C}$, $V_{DD} = 1.85$ V, $V_{SS} = 0$ V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Operation point* ¹	S pole	B_{OPS}	–	2.5	4.5	6.0	mT	5
	N pole	B_{OPN}	–	–6.0	–4.5	–2.5	mT	5
Release point* ²	S pole	B_{RPS}	–	2.0	3.5	5.5	mT	5
	N pole	B_{RPN}	–	–5.5	–3.5	–2.0	mT	5
Hysteresis width* ³	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	1.0	–	mT	5
	N pole	B_{HYSN}	$B_{HYSN} = B_{OPN} - B_{RPN} $	–	1.0	–	mT	5

1.4 **Product with $B_{OP} = 7.0$ mT typ.**

Table 19

($T_a = +25^\circ\text{C}$, $V_{DD} = 1.85$ V, $V_{SS} = 0$ V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit	
Operation point* ¹	S pole	B_{OPS}	–	5.0	7.0	8.5	mT	5
	N pole	B_{OPN}	–	–8.5	–7.0	–5.0	mT	5
Release point* ²	S pole	B_{RPS}	–	3.7	5.2	7.2	mT	5
	N pole	B_{RPN}	–	–7.2	–5.2	–3.7	mT	5
Hysteresis width* ³	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	1.8	–	mT	5
	N pole	B_{HYSN}	$B_{HYSN} = B_{OPN} - B_{RPN} $	–	1.8	–	mT	5

2. Product with S pole detection

2.1 Product with $B_{OP} = 1.8$ mT typ.

Table 20

($T_a = +25^\circ\text{C}$, $V_{DD} = 1.85$ V, $V_{SS} = 0$ V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point ^{*1}	S pole	B_{OPS}	–	0.6	1.8	3.0	mT	5
Release point ^{*2}	S pole	B_{RPS}	–	0.1	1.1	2.4	mT	5
Hysteresis width ^{*3}	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	0.7	–	mT	5

2.2 Product with $B_{OP} = 3.0$ mT typ.

Table 21

($T_a = +25^\circ\text{C}$, $V_{DD} = 1.85$ V, $V_{SS} = 0$ V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point ^{*1}	S pole	B_{OPS}	–	1.4	3.0	4.0	mT	5
Release point ^{*2}	S pole	B_{RPS}	–	1.1	2.2	3.7	mT	5
Hysteresis width ^{*3}	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	0.8	–	mT	5

2.3 Product with $B_{OP} = 4.5$ mT typ.

Table 22

($T_a = +25^\circ\text{C}$, $V_{DD} = 1.85$ V, $V_{SS} = 0$ V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point ^{*1}	S pole	B_{OPS}	–	2.5	4.5	6.0	mT	5
Release point ^{*2}	S pole	B_{RPS}	–	2.0	3.5	5.5	mT	5
Hysteresis width ^{*3}	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	1.0	–	mT	5

2.4 Product with $B_{OP} = 7.0$ mT typ.

Table 23

($T_a = +25^\circ\text{C}$, $V_{DD} = 1.85$ V, $V_{SS} = 0$ V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point ^{*1}	S pole	B_{OPS}	–	5.0	7.0	8.5	mT	5
Release point ^{*2}	S pole	B_{RPS}	–	3.7	5.2	7.2	mT	5
Hysteresis width ^{*3}	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	1.8	–	mT	5

3. Product with N pole detection

3.1 Product with $B_{OP} = 1.8 \text{ mT typ.}$

Table 24

($T_a = +25^\circ\text{C}$, $V_{DD} = 1.85 \text{ V}$, $V_{SS} = 0 \text{ V}$ unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point ^{*1}	N pole	B_{OPN}	–	–3.0	–1.8	–0.6	mT	5
Release point ^{*2}	N pole	B_{RPN}	–	–2.4	–1.1	–0.1	mT	5
Hysteresis width ^{*3}	N pole	B_{HYSN}	$B_{HYSN} = B_{OPN} - B_{RPN} $	–	0.7	–	mT	5

3.2 Product with $B_{OP} = 3.0 \text{ mT typ.}$

Table 25

($T_a = +25^\circ\text{C}$, $V_{DD} = 1.85 \text{ V}$, $V_{SS} = 0 \text{ V}$ unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point ^{*1}	N pole	B_{OPN}	–	–4.0	–3.0	–1.4	mT	5
Release point ^{*2}	N pole	B_{RPN}	–	–3.7	–2.2	–1.1	mT	5
Hysteresis width ^{*3}	N pole	B_{HYSN}	$B_{HYSN} = B_{OPN} - B_{RPN} $	–	0.8	–	mT	5

3.3 Product with $B_{OP} = 4.5 \text{ mT typ.}$

Table 26

($T_a = +25^\circ\text{C}$, $V_{DD} = 1.85 \text{ V}$, $V_{SS} = 0 \text{ V}$ unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point ^{*1}	N pole	B_{OPN}	–	–6.0	–4.5	–2.5	mT	5
Release point ^{*2}	N pole	B_{RPN}	–	–5.5	–3.5	–2.0	mT	5
Hysteresis width ^{*3}	N pole	B_{HYSN}	$B_{HYSN} = B_{OPN} - B_{RPN} $	–	1.0	–	mT	5

3.4 Product with $B_{OP} = 7.0 \text{ mT typ.}$

Table 27

($T_a = +25^\circ\text{C}$, $V_{DD} = 1.85 \text{ V}$, $V_{SS} = 0 \text{ V}$ unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point ^{*1}	N pole	B_{OPN}	–	–8.5	–7.0	–5.0	mT	5
Release point ^{*2}	N pole	B_{RPN}	–	–7.2	–5.2	–3.7	mT	5
Hysteresis width ^{*3}	N pole	B_{HYSN}	$B_{HYSN} = B_{OPN} - B_{RPN} $	–	1.8	–	mT	5

***1.** B_{OPN} , B_{OPS} : Operation points

B_{OPN} and B_{OPS} are the values of magnetic flux density when the output voltage (V_{OUT}) changes after the magnetic flux density applied to this IC by the magnet (N pole or S pole) is increased (by moving the magnet closer).
Even when the magnetic flux density exceeds B_{OPN} or B_{OPS} , V_{OUT} retains the status.

***2.** B_{RPN} , B_{RPS} : Release points

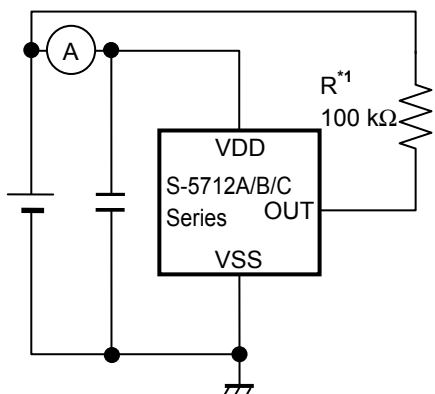
B_{RPN} and B_{RPS} are the values of magnetic flux density when the output voltage (V_{OUT}) changes after the magnetic flux density applied to this IC by the magnet (N pole or S pole) is decreased (the magnet is moved further away).
Even when the magnetic flux density falls below B_{RPN} or B_{RPS} , V_{OUT} retains the status.

***3.** B_{HYSN} , B_{HYSS} : Hysteresis widths

B_{HYSN} and B_{HYSS} are the difference between B_{OPN} and B_{RPN} , and B_{OPS} and B_{RPS} , respectively.

Remark The unit of magnetic density mT can be converted by using the formula $1 \text{ mT} = 10 \text{ Gauss}$.

■ Test Circuits



*1. Resistor (R) is unnecessary for the CMOS output product.

Figure 5 Test Circuit 1

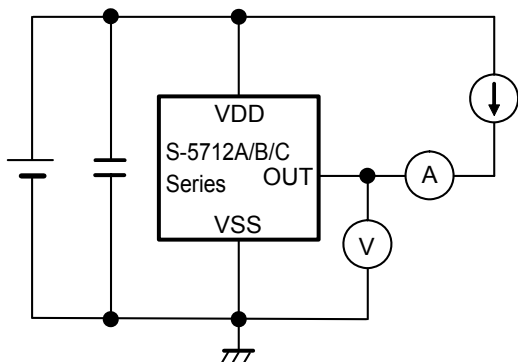


Figure 6 Test Circuit 2

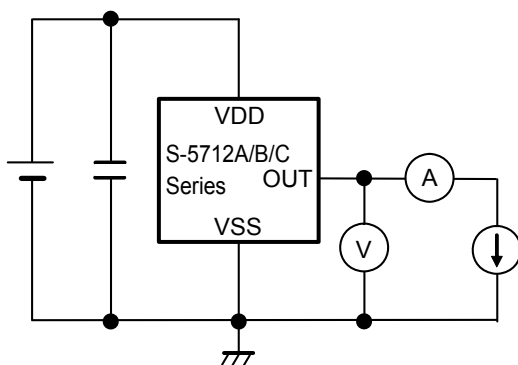


Figure 7 Test Circuit 3

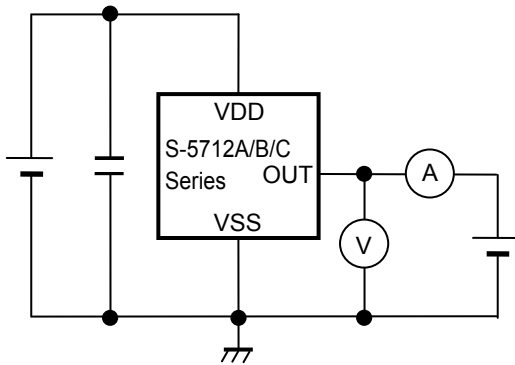
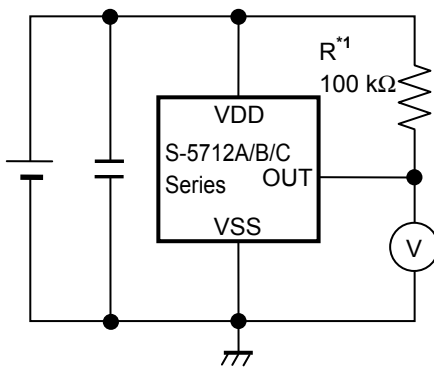


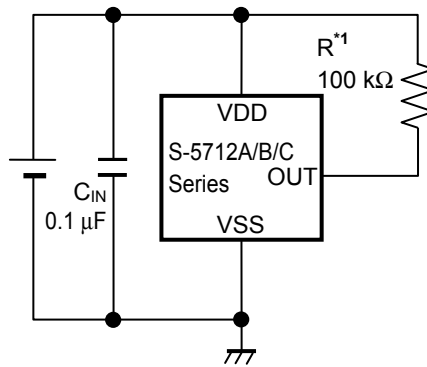
Figure 8 Test Circuit 4



*1. Resistor (R) is unnecessary for the CMOS output product.

Figure 9 Test Circuit 5

■ Standard Circuit



*1. Resistor (R) is unnecessary for the CMOS output product.

Figure 10

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

■ Operation

1. Direction of applied magnetic flux

This IC detects the flux density which is vertical to the marking surface.

Figure 11 and Figure 12 show the direction in which magnetic flux is being applied.

1.1 SOT-23-3

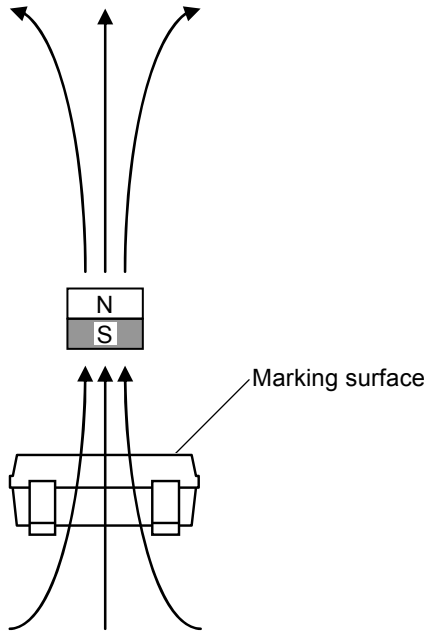


Figure 11

1.2 SNT-4A

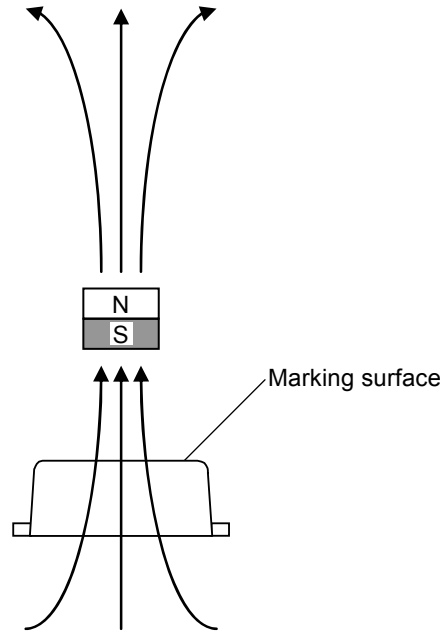


Figure 12

2. Position of Hall sensor

Figure 13 and Figure 14 show the position of Hall sensor.

The center of this Hall sensor is located in the area indicated by a circle, which is in the center of a package as described below.

The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.

2.1 SOT-23-3

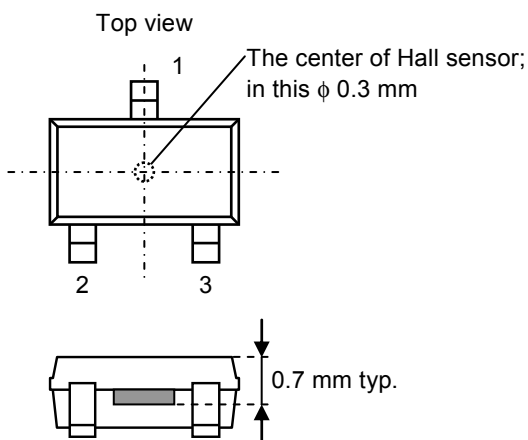


Figure 13

2.2 SNT-4A

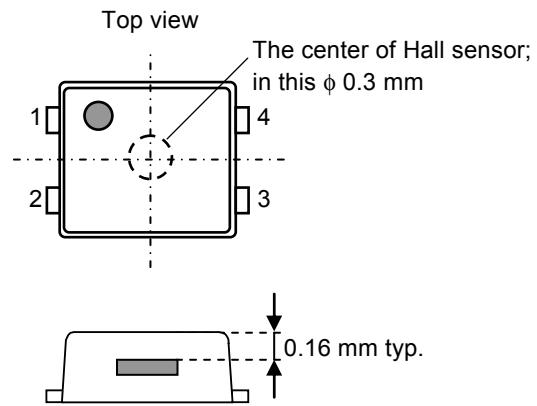


Figure 14

3. Basic operation

This IC changes the output voltage level (V_{OUT}) according to the level of the magnetic flux density (N pole or S pole) applied by a magnet.

The following explains the operation when the output logic is active "L".

3.1 Product with omnipolar detection

When the magnetic flux density vertical to the marking surface exceeds the operation point (B_{OPN} or B_{OPS}) after the S pole or N pole of a magnet is moved closer to the marking surface of this IC, V_{OUT} changes from "H" to "L". When the S pole or N pole of a magnet is moved further away from the marking surface of this IC and the magnetic flux density is lower than the release point (B_{RPN} or B_{RPS}), V_{OUT} changes from "L" to "H".

Figure 15 shows the relationship between the magnetic flux density and V_{OUT} .

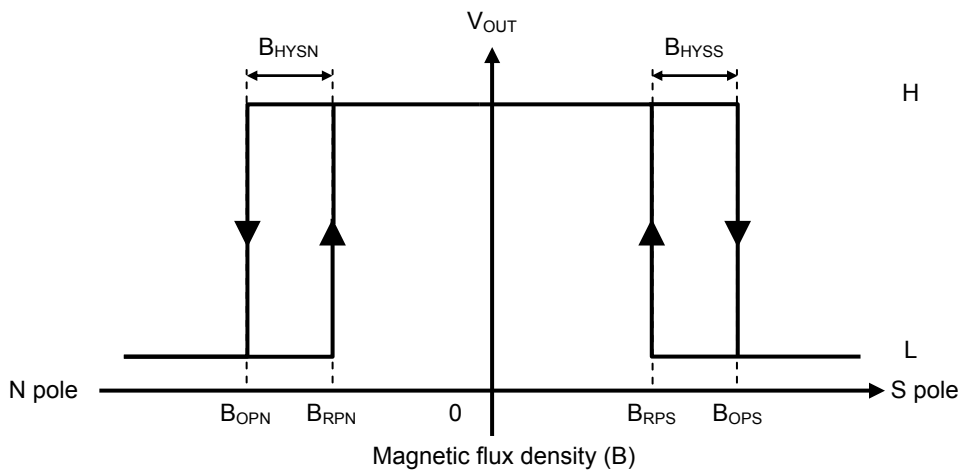


Figure 15

3.2 Product with S pole detection

When the magnetic flux density vertical to the marking surface exceeds B_{OPS} after the S pole of a magnet is moved closer to the marking surface of this IC, V_{OUT} changes from "H" to "L". When the S pole of a magnet is moved further away from the marking surface of this IC and the magnetic flux density is lower than B_{RPS} , V_{OUT} changes from "L" to "H".

Figure 16 shows the relationship between the magnetic flux density and V_{OUT} .

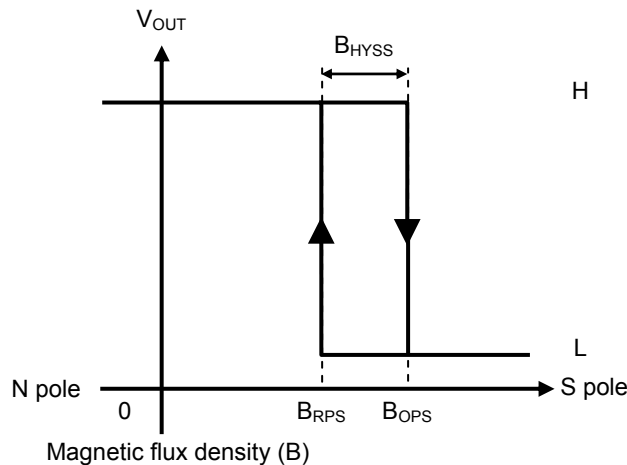


Figure 16

3.3 Product with N pole detection

When the magnetic flux density vertical to the marking surface exceeds B_{OPN} after the N pole of a magnet is moved closer to the marking surface of this IC, V_{OUT} changes from "H" to "L". When the N pole of a magnet is moved further away from the marking surface of this IC and the magnetic flux density is lower than B_{RPN} , V_{OUT} changes from "L" to "H".

Figure 17 shows the relationship between the magnetic flux density and V_{OUT} .

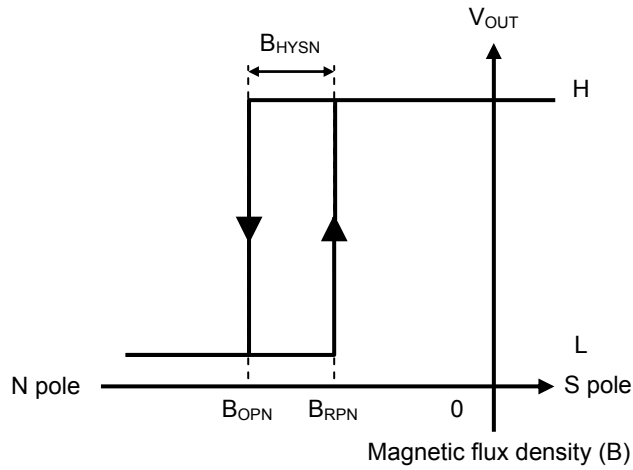


Figure 17

4. Time dependency in the current consumption

This IC performs the intermittent operation, and operates at low current consumption due to repeating the sleep mode (t_{SL}) and the awake mode (t_{AW}).

Figure 18 shows the time dependency in the current consumption.

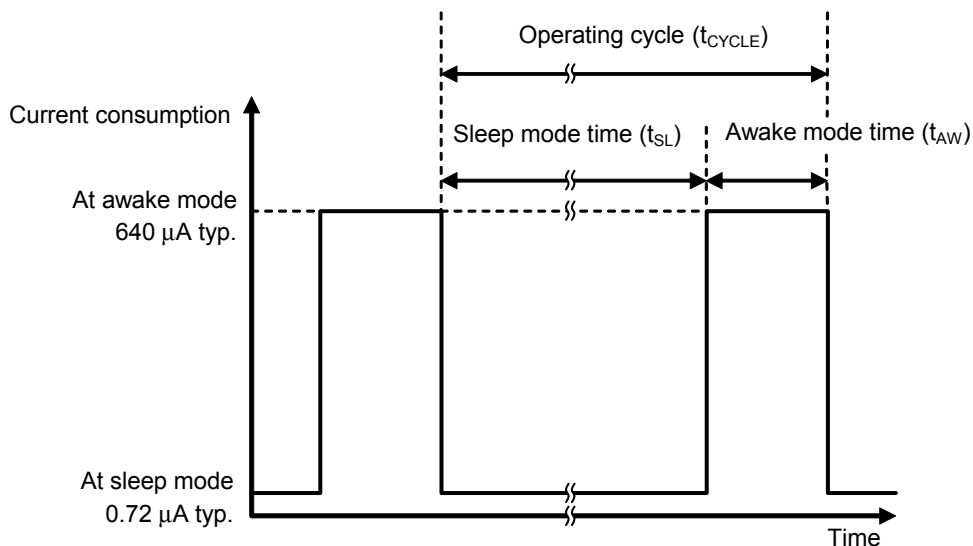


Figure 18

5. Timing chart

Figure 19 shows the operation timing of this IC.

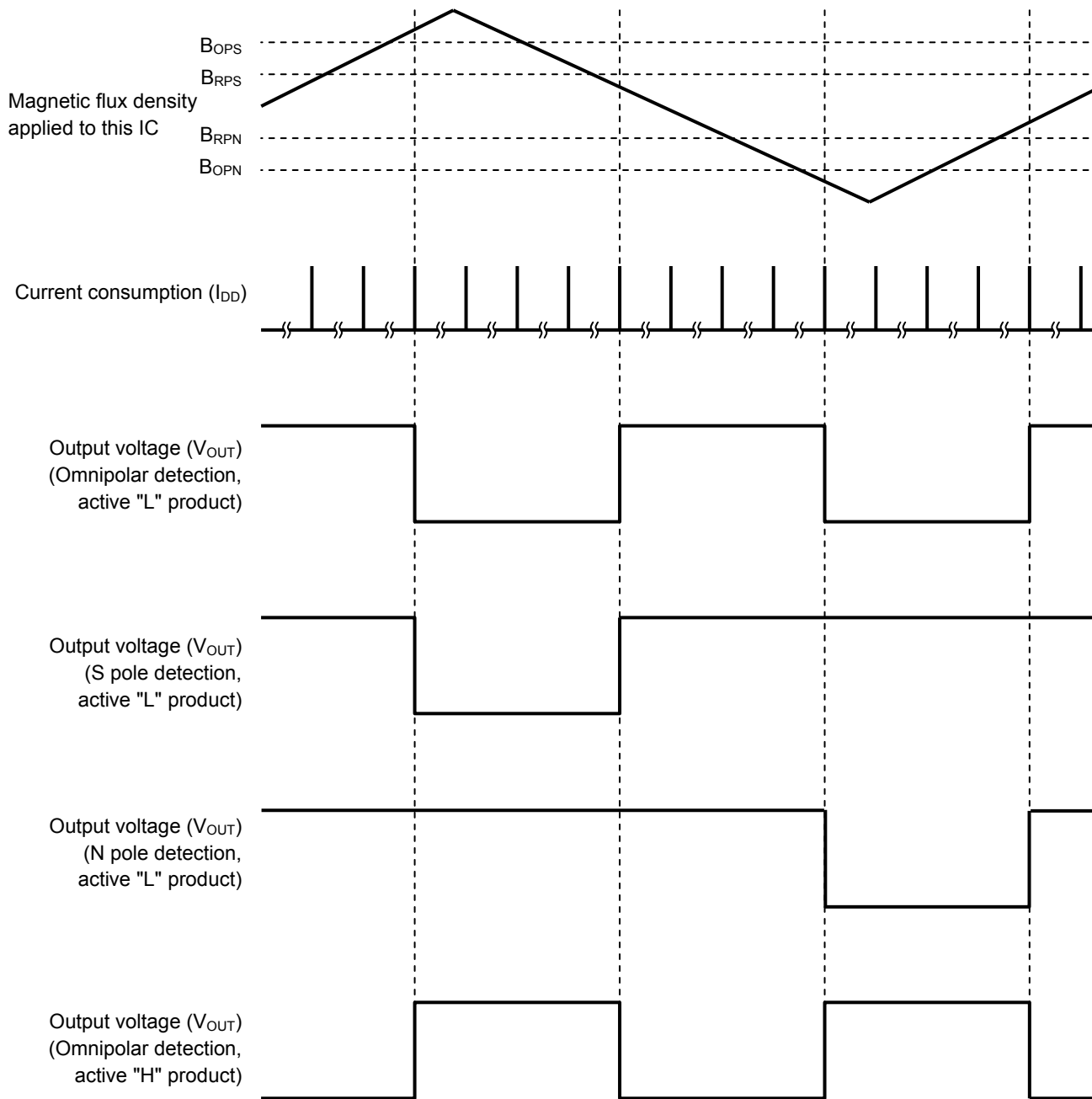


Figure 19

■ **Precautions**

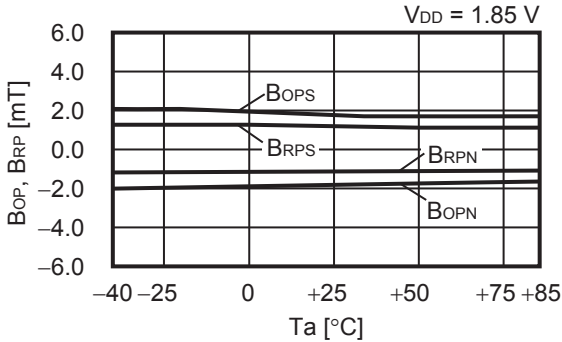
- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.
- Note that the IC may malfunction if the power supply voltage rapidly changes.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Large stress on this IC may affect the magnetic characteristics. Avoid large stress which is caused by the handling during or after mounting the IC on a board.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

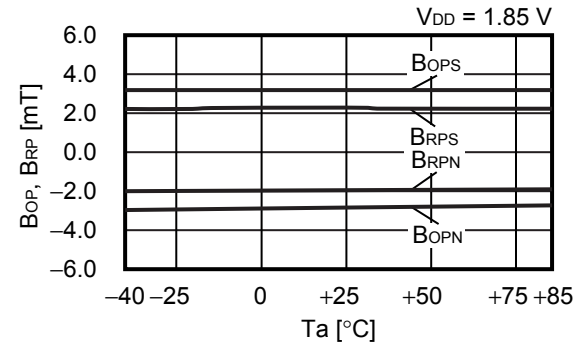
1. S-5712AxDxx

1.1 Operation point, release point (B_{OP} , B_{RP}) vs. Temperature (T_a)

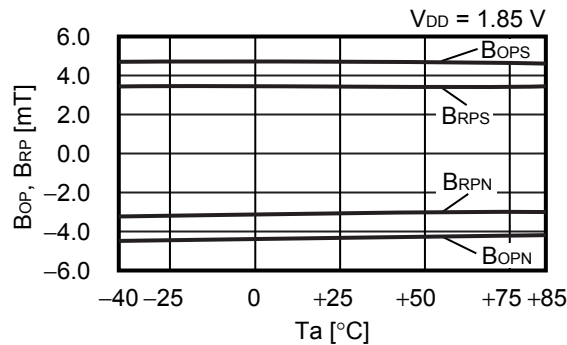
1.1.1 S-5712AxDx0



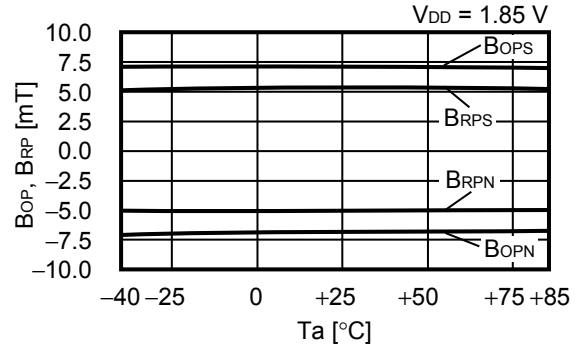
1.1.2 S-5712AxDx1



1.1.3 S-5712AxDx2

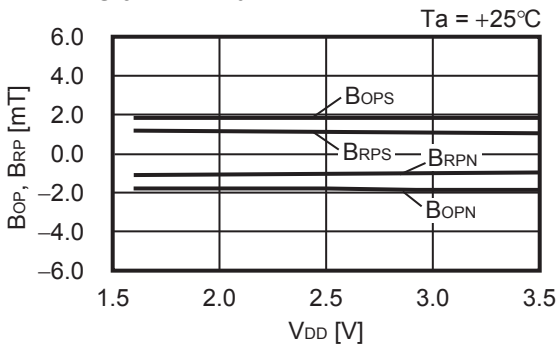


1.1.4 S-5712AxDx3

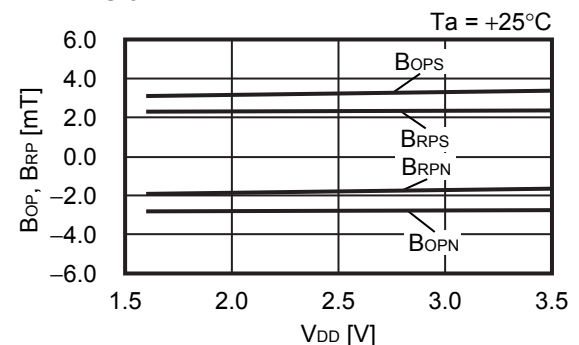


1.2 Operation point, release point (B_{OP} , B_{RP}) vs. Power supply voltage (V_{DD})

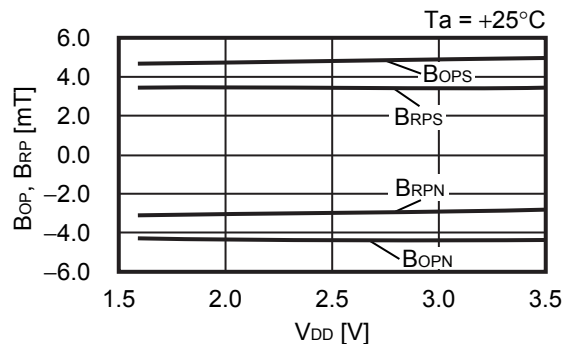
1.2.1 S-5712AxDx0



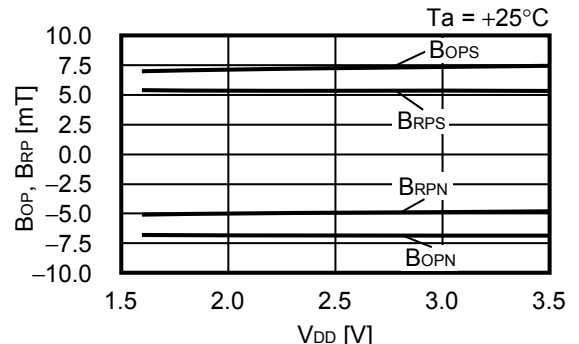
1.2.2 S-5712AxDx1



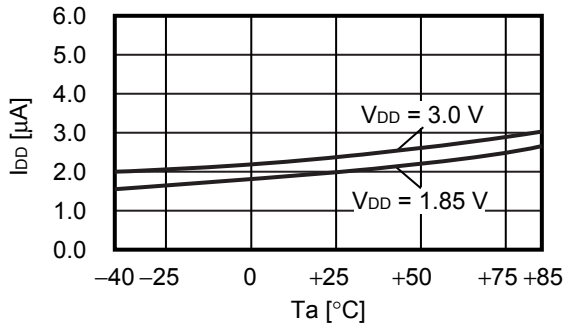
1.2.3 S-5712AxDx2



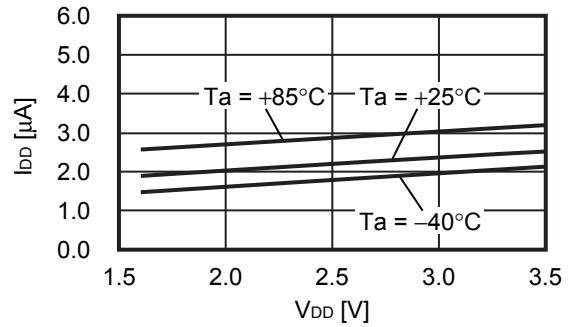
1.2.4 S-5712AxDx3



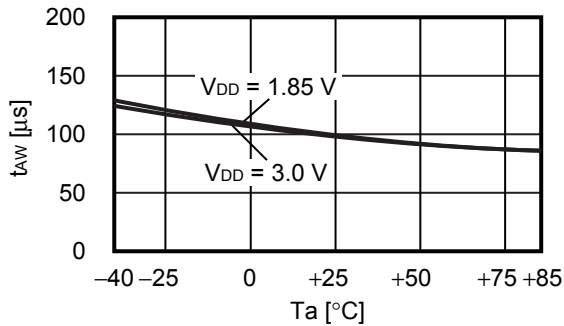
1.3 Current consumption (I_{DD}) vs. Temperature (T_a)



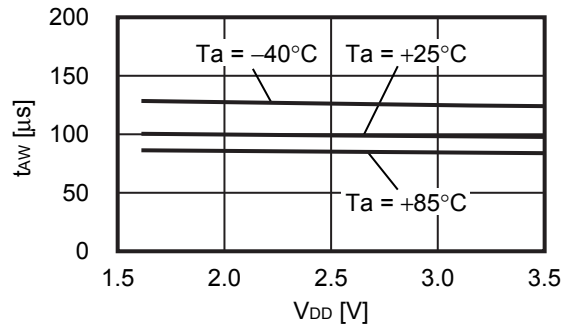
1.4 Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



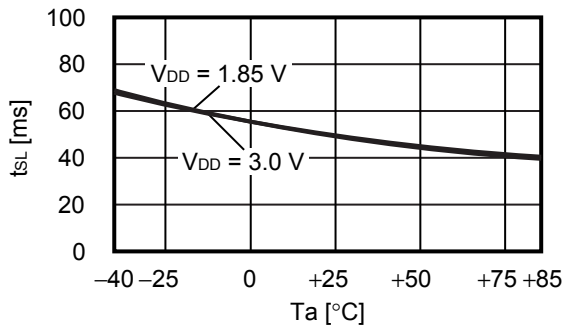
1.5 Awake mode time (t_{AW}) vs. Temperature (T_a)



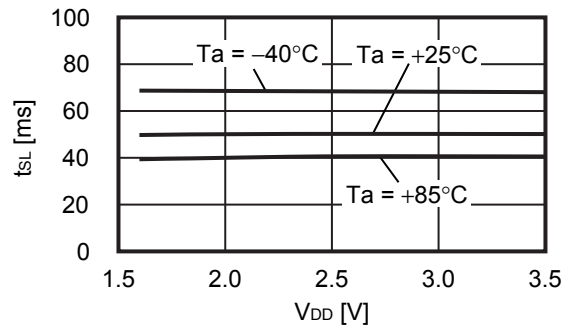
1.6 Awake mode time (t_{AW}) vs. Power supply voltage (V_{DD})



1.7 Sleep mode time (t_{SL}) vs. Temperature (T_a)



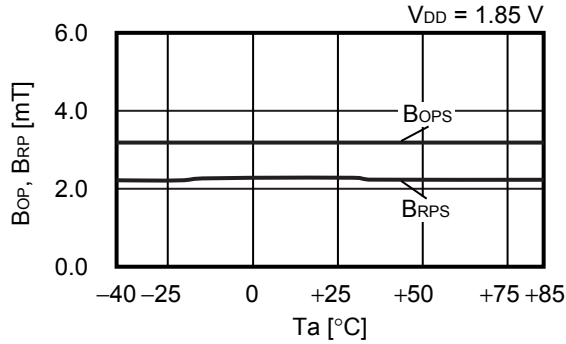
1.8 Sleep mode time (t_{SL}) vs. Power supply voltage (V_{DD})



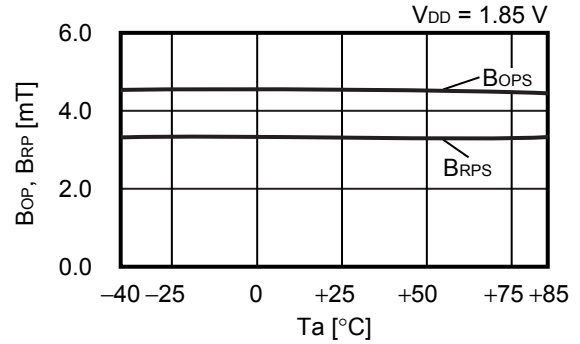
2. S-5712AxSxx, S-5712AxNxx

2.1 Operation point, release point (B_{OP} , B_{RP}) vs. Temperature (T_a)

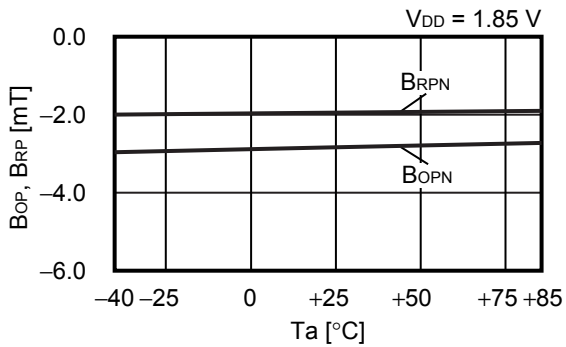
2.1.1 S-5712AxSx1



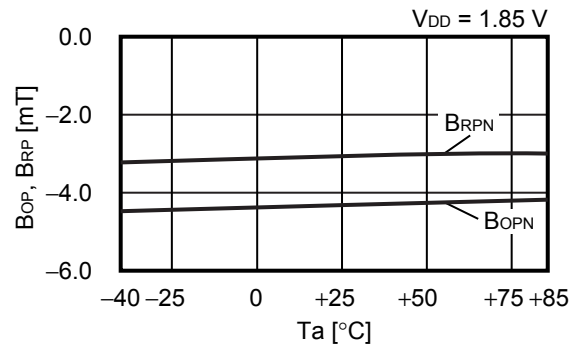
2.1.2 S-5712AxSx2



2.1.3 S-5712AxNx1



2.1.4 S-5712AxNx2



2.1.5 S-5712AxNx3

