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# S-7760A

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## PROGRAMMABLE PORT CONTROLLER (PORT EXPANDER WITH BUILT-IN E$^2$PROM CIRCUIT)



Rev.3.0_00

The S-7760A is a programmable port controller IC comprised of an E$^2$PROM, a control circuit for data output, a circuit to prevent malfunction caused by low power supply voltage and others.
This IC operates at 400 kHz and interfaces with exteriors via I$^2$C-bus, controls an 8ch digital output with a serial signal.
Among the digital output ports of 8 channels, the lower 4 channels have a timer function so that at each port, users are able to set the default value and inverted delay time. In the higher 4 channels, setting the fixed output is available at each port.
The default value is maintained despite power-off because this IC has an E$^2$PROM.
The S-7760A is able to be used to control ON/OFF for the chips surrounding MPU and to output the default data that devices fundamentally have.

## ■ Features

- Operating voltage range: 2.3 to 4.5 V
- 8ch digital output: Higher 4 channels; fixed output/lower 4 channels; timer action
- Operating frequency of I$^2$C-bus interface: 400 kHz
- Low current consumption at standby: 10.0 µA Max. ($V_{CCH}$ = 4.5 V)
- Built-in E$^2$PROM circuit: 6-byte
- E$^2$PROM endurance: $10^5$ cycles / word*1 (at −40 to +85°C)
- E$^2$PROM data retention: 10 years (after rewriting $10^5$ cycles / word)
- Function to protect write in E$^2$PROM
- Function to prevent malfunction during low power supply voltage operation
- Lead-free, halogen-free*2

***1.** For each address (Word: 8 bits)
***2.** Refer to "■ **Product Name Structure**" for details.

## ■ Applications

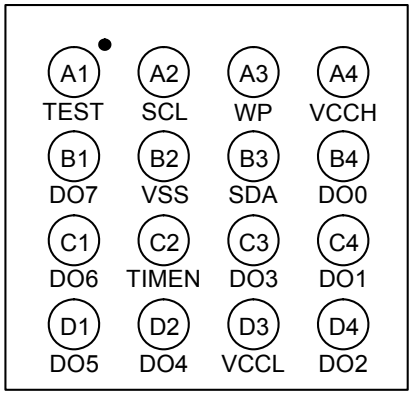
- IoT
- Wearable device
- Mobile phone
- Portable communication device
- Digital still camera
- Digital video camera

## ■ Package

- WLP-16A

## ■ Pin Configuration

**WLP-16A**
**Bottom View**




（1.93 × 2.07 × 0.6 max.）

**Figure 1**

## ■ List of Pin

| Pin No. | Pin name | Description |
|---|---|---|
| A1 | TEST | Test pin |
| A2 | SCL | Input for serial clock |
| A3 | WP | Input for Write protect |
| A4 | VCCH | Power supply |
| B1 | DO7 | Output port 7 |
| B2 | VSS | GND |
| B3 | SDA | Serial data I/O |
| B4 | DO0 | Output port 0 |
| C1 | DO6 | Output port 6 |
| C2 | TIMEN | Input for timer enable |
| C3 | DO3 | Output port 3 |
| C4 | DO1 | Output port 1 |
| D1 | DO5 | Output port 5 |
| D2 | DO4 | Output port 4 |
| D3 | VCCL | Power supply for output port |
| D4 | DO2 | Output port 2 |

## ■ Block Diagram

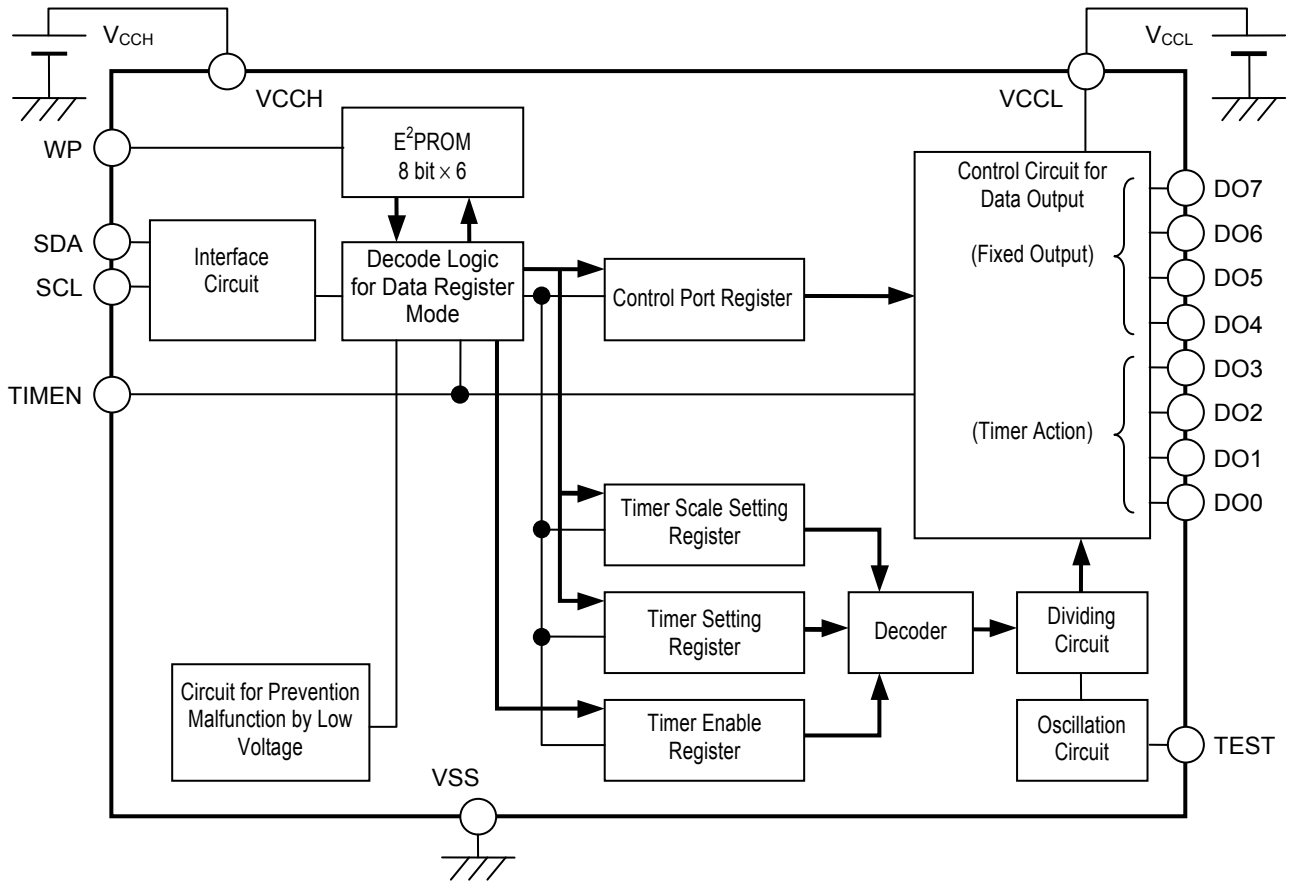



**Figure 2**

## ■ General Description of Pin Function

### 1. SDA (Serial data I/O) pin

The SDA pin transmits serial data bi-directionally, is comprised of a signal input pin and a pin with Nch transistor open drain output. In use, generally, connect the SDA line to any other device which has the open-drain or open-collector output with Wired-OR connection by pulling up to $V_{CCH}$ by a resistor.

### 2. SCL (Input for serial clock) pin

The SCL pin is an input pin for serial clock, processes a signal at a rising/falling edge of SCL clock. Pay attention fully to the rising/falling time and comply with specifications.

### 3. WP (Input for Write protect) pin

This pin performs Write Protect to $E^2$PROM (This pin does not have a function for Write protect to the register).
Set the WP pin in $V_{CCH}$ when using the Write Protect function. If not, set the WP pin to GND.

### 4. TIMEN (Input for timer enable) pin

The TIMEN pin controls enable (“H”)/disable (“L”)/Start (“L”→”H”) in the timer action (inversion of digital output due to elapsed period). Refer to the description of related register in “■ **Command**” and “■ **Condition to Start Timer**” regarding details of timer action.

### 5. DO0, DO1, DO2, DO3 (Digital output) pin

These are lower 4 channels in the digital output ports. Their default values are equal to the ones of a control port register during output. These lower 4 channels are for timer action. Its output inverts after; the timer starts and delay time has elapsed.

### 6. DO4, DO5, DO6, DO7 (Digital output) pin

These are the higher 4 channels in the digital output ports. Their default values are equal to the ones of a control port register during output. These higher 4 channels have fixed output. The elapsed period does not make outputs inverted.

### 7. TEST pin

This is an input pin for testing. Connect it to the VCCH pin or GND.

### 8. VSS pin

Connect to GND.

### 9. VCCH pin

Except for the output ports, the power supply is applied to the entire circuit via this pin. Regarding the voltage’s value to be applied to this pin, refer to “■ **Recommended Operating Conditions**”.

### 10. VCCL pin

This pin is to apply the power supply for the output ports. Regarding the voltage’s value to be applied to this pin, refer to “■ **Recommended Operating Conditions**”.

## ■ Equivalent Circuit of I/O Pin

This IC's I/O pin does not have an element of pull-up or pull-down. The SDA line has an open drain output. The followings are equivalent circuits.

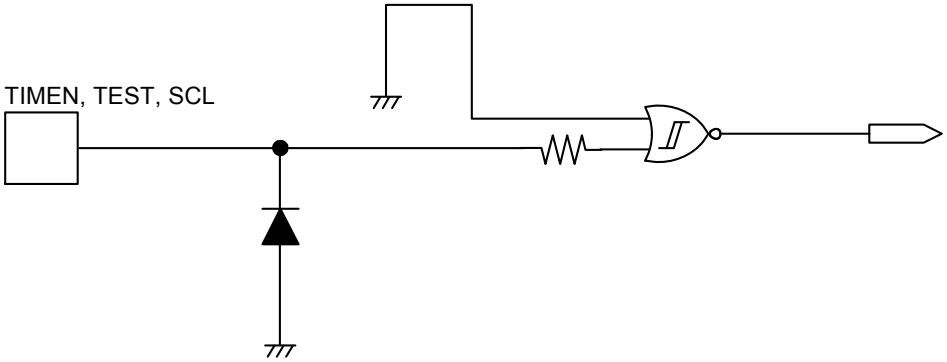



**Figure 3 TIMEN, TEST, SCL Pin**

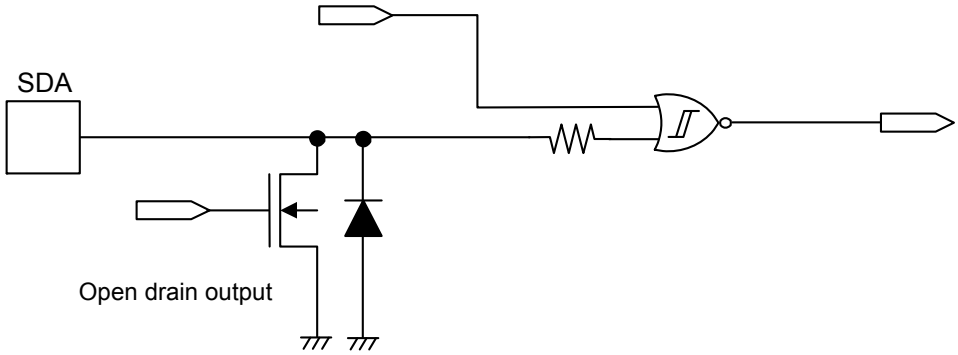



**Figure 4 SDA Pin**

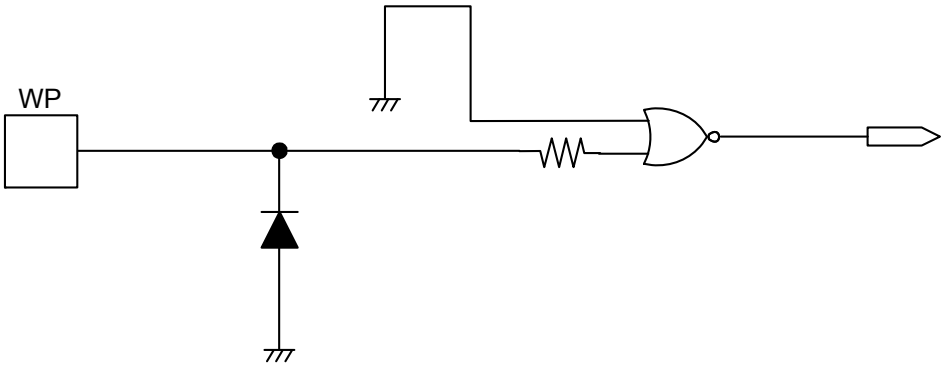



**Figure 5 WP Pin**

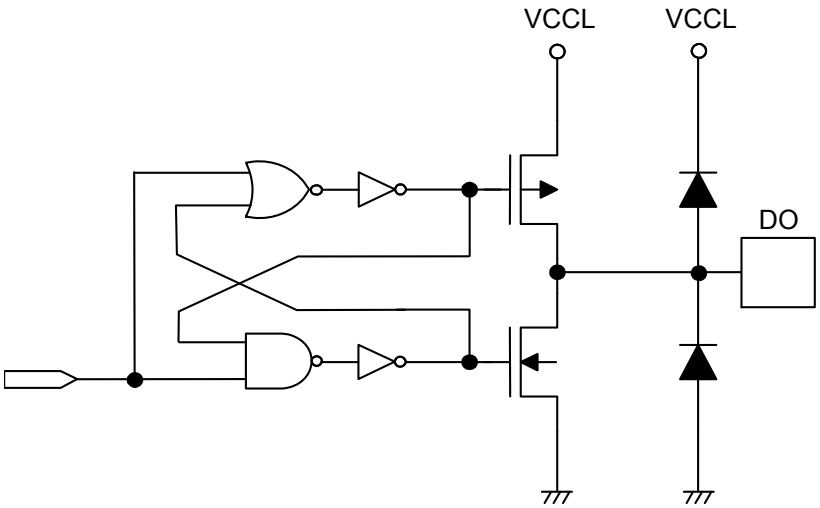



**Figure 6 DO Pin**

## ■ High-level input voltage 2 ($V_{IH2}$), low-level input voltage 2 ($V_{IL2}$)

The SDA, SCL and TIMEN pins are low voltage input types.
In low voltage input type, even when the power supply voltage at MPU is lower than the one of the S-7760A, setting a level-shifter for an interface signal is unnecessary.
Independent of the power supply voltage, $V_{IH2}$ and $V_{IL2}$ are constant. Each of them is $V_{IH2} \geq 1.5$ V, $V_{IL2} \leq 0.3$ V.

## ■ Absolute Maximum Ratings

**Table 2**

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Power supply voltage 1 | $V_{CCH}$ | −0.3 to +7.0 | V |
| Power supply voltage 2 | $V_{CCL}$ | −0.3 to $V_{CCH}$ | V |
| Input voltage | $V_{IN}$ | −0.3 to $V_{CCH}$+0.3 | V |
| Output voltage (SDA) | $V_{OUT1}$ | −0.3 to $V_{CCH}$ | V |
| Output voltage (DO) | $V_{OUT2}$ | −0.3 to $V_{CCL}$ | V |
| Operating ambient temperature | $T_{opr}$ | −40 to +85 | °C |
| Storage temperature | $T_{stg}$ | −65 to +150 | °C |

**Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

## ■ Recommended Operating Conditions

**Table 3**

| Item | Symbol | Applicable Pin | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Power supply voltage | $V_{CCH}$ | VCCH | 2.3*1 | 4.5 | V |
| Output power supply voltage | $V_{CCL}$ | VCCL | 1.5 | $V_{CCH}$*2 | V |
| High-level input voltage 1 | $V_{IH1}$ | WP, TEST | 0.7 × $V_{CCH}$ | $V_{CCH}$ | V |
| Low-level input voltage 1 | $V_{IL1}$ | | 0.0 | 0.3 × $V_{CCH}$ | V |
| High-level input voltage 2 | $V_{IH2}$ | SDA, SCL, TIMEN | 1.5 | $V_{CCH}$ | V |
| Low-level input voltage 2 | $V_{IL2}$ | | 0.0 | 0.3 | V |

***1.** Set $V_{CCH} \geq 2.5$ V when rising VCCH and TIMEN simultaneously.
***2.** Set the voltage of VCCL as $V_{CCH} \geq V_{CCL}$.

## ■ Pin Capacitance

**Table 4**

(Ta = 25°C, f = 1.0 MHz, $V_{CCH}$ = 3 V)

| Item | Symbol | Pin | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | SCL, WP, TIMEN, TEST | $V_{IN}$ = 0 V | − | 10 | pF |
| Input/output capacitance | $C_{I/O}$ | SDA | $V_{I/O}$ = 0 V | − | 10 | pF |

## ■ Endurance

**Table 5**

| Item | Symbol | Operation Ambient Temperature | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Endurance | $N_W$ | −40 to +85°C | $10^5$ | − | cycles / word*1 |

***1.** For each address (Word: 8 bits)

## ■ Data Retention

**Table 6**

| Item | Symbol | Operation Ambient Temperature | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Data retention*1 | − | −40 to +85°C | 10 | − | year |

***1.** After rewriting $10^5$ cycles / word

## ■ DC Electrical Characteristics

**Table 7 DC Characteristcs 1**

| Item | Symbol | Condition*1 | $V_{CCH}$ = $V_{CCL}$ = 2.3 to 4.5 V | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| Current consumption during standby | $I_{SB}$ | $f_{SCL}$ = 0 Hz | − | 10.0 | μA |
| Current consumption (READ) | $I_{CC1}$ | $f_{SCL}$ = 400 kHz | − | 0.8 | mA |
| Current consumption (WRITE) | $I_{CC2}$ | $f_{SCL}$ = 400 kHz | − | 4.0 | mA |
| Current consumption during operation of internal oscillation circuit | $I_{CC3}$ | $f_{SCL}$ = 0 Hz | − | 0.8 | mA |

***1.** The total current consumption when $V_{CCH}$ = $V_{CCL}$. No load on pins DO7 to 0.

**Table 8 DC Characteristcs 2**

| Item | Symbol | Pin | Condition | $V_{CCH}$ = 2.3 to 4.5 V | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Input leakage current | $I_{IZH}$ | TEST, TIMEN, WP, SDA, SCL | $V_{IN}$ = $V_{CCH}$ | −1.0 | 1.0 | μA |
| | $I_{IZL}$ | | $V_{IN}$ = GND | −1.0 | 1.0 | μA |
| Output leakage current | $I_{OZH}$ | SDA | $V_{IN}$ = $V_{CCH}$ | −1.0 | 1.0 | μA |
| | $I_{OZL}$ | | $V_{IN}$ = GND | −1.0 | 1.0 | μA |
| Low-level output voltage | $V_{OL1}$ | SDA | $I_{OL}$ = 3.2 mA | − | 0.4 | V |
| | | | $I_{OL}$ = 1.5 mA | − | 0.3 | V |
| | $V_{OL2}$ | DO | $I_{OL}$ = 100 μA<br>$V_{CCL}$ = $V_{CCH}$ to 1.5 V | − | 0.1 | V |
| High-level output voltage | $V_{OH2}$ | DO | $I_{OH}$ = −100 μA<br>$V_{CCL}$ = $V_{CCH}$ to 1.5 V | $V_{CCL}$−0.2 | − | V |

## ■ AC Electrical Characteristics

**Table 9 Measurement Conditions**

| | |
|---|---|
| Input pulse voltage | $V_{IL} = 0.1 \times V_{CCH}$, $V_{IH} = 0.9 \times V_{CCH}$ |
| Rising/falling time of input pulse | 20 ns |
| Output reference voltage | $0.5 \times V_{CCH}$ |
| Output load | 100 pF+ Pull-up resistor 1.0 kΩ |

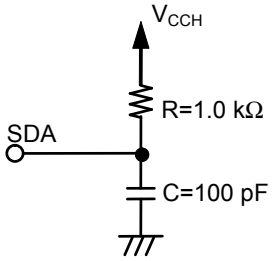



**Figure 7 Output Load Circuit**

**Table 10 AC Electrical Characteristics**

| Item | Symbol | $V_{CCH}$ = 2.3 to 4.5 V | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| SCL clock frequency*1 | $f_{SCL}$ | 0 | 400 | kHz |
| SCL clock time "L"*1 | $t_{LOW}$ | 1.3 | – | µs |
| SCL clock time "H"*1 | $t_{HIGH}$ | 0.6 | – | µs |
| SDA output delay time*1 | $t_{AA}$ | – | 0.9 | µs |
| SDA output hold time*1 | $t_{DH}$ | 50 | – | ns |
| Start condition setup time*1 | $t_{SU.STA}$ | 0.6 | – | µs |
| Start condition hold time*1 | $t_{HD.STA}$ | 0.6 | – | µs |
| Data input setup time*1 | $t_{SU.DAT}$ | 100 | – | ns |
| Data input hold time*1 | $t_{HD.DAT}$ | 0 | – | ns |
| Stop condition setup time*1 | $t_{SU.STO}$ | 0.6 | – | µs |
| SCL, SDA rise time*1 | $t_R$ | – | 0.3 | µs |
| SCL, SDA fall time*1 | $t_F$ | – | 0.3 | µs |
| Bus release time*1 | $t_{BUF}$ | 1.3 | – | µs |
| Noise suppression time*1 | $t_I$ | – | 50 | ns |

***1.** The timing is defined by 10% and 90% of the waveform.

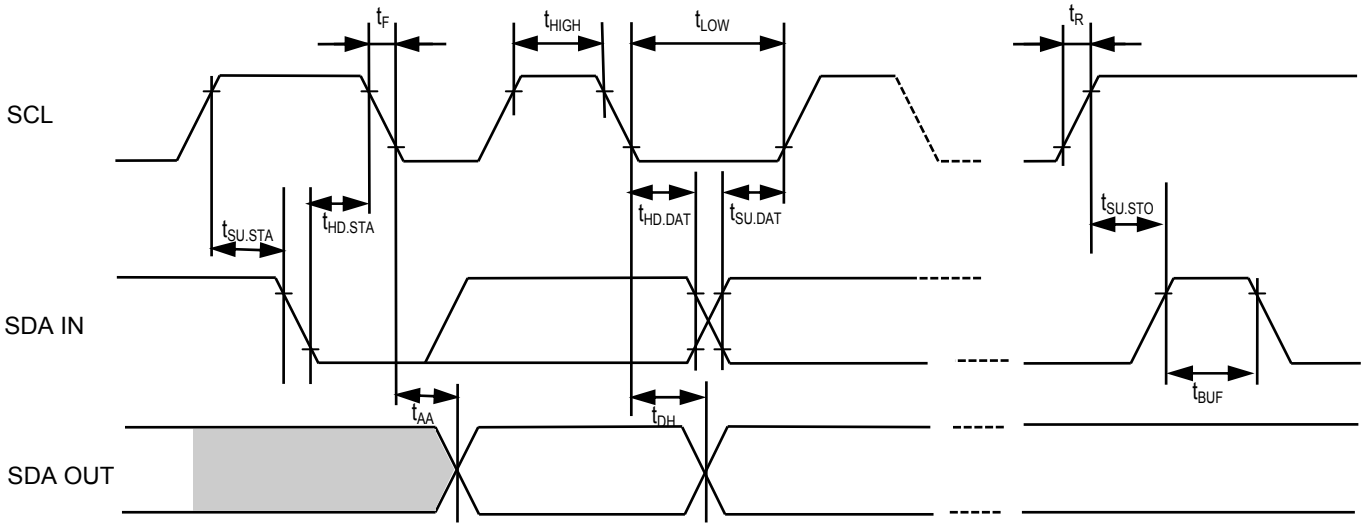



**Figure 8 Bus Timing**

**Table 11 Characteristics of Period**

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Write period to E²PROM | $t_{WR}$ | – | 2.0 | 5.0 | ms |
| Delay time accuracy (short-time setting)*1 | $t_{DLY1}$ | 0.8 × T | T | 1.2 × T | µs |
| Delay time accuracy (long-time setting)*1 | $t_{DLY2}$ | 0.8 × LT | LT | 1.2 × LT | µs |

***1.** Refer to **Figure 13 Timer Scale Setting Register**.
T represents time reference (timer scale) in the short-time setting.
LT represents time reference (timer scale) in the long-time setting.

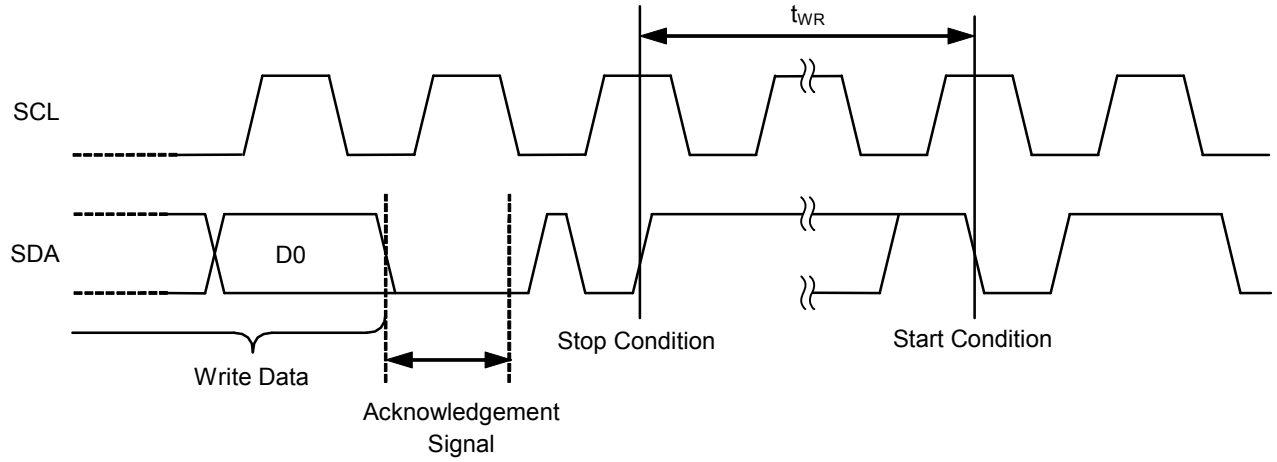



**Figure 9 Write Cycle Timing**

## ■ Device Addressing

To start communication, the master device (MPU) on the system generates a start condition for the slave device (S-7760A). After that, the master device sends a device address with 7-bit length and Read/Write instruction code with 1-bit length on the SDA bus. The higher 3 bits in a device address (DC2, DC1, DC0) are device codes, which are fixed to "100". Command is omitted if a device code does not correspond. Set the command in the following 4 bits (C3, C2, C1, C0). Next, by selecting either of Read or Write by Read/Write bit, the S-7760A sends an acknowledgement signal back. If the second byte is Read, MPU sends an acknowledgement signal back after outputting data Read with 8-bit length. If it is Write, after outputting Write data with 8-bit length, the S-7760A sends an acknowledgement signal back. To finish these sequential commands, the S-7760A generates a stop condition as its final procedure.
There is a 1-byte command for the S-7760A, but inputting the second byte as a dummy does not affect on this device addressing. In this case, the operation for the second byte is as well as for Read/Write because of the bit corresponding to Read/Write in the first byte.

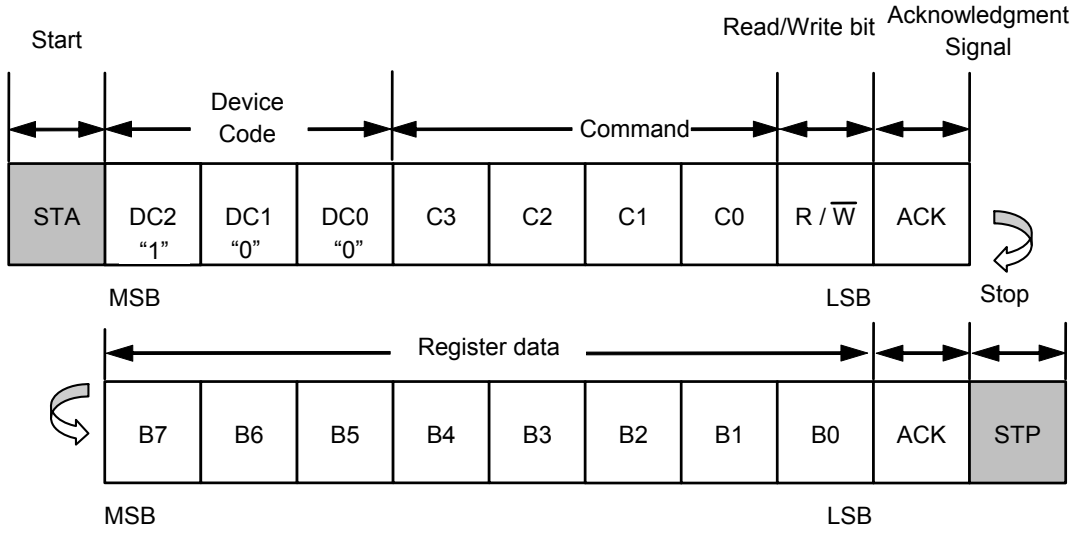



**Figure 10 Device Address**

## ■ Configuration of Command

**Table 12 List of Command**

| Command | C3 | C2 | C1 | C0 | R / $\overline{W}$ | Data | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Reload | 0 | 0 | 0 | 0 | R / $\overline{W}$ *1 | — | | | | | | | |
| Switching access to register/E²PROM | 0 | 0 | 0 | 1 | —*2 | — | | | | | | | |
| Timer enable register | 0 | 0 | 1 | 0 | $\overline{W}$ | — | — | — | — | TEN3 | TEN2 | TEN1 | TEN0 |
| Do not use (Do not access) | 0 | 0 | 1 | 1 | — | — | | | | | | | |
| Do not use (Do not access) | 0 | 1 | 0 | 0 | — | — | | | | | | | |
| Control port | 0 | 1 | 0 | 1 | R / $\overline{W}$ *3 | CTR7 | CTR6 | CTR5 | CTR4 | CTR3 | CTR2 | CTR1 | CTR0 |
| Setting for timer scale | 0 | 1 | 1 | 0 | R / $\overline{W}$ *3 | TS7 | TS6 | TS5 | TS4 | TS3 | TS2 | TS1 | TS0 |
| Do not use (Do not access) | 0 | 1 | 1 | 1 | — | — | | | | | | | |
| Timer setting for DO0 | 1 | 0 | 0 | 0 | R / $\overline{W}$ *3 | 8×T | 7×T | 6×T | 5×T | 4×T | 3×T | 2×T | 1×T |
| Timer setting for DO1 | 1 | 0 | 0 | 1 | R / $\overline{W}$ *3 | 8×T | 7×T | 6×T | 5×T | 4×T | 3×T | 2×T | 1×T |
| Timer setting for DO2 | 1 | 0 | 1 | 0 | R / $\overline{W}$ *3 | 8×T | 7×T | 6×T | 5×T | 4×T | 3×T | 2×T | 1×T |
| Timer setting for DO3 | 1 | 0 | 1 | 1 | R / $\overline{W}$ *3 | 8×T | 7×T | 6×T | 5×T | 4×T | 3×T | 2×T | 1×T |
| Do not use (Do not access) | 1 | 1 | 0 | 0 | — | — | | | | | | | |
| Do not use (Do not access) | 1 | 1 | 0 | 1 | — | — | | | | | | | |
| Do not use (Do not access) | 1 | 1 | 1 | 0 | — | — | | | | | | | |
| Do not use (Do not access) | 1 | 1 | 1 | 1 | — | — | | | | | | | |

***1.** R / $\overline{W}$ = 1/0 Both execute “reload”.

***2.** It is register access mode when R / $\overline{W}$ = 0, E²PROM access mode when R / $\overline{W}$ = 1.

***3.** By Switching access to register/E²PROM, users can select either register or E²PROM when Read/Write. Refer to “■ **Register and E²PROM**”.

## ■ Register and E²PROM

This IC has an E²PROM. Data in the E²PROM is maintained despite power-off. The S-7760A has a register which corresponds to the data in the E²PROM, the S-7760A sends data to this corresponding register during power-on (releasing detection of the low voltage) and inputting the reload command. The following registers are the ones to be reloaded;

- Control port register (1-byte)
- Timer scale setting register (1-byte)
- DO3 to 0 Timer setting register (1-byte in each port, total 4 bytes)

Users are able to switch access between corresponding register and E²PROM by “Switching access to register/E²PROM” command. Immediately after power-on, the S-7760A is in “register access mode”. In this register access mode, only the register is rewritten, the E²PROM maintains the prior data. But in “E²PROM access mode”, both data in the register and the E²PROM is rewritten. In data Read, access mode data which is being selected by user; is read.

## ■ Command

### 1. Reload

This is a 1-byte command. Users can reload by inputting either of $R/\overline{W}$ in 0/1. When inputting this command, the data corresponding to the $E^2$PROM is loaded to the register. After completing reload, (if the condition is satisfied), the timer action starts. The reload command is not accepted during the timer action (from its start to the final invert of output). Refer to "■ **Condition to Start Timer**" regarding details.

### 2. Switching access to register/$E^2$PROM

This is a 1-byte command. The mode is in "register access mode" when this command is $R/\overline{W}$ = 0, "$E^2$PROM access mode" when this command is $R/\overline{W}$ = 1. The register corresponding to the $E^2$PROM is the one to be reloaded. In register access mode, only the register is rewritten, the $E^2$PROM maintains the prior data. In "$E^2$PROM access mode", both data in the register and $E^2$PROM is rewritten.

### 3. Timer enable register

A timer enable register is a 4-bit register for Write only (it sends back FFh during Read). By setting each bit in the register in "1", an oscillation circuit starts, output from the lower 4ch ports (DO3 to 0) invert after the elapsed period which is set by a timer setting register. This action is called "timer action". This timer action starts at the point when receiving TEN0 which is LSB in the register. The bit automatically goes back in "0" after writing "1" in the timer enable register. Users cannot write in this register during the timer action (from the start to the final invert of output). This register is not the one to be reloaded, thus it does not have the data which corresponds to the $E^2$PROM. To start a timer, Condition AND with TIMEN = High is required. Refer to"■ **Condition to Start Timer**" regarding details.

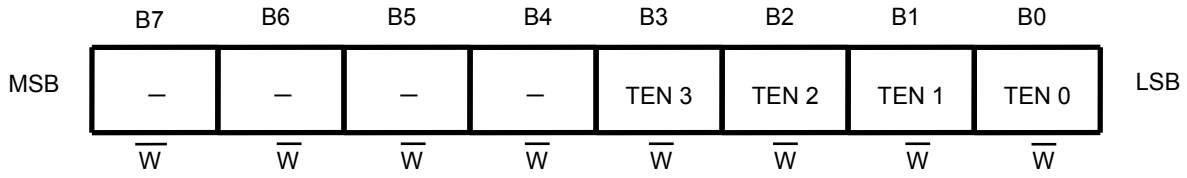



**Figure 11 Timer Enable Register**

0 : Disable to invert output
1 : Enable to invert output

### 4. Control port register

Control port register is an 8-bit register. Users can set output data which is from output ports (DO7 to 0). If data is “1”, output is “H”, and if it is “0”, output is “L”. This register is the one to be reloaded. Data in this register does not change even if output from the port is inverted by timer action.

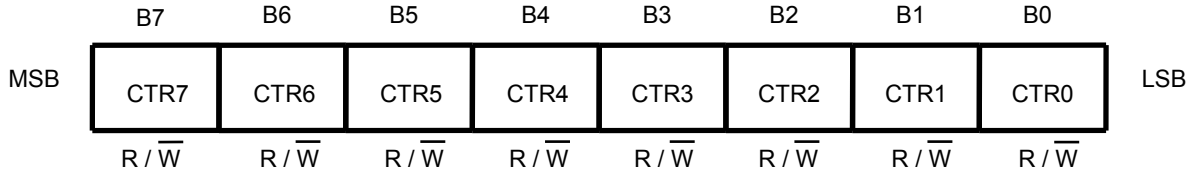
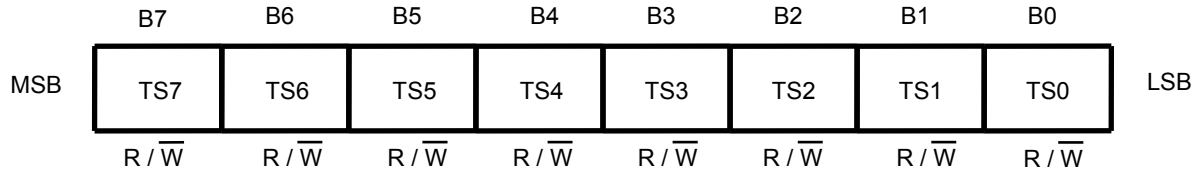



**Figure 12 Control Port Register**

### 5. Timer scale setting register

The lower 4 bits are registers for timer scale setting. Users can set, whether short-time or long-time, time reference (scale) for the delay time setting at each port DO3 to 0.
The higher 4 bits are Read/Write-able bits, however, they do not affect on circuit action because DO7 to 4 have fixed output. This register is the one to be reloaded.




TSn = 1 : Timer scale DO3 to 0 Short-time setting
TSn = 0 : Timer scale DO3 to 0 Long-time setting

**Figure 13 Timer Scale Setting Register**

### 6. DO0 to 3 Timer setting registers

These registers are 8-bit registers which correspond to each port, with these registers, users can set delay time for the change of output at output ports (DO0 to 3). When delay time is set, its value is a multiple of timer scale. The multiple is integers 1 to 8. By setting the corresponding bits seen in **Figure 14** in "1", a multiple is selected to determine delay time. For each port, set only 1-bit in the bit that you set "1". And if setting all 8 bits in "0", output is not inverted even if the condition to start a timer matches.

| MSB | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | LSB |
|---|---|---|---|---|---|---|---|---|---|
| DO0 | 8 × T | 7 × T | 6 × T | 5 × T | 4 × T | 3 × T | 2 × T | 1 × T | |
| DO1 | 8 × T | 7 × T | 6 × T | 5 × T | 4 × T | 3 × T | 2 × T | 1 × T | |
| DO2 | 8 × T | 7 × T | 6 × T | 5 × T | 4 × T | 3 × T | 2 × T | 1 × T | |
| DO3 | 8 × T | 7 × T | 6 × T | 5 × T | 4 × T | 3 × T | 2 × T | 1 × T | |
| | R / $\overline{W}$ | R / $\overline{W}$ | R / $\overline{W}$ | R / $\overline{W}$ | R / $\overline{W}$ | R / $\overline{W}$ | R / $\overline{W}$ | R / $\overline{W}$ | |

**Figure 14 Timer Setting Register DO0 to 3**

**Figure 14** shows a short-time setting scale. In case of a long-time setting scale, substitute T with LT.
Each timer scale is as follow;

Short-time setting scale Typ. = T = 10 μs
Long-time setting scale Typ. = LT = 640 μs

If setting "1" in B6 bit in the DO3 timer setting register, "1" in TS3 in the timer scale register, DO3 inverts at delay time of 70 μs (7 × 10 μs). Other examples are shown in **Figure 15**.

| MSB | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | LSB |
|---|---|---|---|---|---|---|---|---|---|
| Example 1 | 80 μs | 70 μs | 60 μs | 50 μs | 40 μs | 30 μs | 20 μs | 10 μs | |
| Example 2 | 5.12 ms | 4.48 ms | 3.84 ms | 3.2 ms | 2.56 ms | 1.92 ms | 1.28 ms | 0.64 ms | |

Example 1 In case of; Timer scale register "1" (short-time setting); (T = 10 μs)
Example 2 In case of; Timer scale register "0" (long-time setting); (LT = 640 μs)

**Figure 15 Example of Using Timer Setting Register 0 to 3**

## ■ Condition to Start Timer

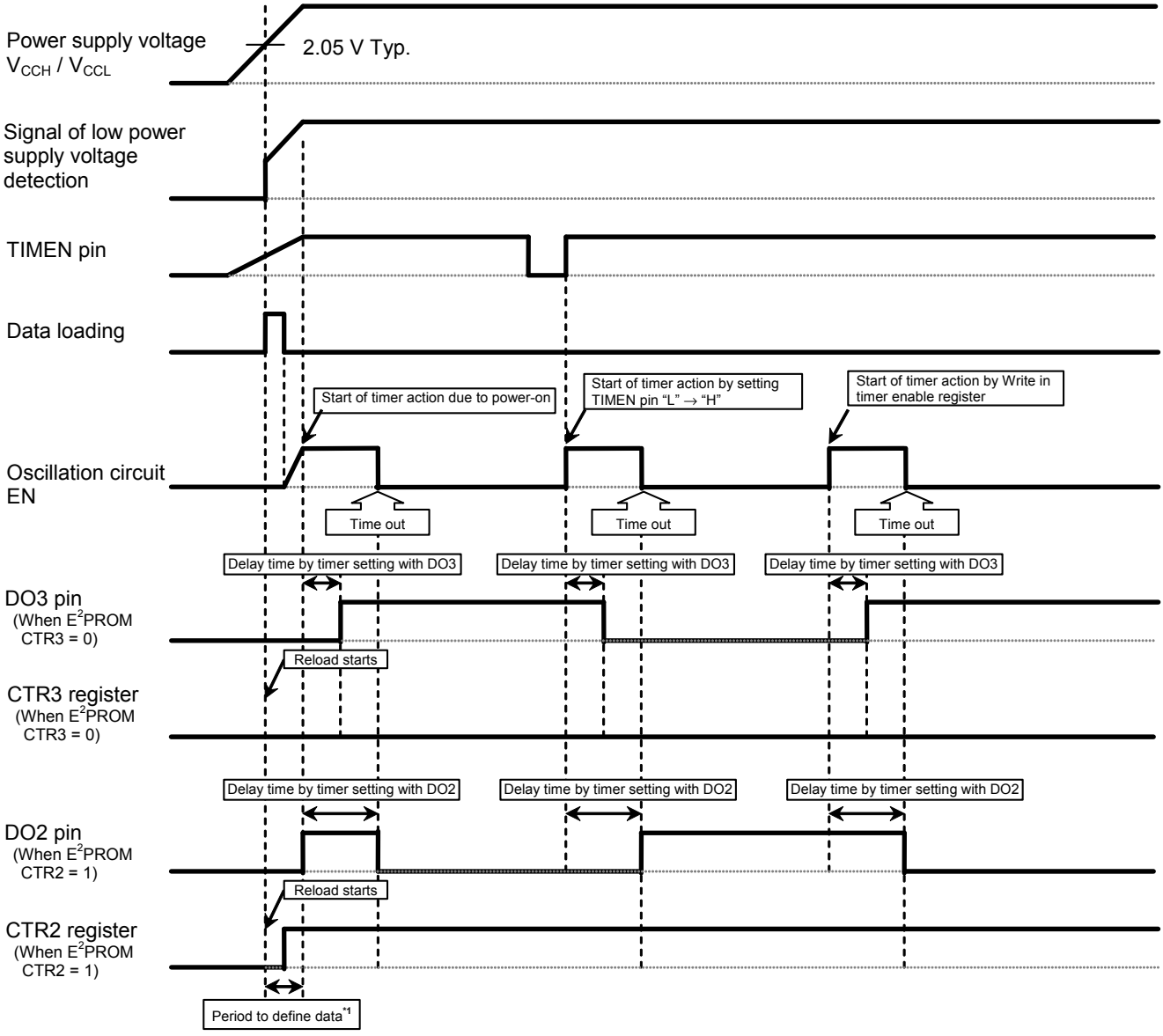
**Table 13 Condition to Start Timer**

| Condition | Reload | TIMEN Pin | Bit TEN3 to 0 |
|---|---|---|---|
| A | Start → Finish | "H" | Don't care |
| B | Regular status | "L" → "H" | Don't care |
| C | Regular status | "H" | Write "0" → "1" |

The condition to start a timer is three, A/B/C.
During power-on of power supply VCCH, the S-7760A automatically reloads (transmits data from the E$^2$PROM to the register). In this case, if TIMEN = "H", the S-7760A goes in the timer action after reloading. Thus the sequential action is; after power-on of power supply VCCH, reload → timer. This is as well if the status changed from detection to release of the low power supply voltage.
The timer action does not stop in the middle of its process even if setting TIMEN in "H" → "L" after the timer action has started. The oscillation circuit is generally being stopped, but the oscillation starts when the condition to start a timer matches. And it stops by finishing the timer action (the final invert of output).

## ■ Timing of Data Loading from E²PROM and Timer Action

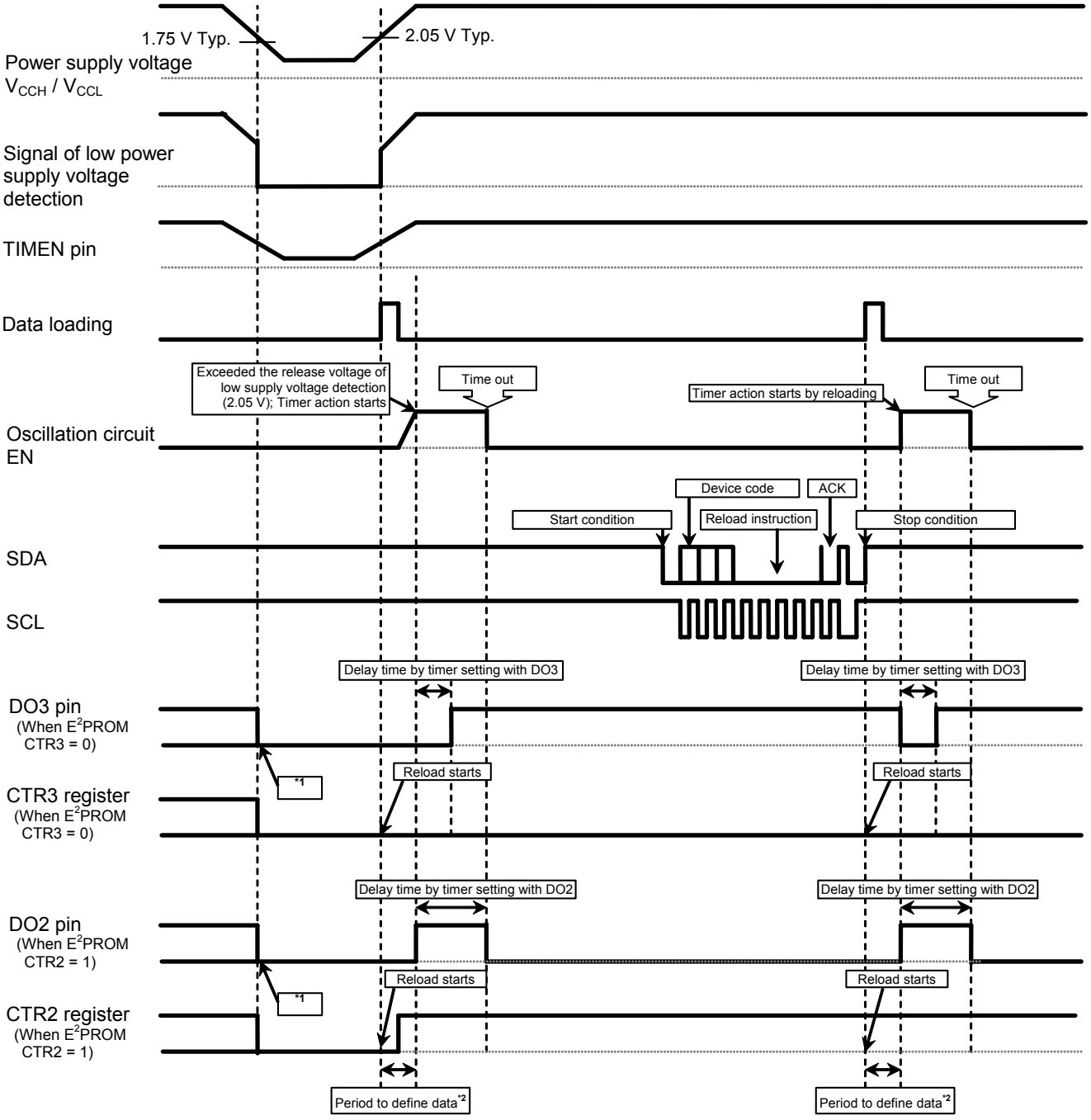
The example of timing chart of data loading from the E²PROM and timer action is shown in **Figure 16** and **17**.
Set $V_{CCH} \geq 2.5$ V when rising VCCH and TIMEN simultaneously.




***1.** A period to define data is; the loading period from E²PROM + the period to stabilize output from DO7 to 0 pin = within 100 µs.

**Figure 16 Data Loading and Timer Action Example 1**

This IC goes in the status to reset the circuits when the power supply voltage decreases less than the level of the detection voltage of the circuit for prevention malfunction by low voltage (1.75 V Typ.). And the DO7 to 0 pins go in "L". After that, when the power supply voltage increases more than the level of the release voltage of the circuit for prevention malfunction by low voltage (2.05 V Typ.), data is reloaded from the E²PROM to the register, the values of DO7 to 0 pins go back to its default.




***1.** Output from DO7 to 0 goes in "L" when the power supply voltage decreases more than the level of the detection voltage of the circuit for prevention malfunction by low voltage.

***2.** A period to define data is; the loading period from E²PROM + the period to stabilize output from DO7 to 0 pin = within 100 μs.

**Figure 17 Data Loading and Timer Action Example 2**

## ■ Flowchart of Data Loading from E²PROM and Timer Action

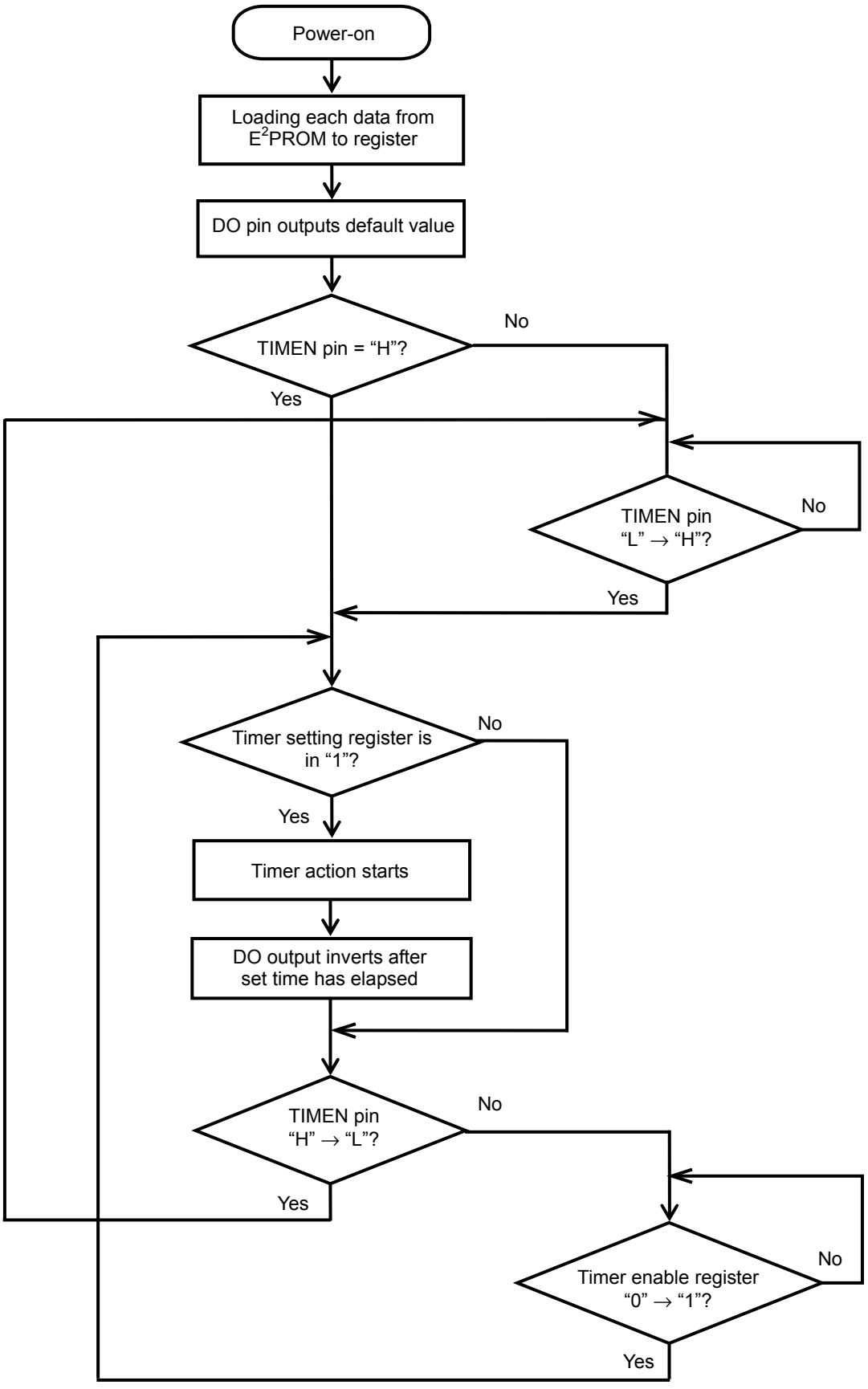



**Figure 18 Flowchart of S-7760A's Action**

## ■ Operation

### 1. Start condition

A start condition starts by changing the SDA line from “H” to “L” while the SCL line is “H”. Input a start condition first when inputting a command via I$^2$C-bus interface.

### 2. Stop condition

A stop condition starts by changing the SDA line from “L” to “H” while the SCL line is “H”. Input a stop condition in the end when inputting a command via I$^2$C-bus interface.

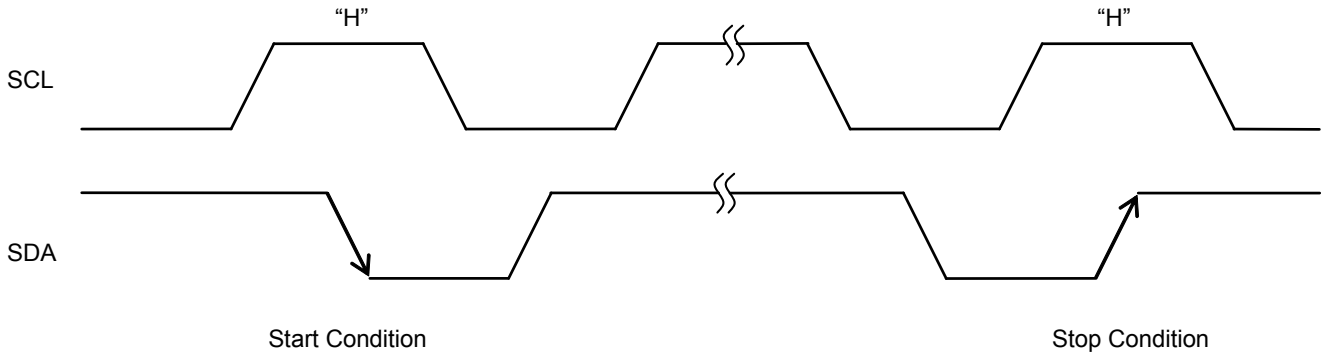



**Figure 19 Start / Stop Condition**

### 3. Data transfer

The S-7760 installs data in the SDA line at a rising edge of the SCL line.
Change the SDA line while the SCL line is “L” during the data transmission.
If changing the SDA line while the SCL line is “H”, the S-7760A goes in the start or stop condition status.

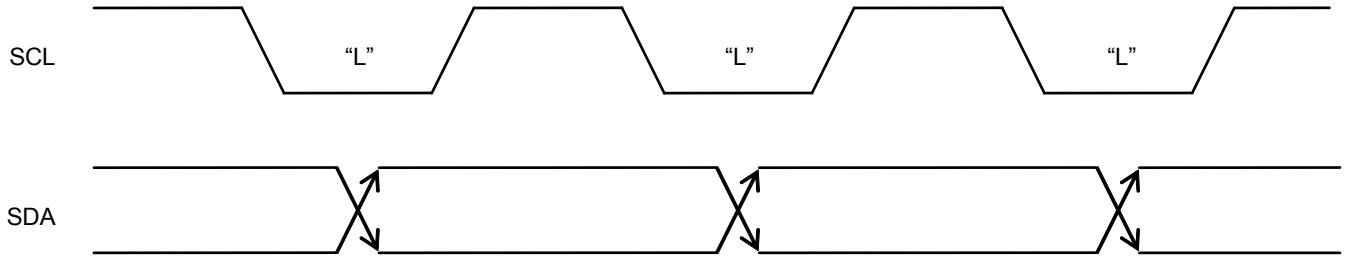



**Figure 20 Data Transfer Timing**

### 4. Acknowledgment

Data is transmitted sequentially in 8-bit. Changing the SDA line to "L" indicates that the devices on the system bus have received data, thus the devices send an acknowledgment signal back during the 9th clock of cycle.
The S-7760A does not send an acknowledgment signal back during the Write operation.

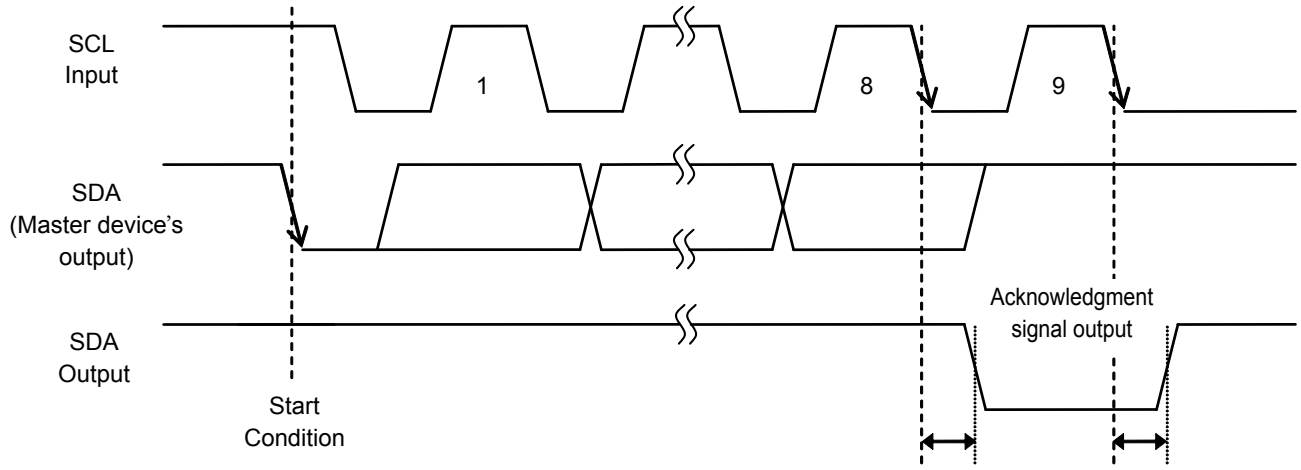



**Figure 21 Acknowledgment Output Timing**

### 5. Read operation

When this IC receives the 7-bit device address and the Read/Write instruction code "1" after receiving a start condition, it generates an acknowledgment signal.
Next, data with 8-bit length is output from this IC synchronizing with the SCL clock.
After that, the master device sends a stop condition, not an acknowledgment signal in order to finish the Read operation.

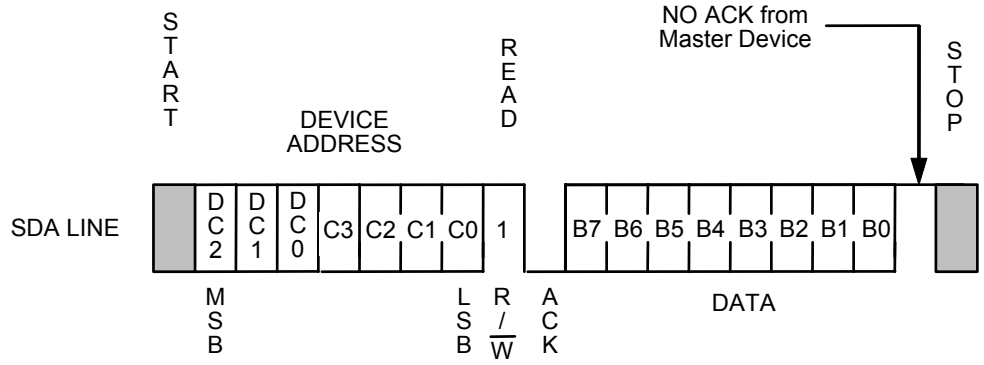



**Figure 22 Read**

## 6. Write operation

### 6. 1 Write

When this IC receives the 7-bit device address and the Read/Write instruction code “0” after receiving a start condition, it generates an acknowledgment signal.
Next, after it receives the 8-bit word address and generates an acknowledgment signal, it receives a stop condition to finish the Write command.
In the Write operation to the E²PROM, the Write operation starts with a stop condition, the S-7760A finishes it after the period to Write (max. 5 ms) has elapsed. During Write to the E²PROM, all operations are inhibited to be performed and the S-7760A does not send back any acknowledgment signals for command inputs.

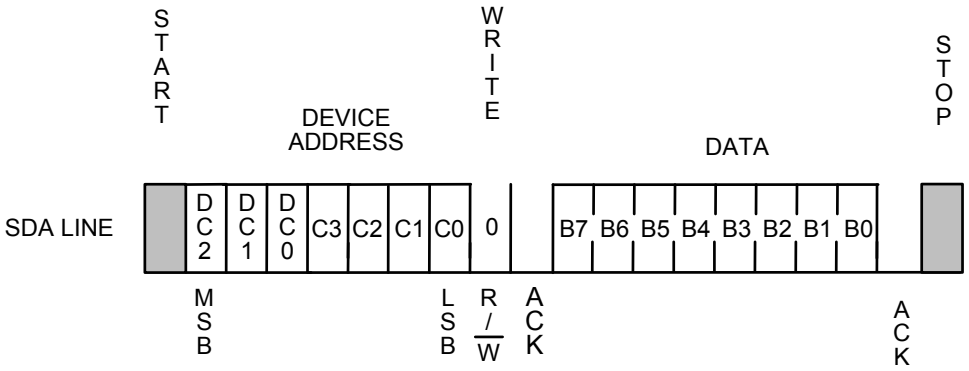



**Figure 23 Write**

### 6. 2 Write Protect

Write protect is available in the S-7760A.
When the WP pin is connected to $V_{CCH}$, the Write operation in all memory area is inhibited. When the WP pin is connected to GND, Write protect becomes invalid so that the Write operation in all memory area is accepted.
Fix the WP pin during the period; from rising of SCL at installing the last bit in Write data until the completion of Write period (max. 5 ms).
Written data in the address is not assured if the condition of the WP pin is changed during this period. Be sure to connect the WP pin to GND when you don’t use Write Protect. Write Protect is valid in the range of power supply voltage.

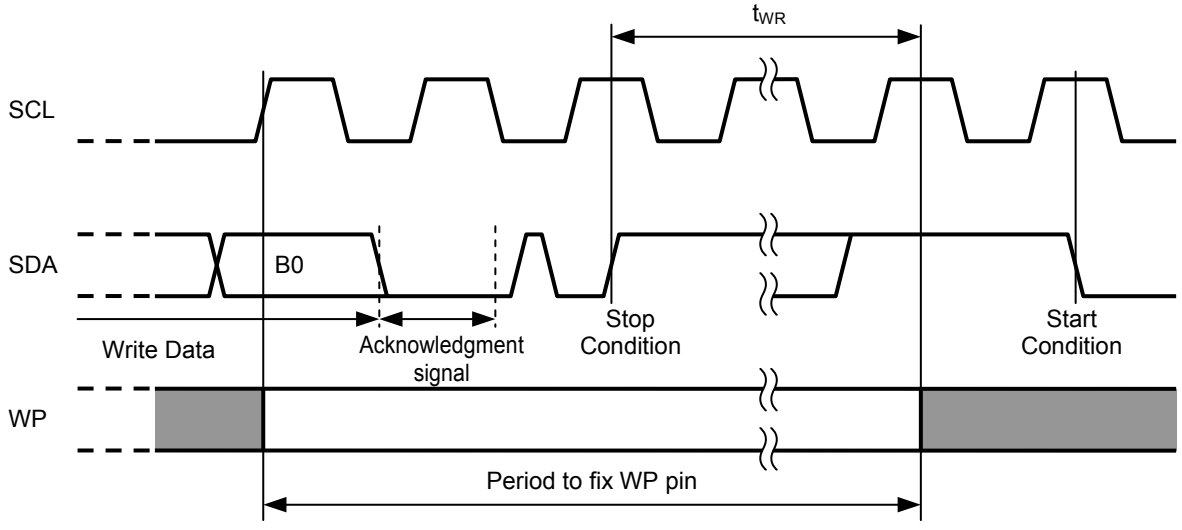



**Figure 24 Period to Fix WP Pin**

### 6. 3 Acknowledgment polling

Acknowledge polling is used to find when the Write operation has completed. After receiving a stop condition the Write operation has once started, all operations are inhibited to be performed so that the S-7760A cannot respond to the signals transmitted from the master device. The master device sends a start condition, the device address and Read/Write instruction code to the S-7760A (slave device), and detects the response from the slave device. It is possible to find when the Write operation has completed. Thus if the slave device does not send an acknowledgment signal back, the Write operation is in progress. If it sends an acknowledgment signal back, the Write operation has completed. Fix the WP pin until an acknowledgment is confirmed. It is recommended to use the Read instruction "1" for the Read/Write instruction code transmitted from the master device during acknowledgment polling.

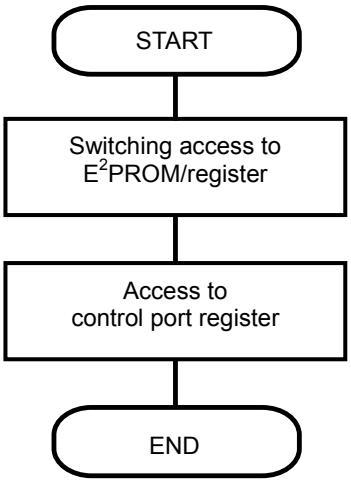
### 6. 4 Irregular action

In the middle of inputting Write data, if inputting a stop condition in clock less than the specified data length (8-bit), the S-7760A does not perform Write to the $E^2$PROM. And it either does not perform Write to the $E^2$PROM if receiving a stop condition after receiving data over 9-bit. However, data in the register has been rewritten at the point when the S-7760A has received the specified length data. Be sure not to input clock which exceeds the specified value due to noise or other causes.

## ■ Example of Flowchart for Software

**1. Read/Write in register**

The example of flowchart for software when accessing to the control port register is shown in **Figure 25**.




1-byte command

(ST, DC2 to 0, 0001, **0**, ACK, SP)*1

2-byte command

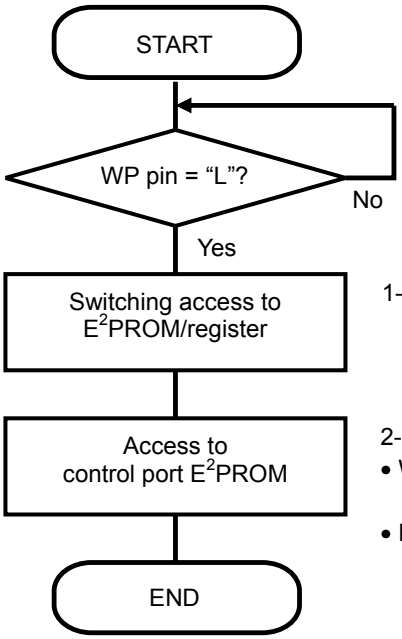
- Write
  (ST, DC2 to 0, 0101, **0**, ACK, CTR7 to 0, ACK, SP)*1
- Read
  (ST, DC2 to 0, 0101, **1**, ACK, CTR7 to 0, ACK, SP)*1

***1.** ST : Start condition
DC2 to 0 : Device code
ACK : Acknowledgment
CTR7 to 0 : Control port register
SP : Stop condition

**Figure 25 Flowchart for Software Example 1**

**2. Read/Write in E²PROM**

The example of flowchart for software when accessing to the E²PROM is shown in **Figure 26**.




1-byte command
(ST, DC2 to 0, 0001, **1**, ACK, SP)*1

2-byte command
- Write
  (ST, DC2 to 0, 0101, **0**, ACK, CTR7 to 0, ACK, SP)*1
- Read
  (ST, DC2 to 0, 0101, **1**, ACK, CTR7 to 0, ACK, SP)*1

***1.** ST : Start condition
DC2 to 0 : Device code
ACK : Acknowledgment
CTR7 to 0 : Control port register
SP : Stop condition

**Figure 26 Flowchart for Software Example 2**