S-8213 Series

BATTERY PROTECTION IC FOR 2-SERIAL / 3-SERIAL CELL PACK (SECONDARY PROTECTION)

www.sii-ic.com

Rev.1.4_00

The S-8213 Series is used for secondary protection of lithium-ion rechargeable batteries, and incorporates a high-accuracy voltage detection circuit and a delay circuit. Short-circuits between VC3 to VSS accommodate serial connection of two cells or three cells.

■ Features

- High-accuracy voltage detection circuit for each cell
  - Overcharge detection voltage n (n = 1 to 3)
    - 4.100 V to 4.500 V (in 50 mV steps)
    - Accuracy: ±25 mV (Ta = +25°C)
    - Accuracy: ±30 mV (Ta = 0°C to +60°C)
  - Overcharge hysteresis voltage n (n = 1 to 3)
    - 0 V ± 25 mV, –0.05 V ± 25 mV, –0.40 V ± 80 mV
- Delay times for overcharge detection can be set by an internal circuit only (external capacitors are unnecessary)
- Output form is selectable: CMOS output, Nch open-drain output
- Output logic is selectable: Active "H", Active "L"
- High-withstand voltage: Absolute maximum rating 26 V
- Wide operation voltage range: 3.6 V to 24 V
- Wide operation temperature range: Ta = –40°C to +85°C
- Low current consumption
  - At V_{CUn} – 1.0 V for each cell: 2.0 μA max. (Ta = +25°C)
  - At 2.0 V for each cell: 0.3 μA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

■ Application

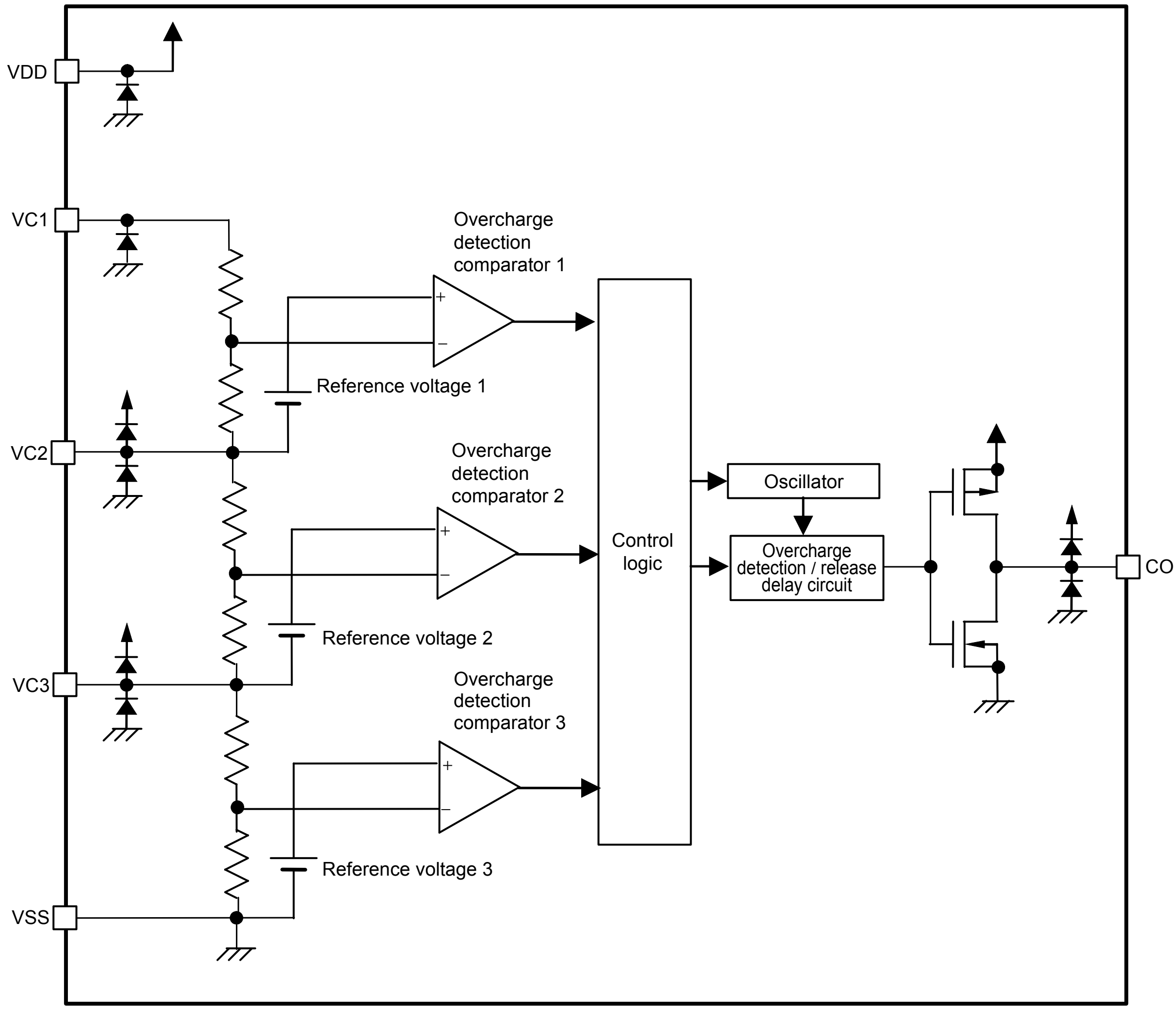
- Lithium-ion rechargeable battery pack (for secondary protection)

■ Packages

- SOT-23-6
- SNT-6A

■ Block Diagram

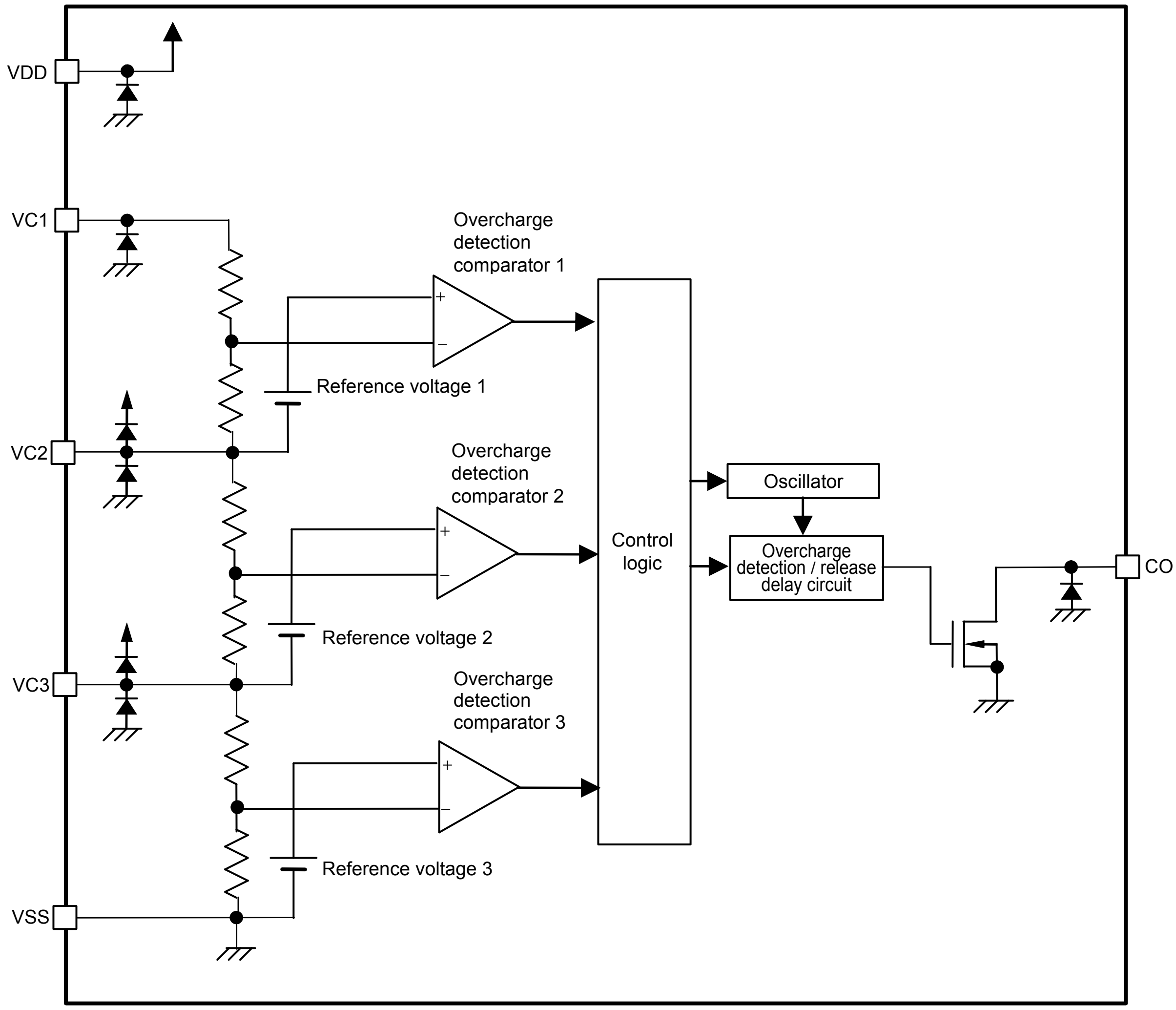
1. CMOS output product



Remark The diodes in the figure are parasitic diodes.

Figure 1

2. Nch open-drain output product



Remark The diodes in the figure are parasitic diodes.

Figure 2

■ Product Name Structure

1. Product name

S-8213 xxx - xxxx U

- U: Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- xxxx: Package abbreviation and IC packing specifications*1
  - M6T1: SOT-23-6, Tape
  - I6T1: SNT-6A, Tape
- xxx: Serial code*2
  - Sequentially set from AAA to AAZ

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SOT-23-6	MP006-A-P-SD	MP006-A-C-SD	MP006-A-R-SD	–
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD

3. Product name list

3. 1 SNT-6A

Table 2

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Hysteresis Voltage [V_{HC}]	Overcharge Detection Delay Time [t_{CU}]	Output Form	Output Logic
S-8213AAB-I6T1U	4.300 V	–0.40 V	2.0 s	CMOS output	Active "H"
S-8213AAC-I6T1U	4.350 V	–0.40 V	2.0 s	CMOS output	Active "H"
S-8213AAD-I6T1U	4.400 V	–0.40 V	2.0 s	CMOS output	Active "H"
S-8213AAE-I6T1U	4.450 V	–0.40 V	2.0 s	CMOS output	Active "H"
S-8213AAF-I6T1U	4.500 V	–0.40 V	2.0 s	CMOS output	Active "H"
S-8213AAG-I6T1U	4.300 V	–0.40 V	4.0 s	CMOS output	Active "H"
S-8213AAH-I6T1U	4.350 V	–0.40 V	4.0 s	CMOS output	Active "H"
S-8213AAI-I6T1U	4.400 V	–0.40 V	4.0 s	CMOS output	Active "H"
S-8213AAJ-I6T1U	4.450 V	–0.40 V	4.0 s	CMOS output	Active "H"
S-8213AAK-I6T1U	4.500 V	–0.40 V	4.0 s	CMOS output	Active "H"
S-8213AAL-I6T1U	4.300 V	–0.40 V	8.0 s	CMOS output	Active "H"
S-8213AAM-I6T1U	4.350 V	–0.40 V	8.0 s	CMOS output	Active "H"
S-8213AAN-I6T1U	4.400 V	–0.40 V	8.0 s	CMOS output	Active "H"
S-8213AAO-I6T1U	4.450 V	–0.40 V	8.0 s	CMOS output	Active "H"
S-8213AAP-I6T1U	4.500 V	–0.40 V	8.0 s	CMOS output	Active "H"
S-8213AAQ-I6T1U	4.150 V	–0.05 V	2.0 s	CMOS output	Active "L"
S-8213AAR-I6T1U	4.250 V	–0.05 V	2.0 s	CMOS output	Active "L"
S-8213AAS-I6T1U	4.150 V	–0.05 V	2.0 s	Nch open-drain output	Active "H"
S-8213AAT-I6T1U	4.250 V	–0.05 V	2.0 s	Nch open-drain output	Active "H"

Remark Please contact our sales department for the products with detection voltage value other than those specified above.

■ Pin Configurations

1. SOT-23-6

Top view

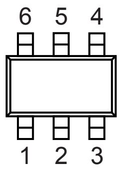


Figure 3

Table 3

Pin No.	Symbol	Description
1	VSS	Input pin for negative power supply, connection pin for negative voltage of battery 3
2	VC3	Connection pin for negative voltage of battery 2, connection pin for positive voltage of battery 3
3	VC2	Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2
4	VC1	Connection pin for positive voltage of battery 1
5	VDD	Input pin for positive power supply
6	CO	Connection pin of charge control FET gate

2. SNT-6A

Top view

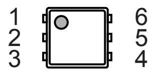


Figure 4

Table 4

Pin No.	Symbol	Description
1	CO	Connection pin of charge control FET gate
2	VDD	Input pin for positive power supply
3	VC1	Connection pin for positive voltage of battery 1
4	VC2	Connection pin for negative voltage of battery 1, connection pin for positive voltage of battery 2
5	VC3	Connection pin for negative voltage of battery 2, connection pin for positive voltage of battery 3
6	VSS	Input pin for negative power supply, connection pin for negative voltage of battery 3

■ Absolute Maximum Ratings

Table 5

(Ta = +25°C unless otherwise specified)

Item		Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD and VSS		V_{DS}	VDD	V_{SS} − 0.3 to V_{SS} + 26	V
Input pin voltage		V_{IN}	VC1, VC2, VC3	V_{SS} − 0.3 to V_{DD} + 0.3	V
CO output pin voltage	CMOS output product	V_{CO}	CO	V_{SS} − 0.3 to V_{DD} + 0.3	V
	Nch open-drain output product			V_{SS} − 0.3 to V_{SS} + 26	V
Power dissipation	SOT-23-6	P_D	−	650[*1]	mW
	SNT-6A			400[*1]	mW
Operation ambient temperature		T_{opr}	−	−40 to +85	°C
Storage temperature		T_{stg}	−	−40 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

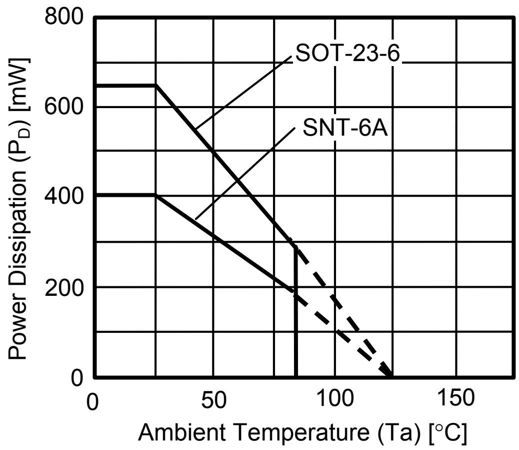


Figure 5 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 6

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
DETECTION VOLTAGE							
Overcharge detection voltage n (n = 1, 2, 3)	V_{CUn}	–	V_{CU} − 0.025	V_{CU}	V_{CU} + 0.025	V	1
		Ta = 0°C to +60°C*1	V_{CU} − 0.030	V_{CU}	V_{CU} + 0.030	V	1
Overcharge hysteresis voltage n (n = 1, 2, 3)	V_{HCn}	V_{HC} = −0.40 V	V_{HC} − 0.080	V_{HC}	V_{HC} + 0.080	V	1
		V_{HC} = 0 V, −0.05 V	V_{HC} − 0.025	V_{HC}	V_{HC} + 0.025	V	1
INPUT VOLTAGE							
Operation voltage between VDD and VSS	V_{DSOP}	–	3.6	–	24	V	–
INPUT CURRENT							
Current consumption during operation	I_{OPE}	V1 = V2 = V3 = V_{CU} − 1.0 V	–	–	2.0	μA	3
Current consumption during overdischarge	I_{PDN}	V1 = V2 = V3 = 2.0 V	–	–	0.3	μA	3
VC1 pin current	I_{VC1}	V1 = V2 = V3 = V_{CU} − 1.0 V	–	–	0.3	μA	4
VC2 pin, VC3 pin current	I_{VC2}, I_{VC3}	V1 = V2 = V3 = V_{CU} − 1.0 V	−0.3	0	0.3	μA	4
OUTPUT CURRENT							
CO pin sink current	I_{COL}	–	0.4	–	–	mA	5
CO pin source current (CMOS output product)	I_{COH}	–	20	–	–	μA	5
CO pin leakage current (Nch open-drain output product)	I_{COLL}	–	–	–	0.1	μA	5
DELAY TIME							
Overcharge detection delay time	t_{CU}	–	t_{CU} × 0.8	t_{CU}	t_{CU} × 1.2	s	1
Transition time to test mode	t_{TST}	–	–	–	20	ms	2

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

1. Overcharge detection voltage, overcharge hysteresis voltage (Test circuit 1)

Set SW1 to OFF and ON in CMOS output product and Nch open-drain output product, respectively.

1. 1 Overcharge detection voltage n (V_{CUn})

Set V1 = V2 = V3 = V_{CU} − 0.05 V. The Overcharge detection voltage 1 (V_{CU1}) is the V1 voltage when the CO pin's output changes after the voltage of V1 has been gradually increased.
Overcharge detection voltage V_{CUn} (n = 2, 3) can be determined in the same way as when n = 1.

1. 2 Overcharge hysteresis voltage n (V_{HCn})

Set V1 = V_{CU} + 0.05 V, V2 = V3 = 2.5 V. The overcharge hysteresis voltage 1 (V_{HC1}) is the difference between V1 voltage and V_{CU1} when the CO pin's output changes after the V1 voltage has been gradually decreased.
Overcharge hysteresis voltage V_{HCn} (n = 2, 3) can be determined in the same way as when n = 1.

2. Output current (Test circuit 5)

Set SW1 and SW2 to OFF.

2. 1 Active "H"

2. 1. 1 CO pin source current (I_{COH})

Set SW1 to ON after setting V1 = 5.0 V, V2 = V3 = 3.0 V, V4 = 0.5 V. I1 is the CO pin source current (I_{COH}) at that time.

2. 1. 2 CO pin sink current (I_{COL})

Set SW2 to ON after setting V1 to V3 = 3.5 V, V5 = 0.5 V. I2 is the CO pin sink current (I_{COL}) at that time.

2. 1. 3 CO pin leakage current (I_{COLL})

Set SW2 to ON after setting V1 = 5.0 V, V2 = V3 = 3.0 V, V5 = 26 V. I2 is the CO pin leakage current (I_{COLL}) at that time.

2. 2 Active "L"

2. 2. 1 CO pin source current (I_{COH})

Set SW1 to ON after setting V1 to V3 = 3.5 V, V4 = 0.5 V. I1 is the CO pin source current (I_{COH}) at that time.

2. 2. 2 CO pin sink current (I_{COL})

Set SW2 to ON after setting V1 = 5.0 V, V2 = V3 = 3.0 V, V5 = 0.5 V. I2 is the CO pin sink current (I_{COL}) at that time.

2. 2. 3 CO pin leakage current (I_{COLL})

Set SW2 to ON after setting V1 to V3 = 3.5 V, V5 = 26 V. I2 is the CO pin leakage current (I_{COLL}) at that time.

3. Overcharge detection delay time (t_{CU}) (Test circuit 1)

Set SW1 to OFF and ON in CMOS output product and Nch open-drain output product, respectively.

Increase V1 up to 5.0 V after setting V1 = V2 = V3 = 3.5 V. The overcharge detection delay time (t_{CU}) is the time period until the CO pin output changes.

4. Transition time to test mode (t_{TST}) (Test circuit 2)

Set SW1 to OFF and ON in CMOS output product and Nch open-drain output product, respectively.

Increase V4 up to 4.0 V, and decrease V4 again to 0 V after setting V1 = V2 = V3 = 3.5 V, and V4 = 0 V.
When the period from when V4 was raised to when it has fallen is short, if an overcharge detection operation is performed subsequently, the delay time is t_{CU}. However, when the period from when V4 is raised to when it has fallen is gradually made longer, the delay time during the subsequent overcharge detection operation is shorter than t_{CU}. The transition time to test mode (t_{TST}) is the period from when V4 was raised to when it has fallen at that time.

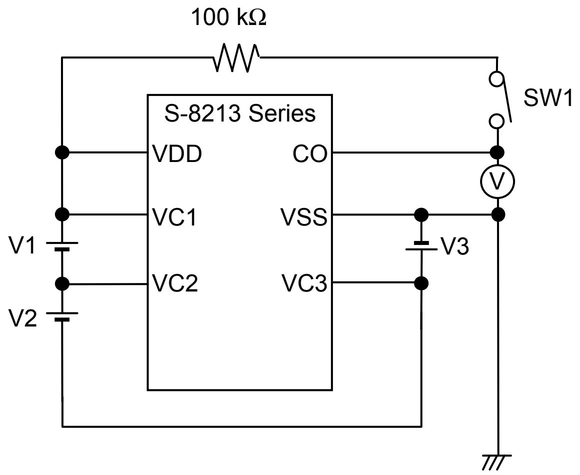


Figure 6 Test Circuit 1

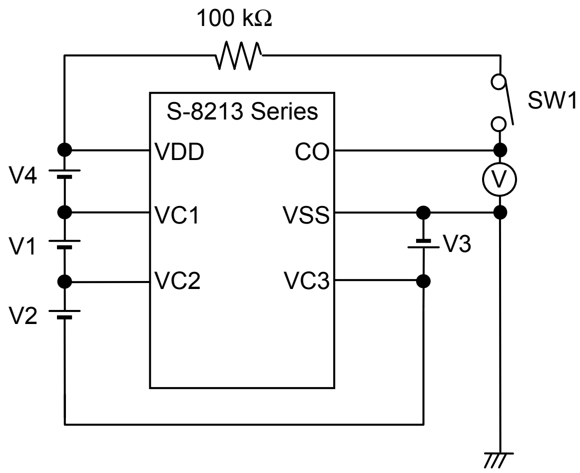


Figure 7 Test Circuit 2

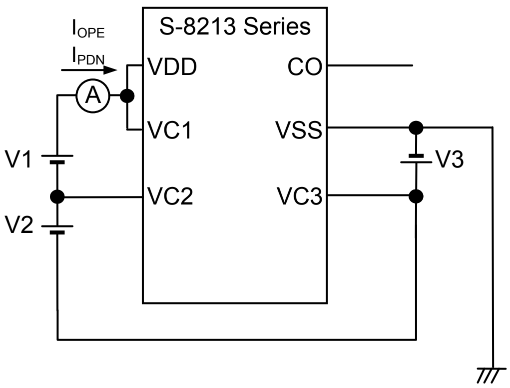


Figure 8 Test Circuit 3

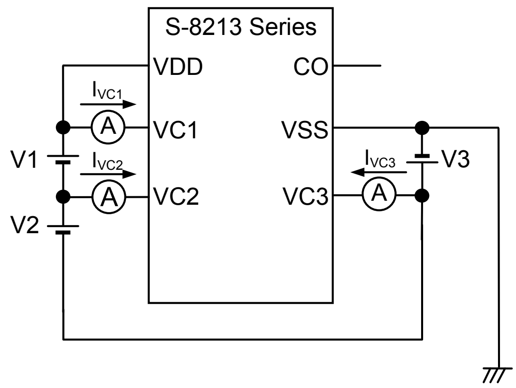


Figure 9 Test Circuit 4

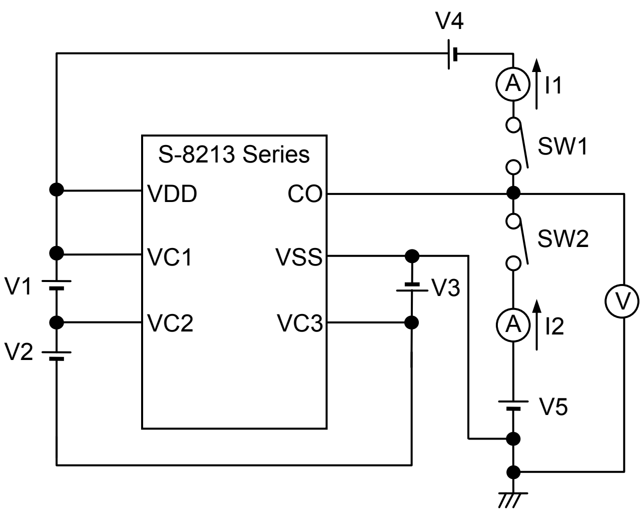


Figure 10 Test Circuit 5

■ Operation

Remark Refer to **"■ Battery Protection IC Connection Examples".**

1. Normal status

If the voltage of each of the batteries is lower than "the overcharge detection voltage (V_{CUn}) + the overcharge hysteresis voltage (V_{HCn})", CO pin output changes to "L" (Active "H") or "H" (Active "L"). This is called normal status.

2. Overcharge status

When the voltage of one of the batteries exceeds V_{CUn} during charging under normal conditions and the status is retained for the overcharge detection delay time (t_{CU}) or longer, CO pin output changes. This is called overcharge status. Connecting FET to the CO pin provides charge control and a second protection.
If the voltage of each of the batteries is lower than V_{CUn} + V_{HCn} and the status is retained for 2.0 ms typ. or longer, the S-8213 Series changes to normal status.

3. Test mode

The overcharge detection delay time (t_{CU}) can be shortened by entering the test mode.

The test mode can be set by retaining the VDD pin voltage 4.0 V or more higher than the VC1 pin voltage for 20 ms or longer. The status is retained by the internal latch and the test mode is retained even if the VDD pin voltage is decreased to the same voltage as that of the VC1 pin voltage.

After that, the latch for retaining the test mode is reset and the S-8213 Series exits from test mode under the overcharge status.

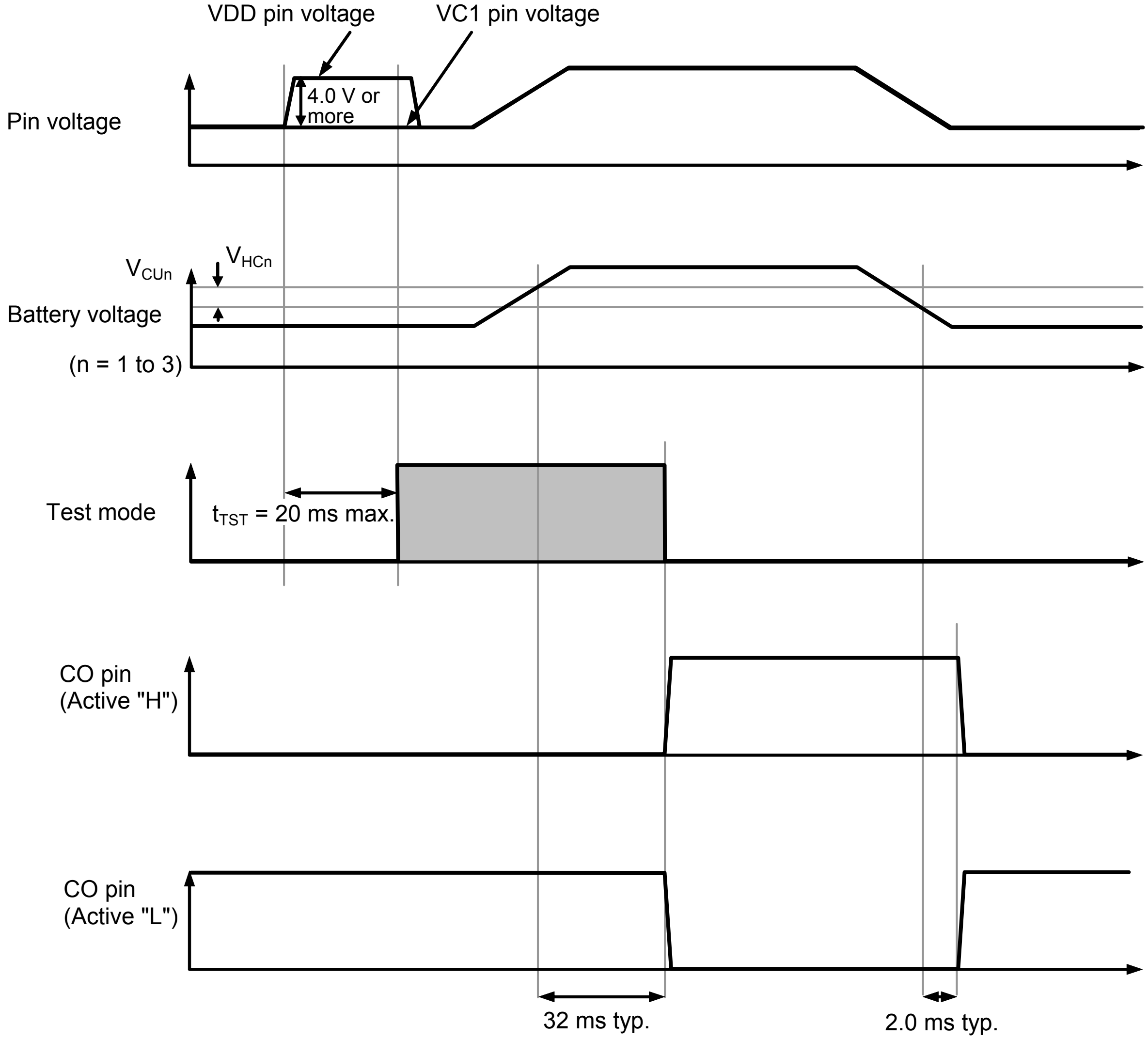


Figure 11

■ Timing Charts

1. Overcharge detection operation

1. 1 CMOS output product

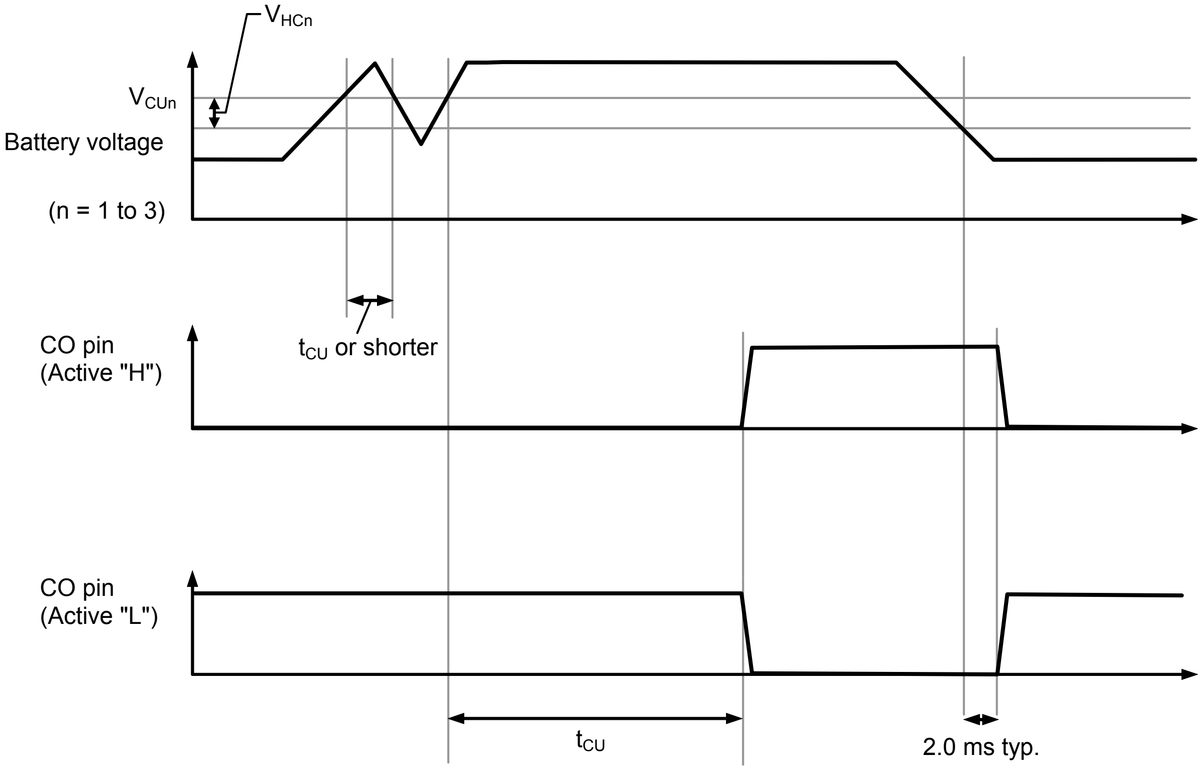


Figure 12

1. 2 Nch open-drain output product

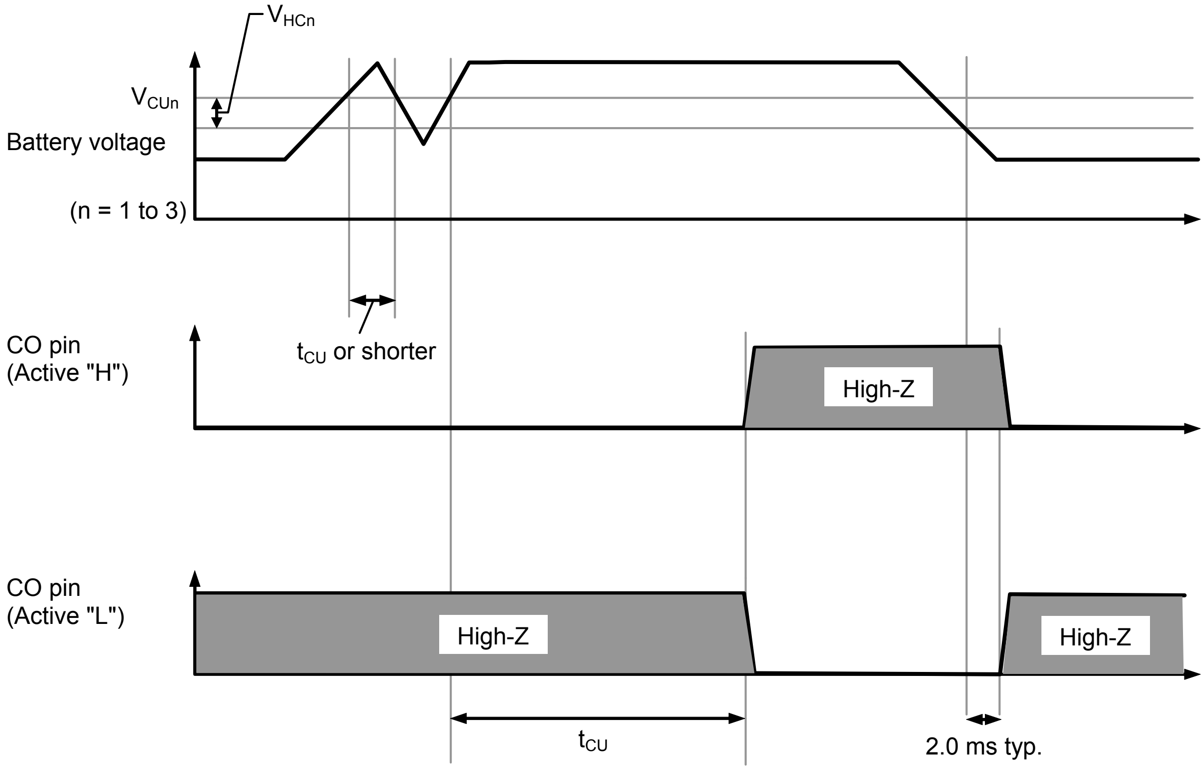


Figure 13

■ Battery Protection IC Connection Examples

1. 3-serial cell (CMOS output product)

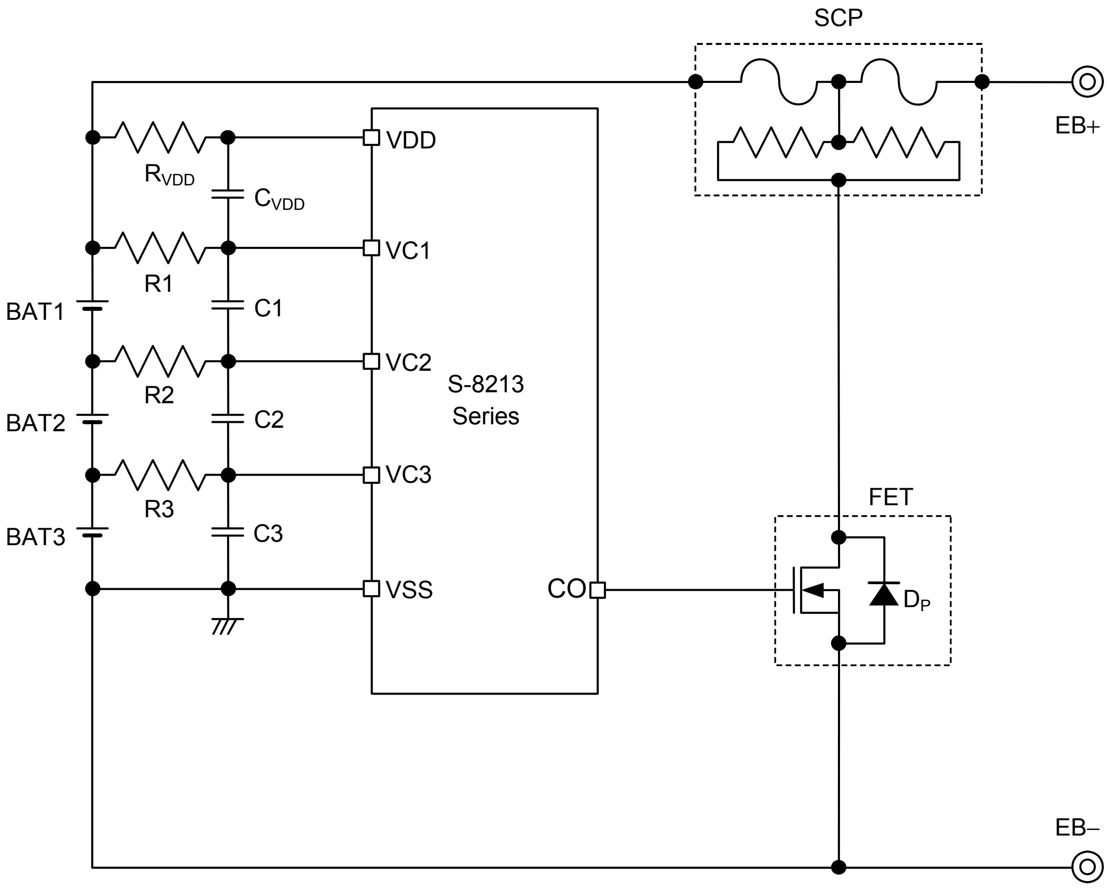


Figure 14

Table 7 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1 to R3	0.2	1	2	kΩ
2	C1 to C3, C_{VDD}	0.01	0.1	1	μF
3	R_{VDD}	50	100	500	Ω

Caution

1. **The above constants are subject to change without prior notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**
3. **Set the same constants to R1 to R3 and to C1 to C3 and C_{VDD}.**
4. **Set R_{VDD}, C1 to C3, and C_{VDD} so that the condition (R_{VDD}) × (C1 to C3, C_{VDD}) ≥ 5 × 10^{-6} is satisfied.**
5. **Set R1 to R3, C1 to C3, and C_{VDD} so that the condition (R1 to R3) × (C1 to C3, C_{VDD}) ≥ 1 × 10^{-4} is satisfied.**
6. **Since CO pin may become detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.**

2. 2-serial cell (CMOS output product)

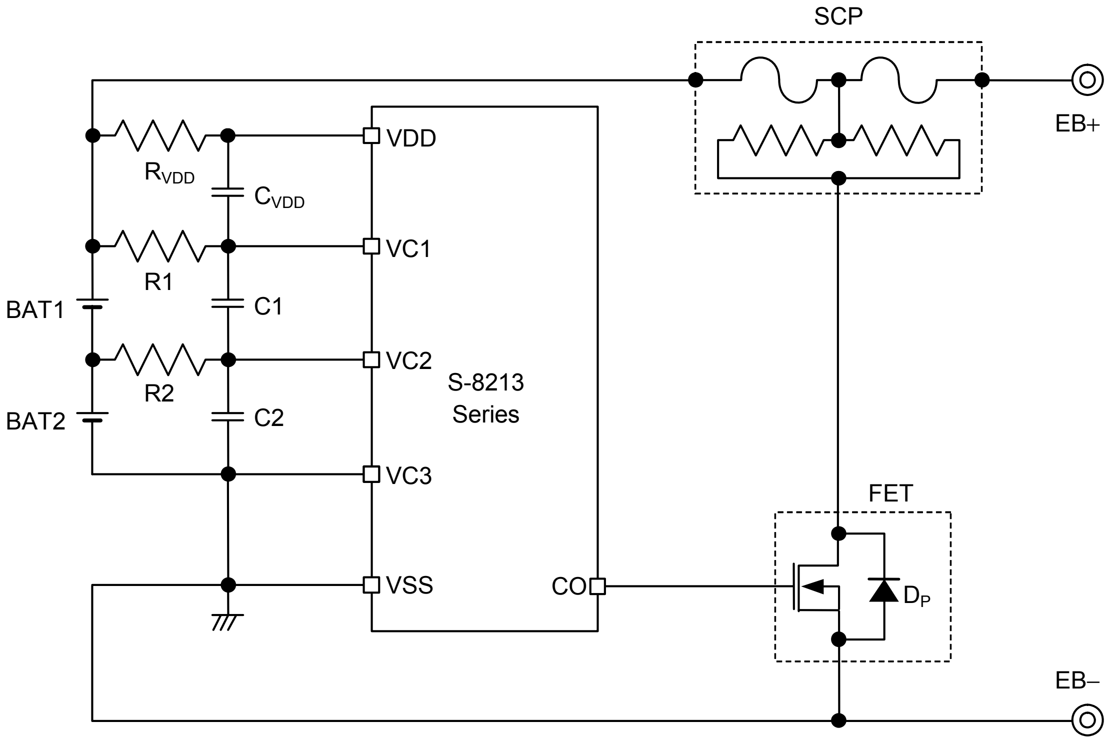


Figure 15

Table 8 Constants for External Components

No.	Part	Min.	Typ.	Max.	Unit
1	R1, R2	0.2	1	2	kΩ
2	C1, C2, C_{VDD}	0.01	0.1	1	μF
3	R_{VDD}	50	100	500	Ω

Caution
1. **The above constants are subject to change without prior notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.**
3. **Set the same constants to R1, R2 and to C1, C2 and C_{VDD}.**
4. **Set R_{VDD}, C1, C2, and C_{VDD} so that the condition (R_{VDD}) × (C1, C2, C_{VDD}) ≥ 5×10^{-6} is satisfied.**
5. **Set R1, R2, C1, C2, and C_{VDD} so that the condition (R1, R2) × (C1, C2, C_{VDD}) ≥ 1×10^{-4} is satisfied.**
6. **Since CO pin may become detection status transiently when the battery is being connected, connect the positive terminal of BAT1 last in order to prevent the three terminal protection fuse from cutoff.**

[For SCP, contact]
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Contact Us: http://www.dexerials.jp/en/

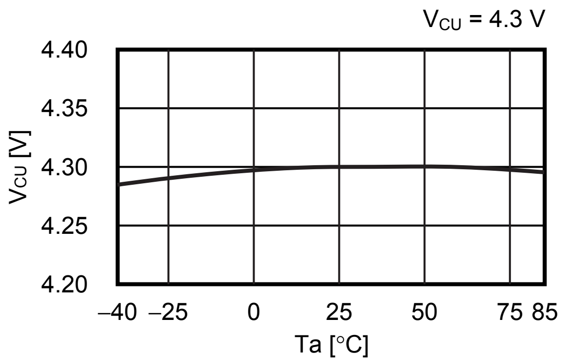
■ Precautions

- Do not connect batteries charged with V_{CUn} + V_{HCn} or higher. If the connected batteries include a battery charged with V_{CUn} + V_{HCn} or more, the S-8213 series may become overcharge status after all pins are connected.
- In some application circuits, even if an overcharged battery is not included, the order of connecting batteries may be restricted to prevent transient output of CO detection pulses when the batteries are connected. Perform thorough evaluation with the actual application circuit.
- Before the battery connection, short-circuit the battery side pins R_{VDD} and R1, shown in the figure in "**■ Battery Protection IC Connection Examples**".
- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply to this IC an electrostatic discharge that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII Semiconductor Corporation claims no responsibility for any disputes arising out of or in connection with any infringement of patents owned by a third party by products including this IC.

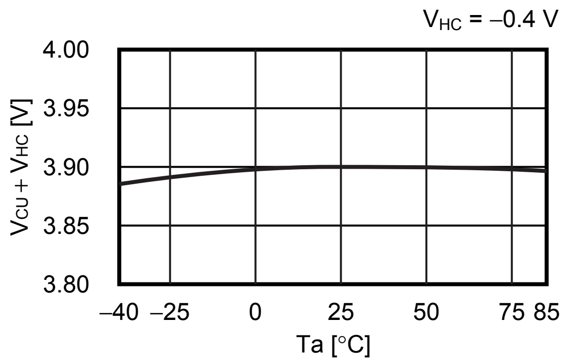
■ Characteristics (Typical Data)

1. Detection voltage

1. 1 V_{CU} vs. Ta

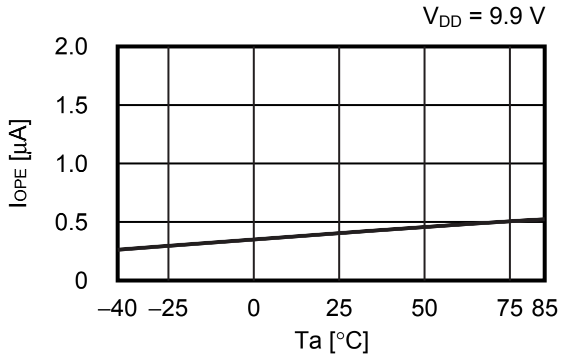


1. 2 $V_{CU} + V_{HC}$ vs. Ta

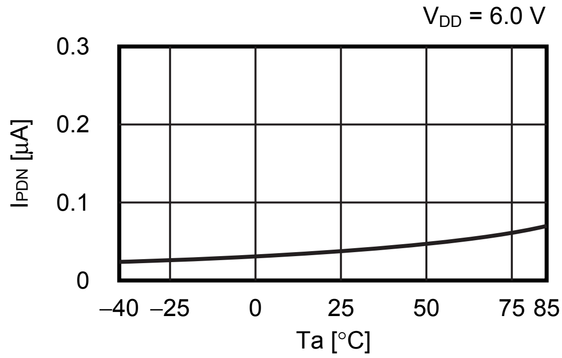


2. Current consumption

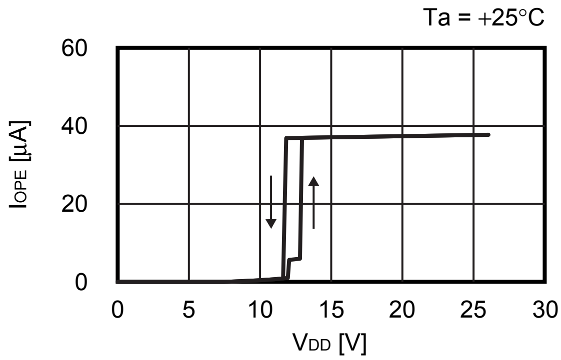
2. 1 I_{OPE} vs. Ta



2. 2 I_{PDN} vs. Ta

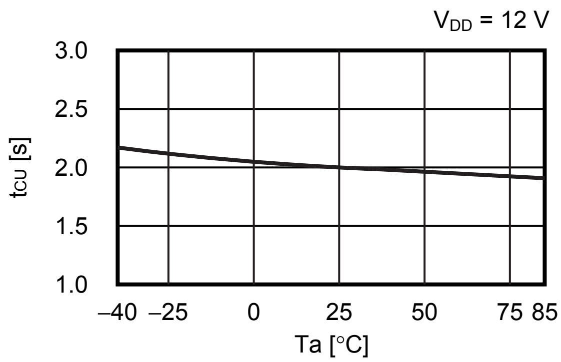


2. 3 I_{OPE} vs. V_{DD}



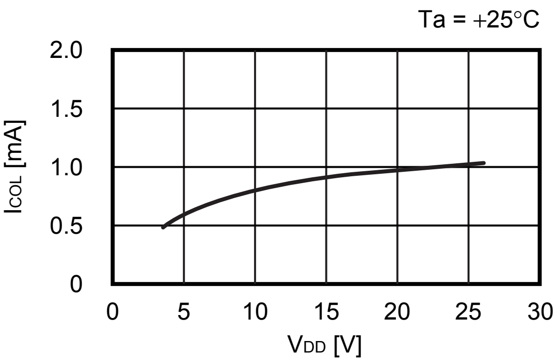
3. Delay time

3. 1 t_{CU} vs. Ta

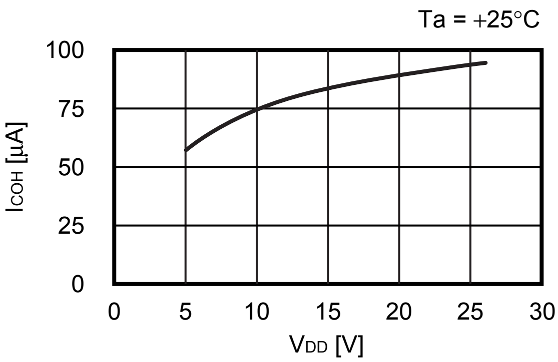


4. Output current

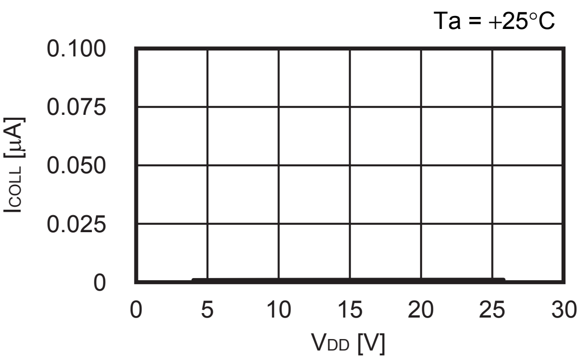
4. 1 I_{COL} vs. V_{DD}



4. 2 I_{COH} vs. V_{DD}

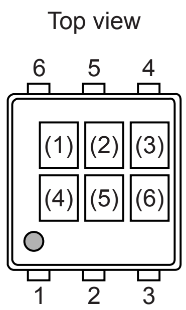


4. 3 I_{COLL} vs. V_{DD}



■ Marking Specification

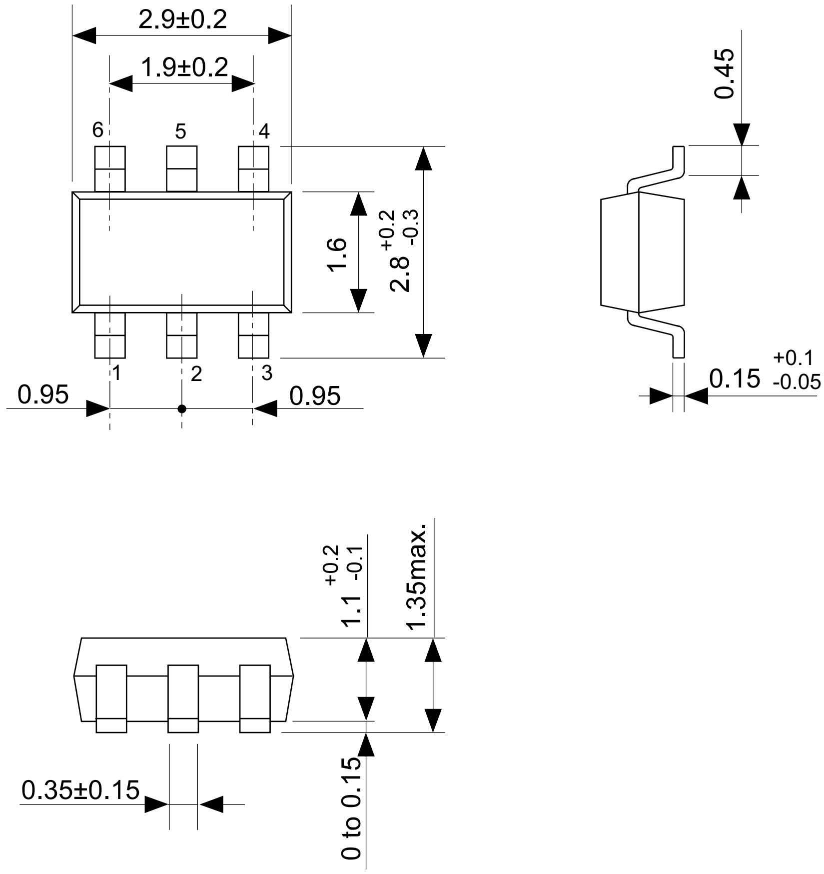
1. SNT-6A



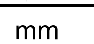
(1) to (3): Product code (Refer to **Product name vs. Product code**)
(4) to (6): Lot number

Product name vs. Product code

Product Name	Product Code		
	(1)	(2)	(3)
S-8213AAB-I6T1U	S	U	B
S-8213AAC-I6T1U	S	U	C
S-8213AAD-I6T1U	S	U	D
S-8213AAE-I6T1U	S	U	E
S-8213AAF-I6T1U	S	U	F
S-8213AAG-I6T1U	S	U	G
S-8213AAH-I6T1U	S	U	H
S-8213AAI-I6T1U	S	U	I
S-8213AAJ-I6T1U	S	U	J
S-8213AAK-I6T1U	S	U	K
S-8213AAL-I6T1U	S	U	L
S-8213AAM-I6T1U	S	U	M
S-8213AAN-I6T1U	S	U	N
S-8213AAO-I6T1U	S	U	O
S-8213AAP-I6T1U	S	U	P
S-8213AAQ-I6T1U	S	U	Q
S-8213AAR-I6T1U	S	U	R
S-8213AAS-I6T1U	S	U	S
S-8213AAT-I6T1U	S	U	T



No. MP006-A-P-SD-2.1

TITLE	SOT236-A-PKG Dimensions
No.	MP006-A-P-SD-2.1
ANGLE	
UNIT	mm

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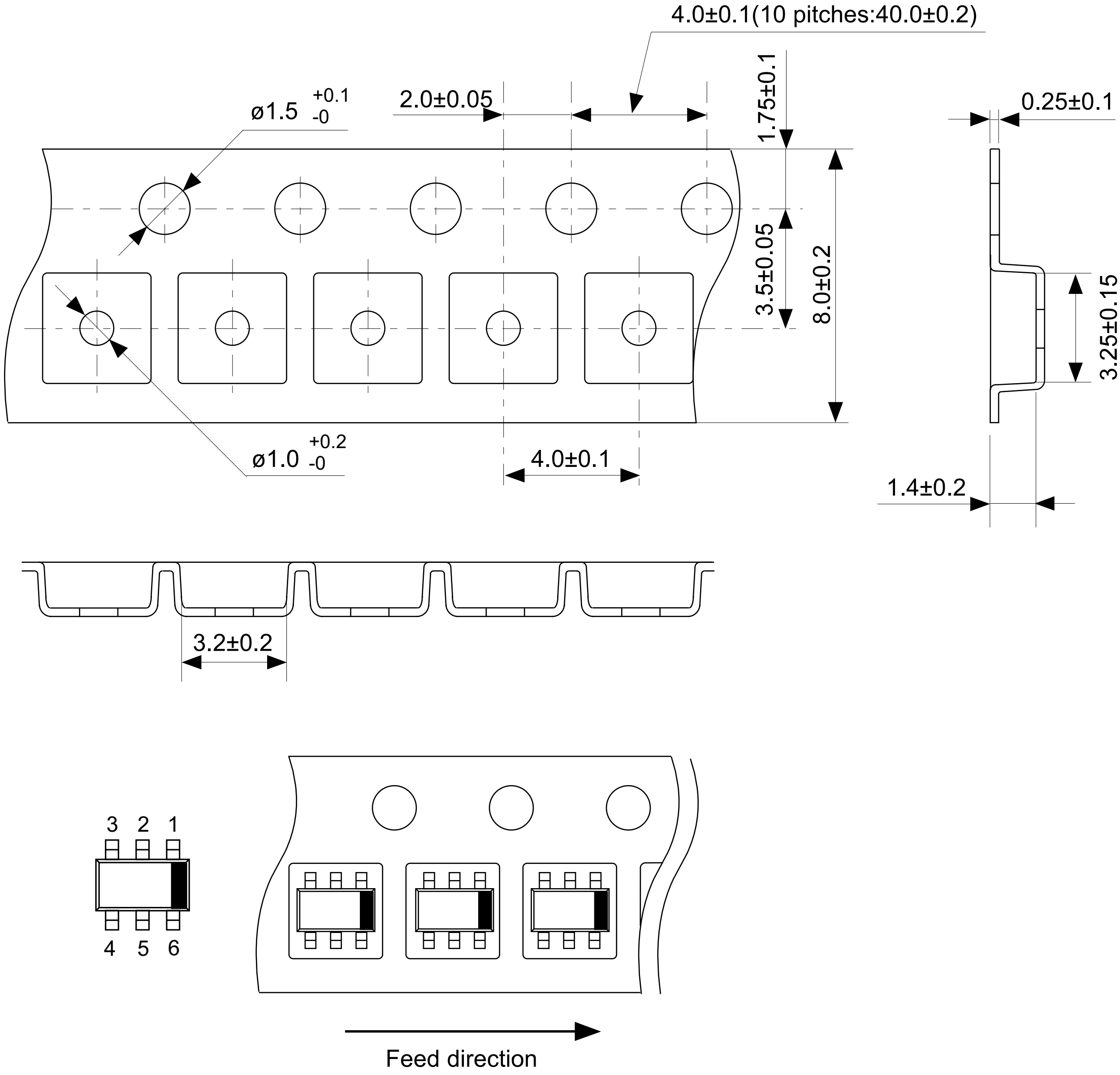

No. MP006-A-C-SD-3.1

TITLE	SOT236-A-Carrier Tape
No.	MP006-A-C-SD-3.1
ANGLE	
UNIT	mm

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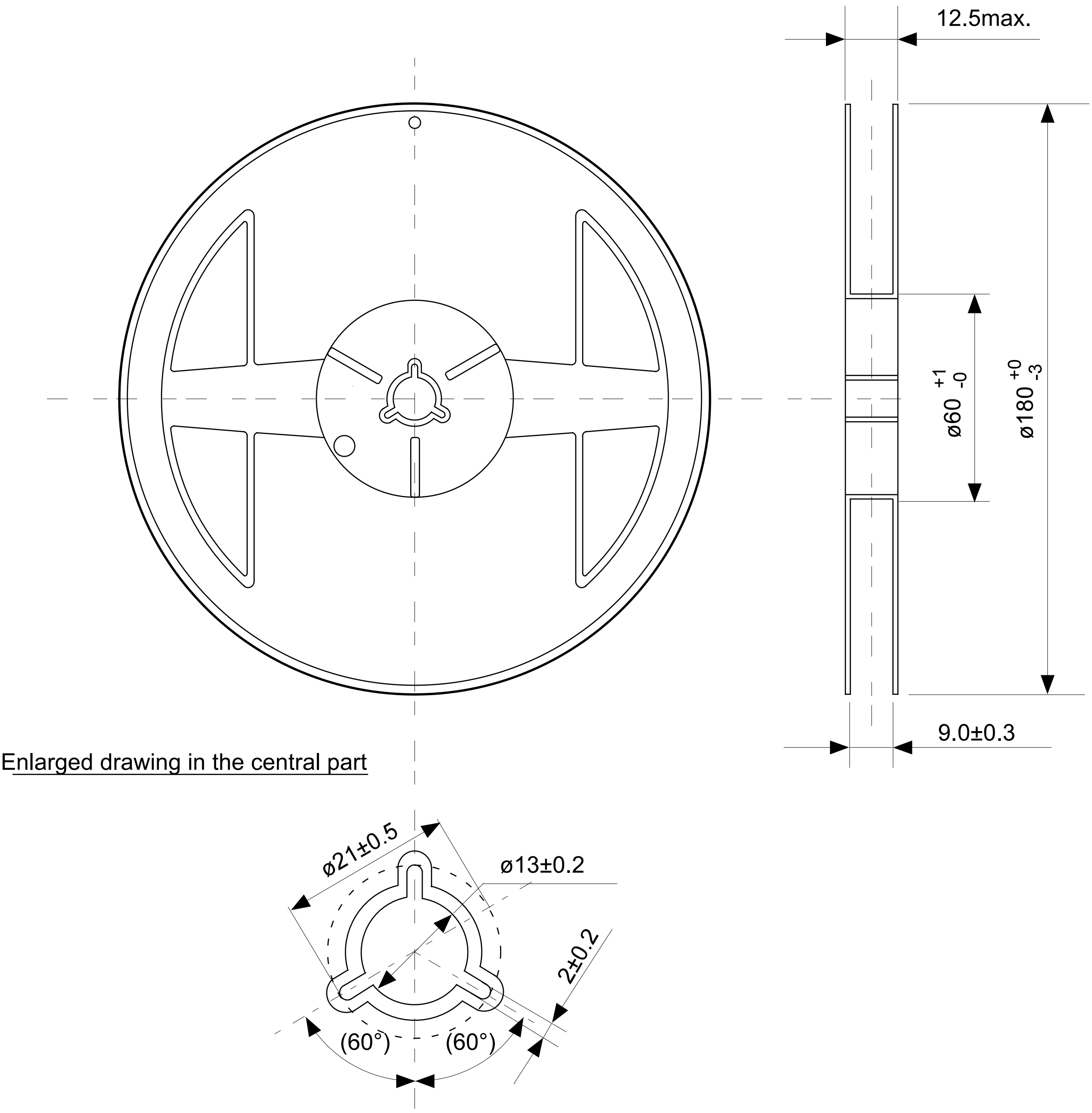
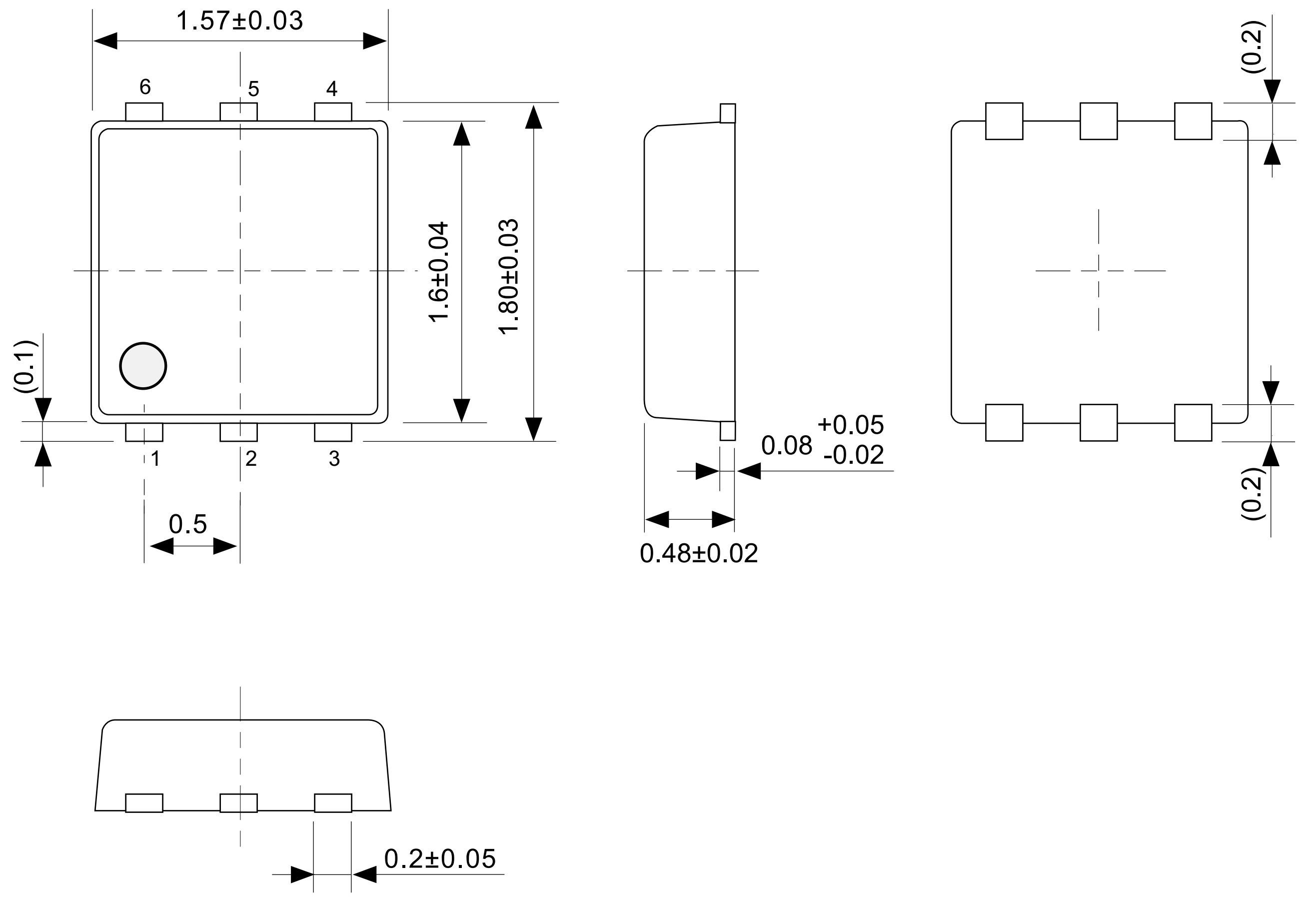


No. MP006-A-R-SD-2.1

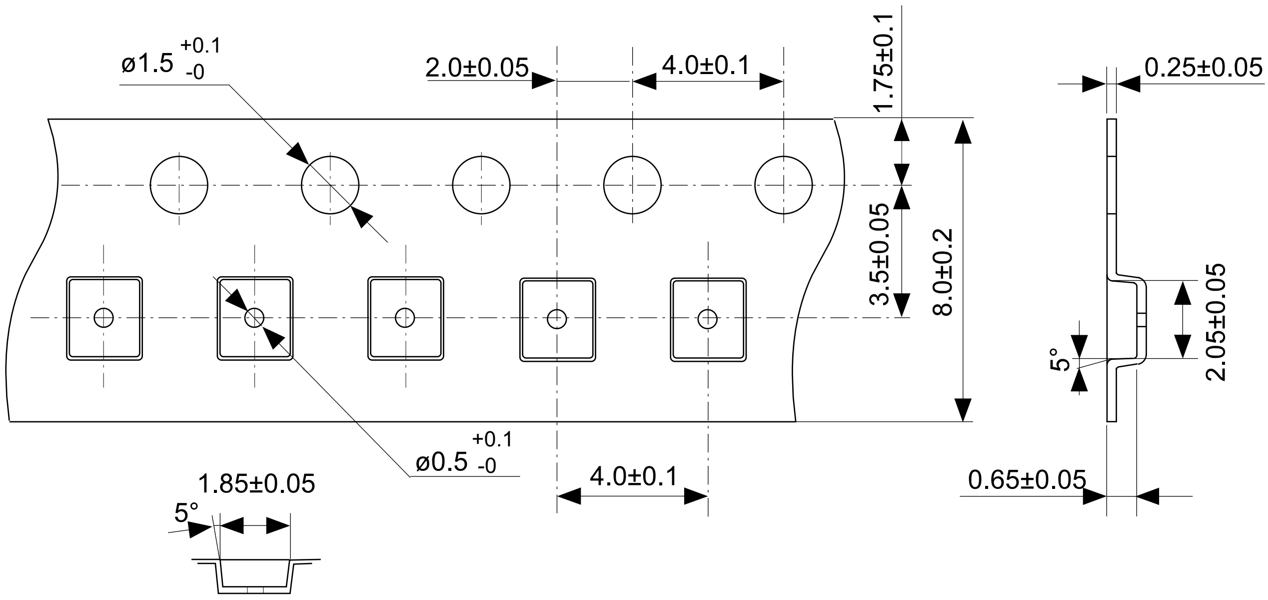
TITLE	SOT236-A-Reel		
No.	MP006-A-R-SD-2.1		
ANGLE		QTY	3,000
UNIT	mm		
SII Semiconductor Corporation			

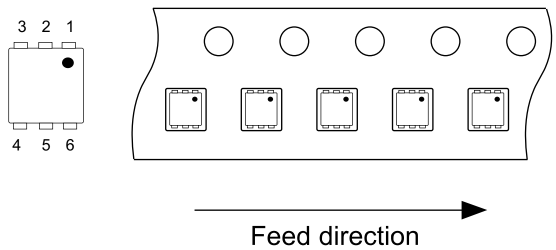


No. PG006-A-P-SD-2.1

TITLE	SNT-6A-A-PKG Dimensions
No.	PG006-A-P-SD-2.1
ANGLE	
UNIT	mm

SII Semiconductor Corporation





No. PG006-A-C-SD-1.0

TITLE	SNT-6A-A-Carrier Tape
No.	PG006-A-C-SD-1.0
ANGLE	
UNIT	mm

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