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BATTERY PROTECTION IC WITH DISCHARGE CONTROL FUNCTION FOR 1-CELL PACK

www.sii-ic.com

Rev.2.5_00

The S-8230A/B Series is a protection IC for 1-cell lithium-ion / lithium polymer rechargeable batteries and includes high-accuracy voltage detection circuits and delay circuits.
The S-8230A/B Series is suitable for protecting 1-cell lithium-ion / lithium polymer rechargeable battery packs from overcharge, overdischarge, overcurrent, and controlling discharge by external signal.

■ Features

- High-accuracy voltage detection circuit

Overcharge detection voltage	3.5 V to 4.5 V (5 mV step)	Accuracy ±20 mV (Ta = +25°C) Accuracy ±25 mV (Ta = −10°C to +60°C)
Overcharge release voltage	3.1 V to 4.5 V*1	Accuracy ±30 mV
Overdischarge detection voltage	2.0 V to 3.4 V (10 mV step)	Accuracy ±35 mV
Overdischarge release voltage	2.0 V to 3.4 V*2	Accuracy ±50 mV
Discharge overcurrent detection voltage	0.05 V to 0.20 V (10 mV step)	Accuracy ±10 mV
Load short-circuiting detection voltage	0.5 V (fixed)	Accuracy ±100 mV
Charge overcurrent detection voltage	−0.20 V to −0.05 V (25 mV step) −0.16 V to −0.08 V (40 mV step)	Accuracy ±15 mV

- Detection delay times are generated only by an internal circuit (External capacitors are unnecessary). Accuracy ±20%
- Discharge control function
  - CTL pin control logic is selectable: Active "H", active "L"
  - CTL pin internal resistance connection is selectable: Pull-up, pull-down
  - CTL pin internal resistance value is selectable: 1.0 MΩ, 2.5 MΩ, 5.0 MΩ
  - Discharge inhibition status latch function is selectable: Available, unavailable
- 0 V battery charge function is selectable: Available, unavailable
- Power-down function is selectable: Available, unavailable
- Release condition of discharge overcurrent status is selectable: Load disconnection, charger connection
- High-withstand voltage: VM pin and CO pin: Absolute maximum rating 28 V
- Wide operation temperature range: Ta = −40°C to +85°C
- Low current consumption
  - During operation: 2.8 μA typ., 5.5 μA max. (Ta = +25°C)
  - During power-down: 0.1 μA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

***1.** Overcharge release voltage = Overcharge detection voltage − Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV step.)
***2.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV step.)

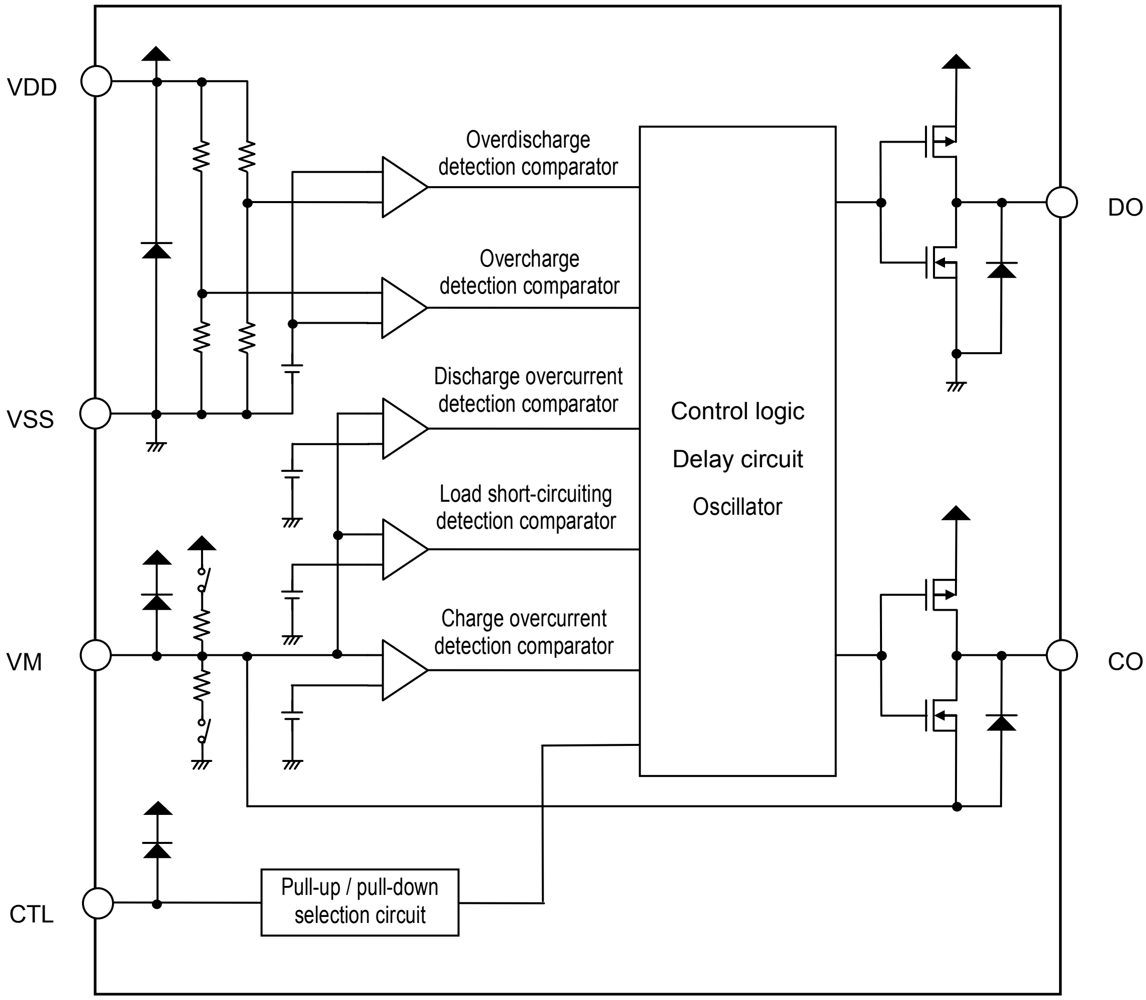
■ Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

■ Package

- SNT-6A

■ Block Diagram



Remark All the diodes shown in the figure are parasitic diodes.

Figure 1

■ Product Name Structure

1. Product name

S-8230 x xx - I6T1 U

- **U** — Environmental code
  - U: Lead-free (Sn 100%), halogen-free
- **I6T1** — Package abbreviation and IC packing specifications*1
  - I6T1: SNT-6A, Tape
- **xx** — Serial code*2
  - Sequentially set from AA to ZZ
- **x** — Discharge inhibition status latch function
  - A: Unavailable
  - B: Available

***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD

3. Product name list

3. 1 SNT-6A

3. 1. 1 S-8230A Series

Table 2

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Over-discharge Detection Voltage [V_{DL}]	Over-discharge Release Voltage [V_{DU}]	Discharge Overcurrent Detection Voltage [V_{DIOV}]	Charge Overcurrent Detection Voltage [V_{CIOV}]	Delay Time Combination*1	Function Combination*2
S-8230AAD-I6T1U	4.425 V	4.225 V	2.500 V	2.500 V	0.130 V	−0.100 V	(3)	(3)
S-8230AAE-I6T1U	4.415 V	4.215 V	2.500 V	2.900 V	0.050 V	−0.040 V	(5)	(5)
S-8230AAF-I6T1U	4.425 V	4.225 V	2.800 V	2.800 V	0.130 V	−0.100 V	(3)	(6)

***1.** Refer to **Table 4** about the details of the delay time combinations.
***2.** Refer to **Table 6** about the details of the function combinations.

Remark Please contact our sales office for the products with detection voltage value other than those specified above.

3. 1. 2 S-8230B Series

Table 3

Product Name	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Over-discharge Detection Voltage [V_{DL}]	Over-discharge Release Voltage [V_{DU}]	Discharge Overcurrent Detection Voltage [V_{DIOV}]	Charge Overcurrent Detection Voltage [V_{CIOV}]	Delay Time Combination*1	Function Combination*2
S-8230BAA-I6T1U	4.280 V	4.080 V	2.300 V	2.300 V	0.080 V	−0.100 V	(1)	(1)
S-8230BAB-I6T1U	4.280 V	3.880 V	2.500 V	3.000 V	0.200 V	−0.050 V	(2)	(2)
S-8230BAE-I6T1U	4.280 V	3.880 V	2.300 V	2.300 V	0.140 V	−0.050 V	(4)	(4)
S-8230BAF-I6T1U	4.425 V	4.225 V	2.500 V	2.500 V	0.130 V	−0.100 V	(3)	(1)
S-8230BAG-I6T1U	4.425 V	4.225 V	2.500 V	2.500 V	0.130 V	−0.050 V	(2)	(2)

***1.** Refer to **Table 4** about the details of the delay time combinations.
***2.** Refer to **Table 6** about the details of the function combinations.

Remark Please contact our sales office for the products with detection voltage value other than those specified above.

Table 4

Delay Time Combination	Overcharge Detection Delay Time [t_{CU}]	Overdischarge Detection Delay Time [t_{DL}]	Discharge Overcurrent Detection Delay Time [t_{DIOV}]	Load Short-circuiting Detection Delay Time [t_{SHORT}]	Charge Overcurrent Detection Delay Time [t_{CIOV}]	Discharge Inhibition Delay Time [t_{CTL}]
(1)	1.0 s	128 ms	16 ms	280 μs	8 ms	256 ms
(2)	1.0 s	128 ms	16 ms	1 ms	8 ms	256 ms
(3)	1.0 s	32 ms	8 ms	280 μs	8 ms	256 ms
(4)	1.0 s	128 ms	32 ms	1 ms	8 ms	256 ms
(5)	1.0 s	64 ms	8 ms	280 μs	8 ms	256 ms

Remark The delay times can be changed within the range listed in **Table 5**. For details, please contact our sales office.

Table 5

Delay Time	Symbol	Selection Range			Remark
Overcharge detection delay time	t_{CU}	256 ms	512 ms	1.0 s*1	Select a value from the left.
Overdischarge detection delay time	t_{DL}	32 ms	64 ms*1	128 ms	Select a value from the left.
Discharge overcurrent detection delay time	t_{DIOV}	4 ms	8 ms*1	16 ms	Select a value from the left.
Load short-circuiting detection delay time	t_{SHORT}	280 μs*1	530 μs	1 ms	Select a value from the left.
Charge overcurrent detection delay time	t_{CIOV}	4 ms	8 ms*1	16 ms	Select a value from the left.
Discharge inhibition delay time	t_{CTL}	64 ms	128 ms	256 ms*1	Select a value from the left.

***1.** This value is the delay time of the standard products.

Table 6

Function Combination	CTL Pin			Discharge Inhibition Status Latch Function*4	0 V Battery Charge Function*5	Power-down Function*6	Release Condition of Discharge Overcurrent Status*7
	Control Logic*1	Internal Resistance Connection*2	Internal Resistance Value*3 [R_{CTL}]				
(1)	Active "L"	Pull-down	1.0 MΩ	Available	Available	Available	Load disconnection
(2)	Active "L"	Pull-up	1.0 MΩ	Available	Unavailable	Available	Charger connection
(3)	Active "L"	Pull-up	5.0 MΩ	Unavailable	Available	Available	Load disconnection
(4)	Active "L"	Pull-down	1.0 MΩ	Available	Unavailable	Available	Charger connection
(5)	Active "L"	Pull-up	5.0 MΩ	Unavailable	Available	Unavailable	Load disconnection
(6)	Active "H"	Pull-down	5.0 MΩ	Unavailable	Unavailable	Available	Load disconnection

Caution The combination of CTL pin control logic active "H" and CTL pin internal resistance connection "pull-up" worsens the accuracy of overcharge detection voltage. Therefore, this combination can not be set up.

***1.** CTL pin control logic active "H" / active "L" is selectable.
***2.** CTL pin internal resistance connection "pull-up" / "pull-down" is selectable.
***3.** CTL pin internal resistance value 1.0 MΩ / 2.5 MΩ / 5.0 MΩ is selectable.
***4.** Discharge inhibition status latch function "available" / "unavailable" is selectable.
***5.** 0 V battery charge function "available" / "unavailable" is selectable.
***6.** Power-down function "available" / "unavailable" is selectable.
***7.** Release condition of discharge overcurrent status "load disconnection" / "charger connection" is selectable.

Remark Please contact our sales office for the products with function combinations other than those specified above.

■ Pin Configuration

1. SNT-6A

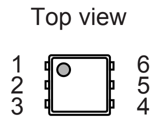


Figure 2

Table 7

Pin No.	Symbol	Description
1	CTL	Discharge control pin
2	CO	Connection pin of charge control FET gate (CMOS output)
3	DO	Connection pin of discharge control FET gate (CMOS output)
4	VSS	Input pin for negative power supply
5	VDD	Input pin for positive power supply
6	VM	Voltage detection pin between VM pin and VSS pin (Overcurrent / charger detection pin)

■ Absolute Maximum Ratings

Table 8

(Ta = +25°C unless otherwise specified)

Item	Symbol	Applied pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V_{DS}	VDD	V_{SS} − 0.3 to V_{SS} + 12	V
VM pin input voltage	V_{VM}	VM	V_{DD} − 28 to V_{DD} + 0.3	V
DO pin output voltage	V_{DO}	DO	V_{SS} − 0.3 to V_{DD} + 0.3	V
CO pin output voltage	V_{CO}	CO	V_{VM} − 0.3 to V_{DD} + 0.3	V
CTL pin input voltage	V_{CTL}	CTL	V_{SS} − 0.3 to V_{DD} + 0.3	V
Power dissipation	P_D	−	400*1	mW
Operation ambient temperature	T_{opr}	−	−40 to +85	°C
Storage temperature	T_{stg}	−	−55 to +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

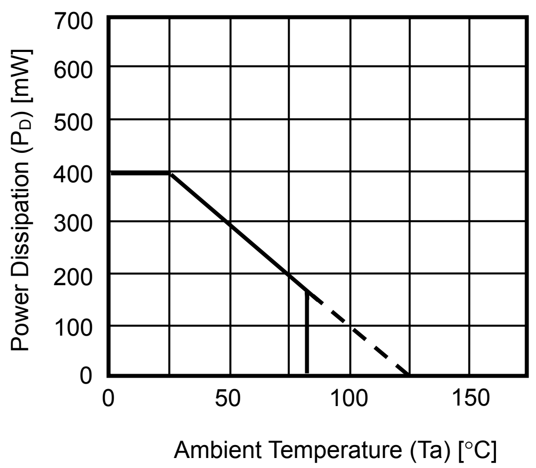


Figure 3 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

1. Ta = +25°C

Table 9

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	–	V_{CU} – 0.020	V_{CU}	V_{CU} + 0.020	V	1
		Ta = –10°C to +60°C*1	V_{CU} – 0.025	V_{CU}	V_{CU} + 0.025	V	1
Overcharge release voltage	V_{CL}	$V_{CL} \neq V_{CU}$	V_{CL} – 0.030	V_{CL}	V_{CL} + 0.030	V	1
		$V_{CL} = V_{CU}$	V_{CL} – 0.025	V_{CL}	V_{CL} + 0.020	V	1
Overdischarge detection voltage	V_{DL}	–	V_{DL} – 0.035	V_{DL}	V_{DL} + 0.035	V	2
Overdischarge release voltage	V_{DU}	$V_{DL} \neq V_{DU}$	V_{DU} – 0.050	V_{DU}	V_{DU} + 0.050	V	2
		$V_{DL} = V_{DU}$	V_{DU} – 0.035	V_{DU}	V_{DU} + 0.035	V	2
Discharge overcurrent detection voltage	V_{DIOV}	–	V_{DIOV} – 0.010	V_{DIOV}	V_{DIOV} + 0.010	V	2
Load short-circuiting detection voltage	V_{SHORT}	–	0.40	0.50	0.60	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	V_{CIOV} – 0.015	V_{CIOV}	V_{CIOV} + 0.015	V	2
0 V Battery Charge Function							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge function "available"	0.0	0.7	1.0	V	2
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge function "unavailable"	1.0	1.2	1.4	V	2
Internal Resistance							
Resistance between VM pin and VDD pin	R_{VMD}	–	100	300	900	kΩ	3
Resistance between VM pin and VSS pin	R_{VMS}	–	10	20	40	kΩ	3
CTL pin internal resistance	R_{CTL}	–	R_{CTL} × 0.45	R_{CTL}	R_{CTL} × 1.75	MΩ	3
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	6.5	V	–
Operation voltage between VDD pin and VM pin	V_{DSOP2}	–	1.5	–	28	V	–
CTL pin voltage "H"	V_{CTLH}	–	–	–	V_{DD} × 0.9	V	2
CTL pin voltage "L"	V_{CTLL}	–	V_{DD} × 0.1	–	–	V	2
Input Current							
Current consumption during operation	I_{OPE}	–	1.0	2.8	5.5	μA	3
Current consumption during power-down	I_{PDN}	–	–	–	0.1	μA	3
Current consumption during overdischarge	I_{OPED}	–	–	–	4.0	μA	3
Current consumption during discharge inhibition	I_{OPEC}	–	1.0	2.8	5.5	μA	3
Output Resistance							
CO pin resistance "H"	R_{COH}	–	5	10	20	kΩ	4
CO pin resistance "L"	R_{COL}	–	5	10	20	kΩ	4
DO pin resistance "H"	R_{DOH}	–	5	10	20	kΩ	4
DO pin resistance "L"	R_{DOL}	–	5	10	20	kΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	t_{CU} × 0.8	t_{CU}	t_{CU} × 1.2	–	5
Overdischarge detection delay time	t_{DL}	–	t_{DL} × 0.8	t_{DL}	t_{DL} × 1.2	–	5
Discharge overcurrent detection delay time	t_{DIOV}	–	t_{DIOV} × 0.8	t_{DIOV}	t_{DIOV} × 1.2	–	5
Load short-circuiting detection delay time	t_{SHORT}	–	t_{SHORT} × 0.8	t_{SHORT}	t_{SHORT} × 1.2	–	5
Charge overcurrent detection delay time	t_{CIOV}	–	t_{CIOV} × 0.8	t_{CIOV}	t_{CIOV} × 1.2	–	5
Discharge inhibition delay time	t_{CTL}	–	t_{CTL} × 0.8	t_{CTL}	t_{CTL} × 1.2	–	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

2. Ta = −40°C to +85°C*1

Table 10

(Ta = −40°C to +85°C*1 unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	–	$V_{CU} - 0.045$	V_{CU}	$V_{CU} + 0.030$	V	1
Overcharge release voltage	V_{CL}	$V_{CL} \neq V_{CU}$	$V_{CL} - 0.070$	V_{CL}	$V_{CL} + 0.040$	V	1
		$V_{CL} = V_{CU}$	$V_{CL} - 0.050$	V_{CL}	$V_{CL} + 0.030$	V	1
Overdischarge detection voltage	V_{DL}	–	$V_{DL} - 0.070$	V_{DL}	$V_{DL} + 0.045$	V	2
Overdischarge release voltage	V_{DU}	$V_{DL} \neq V_{DU}$	$V_{DU} - 0.090$	V_{DU}	$V_{DU} + 0.060$	V	2
		$V_{DL} = V_{DU}$	$V_{DU} - 0.070$	V_{DU}	$V_{DU} + 0.045$	V	2
Discharge overcurrent detection voltage	V_{DIOV}	–	$V_{DIOV} - 0.010$	V_{DIOV}	$V_{DIOV} + 0.010$	V	2
Load short-circuiting detection voltage	V_{SHORT}	–	0.40	0.50	0.60	V	2
Charge overcurrent detection voltage	V_{CIOV}	–	$V_{CIOV} - 0.015$	V_{CIOV}	$V_{CIOV} + 0.015$	V	2
0 V Battery Charge Function							
0 V battery charge starting charger voltage	V_{0CHA}	0 V battery charge function "available"	0.0	0.7	1.5	V	2
0 V battery charge inhibition battery voltage	V_{0INH}	0 V battery charge function "unavailable"	0.9	1.2	1.5	V	2
Internal Resistance							
Resistance between VM pin and VDD pin	R_{VMD}	–	78	300	1310	kΩ	3
Resistance between VM pin and VSS pin	R_{VMS}	–	7.2	20	44	kΩ	3
CTL pin internal resistance	R_{CTL}	–	$R_{CTL} \times 0.27$	R_{CTL}	$R_{CTL} \times 3.50$	MΩ	3
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP1}	–	1.5	–	6.5	V	–
Operation voltage between VDD pin and VM pin	V_{DSOP2}	–	1.5	–	28	V	–
CTL pin voltage "H"	V_{CTLH}	–	–	–	$V_{DD} \times 0.95$	V	2
CTL pin voltage "L"	V_{CTLL}	–	$V_{DD} \times 0.05$	–	–	V	2
Input Current							
Current consumption during operation	I_{OPE}	–	0.7	2.8	6.0	μA	3
Current consumption during power-down	I_{PDN}	–	–	–	0.15	μA	3
Current consumption during overdischarge	I_{OPED}	–	–	–	4.2	μA	3
Current consumption during discharge inhibition	I_{OPEC}	–	0.7	2.8	6.0	μA	3
Output Resistance							
CO pin resistance "H"	R_{COH}	–	2.4	10	30	kΩ	4
CO pin resistance "L"	R_{COL}	–	2.4	10	30	kΩ	4
DO pin resistance "H"	R_{DOH}	–	2.4	10	30	kΩ	4
DO pin resistance "L"	R_{DOL}	–	2.4	10	30	kΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.6$	t_{CU}	$t_{CU} \times 1.6$	–	5
Overdischarge detection delay time	t_{DL}	–	$t_{DL} \times 0.6$	t_{DL}	$t_{DL} \times 1.6$	–	5
Discharge overcurrent detection delay time	t_{DIOV}	–	$t_{DIOV} \times 0.6$	t_{DIOV}	$t_{DIOV} \times 1.6$	–	5
Load short-circuiting detection delay time	t_{SHORT}	–	$t_{SHORT} \times 0.6$	t_{SHORT}	$t_{SHORT} \times 1.6$	–	5
Charge overcurrent detection delay time	t_{CIOV}	–	$t_{CIOV} \times 0.6$	t_{CIOV}	$t_{CIOV} \times 1.6$	–	5
Discharge inhibition delay time	t_{CTL}	–	$t_{CTL} \times 0.6$	t_{CTL}	$t_{CTL} \times 1.6$	–	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

When CTL pin control logic is active "H", SW1 and SW3 are turned off, SW2 and SW4 are turned on. When CTL pin control logic is active "L", SW1 and SW3 are turned on, SW2 and SW4 are turned off.

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) and DO pin (V_{DO}) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to V_{VM} and the DO pin level with respect to V_{SS}.

1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

Overcharge detection voltage (V_{CU}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased from the starting condition of V1 = 3.4 V. Overcharge release voltage (V_{CL}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL}.

2. Overdischarge detection voltage, overdischarge release voltage (Test circuit 2)

Overdischarge detection voltage (V_{DL}) is defined as the voltage V1 at which V_{DO} goes from "H" to "L" when the voltage V1 is gradually decreased from the starting conditions of V1 = 3.4 V, V2 = V5 = 0 V. Overdischarge release voltage (V_{DU}) is defined as the voltage V1 at which V_{DO} goes from "L" to "H" when the voltage V1 is then gradually increased. Overdischarge hysteresis voltage (V_{HD}) is defined as the difference between V_{DU} and V_{DL}.

3. Discharge overcurrent detection voltage (Test circuit 2)

Discharge overcurrent detection voltage (V_{DIOV}) is defined as the voltage V2 whose delay time for changing V_{DO} from "H" to "L" is discharge overcurrent detection delay time (t_{DIOV}) when the voltage V2 is increased from the starting conditions of V1 = 3.4 V, V2 = V5 = 0 V.

4. Load short-circuiting detection voltage (Test circuit 2)

Load short-circuiting detection voltage (V_{SHORT}) is defined as the voltage V2 whose delay time for changing V_{DO} from "H" to "L" is load short-circuiting detection delay time (t_{SHORT}) when the voltage V2 is increased from the starting conditions of V1 = 3.4 V, V2 = V5 = 0 V.

5. Charge overcurrent detection voltage (Test circuit 2)

Charge overcurrent detection voltage (V_{CIOV}) is defined as the voltage V2 whose delay time for changing V_{CO} from "H" to "L" is charge overcurrent detection delay time (t_{CIOV}) when the voltage V2 is decreased from the starting conditions of V1 = 3.4 V, V2 = V5 = 0 V.

6. Current consumption during operation (Test circuit 3)

The current consumption during operation (I_{OPE}) is the current that flows through the VDD pin (I_{DD}) under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

7. Current consumption during power-down, current consumption during overdischarge (Test circuit 3)

7. 1 With power-down function

The current consumption during power-down (I_{PDN}) is I_{DD} under the set conditions of V1 = V2 = 1.5 V, V5 = 0 V.

7. 2 Without power-down function

The current consumption during overdischarge (I_{OPED}) is I_{DD} under the set conditions of V1 = V2 = 1.5 V, V5 = 0 V.

8. Current consumption during discharge inhibition (Test circuit 3)

8. 1 CTL pin control logic active "L" and CTL pin internal resistance connection "pull-up"

Current consumption during discharge inhibition (I_{OPEC}) is the difference of absolute value between I_{DD} and I_{CTL} under the set conditions of V1 = V2 = V5 = 3.4 V.

8. 2 Other function combinations

Current consumption during discharge inhibition (I_{OPEC}) is I_{DD} under the set conditions of V1 = V2 = V5 = 3.4 V.

9. Resistance between VM pin and VDD pin (Test circuit 3)

Resistance between VM pin and VDD pin is R_{VMD} under the set conditions of V1 = 1.8 V, V2 = V5 = 0 V.

10. Resistance between VM pin and VSS pin (Release condition of discharge overcurrent status "load disconnection") (Test circuit 3)

Resistance between VM pin and VSS pin is R_{VMS} under the set conditions of V1 = 3.4 V, V2 = 1.0 V, V5 = 0 V.

11. CTL pin internal resistance (Test circuit 3)

11. 1 CTL pin control logic active "H" and CTL pin internal resistance connection "pull-down"

Resistance between CTL pin and VSS pin is R_{CTL} under the set conditions of V1 = V5 = 3.4 V, V2 = 0 V.

11. 2 CTL pin control logic active "L" and CTL pin internal resistance connection "pull-up"

Resistance between CTL pin and VDD pin is R_{CTL} under the set conditions of V1 = V5 = 3.4 V, V2 = 0 V.

11. 3 CTL pin control logic active "L" and CTL pin internal resistance connection "pull-down"

Resistance between CTL pin and VSS pin is R_{CTL} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

12. CO pin resistance "H" (Test circuit 4)

The CO pin resistance "H" (R_{COH}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 3.4 V, V2 = 0 V, V3 = 3.0 V.

13. CO pin resistance "L" (Test Circuit 4)

The CO pin resistance "L" (R_{COL}) is the resistance between VM pin and CO pin under the set conditions of V1 = 4.6 V, V2 = 0 V, V3 = 0.4 V.

14. DO pin resistance "H" (Test circuit 4)

The DO pin resistance "H" (R_{DOH}) is the resistance between VDD pin and DO pin under the set conditions of V1 = 3.4 V, V2 = 0 V, V4 = 3.0 V.

15. DO pin resistance "L" (Test circuit 4)

The DO pin resistance "L" (R_{DOL}) is the resistance between VSS pin and DO pin under the set conditions of V1 = 1.8 V, V2 = 0 V, V4 = 0.4 V.

16. CTL pin voltage "H", CTL pin voltage "L" (Test circuit 2)

16. 1 CTL pin control logic active "H"

The CTL pin voltage "H" (V_{CTLH}) is defined as the voltage V5 at which V_{DO} goes from "H" to "L" when the voltage V5 is gradually increased under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V. After that, the CTL pin voltage "L" (V_{CTLL}) is defined as the voltage V5 at which V_{DO} goes from "L" to "H" after V5 is gradually decreased.

16. 2 CTL pin control logic active "L"

The CTL pin voltage "L" (V_{CTLL}) is defined as the voltage difference between the voltage V5 and the voltage V1 (V1 − V5) at which V_{DO} goes from "H" to "L" when the voltage V5 is gradually increased under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V. After that, the CTL pin voltage "H" (V_{CTLH}) is defined as the voltage difference between V1 − V5 at which V_{DO} goes from "L" to "H" after V5 is gradually decreased.

17. Overcharge detection delay time (Test circuit 5)

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to go to "L" after the voltage V1 increases and exceeds V_{CU} under the set condition of V1 = 3.4 V, V2 = V5 = 0 V.

18. Overdischarge detection delay time (Test circuit 5)

The overdischarge detection delay time (t_{DL}) is the time needed for V_{DO} to go to "L" after the voltage V1 decreases and falls below V_{DL} under the set condition of V1 = 3.4 V, V2 = V5 = 0 V.

19. Discharge overcurrent detection delay time (Test circuit 5)

t_{DIOV} is the time needed for V_{DO} to go to "L" after the voltage V2 increases and exceeds V_{DIOV} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

20. Load short-circuiting detection delay time (Test circuit 5)

t_{SHORT} is the time needed for V_{DO} to go to "L" after the voltage V2 increases and exceeds V_{SHORT} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

21. Charge overcurrent detection delay time (Test circuit 5)

t_{CIOV} is the time needed for V_{CO} to go to "L" after the voltage V2 decreases and falls below V_{CIOV} under the set condition of V1 = 3.4 V, V2 = V5 = 0 V.

22. Discharge inhibition delay time (Test circuit 5)

22. 1 CTL pin control logic active "H"

Discharge inhibition delay time (t_{CTL}) is the time needed for V_{DO} to go to "L" after the voltage V5 increases and exceeds V_{CTLH} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

22. 2 CTL pin control logic active "L"

Discharge inhibition delay time (t_{CTL}) is the time needed for V_{DO} to go to "L" after the voltage V5 increases and V1 − V5 falls below V_{CTLL} under the set conditions of V1 = 3.4 V, V2 = V5 = 0 V.

23. 0 V battery charge starting charger voltage (0 V battery charge function "available") (Test circuit 2)

The 0 V battery charge starting charger voltage (V_{0CHA}) is defined as absolute value of the voltage V2 at which V_{CO} goes to "H" (V_{CO} = V_{DD}) when the voltage V2 is gradually decreased under the set condition of V1 = V2 = V5 = 0 V.

24. 0 V battery charge inhibition battery voltage (0 V battery charge function "unavailable") (Test circuit 2)

The 0 V battery charge inhibition battery voltage (V_{0INH}) is defined as the voltage V1 at which V_{CO} goes to "H" (V_{CO} = V_{DD}) when the voltage V1 is gradually increased under the set condition of V1 = V5 = 0 V, V2 = –4.0 V.

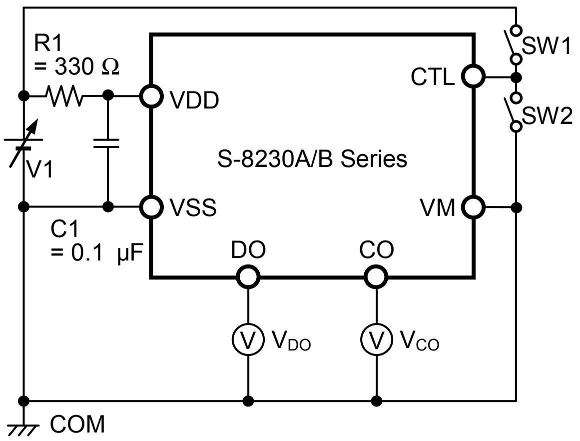


Figure 4 Test Circuit 1

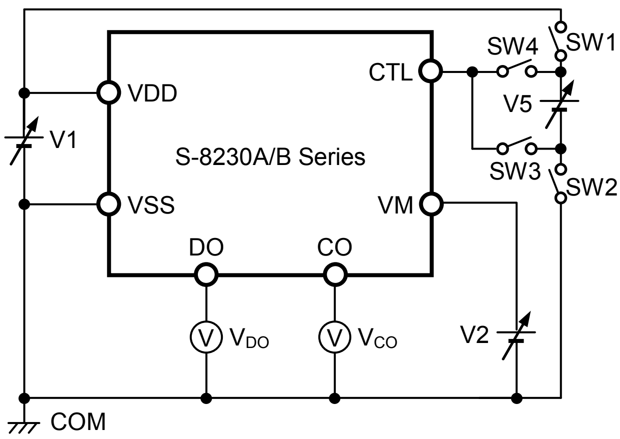


Figure 5 Test Circuit 2

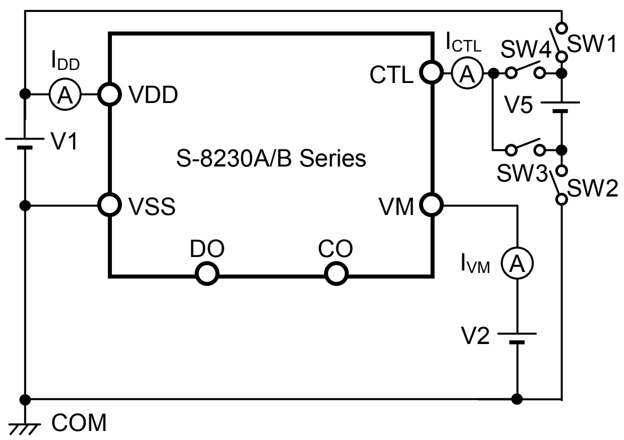


Figure 6 Test Circuit 3

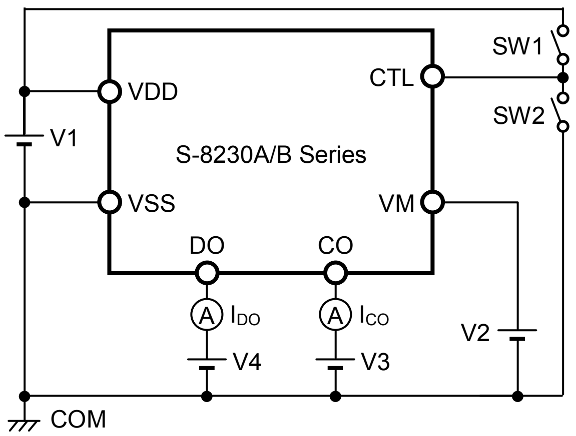


Figure 7 Test Circuit 4

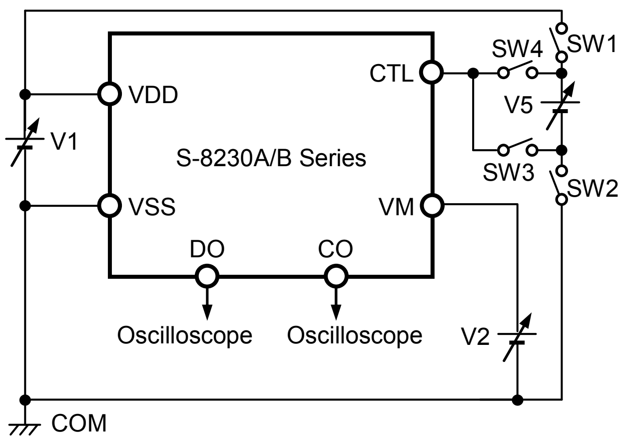


Figure 8 Test Circuit 5

■ Operation

Remark Refer to "**■ Battery Protection IC Connection Example**".

1. Normal status

The S-8230A/B Series monitors the voltage of the battery connected between the VDD pin and VSS pin, the voltage between the VM pin and VSS pin and the voltage between the CTL pin and VSS pin to control charging and discharging.

1. 1 CTL pin control logic active "H"

When the battery voltage is in the range from the overdischarge detection voltage (V_{DL}) to the overcharge detection voltage (V_{CU}), and the VM pin voltage is in the range from the charge overcurrent detection voltage (V_{CIOV}) to the discharge overcurrent detection voltage (V_{DIOV}), the S-8230A/B Series turns both the charge and discharge control FETs on if the CTL pin voltage is equal to or lower than the CTL pin voltage "L" (V_{CTLL}). This condition is called the normal status, and in this condition charging and discharging can be carried out freely.
The resistance between the VM pin and VDD pin (R_{VMD}) and the resistance between the VM pin and VSS pin (R_{VMS}) are not connected in the normal status.

1. 2 CTL pin control logic active "L"

When the battery voltage is in the range from the overdischarge detection voltage (V_{DL}) to the overcharge detection voltage (V_{CU}), and the VM pin voltage is in the range from the charge overcurrent detection voltage (V_{CIOV}) to the discharge overcurrent detection voltage (V_{DIOV}), the S-8230A/B Series turns both the charge and discharge control FETs on if the CTL pin voltage is equal to or higher than the CTL pin voltage "H" (V_{CTLH}). This condition is called the normal status, and in this condition charging and discharging can be carried out freely.
The resistance between the VM pin and VDD pin (R_{VMD}) and the resistance between the VM pin and VSS pin (R_{VMS}) are not connected in the normal status.

Caution When the battery is connected for the first time, the S-8230A/B Series may not be in the normal status. In this case, short the VM pin and VSS pin, or set the VM pin voltage at the level of V_{CIOV} or more and at the level of V_{DIOV} or less by connecting the charger. The S-8230A/B Series then becomes the normal status.

2. Overcharge status

2. 1 $V_{CL} \neq V_{CU}$ (Product in which overcharge release voltage differs from overcharge detection voltage)

When the battery voltage becomes higher than V_{CU} during charging in the normal status and detection continues for the overcharge detection delay time (t_{CU}) or longer, the S-8230A/B Series turns the charge control FET off to stop charging. This condition is called the overcharge status.
R_{VMD} and R_{VMS} are not connected in the overcharge status.
The overcharge status is released in the following two cases.

(1) In the case that the VM pin voltage is lower than V_{DIOV}, the S-8230A/B Series releases the overcharge status when the battery voltage falls below overcharge release voltage (V_{CL}).
(2) In the case that the VM pin voltage is equal to or higher than V_{DIOV}, the S-8230A/B Series releases the overcharge status when the battery voltage falls below V_{CU}.

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the V_f voltage of the parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or higher than V_{DIOV}, the S-8230A/B Series releases the overcharge status when the battery voltage is equal to or lower than V_{CU}.

Caution If the battery is charged to a voltage higher than V_{CU} and the battery voltage does not fall below V_{CU} even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below V_{CU}. Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.

2. 2 V_{CL} = V_{CU} (Product in which overcharge release voltage is the same as overcharge detection voltage)

When the battery voltage becomes higher than V_{CU} during charging in the normal status and detection continues for the overcharge detection delay time (t_{CU}) or longer, the S-8230A/B Series turns the charge control FET off to stop charging. This condition is called the overcharge status.
R_{VMD} and R_{VMS} are not connected in the overcharge status.
The overcharge status is released in the following two cases.

(1) In the case that the VM pin voltage is equal to or higher than V_{CIOV}, and is lower than V_{DIOV}, the S-8230A/B Series releases the overcharge status when the battery voltage falls below overcharge release voltage (V_{CL}).
(2) In the case that the VM pin voltage is equal to or higher than V_{DIOV}, the S-8230A/B Series releases the overcharge status when the battery voltage falls below V_{CU}.

The discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises more than the VSS pin voltage due to the V_f voltage of the parasitic diode, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is equal to or higher than V_{DIOV}, the S-8230A/B Series releases the overcharge status when the battery voltage is equal to or lower than V_{CU}.

Caution 1. If the battery is charged to a voltage higher than V_{CU} and the battery voltage does not fall below V_{CU} even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below V_{CU}. Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.
2. When a charger is connected after overcharge detection, the overcharge status is not released even if the battery voltage is below V_{CL}. The overcharge status is released when the VM pin voltage goes over V_{CIOV} by removing the charger.

3. Overdischarge status

When the battery voltage falls below V_{DL} during discharging in the normal status and the detection continues for the overdischarge detection delay time (t_{DL}) or longer, the S-8230A/B Series turns the discharge control FET off to stop discharging. This condition is called the overdischarge status.
In the overdischarge status, the VM pin and VDD pin are shorted by R_{VMD} in the S-8230A/B Series. The VM pin voltage is pulled up by R_{VMD}.
When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is lower than −0.7 V typ., the S-8230A/B Series releases the overdischarge status when the battery voltage reaches V_{DL} or higher.
When VM pin voltage is not lower than −0.7 V typ., the S-8230A/B Series releases the overdischarge status when the battery voltage reaches overdischarge release voltage (V_{DU}) or higher.
R_{VMS} is not connected in the overdischarge status.

3. 1 With power-down function

Under the overdischarge status, when voltage between the VDD pin and VM pin is 0.8 V typ. or lower, the power-down function works and the current consumption is reduced to the current consumption during power-down (I_{PDN}). By connecting a charger, the power-down function is released when the VM pin voltage is 0.7 V typ. or lower.

4. Discharge overcurrent status (Discharge overcurrent, load short-circuiting)

When a battery in the normal status is in the status where the VM pin voltage is equal to or higher than V_{DIOV} because the discharge current is equal to or higher than the specified value and the status lasts for the discharge overcurrent detection delay time (t_{DIOV}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.

4. 1 Release condition of discharge overcurrent status "load disconnection"

In the discharge overcurrent status, the VM pin and VSS pin are shorted by R_{VMS} in the S-8230A/B Series. However, the VM pin voltage is the VDD pin voltage due to the load as long as the load is connected. When the load is disconnected, the VM pin voltage returns to the VSS pin voltage. If the VM pin voltage returns to V_{DIOV} or lower, the S-8230A/B Series releases the discharge overcurrent status.
R_{VMD} is not connected in the discharge overcurrent status.

4. 2 Release condition of discharge overcurrent status "charger connection"

In the discharge overcurrent status, the VM pin and VDD pin are shorted by R_{VMD} in the S-8230A/B Series.
If the VM pin voltage returns to V_{DIOV} or lower by connecting a battery charger, the S-8230A/B Series releases the discharge overcurrent status.
R_{VMS} is not connected in the discharge overcurrent status.

5. Charge overcurrent status

When a battery in the normal status is in the status where the VM pin voltage is equal to or lower than V_{CIOV} because the charge current is equal to or higher than the specified value and the status lasts for the charge overcurrent detection delay time (t_{CIOV}) or longer, the charge control FET is turned off and charging is stopped. This status is called the charge overcurrent status.
The S-8230A/B Series releases the charge overcurrent status when the VM pin voltage returns to V_{CIOV} or higher by removing the charger.
The charge overcurrent detection does not function in the overdischarge status and the discharge inhibition status.
R_{VMD} and R_{VMS} are not connected in the charge overcurrent status.

6. Discharge inhibition status

6. 1 CTL pin control logic active "H"

When a battery in the normal status is in the status where CTL pin voltage is equal to or higher than CTL pin voltage "H" (V_{CTLH}) and the status lasts for discharge inhibition delay time (t_{CTL}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge inhibition status.

6. 1. 1 Discharge inhibition status latch function "available"

If CTL pin voltage is equal to or lower than CTL pin voltage "L" (V_{CTLL}), the S-8230A/B Series releases discharge inhibition status when the VM pin voltage becomes equal to or lower than V_{DIOV} by connecting a charger.

6. 1. 2 Discharge inhibition status latch function "unavailable"

The S-8230A/B Series releases discharge inhibition status when the CTL pin voltage becomes equal to or lower than V_{CTLL}.

6. 2 CTL pin control logic active "L"

When a battery in the normal status is in the status where CTL pin voltage is equal to or lower than CTL pin voltage "L" (V_{CTLL}) and the status lasts for discharge inhibition delay time (t_{CTL}) or longer, the discharge control FET is turned off and discharging is stopped. This status is called the discharge inhibition status.

6. 2. 1 Discharge inhibition status latch function "available"

If CTL pin voltage is equal to or higher than CTL pin voltage "H" (V_{CTLH}), the S-8230A/B Series releases discharge inhibition status when the VM pin voltage becomes equal to or lower than V_{DIOV} by connecting a charger.

6. 2. 2 Discharge inhibition status latch function "unavailable"

The S-8230A/B Series releases discharge inhibition status when the CTL pin voltage becomes equal to or higher than V_{CTLH}.

In discharge inhibition status, if the battery voltage exceeds V_{CU} by connecting a charger, the S-8230A/B Series releases discharge inhibition status.
The CTL pin is shorted to the VDD pin or VSS pin by the CTL pin internal resistance (R_{CTL}) in the S-8230A/B Series. When the voltage between the VDD pin and VM pin is 0.8 V typ. or lower in the overdischarge status, R_{CTL} is disconnected and the input and output current to the CTL pin is cut off.
The discharge control by the CTL pin does not function in the overcharge status and the charge overcurrent status.
In the discharge inhibition status, the VM pin and VDD pin are shorted by R_{VMD} in the S-8230A/B Series.

7. 0 V battery charge function "available"

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage (V_{0CHA}) or a higher voltage is applied between the EB+ pin and EB− pin by connecting a charger, the charge control FET gate is fixed to the VDD pin voltage. When the voltage between the gate and source of the charge control FET becomes equal to or higher than the threshold voltage due to the charger voltage, the charge control FET is turned on to start charging. At this time, the discharge control FET is off and the charge current flows through the internal parasitic diode in the discharge control FET. When the battery voltage becomes equal to or higher than V_{DU}, the S-8230A/B Series enters the normal status.

Caution 1. Some battery providers do not recommend charging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge function.
2. The 0 V battery charge function has higher priority than the charge overcurrent detection function. Consequently, a product in which use of the 0 V battery charge function is enabled charges a battery forcibly and the charge overcurrent cannot be detected when the battery voltage is lower than V_{DL}.

8. 0 V battery charge function "unavailable"

This function inhibits recharging when a battery that is internally short-circuited (0 V battery) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage (V_{0INH}) or lower, the charge control FET gate is fixed to the EB– pin voltage to inhibit charging. When the battery voltage is V_{0INH} or higher, charging can be performed.

Caution Some battery providers do not recommend charging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge function.

9. Delay circuit

The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

Remark t_{DIOV} and t_{SHORT} start when V_{DIOV} is detected. When V_{SHORT} is detected over t_{SHORT} after V_{DIOV}, the S-8230A/B Series turns the discharge control FET off within t_{SHORT} from the time of detecting V_{SHORT}.

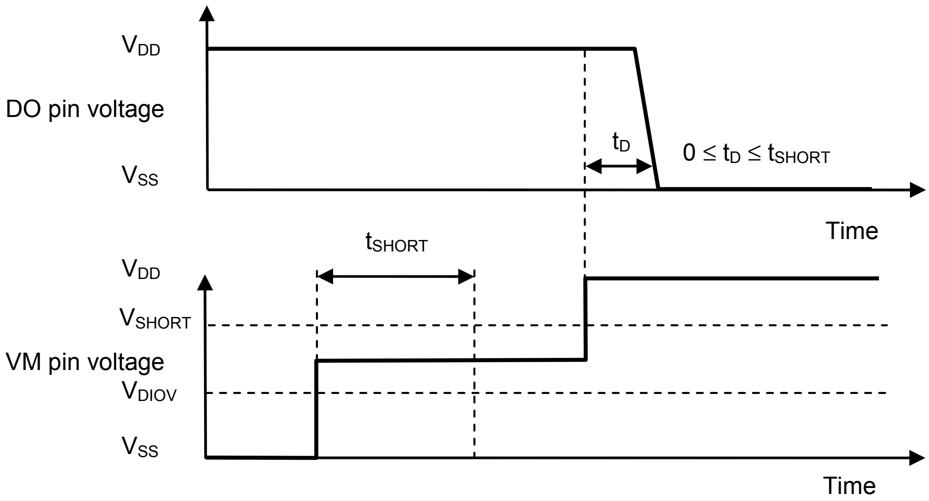
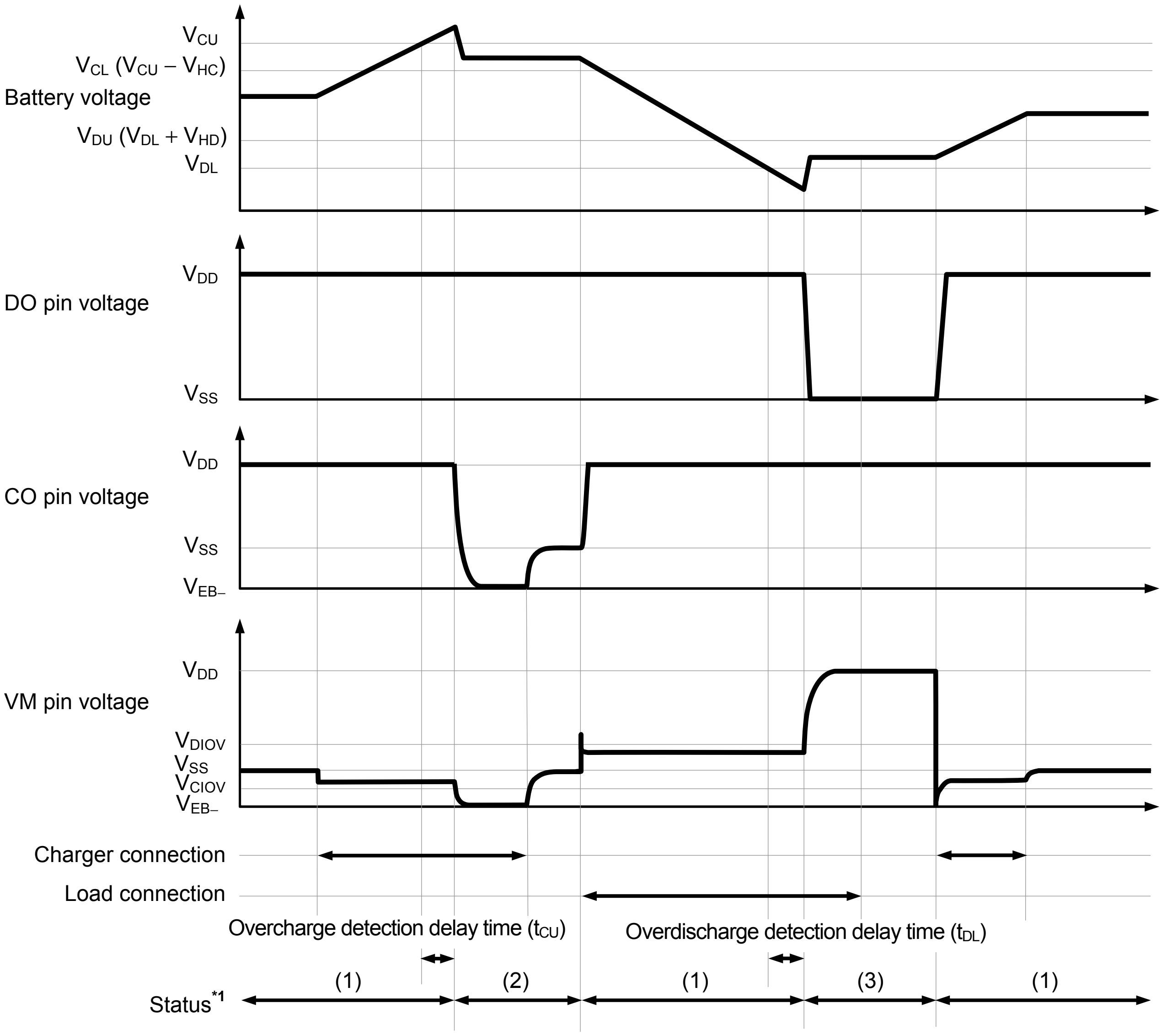


Figure 9

■ Timing Chart

1. Overcharge detection, overdischarge detection



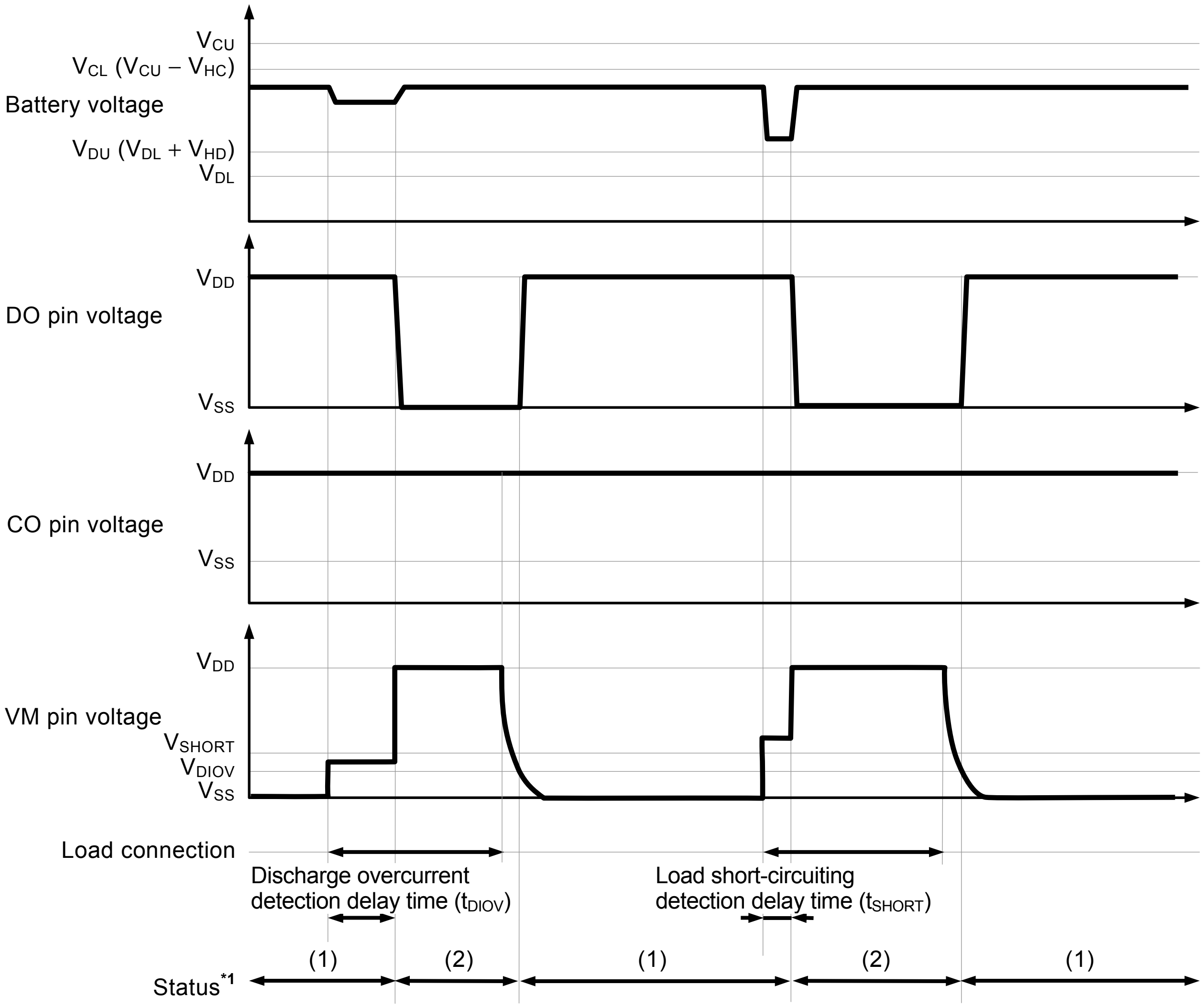
***1.** (1): Normal status
(2): Overcharge status
(3): Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 10

2. Discharge overcurrent detection

2. 1 Release condition of discharge overcurrent status "load disconnection"

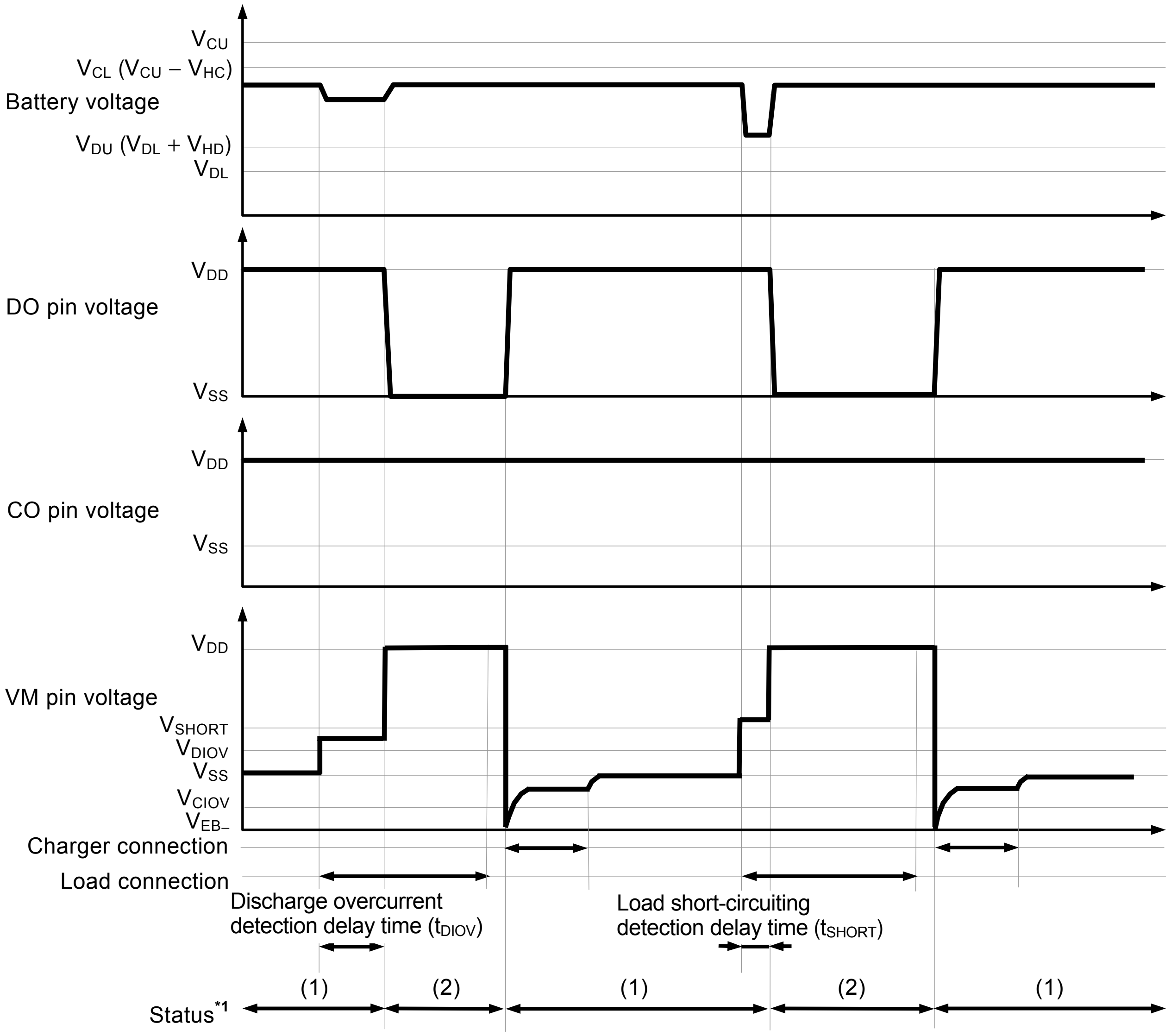


***1.** (1): Normal status
(2): Discharge overcurrent status

Remark The charger is assumed to charge with a constant current.

Figure 11

2. 2 Release condition of discharge overcurrent status "charger connection"

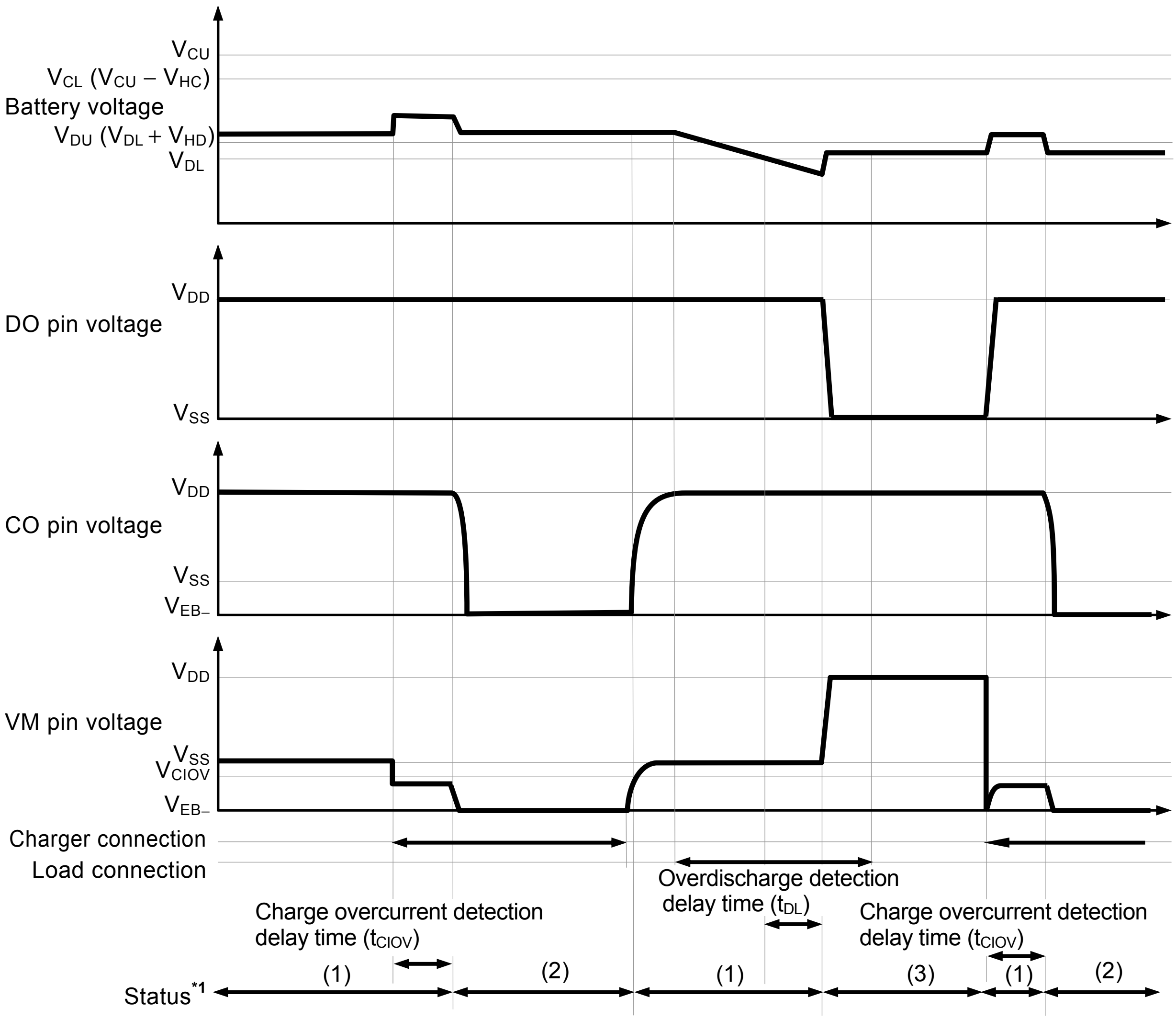


***1.** (1): Normal status
(2): Discharge overcurrent status

Remark The charger is assumed to charge with a constant current.

Figure 12

3. Charge overcurrent detection



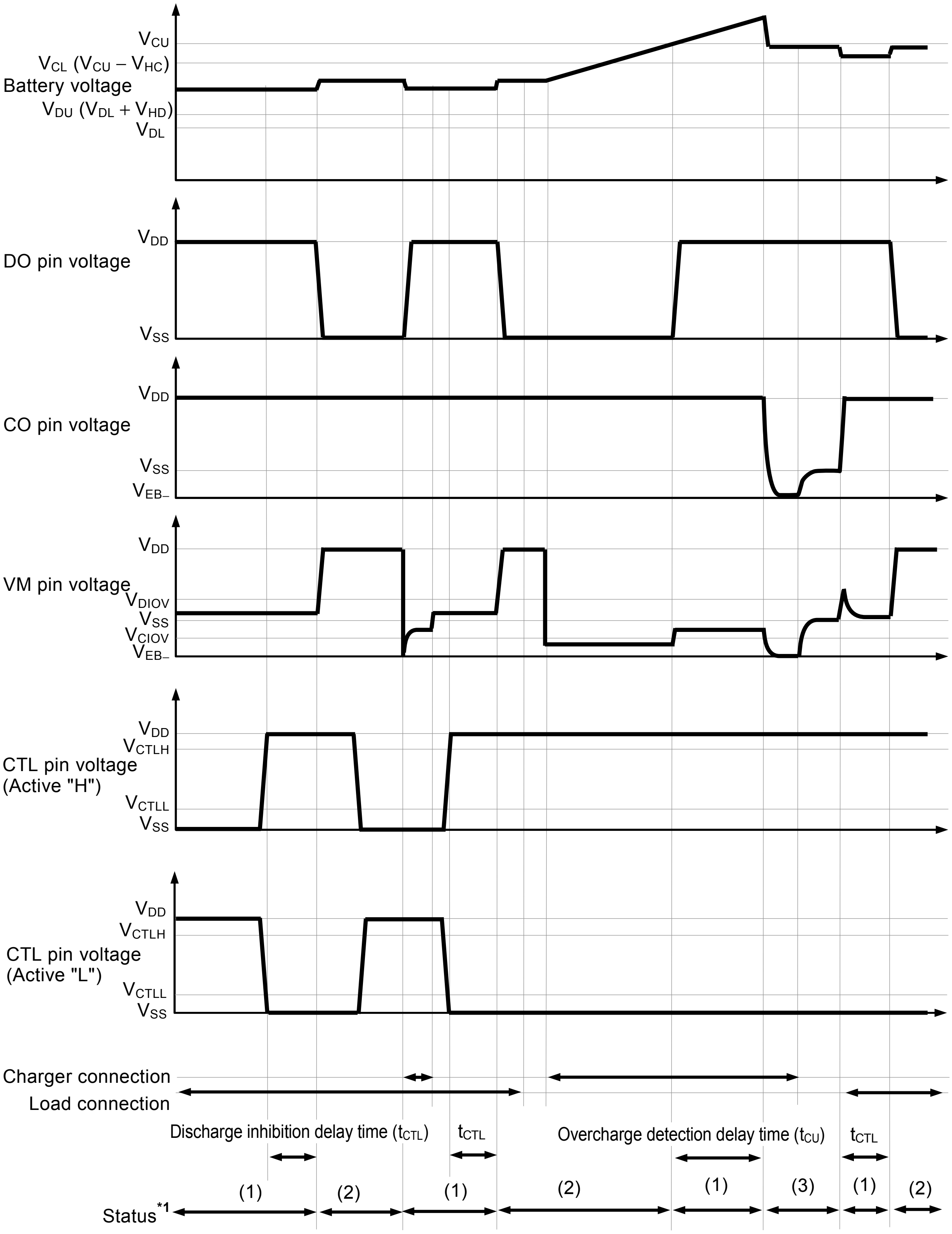
***1.** (1): Normal status
(2): Charge overcurrent status
(3): Overdischarge status

Remark The charger is assumed to charge with a constant current.

Figure 13

4. Discharge inhibition operation

4. 1 Discharge inhibition status latch function "available"

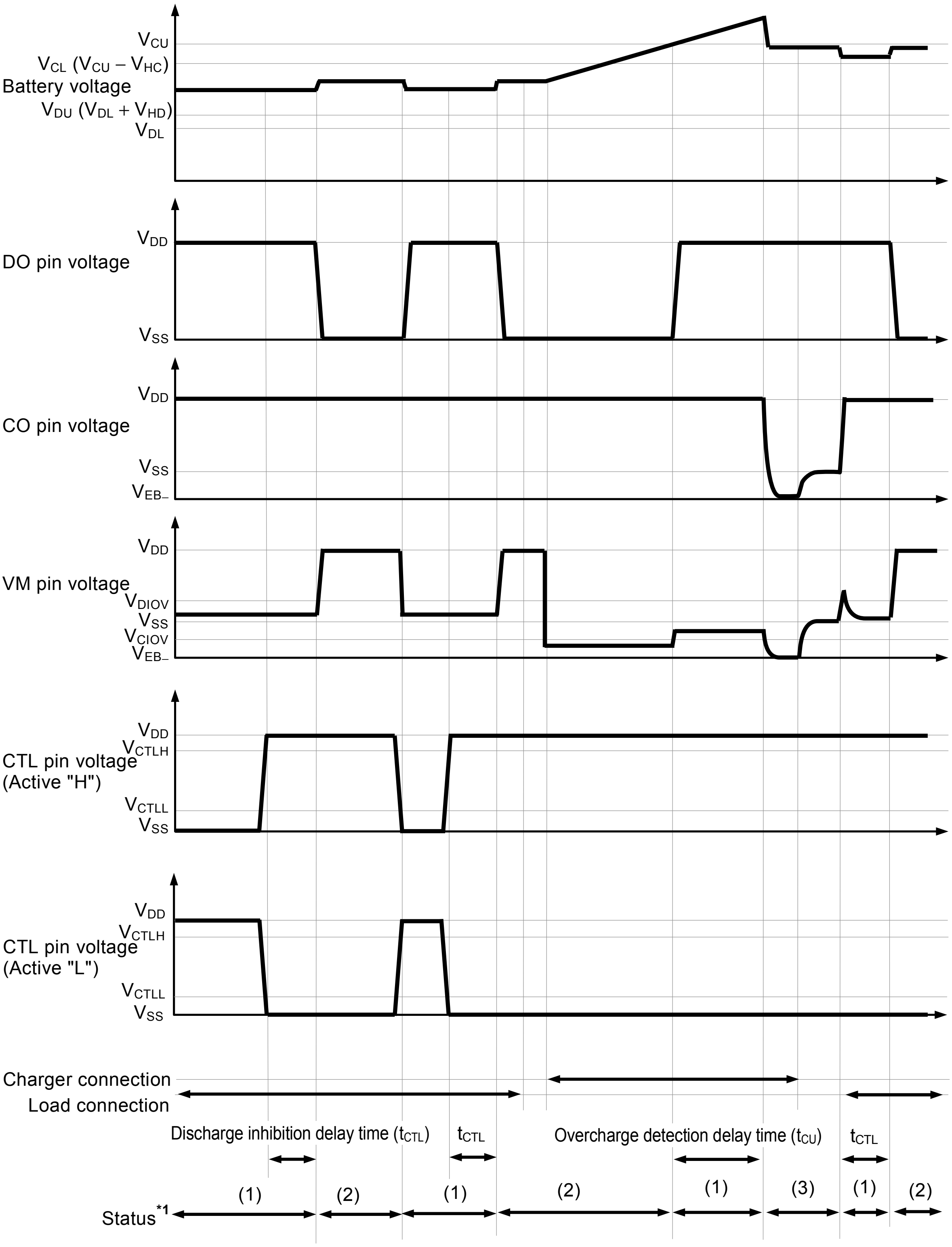


***1.** (1): Normal status
(2): Discharge inhibition status
(3): Overcharge status

Remark The charger is assumed to charge with a constant current.

Figure 14

4. 2 Discharge inhibition status latch function "unavailable"



***1.** (1): Normal status
(2): Discharge inhibition status
(3): Overcharge status

Remark The charger is assumed to charge with a constant current.

Figure 15