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S-8233A Series

BATTERY PROTECTION IC FOR 3-SERIAL-CELL PACK

www.sii-ic.com

The S-8233A Series is a series of lithium-ion rechargeable battery protection ICs incorporating high-accuracy voltage detection circuits and delay circuits. It is suitable for a 3-serial-cell lithium-ion rechargeable battery pack.

■ Features

(1) Internal high-accuracy voltage detection circuit
- Overcharge detection voltage: 4.10 ± 0.05 V to 4.35 ± 0.05 V, 50 mV- step
- Overcharge release voltage: 3.85 ± 0.10 V to 4.35 ± 0.10 V, 50 mV- step

  (The overcharge release voltage can be selected within the range where a difference from overcharge detection voltage is 0 V to 0.3 V)
- Overdischarge detection voltage: 2.00 ± 0.08 V to 2.70 ± 0.08 V, 100 mV- step
- Overdischarge release voltage: 2.00 ± 0.10 V to 3.70 ± 0.10 V, 100 mV - step

  (The overdischarge release voltage can be selected within the range where a difference from overdischarge detection voltage is 0 V to 1.0 V)
- Overcurrent detection voltage 1: 0.15 ± 0.015 V to 0.50 ± 0.05 V, 50 mV-step

(2) High-withstand voltage device (absolute maximum rating: 26 V)
(3) Wide operating voltage range: 2 V to 24 V
(4) The delay time for every detection can be set via an external capacitor.
(5) Three overcurrent detection levels (protection for short-circuiting)
(6) Internal charge/discharge prohibition circuit via the control pin
(7) The function for charging batteries from 0 V is available.
(8) Low current consumption
- Operation: 50 µA max. (+25 °C)
- Power-down: 0.1 µA max. (+25 °C)

(9) Lead-free, Sn 100%, halogen-free*1

***1.** Refer to "■ **Product Name Structure**" for details.

■ Applications

- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

■ Package

- 16-Pin TSSOP

■ Block Diagram

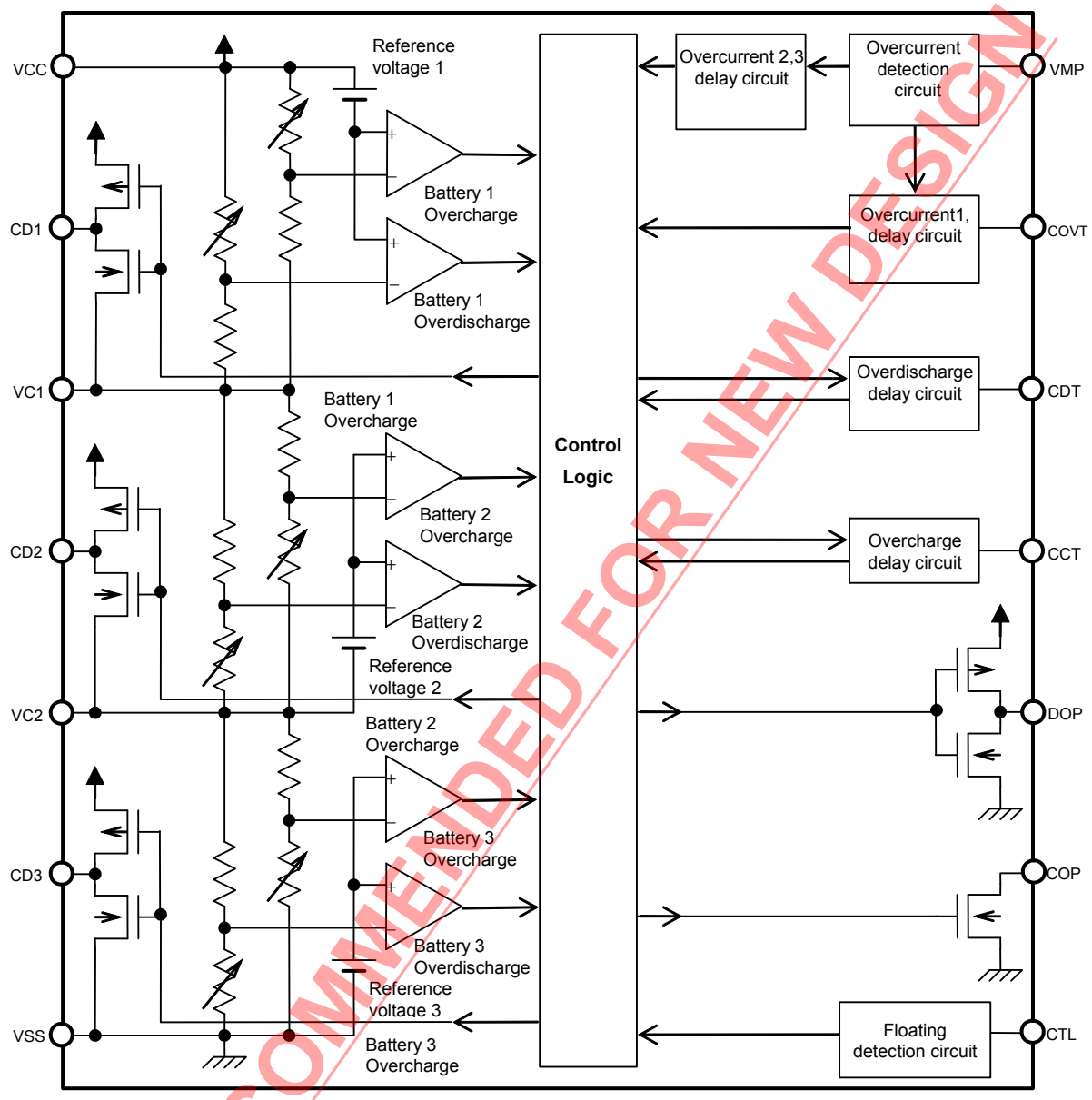
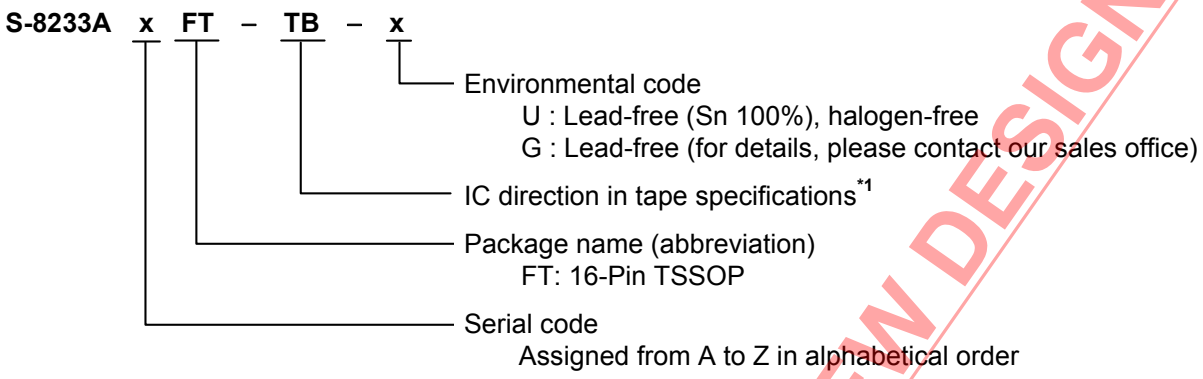


Figure 1

Remark The delay time for overcurrent detection 2 and 3 is fixed by an internal IC circuit. The delay time cannot be changed via an external capacitor.

■ Product Name Structure

1. Product name



***1.** Refer to the tape specifications.

2. Package

Package Name	Drawing Code		
	Package	Tape	Reel
16-Pin TSSOP	FT016-A-P-SD	FT016-A-C-SD	FT016-A-R-SD

3. Product name list

Table 1

Product name / Item	Overcharge detection voltage V_{Cu}	Overcharge release voltage V_{CD}	Overdischarge detection voltage V_{DD}	Overdischarge release voltage V_{DU}	Overcurrent detection voltage1 V_{IOV1}	0 V battery charge function	Conditioning function
S-8233ACFT-TB-x	4.25 V	4.05 V	2.00 V	2.30 V	0.20 V	–	Available
S-8233ADFT-TB-x	4.10 V	4.10 V	2.00 V	2.30 V	0.20 V	–	Unavailable
S-8233AEFT-TB-x	4.25 V	4.10 V	2.30 V	2.70 V	0.15 V	–	Available
S-8233AFFT-TB-x	4.35 V	4.05 V	2.40 V	2.70 V	0.50 V	Available	Available
S-8233AGFT-TB-x	4.25 V	4.05 V	2.40 V	2.70 V	0.40 V	Available	Available
S-8233AIFT-TB-x	4.25 V	4.10 V	2.30 V	3.00 V	0.15 V	–	Available
S-8233AJFT-TB-x	4.35 V	4.05 V	2.40 V	2.70 V	0.30 V	–	Available
S-8233AKFT-TB-x	4.35 V	4.05 V	2.40 V	2.70 V	0.15 V	–	Available
S-8233ALFT-TB-x	4.35 V	4.05 V	2.40 V	2.70 V	0.40 V	Available	Available
S-8233AMFT-TB-x	4.35 V	4.05 V	2.40 V	2.70 V	0.30 V	Available	Available
S-8233ANFT-TB-x	4.35 V	4.05 V	2.40 V	2.40 V	0.15 V	Available	Available
S-8233AOFT-TB-x	4.35 V	4.05 V	2.40 V	2.70 V	0.15 V	Available	Available
S-8233APFT-TB-x	4.25 V	4.05 V	2.70 V	3.00 V	0.30 V	Available	Available
S-8233ARFT-TB-x	4.35 V	4.05 V	2.00 V	2.70 V	0.30 V	Available	Available
S-8233ASFT-TB-x	4.25 V	4.05 V	2.40 V	2.70 V	0.50 V	Available	Available

Remark 1. Please contact our sales office for the products with the detection voltage value other than those specified above.
2. x: G or U
3. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ Pin Configuration

16-Pin TSSOP
Top view

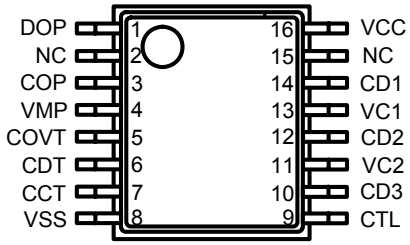


Figure 2

Table 2

Pin No.	Symbol	Description
1	DOP	Connects FET gate for discharge control (CMOS output)
2	NC	No connection*1
3	COP	Connects FET gate for charge control (Nch open-drain output)
4	VMP	Detects voltage between VCC to VMP(Overcurrent detection pin)
5	COVT	Connects capacitor for overcurrent detection1 delay circuit
6	CDT	Connects capacitor for overdischarge detection delay circuit
7	CCT	Connects capacitor for overcharge detection delay circuit
8	VSS	Negative power input, and connects negative voltage for battery 3
9	CTL	Charge/discharge control signal input
10	CD3	Battery 3 conditioning signal output
11	VC2	Connects battery 2 negative voltage and battery 3 positive voltage
12	CD2	Battery 2 conditioning signal output
13	VC1	Connects battery 1 negative voltage and battery 2 positive voltage
14	CD1	Battery 1 conditioning signal output
15	NC	No connection*1
16	VCC	Positive power input and connects battery 1 positive voltage

***1.** The NC pin is electrically open. The NC pin can be connected to VCC or VSS.

■ Absolute Maximum Ratings

Table 3

(Ta = 25°C unless otherwise specified)

Item	Symbol	Applied Pin	Absolute Maximum Ratings	Unit
Input voltage between VCC and VSS	V_{DS}	–	V_{SS}–0.3 ~ V_{SS}+26	V
Input pin voltage	V_{IN}	VC1, VC2, CTL, CCT, CDT, COVT	V_{SS}–0.3 ~ V_{CC}+0.3	V
VMP Input pin voltage	V_{VMP}	VMP	V_{SS}–0.3 ~ V_{SS}+26	V
CD1 output pin voltage	V_{CD1}	CD1	V_{C1}–0.3 ~ V_{CC}+0.3	V
CD2 output pin voltage	V_{CD2}	CD2	V_{C2}–0.3 ~ V_{CC}+0.3	V
CD3 output pin voltage	V_{CD3}	CD3	V_{SS}–0.3 ~ V_{CC}+0.3	V
DOP output pin voltage	V_{DOP}	DOP	V_{SS}–0.3 ~ V_{CC}+0.3	V
COP output pin voltage	V_{COP}	COP	V_{SS}–0.3 ~ V_{SS}+26	V
Power dissipation	P_D	–	300 (When not mounted on board)	mW
		–	1100*1	mW
Operating ambient temperature	T_{opr}	–	–20 ~ +70	°C
Storage temperature	T_{stg}	–	–40 ~ +125	°C

***1.** When mounted on board
[Mounted board]
(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

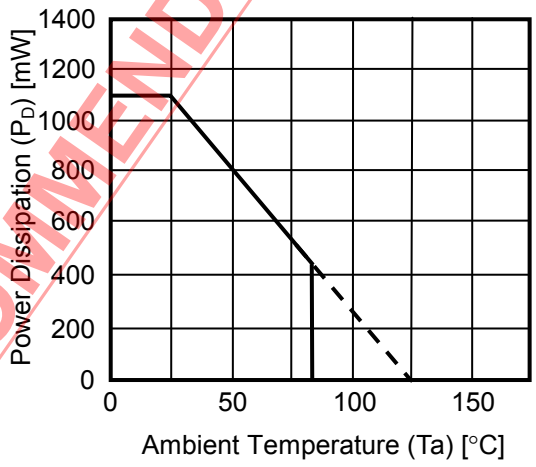


Figure 3 Power Dissipation of Package (When Mounted on Board)

■ Electrical Characteristics

Table 4 (1 / 2)

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
Detection voltage								
Overcharge detection voltage 1	V_{CU1}	4.10 to 4.35 Adjustment	V_{CU1}–0.05	V_{CU1}	V_{CU1}+0.05	V	1	1
Overcharge release voltage 1	V_{CD1}	3.85 to 4.35 Adjustment	V_{CD1}–0.10	V_{CD1}	V_{CD1}+0.10	V	1	1
Overdischarge detection voltage 1	V_{DD1}	2.00 to 2.70 Adjustment	V_{DD1}–0.08	V_{DD1}	V_{DD1}+0.08	V	1	1
Overdischarge release voltage 1	V_{DU1}	2.00 to 3.70 Adjustment	V_{DU1}–0.10	V_{DU1}	V_{DU1}+0.10	V	1	1
Overcharge detection voltage 2	V_{CU2}	4.10 to 4.35 Adjustment	V_{CU2}–0.05	V_{CU2}	V_{CU2}+0.05	V	2	1
Overcharge release voltage 2	V_{CD2}	3.85 to 4.35 Adjustment	V_{CD2}–0.10	V_{CD2}	V_{CD2}+0.10	V	2	1
Overdischarge detection voltage 2	V_{DD2}	2.00 to 2.70 Adjustment	V_{DD2}–0.08	V_{DD2}	V_{DD2}+0.08	V	2	1
Overdischarge release voltage 2	V_{DU2}	2.00 to 3.70 Adjustment	V_{DU2}–0.10	V_{DU2}	V_{DU2}+0.10	V	2	1
Overcharge detection voltage 3	V_{CU3}	4.10 to 4.35 Adjustment	V_{CU3}–0.05	V_{CU3}	V_{CU3}+0.05	V	3	1
Overcharge release voltage 3	V_{CD3}	3.85 to 4.35 Adjustment	V_{CD3}–0.10	V_{CD3}	V_{CD3}+0.10	V	3	1
Overdischarge detection voltage 3	V_{DD3}	2.00 to 2.70 Adjustment	V_{DD3}–0.08	V_{DD3}	V_{DD3}+0.08	V	3	1
Overdischarge release voltage 3	V_{DU3}	2.00 to 3.70 Adjustment	V_{DU3}–0.10	V_{DU3}	V_{DU3}+0.10	V	3	1
Overcurrent detection voltage 1 *1	V_{IOV1}	0.15 to 0.50V Adjustment	V_{IOV1} x 0.9	V_{IOV1}	V_{IOV1} x 1.1	V	4	2
Overcurrent detection voltage 2	V_{IOV2}	V_{CC} Reference	0.54	0.6	0.66	V	4	2
Overcurrent detection voltage 3	V_{IOV3}	V_{SS} Reference	1.0	2.0	3.0	V	4	2
Voltage temperature factor 1 *2	T_{COE1}	Ta = -20 to 70°C *4	–1.0	0	1.0	mV/°C	–	–
Voltage temperature factor 2 *3	T_{COE2}	Ta = -20 to 70°C *4	–0.5	0	0.5	mV/°C	–	–
Delay time								
Overcharge detection delay time 1	t_{CU1}	C_{CCT} = 0.47 µF	0.5	1.0	1.5	s	9	6
Overcharge detection delay time 2	t_{CU2}	C_{CCT} = 0.47 µF	0.5	1.0	1.5	s	10	6
Overcharge detection delay time 3	t_{CU3}	C_{CCT} = 0.47 µF	0.5	1.0	1.5	s	11	6
Overdischarge detection delay time 1	t_{DD1}	C_{CDT} = 0.1 µF	20	40	60	ms	9	6
Overdischarge detection delay time 2	t_{DD2}	C_{CDT} = 0.1 µF	20	40	60	ms	10	6
Overdischarge detection delay time 3	t_{DD3}	C_{CDT} = 0.1 µF	20	40	60	ms	11	6
Overcurrent detection delay time 1	t_{IOV1}	C_{COVT} = 0.1 µF	10	20	30	ms	12	7
Overcurrent detection delay time 2	t_{IOV2}	–	2	4	8	ms	12	7
Overcurrent detection delay time 3	t_{IOV3}	FET gate capacitor = 2000 pF	100	300	550	µs	12	7
Operating voltage								
Operating voltage between VCC and VSS *5	V_{DSOP}	–	2.0	–	24	V	–	–
Current consumption								
Current consumption (during normal operation)	I_{OPE}	V1 = V2 = V3 = 3.5 V	–	20	50	µA	5	3
Current consumption for cell 2	I_{CELL2}	V1 = V2 = V3 = 3.5 V	–300	0	300	nA	5	3
Current consumption for cell 3	I_{CELL3}	V1 = V2 = V3 = 3.5 V	–300	0	300	nA	5	3
Current consumption at power down	I_{PDN}	V1 = V2 = V3 = 1.5 V	–	–	0.1	µA	5	3
Internal resistance								
Resistance between VCC and VMP	R_{VCM}	V1 = V2 = V3 = 3.5 V	0.40	0.90	1.40	MΩ	6	3
		V1 = V2 = V3 = 3.5 V *6	0.20	0.50	0.80	MΩ	6	3
Resistance between VSS and VMP	R_{VSM}	V1 = V2 = V3 = 1.5 V	0.40	0.90	1.40	MΩ	6	3
		V1 = V2 = V3 = 1.5 V *6	0.20	0.50	0.80	MΩ	6	3
Input voltage								
CTL"H" Input voltage	$V_{CTL(H)}$	–	V_{CC}x0.8	–	–	V	–	–
CTL"L" Input voltage	$V_{CTL(L)}$	–	–	–	V_{CC}x0.2	V	–	–

Table 4 (2 / 2)

(Ta = 25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Condition	Test Circuit
Output voltage								
DOP"H" voltage	$V_{DO(H)}$	I_{OUT} = 10 µA	V_{CC}-0.5	–	–	V	7	4
DOP"L" voltage	$V_{DO(L)}$	I_{OUT} = 10 µA	–	–	V_{SS}+0.1	V	7	4
COP"L" voltage	$V_{CO(L)}$	I_{OUT} = 10 µA	–	–	V_{SS}+0.1	V	8	5
COP OFF LEAK current	I_{COL}	V1 = V2 = V3 = 4.5 V	–	–	100	nA	14	9
CD1"H" voltage	$V_{CD1(H)}$	I_{OUT} = 0.1 µA	V_{CC} -0.5	–	–	V	13	8
CD1"L" voltage	$V_{CD1(L)}$	I_{OUT} = 10 µA	–	–	V_{C1}+0.1	V	13	8
CD 2"H" voltage	$V_{CD2(H)}$	I_{OUT} = 0.1 µA	V_{CC} -0.5	–	-	V	13	8
CD 2"L" voltage	$V_{CD2(L)}$	I_{OUT} = 10 µA	–	–	V_{C2}+0.1	V	13	8
CD3"H" voltage	$V_{CD3(H)}$	I_{OUT} = 0.1 µA	V_{CC} -0.5	–	–	V	13	8
CD3"L" voltage	$V_{CD3(L)}$	I_{OUT} = 10 µA	–	–	V_{SS}+0.1	V	13	8
0 V battery charging function								
0 V charging start voltage	V_{0CHAR}	–*6	–	–	1.4	V	15	10

***1.** If overcurrent detection voltage 1 is 0.50 V, both overcurrent detection voltages 1 and 2 are 0.54 to 0.55 V, but $V_{IOV2} > V_{IOV1}$.

***2.** Voltage temperature factor 1 indicates overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, and overdischarge release voltage.

***3.** Voltage temperature factor 2 indicates overcurrent detection voltage.

***4.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

***5.** The DOP and COP logic must be established for the operating voltage.

***6.** This spec applies for only 0 V battery charging function available type.

■ Test Circuits

(1) Test condition 1 Test circuit 1

Set V1, V2, and V3 to 3.5 V under normal status. Increase V1 from 3.5 V gradually. The V1 voltage when COP = 'H' is overcharge detection voltage 1 (V_{CU1}). Decrease V1 gradually. The V1 voltage when COP = 'L' is overcharge release voltage 1 (V_{CD1}). Further decrease V1. The V1 voltage when DOP = 'H' is overdischarge voltage 1 (V_{DD1}). Increase V1 gradually. The V1 voltage when DOP = 'L' is overdischarge release voltage 1 (V_{DU1}).

Remark The voltage change rate is 150 V/s or less.

(2) Test condition 2 Test circuit 1

Set V1, V2, and V3 to 3.5 V under normal status. Increase V2 from 3.5 V gradually. The V2 voltage when COP = 'H' is overcharge detection voltage 2 (V_{CU2}). Decrease V2 gradually. The V2 voltage when COP = 'L' is overcharge release voltage 2 (V_{CD2}). Further decrease V2. The V2 voltage when DOP = 'H' is overdischarge voltage 2 (V_{DD2}). Increase V2 gradually. The V2 voltage when DOP = 'L' is overdischarge release voltage 2 (V_{DU2}).

Remark The voltage change rate is 150 V/s or less.

(3) Test condition 3 Test circuit 1

Set V1, V2, and V3 to 3.5 V under normal status. Increase V3 from 3.5 V gradually. The V3 voltage when COP = 'H' is overcharge detection voltage 3 (V_{CU3}). Decrease V3 gradually. The V3 voltage when COP = 'L' is overcharge release voltage 3 (V_{CD3}). Further decrease V3. The V3 voltage when DOP = 'H' is overdischarge voltage 3 (V_{DD3}). Increase V3 gradually. The V3 voltage when DOP = 'L' is overdischarge release voltage 3 (V_{DU3}).

Remark The voltage change rate is 150 V/s or less.

(4) Test condition 4 Test circuit 2

Set V1, V2, V3 to 3.5 V and V4 to 0 V under normal status. Increase V4 from 0 V gradually. The V4 voltage when DOP = 'H' and COP = 'H', is overcurrent detection voltage 1 (V_{IOV1}).

Set V1, V2, and V3 to 3.5 V and V4 to 0 V under normal status. Fix the COVT pin at V_{SS}, increase V4 from 0 V gradually. The V4 voltage when DOP = 'H' and COP = 'H' is overcurrent detection voltage 2 (V_{IOV2}).

Set V1, V2, and V3 to 3.5 V and V4 to 0 V under normal status. Fix the COVT pin at V_{SS}, increase V4 gradually from 0 V at 400 µs to 2 ms. The V4 voltage when DOP = 'H' and COP = 'H' is overcurrent detection voltage 3 (V_{IOV3}).

(5) Test condition 5 Test circuit 3

Set S1 to ON, V1, V2, and V3 to 3.5 V, and V4 to 0 V under normal status and measure current consumption. I1 is the normal status current consumption (I_{OPE}), I2, the cell 2 current consumption (I_{CELL2}), and I3, the cell 3 current consumption (I_{CELL3}).

Set S1 to ON, V1, V2, and V3 to 1.5 V, and V4 to 4.5 V under overdischarge status. Current consumption I1 is power-down current consumption (I_{PDN}).

(6) Test condition 6 Test circuit 3

Set S1 to ON, V1, V2, and V3 to 3.5 V, and V4 to 10.5 V under normal status. V4/I4 is the internal resistance between VCC and VMP (R_{VCM}).

Set S1 to ON, V1, V2, and V3 to 1.5 V, and V4 to 4.1 V under overdischarge status. (4.5-V4)/I4 is the internal resistance between VSS and VMP (R_{VSM}).

(7) Test condition 7 Test circuit 4

Set S1 to ON, S2 to OFF, V1, V2, and V3 to 3.5 V, and V4 to 0 V under normal status. Increase V5 from 0 V gradually. The V5 voltage when I1 = 10 µA is DOP'L' voltage ($V_{D0(L)}$).

Set S1 to OFF, S2 to ON, V1, V2, V3 to 3.5 V, and V4 to V_{IOV2}+0.1 V under overcurrent status. Increase V6 from 0 V gradually. The V6 voltage when I2 = 10 µA is the DOP'H' voltage ($V_{DO(H)}$).

(8) Test condition 8 Test circuit 5

Set V1, V2, V3 to 3.5 V and V4 to 0 V under normal status. Increase V5 from 0 V gradually. The V5 voltage when I1 = 10 µA is the COP'L' voltage ($V_{C0(L)}$).

(9) Test condition 9 Test circuit 6

Set V1, V2, V3 to 3.5 V under normal status. Increase V1 from 3.5 V to 4.5 V immediately (within 10 µs). The time after V1 becomes 4.5 V until COP goes 'H' is the overcharge detection delay time 1 (t_{CU1}).

Set V1, V2, V3 to 3.5 V under normal status. Decrease V1 from 3.5 V to 1.9 V immediately (within 10 µs). The time after V1 becomes 1.9 V until DOP goes 'H' is the overdischarge detection delay time 1 (t_{DD1}).

(10) Test condition 10 Test circuit 6

Set V1, V2, V3 to 3.5 V under normal status. Increase V2 from 3.5 V to 4.5 V immediately (within 10 µs). The time after V2 becomes 4.5 V until COP goes 'H' is the overcharge detection delay time 2 (t_{CU2}).

Set V1, V2, V3 to 3.5 V under normal status. Decrease V2 from 3.5 V to 1.9 V immediately (within 10 µs). The time after V2 becomes 1.9 V until DOP goes 'H' is the overdischarge detection delay time 2 (t_{DD2}).

(11) Test condition 11 Test circuit 6

Set V1, V2, V3 to 3.5 V under normal status. Increase V3 from 3.5 V to 4.5 V immediately (within 10 µs). The time after V3 becomes 4.5 V until COP goes 'H' is the overcharge detection delay time 3 (t_{CU3}).

Set V1, V2, V3 to 3.5 V under normal status. Decrease V3 from 3.5 V to 1.9 V immediately (within 10 µs). The time after V3 becomes 1.9 V until DOP goes 'H' is the overdischarge detection delay time 3 (t_{DD3}).

(12) Test condition 12 Test circuit 7

Set V1, V2, V3 to 3.5 V and S1 to OFF under normal status. Increase V4 from 0 V to 0.55 V immediately (within 10 µs). The time after V4 becomes 0.55 V until DOP goes 'H' is the overcurrent detection delay time 1 (t_{IOV1}).

Set V1, V2, V3 to 3.5 V and S1 to OFF under normal status. Increase V4 from 0 V to 0.75 V immediately (within 10 µs). The time after V4 becomes 0.75 V until DOP goes 'H' is the overcurrent detection delay time 2 (t_{IOV2})

Set S1 to ON to inhibit overdischarge detection. Set V1, V2, V3 to 4.0 V and increase V4 from 0 V to 6.0 V immediately (within 1 µs) and decrease V1, V2, and V3 to 2.0 V at a time. The time after V4 becomes 6.0 V until DOP goes 'H' is the overcurrent detection delay time 3 (t_{IOV3}).

(13) Test condition 13 Test circuit 8

Set S4 to ON, S1, S2, S3, S5, and S6 to OFF, V1, V2, V3 to 3.5 V and V4, V6, and V7 to 0 V under normal status. Increase V5 from 0 V gradually. The V5 voltage when I2 = 10 µA is the CD1'L' voltage ($V_{CD1(L)}$)

Set S5 to ON, S1, S2, S3, S4, and S6 to OFF, V1, V2, and V3 to 3.5 V and V4, V5, and V7 to 0 V under normal status. Increase V6 from 0 V gradually. The V6 voltage when I3 = 10 µA is the CD2'L' voltage ($V_{CD2(L)}$).

Set S6 to ON, S1, S2, S3, S4, and S5 to OFF, V1, V2, and V3 to 3.5 V and V4, V5, and V6 to 0 V under normal status. Increase V7 from 0 V gradually. The V7 voltage when I4 = 10 µA is the CD3'L' voltage ($V_{CD3(L)}$).

Set S1 to ON, S2, S3, S4, S5, and S6 to OFF, V1 to 4.5 V, V2 and V3 to 3.5 V and V5, V6, and V7 to 0 V under overcharge status. Increase V4 from 0 V gradually. The V4 voltage when I1 = 0.1 µA is the CD1'H' voltage ($V_{CD1(H)}$).

Set S2 to ON, S1, S3, S4, S5, and S6 to OFF, V2 to 4.5 V, V1 and V3 to 3.5 V and V5, V6, and V7 to 0 V under overcharge status. Increase V4 from 0 V gradually. The V4 voltage when I1 = 0.1 µA is the CD2'H' voltage ($V_{CD2(H)}$).

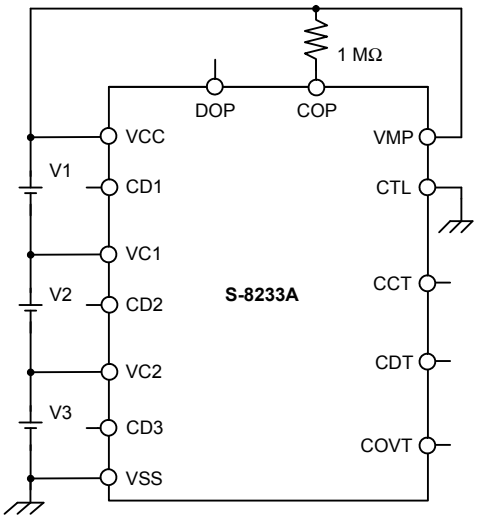
Set S3 to ON, S1, S2, S4, S5, and S6 to OFF, V3 to 4.5 V, V1 and V2 to 3.5 V and V5, V6, and V7 to 0 V under overcharge status. Increase V4 from 0 V gradually. The V4 voltage when I1 = 0.1 µA is the CD3'H' voltage ($V_{CD3(H)}$).

(14) Test condition 14 Test circuit 9

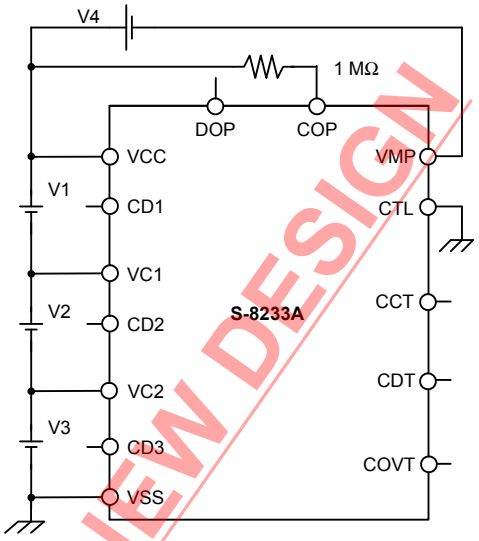
Set V1, V2, and V3 to 4.5 V under overcharge status. The current I1 flowing to COP pin is COP OFF LEAK current (I_{COL}).

(15) Test condition 15 Test circuit 10

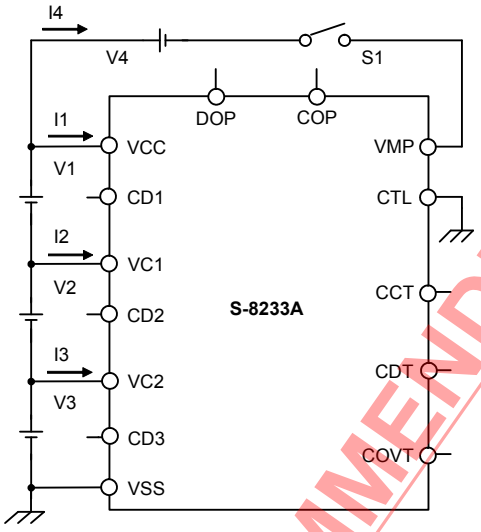
Set V1, V2, and V3 to 0 V, and V8 to 2 V, and decrease V8 gradually. The V8 voltage when COP = 'H' (V_{SS} + 0.1 V or higher) is the 0V charge start voltage (V_{0CHAR}).



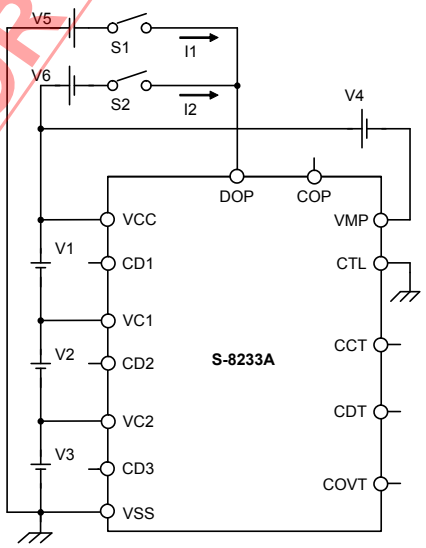
Test circuit 1



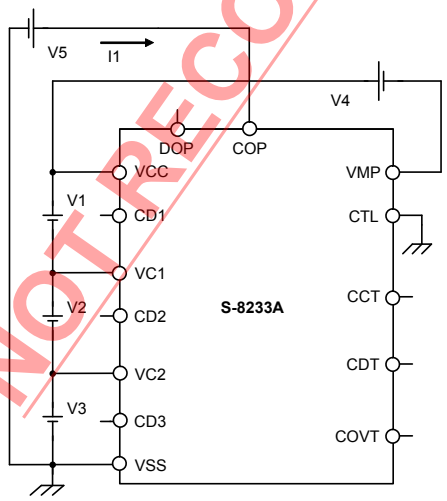
Test circuit 2



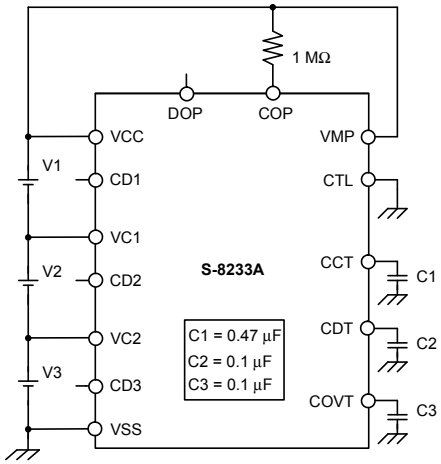
Test circuit 3



Test circuit 4

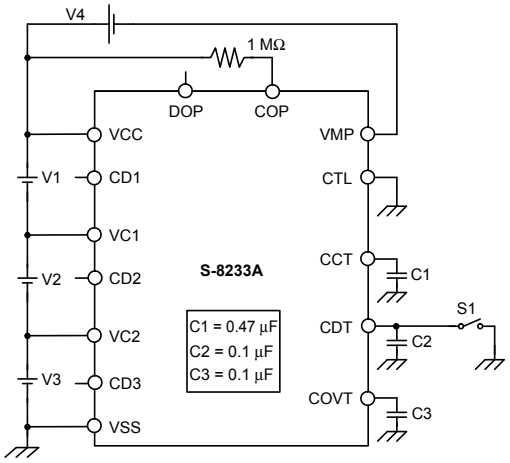


Test circuit 5

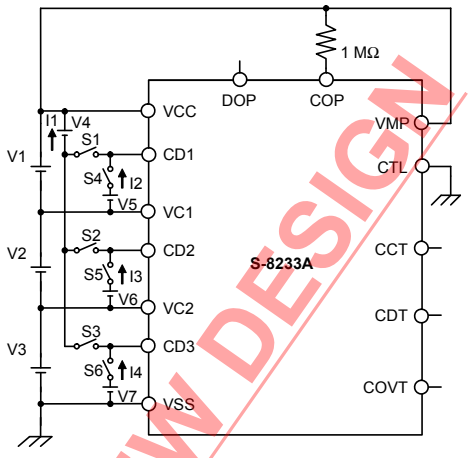


Test circuit 6

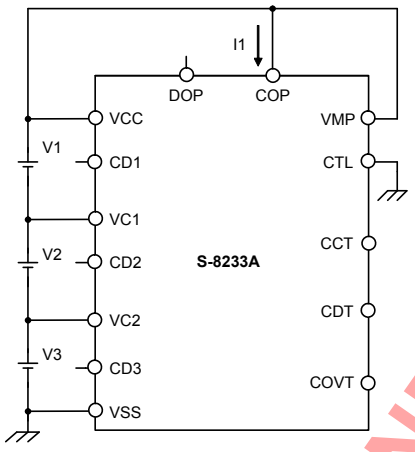
Figure 4 (1 / 2)



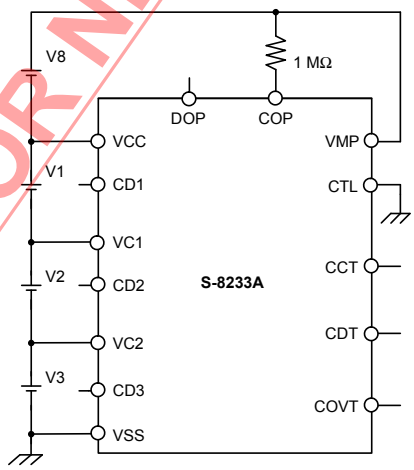
Test circuit 7



Test circuit 8



Test circuit 9



Test circuit 10

Figure 4 (2 / 2)

■ Operation

Remark Refer to "■ **Battery Protection IC Connection Example**".

Normal status

This IC monitors the voltages of the three serially-connected batteries and the discharge current to control charging and discharging. If the voltages of all the three batteries are in the range from the overdischarge detection voltage (V_{DD}) to the overcharge detection voltage (V_{CU}), and the current flowing through the batteries becomes equal or lower than a specified value (the VMP pin voltage is equal or lower than overcurrent detection voltage 1), the charging and discharging FETs turn on. In this status, charging and discharging can be carried out freely. This status is called the normal status. In this status, the VMP and VCC pins are shorted by the R_{VCM} resistor.

Overcurrent status

This IC is provided with the three overcurrent detection levels (V_{IOV1}, V_{IOV2} and V_{IOV3}) and the three overcurrent detection delay time (t_{IOV1}, t_{IOV2} and t_{IOV3}) corresponding to each overcurrent detection level.

If the discharging current becomes equal to or higher than a specified value (the VMP pin voltage is equal to or higher than the overcurrent detection voltage) during discharging under normal status and it continues for the overcurrent detection delay time (t_{IOV}) or longer, the discharging FET turns off to stop discharging. This status is called an overcurrent status. The VMP and VCC pins are shorted by the R_{VCM} resistor at this time. The charging FET turns off.

When the discharging FET is off and a load is connected, the VMP pin voltage equals the V_{SS} potential.

The overcurrent status returns to the normal status when the load is released and the impedance between the EB- and EB+ pins (see **Figure 9**) is 100 MΩ or higher. When the load is released, the VMP pin, which and the VCC pin are shorted with the R_{VCM} resistor, goes back to the V_{CC} potential. The IC detects that the VMP pin potential returns to overcurrent detection voltage 1 (V_{IOV1}) or lower (or the overcurrent detection voltage 2 (V_{IOV2}) or lower if the COVT pin is fixed at the 'L' level and overcurrent detection 1 is inhibited) and returns to the normal status.

Overcharge status

If one of the battery voltages becomes higher than the overcharge detection voltage (V_{CU}) during charging under normal status and it continues for the overcharge detection delay time (t_{CU}) or longer, the charging FET turns off to stop charging. This status is called the overcharge status. The 'H' level signal is output to the conditioning pin corresponding to the battery which exceeds the overcharge detection voltage until the battery becomes equal to lower than the overcharge release voltage (V_{CD}). The battery can be discharged by connecting an Nch FET externally. The discharging current can be limited by inserting R11, R12 and R13 resistors (see **Figure 9**). The VMP and VCC pins are shorted by the R_{VCM} resistor under the overcharge status.

The overcharge status is released in two cases:

<1> The battery voltage which exceeded the overcharge detection voltage (V_{CU}) falls below the overcharge release voltage (V_{CD}), the charging FET turns on and the normal status returns.

<2> If the battery voltage which exceeded the overcharge detection voltage (V_{CU}) is equal or higher than the overcharge release voltage (V_{CD}), but the charger is removed, a load is placed, and discharging starts, the charging FET turns on and the normal status returns.

The release mechanism is as follows: the discharge current flows through an internal parasitic diode of the charging FET immediately after a load is installed and discharging starts, and the VMP pin voltage decreases by about 0.6 V from the VCC pin voltage momentarily. The IC detects this voltage (overcurrent detection voltage 1 or higher), releases the overcharge status and returns to the normal status.

Overdischarge status

If any one of the battery voltages falls below the overdischarge detection voltage (V_{DD}) during discharging under normal status and it continues for the overdischarge detection delay time (t_{DD}) or longer, the discharging FET turns off and discharging stops. This status is called the overdischarge status. When the discharging FET turns off, the VMP pin voltage becomes equal to the VSS voltage and the IC's current consumption falls below the power-down current consumption (I_{PDN}). This status is called the power-down status. The VMP and VSS pins are shorted by the R_{VSM} resistor under the overdischarge and power-down statuses.

The power-down status is canceled when the charger is connected and the voltage between VMP and VSS is 3.0 V or higher (overcurrent detection voltage 3). When all the battery voltages becomes equal to or higher than the overdischarge release voltage (V_{DU}) in this status, the overdischarge status changes to the normal status.

Delay circuits

The overcharge detection delay time (t_{CU1} to t_{CU3}), overdischarge detection delay time (t_{DD1} to t_{DD3}), and overcurrent detection delay time 1 (t_{IOV1}) are changed with external capacitors (C4 to C6).

The delay times are calculated by the following equations:

	Min.	Typ.	Max.	
t_{CU}[s] = Delay factor (	1.07,	2.13,	3.19)×C4 [µF]	
t_{DD}[s] = Delay factor (	0.20,	0.40,	0.60)×C5 [µF]	
t_{IOV1}[s] = Delay factor (	0.10,	0.20,	0.30)×C6 [µF]	

Caution The delay time for overcurrent detection 2 and 3 is fixed by an internal IC circuit. The delay time cannot be changed via an external capacitor.

CTL pin

If the CTL pin is floated under normal status, it is pulled up to the V_{CC} potential in the IC, and both the charging and discharging FETs turn off to inhibit charging and discharging. Both charging and discharging are also inhibited by applying the VCC pin to the CTL pin externally. At this time, the VMP and VCC pins are shorted by the R_{VCM} resistor.

When the CTL pin becomes equal to V_{SS} potential, charging and discharging are enabled and go back to their appropriate statuses for the battery voltages.

Caution Please note unexpected behavior might occur when electrical potential difference between the CTL pin ('L' level) and VSS is generated through the external filter (R_{VSS} and C_{VSS}) as a result of input voltage fluctuations.

0 V battery charging function

This function is used to recharge the three serially-connected batteries after they self-discharge to 0 V. When the 0 V charging start voltage (V_{0CHAR}) or higher is applied to between VMP and VSS by connecting the charger, the charging FET gate is fixed to V_{SS} potential.

When the voltage between the gate sources of the charging FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging FET turns on to start charging. At this time, the discharging FET turns off and the charging current flows through the internal parasitic diode in the discharging FET. If all the battery voltages become equal to or higher than the overdischarge release voltage (V_{DU}), the normal status returns.

Caution In the products without 0 V battery charging function, the resistance between VCC and VMP and between VSS and VMP are lower than the products with 0 V battery charging function. It causes to that overcharge detection voltage increases by the drop voltage of R5 (see Figure 9) with sink current at VMP.

The COP output is undefined below 2.0 V on VCC-VSS voltage in the products without 0 V battery charging function.

Voltage temperature factor

Voltage temperature factor 1 indicates overcharge detection voltage, overcharge release voltage, overdischarge detection voltage, and overdischarge release voltage.

Voltage temperature factor 2 indicates overcurrent detection voltage.

The Voltage temperature factors 1 and 2 are expressed by the oblique line parts in **Figure 5**.

Ex. Voltage temperature factor of overcharge detection voltage Typ.

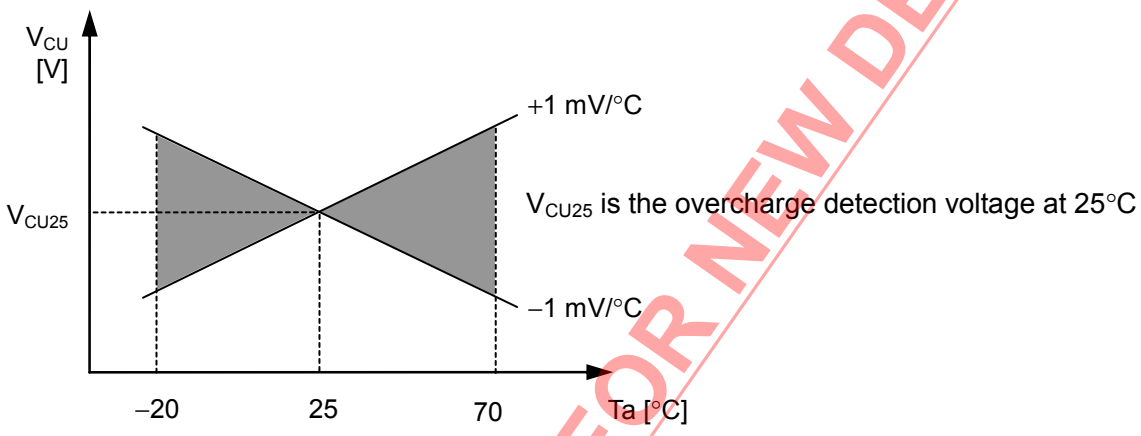
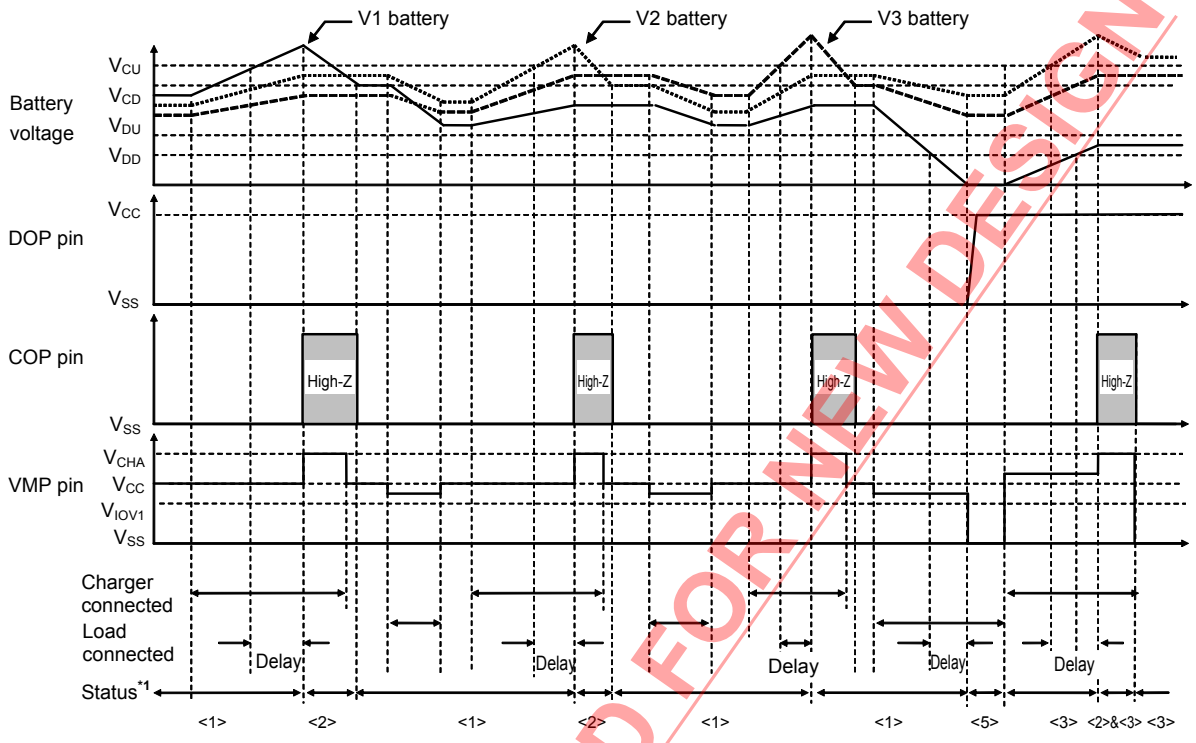


Figure 5

■ Timing Chart

1. Overcharge detection

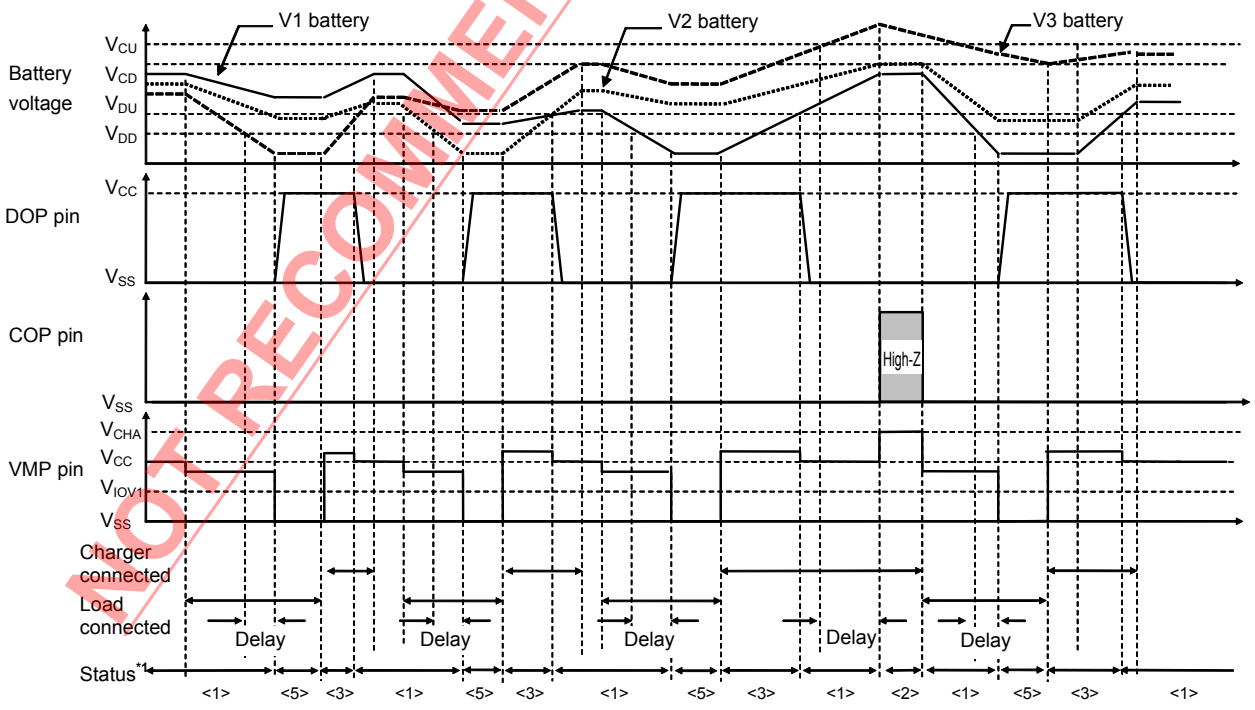


*1. <1>Normal status, <2>Overcharge status, <3>Overdischarge status, <4>Overcurrent status, <5>Power-down status

Remark The charger is assumed to charge with a constant current. V_{CHA} indicates the open voltage of the charger.

Figure 6

2. Overdischarge detection

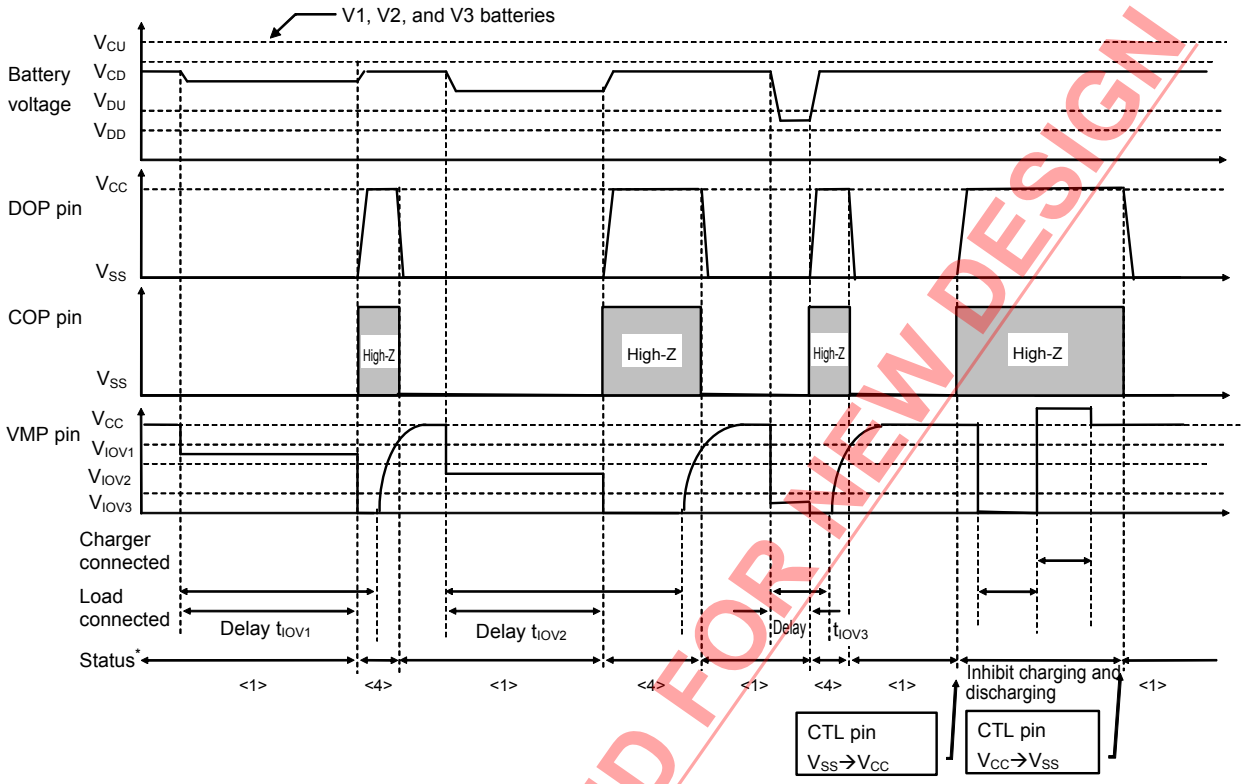


*1. <1>Normal status, <2>Overcharge status, <3>Overdischarge status, <4>Overcurrent status, <5>Power-down status

Remark The charger is assumed to charge with a constant current. V_{CHA} indicates the open voltage of the charger.

Figure 7

3. Overcurrent detection



*1. <1>Normal status, <2>Overcharge status , <3>Overdischarge status, <4>Overcurrent status

Figure 8

■ Battery Protection IC Connection Example

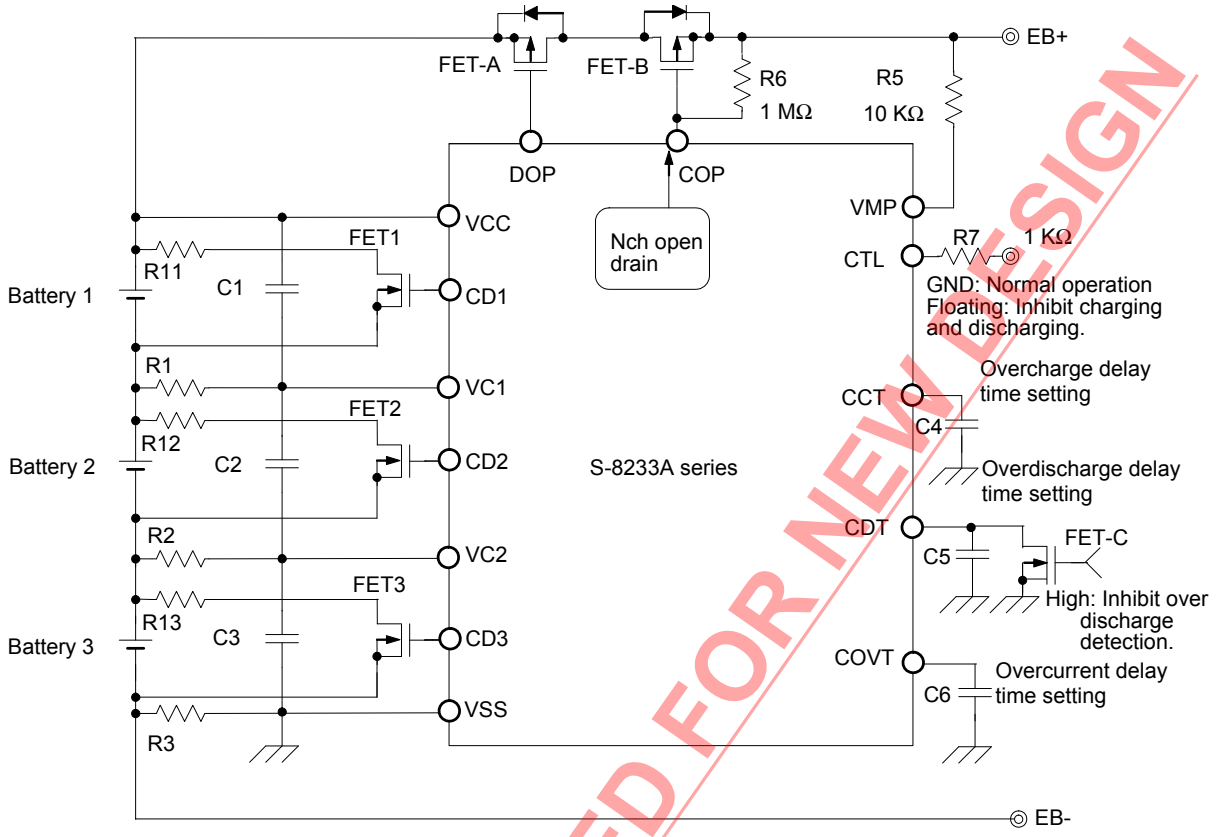


Figure 9

[Description of **Figure 9**]

- R11, R12, and R13 are used to adjust the battery conditioning current.The conditioning current during overcharge detection is given by Vcu (overcharge detection voltage)/R (R: resistance).To disable the conditioning function, open CD1, CD2, and CD3.
- The overcharge detection delay time (t_{CU1} to t_{CU3}), overdischarge detection delay time (t_{DD1} to t_{DD3}), and overcurrent detection delay time (t_{IOV1}) are changed with external capacitors (C4 to C6). See the electrical characteristics.
- R6 is a pull-up resistor that turns FET-B off when the COP pin is opened. Connect a 100 kΩ to 1 MΩ resistor.
- R5 is used to protect the IC if the charger is connected in reverse. Connect a 10 kΩ to 50 kΩ resistor.
- If capacitor C6 is absent, rush current occurs when a capacitive load is connected and the IC enters the overcurrent mode. C6 must be connected to prevent it.
- If capacitor C5 is not connected, the IC may enter the overdischarge status due to variations of battery voltage when the overcurrent occurs. In this case, a charger must be connected to return to the normal status. To prevent this, connect an at least 0.01 μF capacitor to C5.
- If a leak current flows between the delay capacitor connection pin (CCT, CDT, or COVT) and VSS, the delay time increases and an error occurs. The leak current must be 100 nA or less.
- Overdischarge detection can be disabled by using FET-C. The FET-C off leak must be 0.1 μA or less. If overdischarge is inhibited by using this FET, the current consumption does not fall below 0.1 μA even when the battery voltage drops and the IC enters the overdischarge detection mode.
- R1, R2, and R3 must be 1 kΩ or less.
- R7 is the protection of the CTL when the CTL pin voltage higher than V_{CC} voltage. Connect a 300 Ω to 5 kΩ resister. If the CTL pin voltage never greater than the V_{CC} voltage (ex. R7 connect to V_{SS}), without R7 resistance is allowed .

Caution 1. The above constants may be changed without notice.

2. If any electrostatic discharge of 2000 V or higher is not applied to the S-8233A series with a human body model, R1, R2, R3, C1, C2, and C3 are unnecessary.

3. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform through evaluation using the actual application to set the constant.

■ Precautions

- If a charger is connected in the overdischarge status and one of the battery voltages becomes equal to or higher than the overcharge release voltage (V_{CU}) before the battery voltage which is below the overdischarge detection voltage (V_{DD}) becomes equal to or higher than the overdischarge release voltage (V_{DU}), the overdischarge and overcharge statuses are entered and the charging and discharging FETs turn off. Both charging and discharging are disabled. If the battery voltage which was higher than the overcharge detection voltage (V_{CU}) falls to the overcharge release voltage (V_{CD}) due to internal discharging, the charging FET turns on.

  If the charger is detached in the overcharge and overdischarge status, the overcharge status is released, but the overdischarge status remains. If the charger is connected again, the battery status is monitored after that. The charging FET turns off after the overcharge detection delay time, the overcharge and overdischarge statuses are entered.

- If any one of the battery voltages is equal to or lower than the overdischarge release voltage (V_{DU}) when they are connected for the first time, the normal status may not be entered. If the VMP pin voltage is made equal to or higher than the VCC voltage (if a charger is connected), the normal status is entered.

- If the CTL pin floats in power-down mode, it is not pulled up in the IC, charging and discharging may not be inhibited. However, the overdischarge status becomes effective. If the charger is connected, the CTL pin is pulled up, and charging and discharging are inhibited immediately.

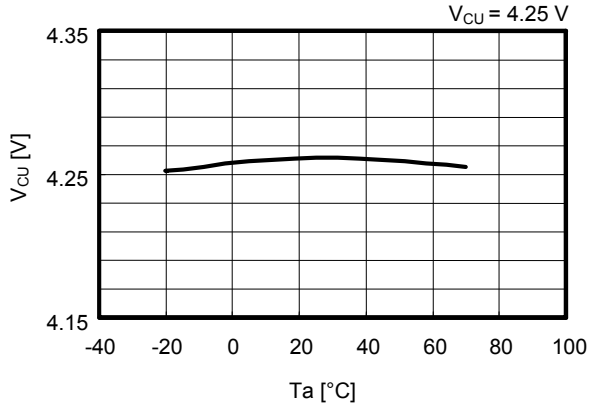
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- SII claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

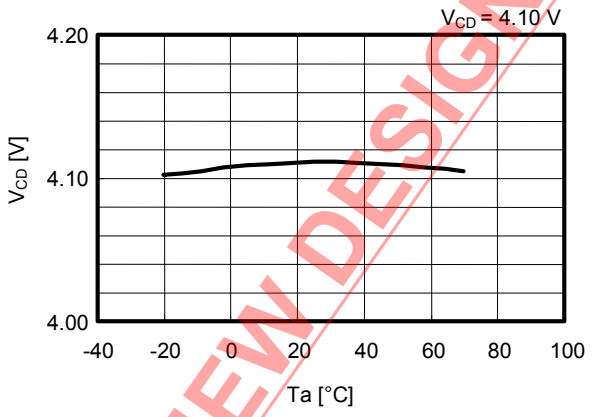
■ Characteristics (Typical Data)

1. Detection voltage temperature characteristics

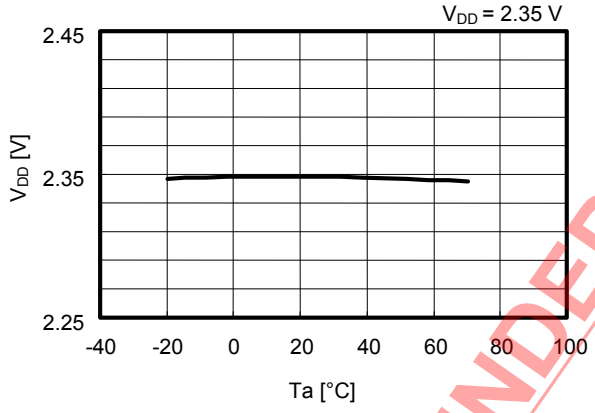
Overcharge detection voltage vs. temperature



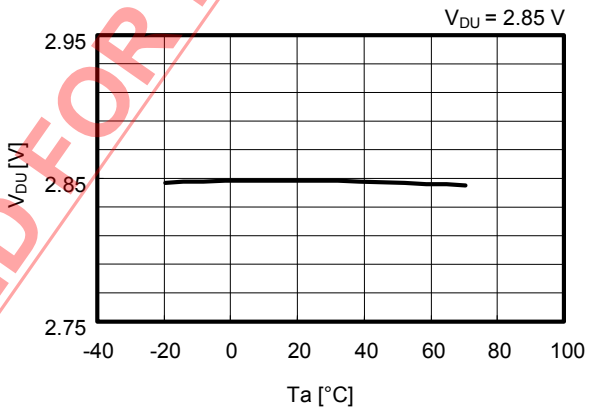
Overcharge release voltage vs. temperature



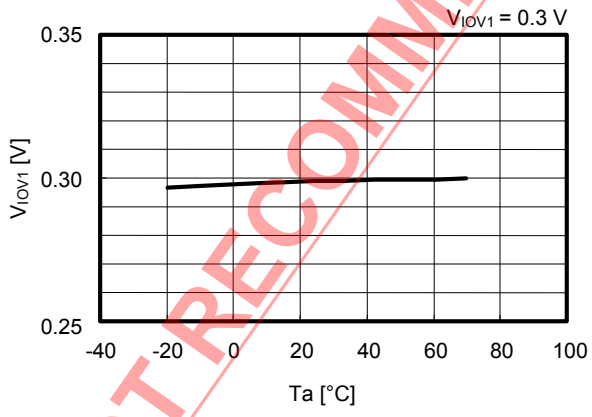
Overdischarge detection voltage vs. temperature



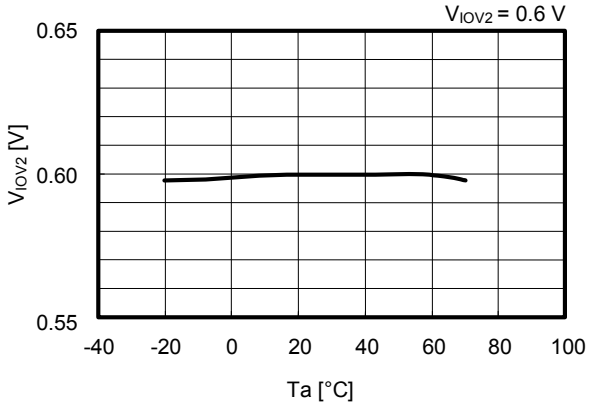
Overdischarge release voltage vs. temperature



Overcurrent1 detection voltage vs. temperature

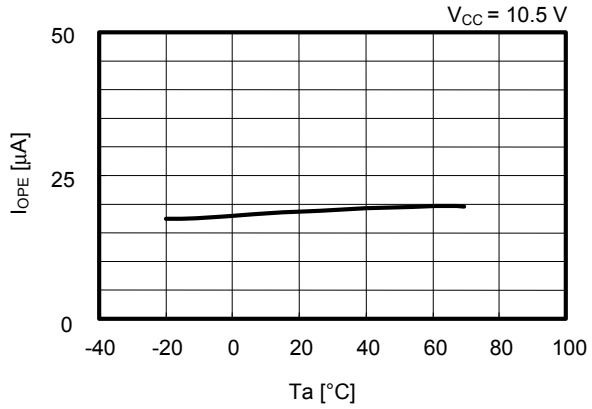


Overcurrent2 detection voltage vs. temperature

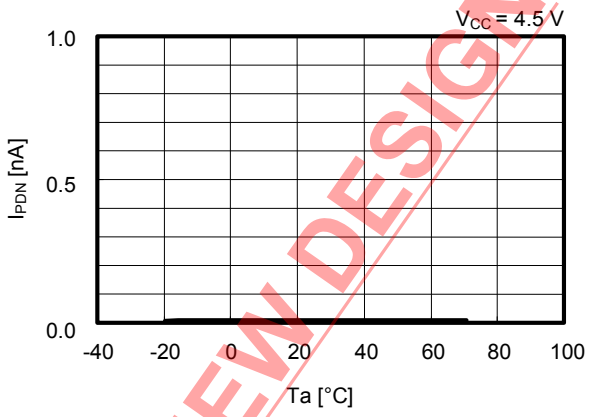


2. Current consumption temperature characteristics

Current consumption vs. temperature in normal mode

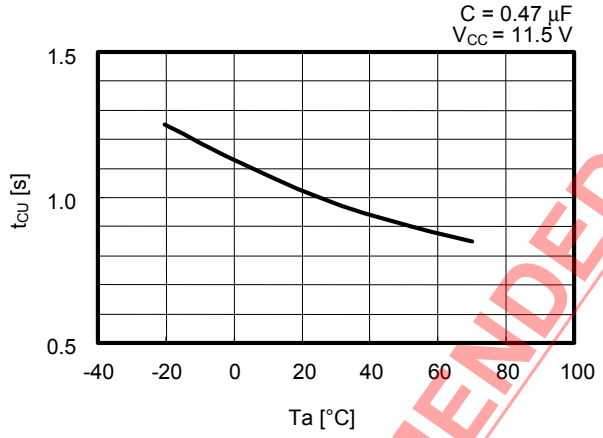


Current consumption vs. temperature in power-down mode

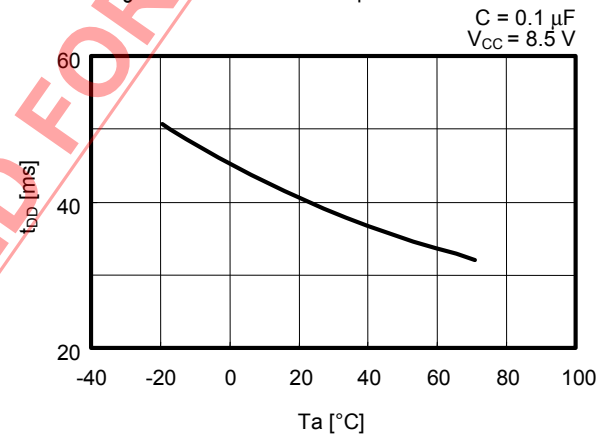


3. Delay time temperature characteristics

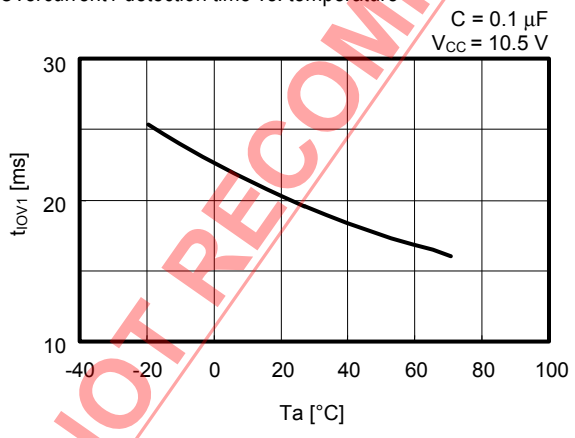
Overcharge detection time vs. temperature



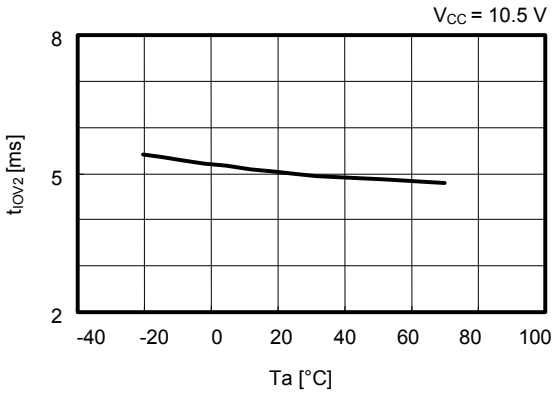
Overdischarge detection time vs. temperature



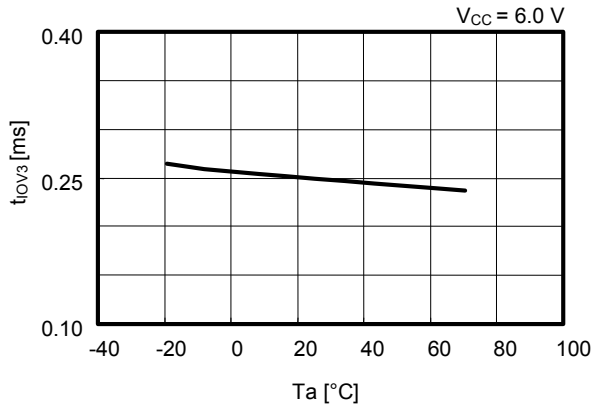
Overcurrent1 detection time vs. temperature



Overcurrent2 detection time vs. temperature

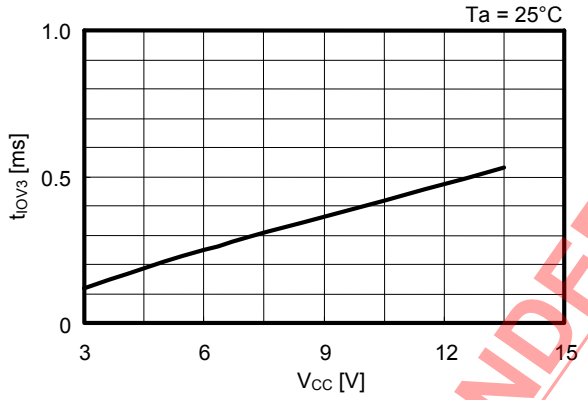


Overcurrent3 (load short) detection time vs. temperature

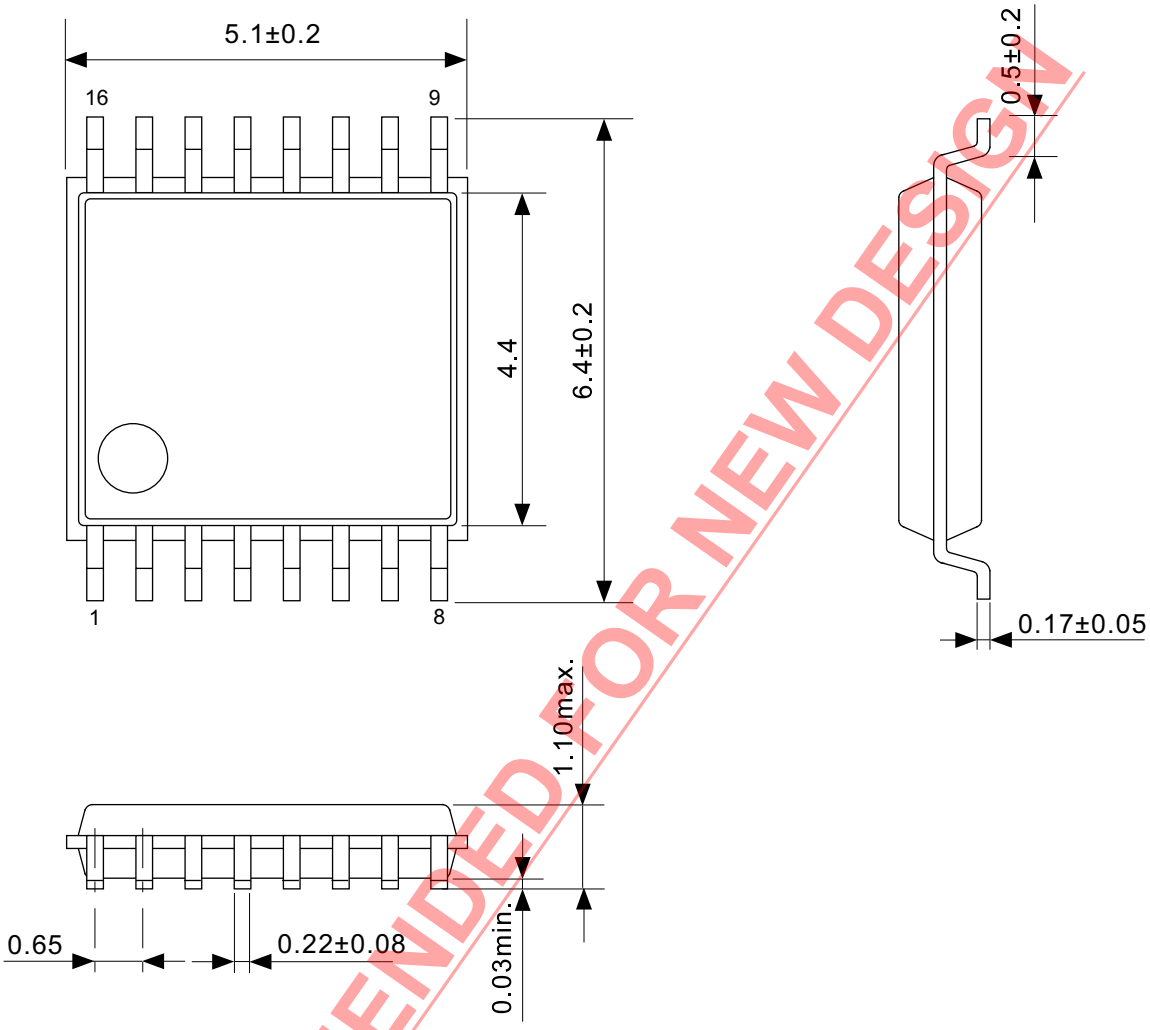


4. Delay time vs. power supply voltage

Overcurrent 3 (load short) detection time vs. power supply voltage



Caution Please design all applications of the S-8233A Series with safety in mind.



No. FT016-A-P-SD-1.1

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No.	FT016-A-P-SD-1.1
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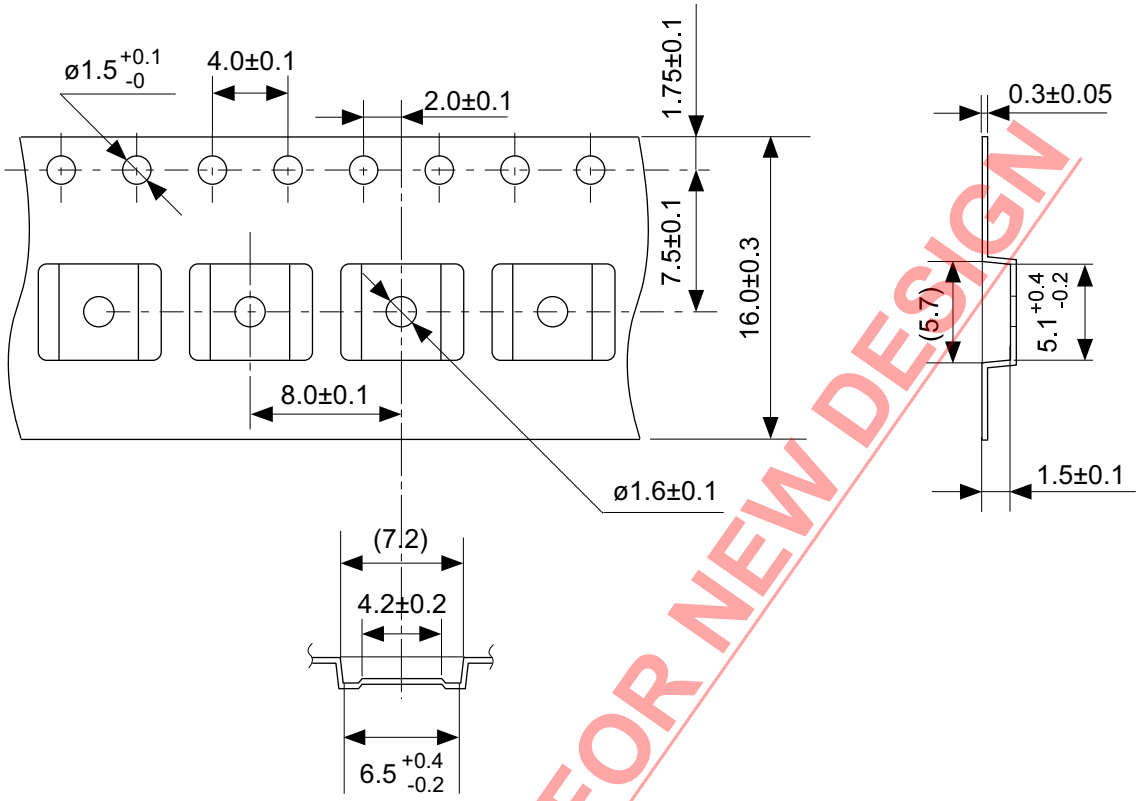
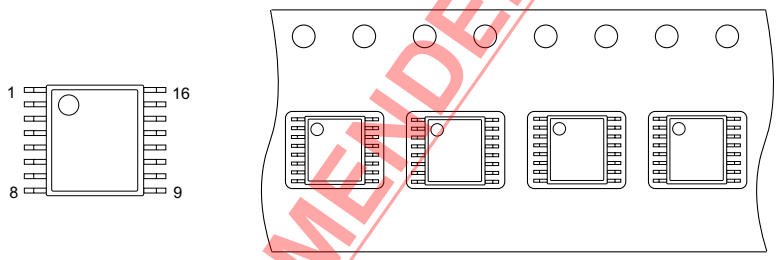
UNIT	mm
Seiko Instruments Inc.	





No. FT016-A-C-SD-1.1

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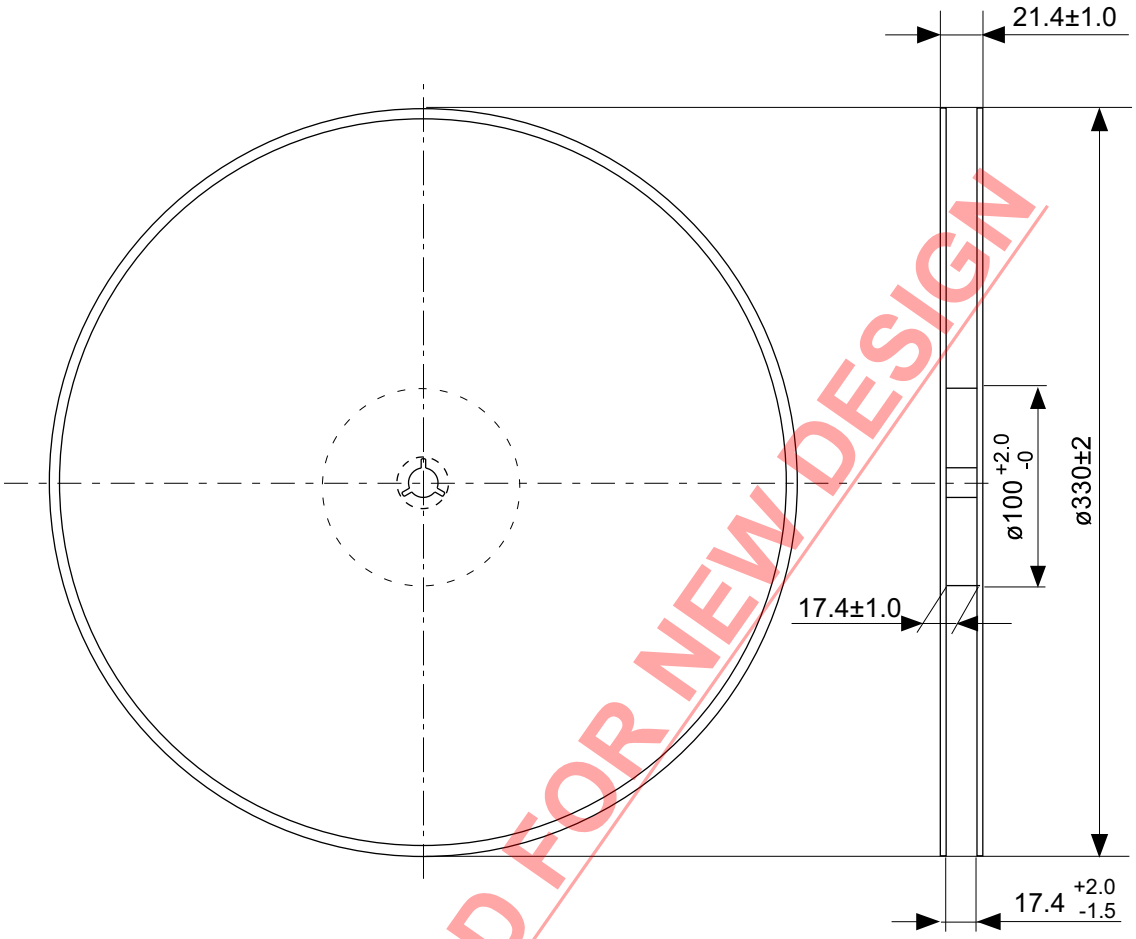
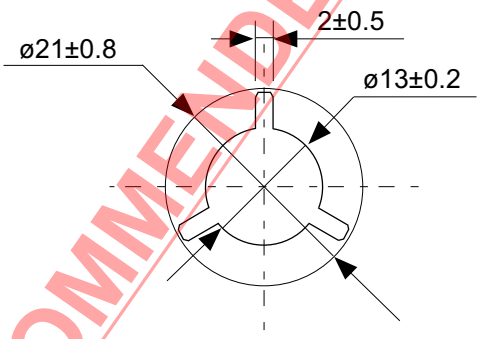
No.	FT016-A-C-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT016-A-R-SD-2.0

TITLE	TSSOP16-A- Reel		
No.	FT016-A-R-SD-2.0		
SCALE		QTY.	2,000
UNIT	mm		
Seiko Instruments Inc.			