Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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BATTERY BACKUP SWITCHING IC

The S-8425 Series is a CMOS IC designed for use in the switching circuits of primary and backup power supplies on a single chip. It consists of three voltage regulators, two voltage detectors, a power supply switch and its controller, as well as other functions.
In addition to the function for switching between the primary and backup power supply, the S-8425 Series can provide microcontrollers with two types of voltage detection output signals corresponding to the power supply voltage.
Moreover, adopting a special sequence for switch control enables the effective use of the backup power supply, making this IC ideal for configuring a backup system.

■ Features

- Low power consumption
  Normal operation: 15 μA max. (V_{IN} = 6 V)
  Backup: 2.1 μA max.
- Voltage regulator
  Output voltage tolerance : ±2%
  Output voltage: Independently selectable in 0.1 V steps in the range of 2.3 V to 5.4 V
- Two built-in voltage detectors (CS, $\overline{\text{RESET}}$)
  Detection voltage tolerance: ±2%
  Detection voltage: Selectable in 0.1 V steps in the range of 2.4 V to 5.3 V ($\overline{\text{CS}}$ voltage detector)
  Selectable in 0.1 V steps in the range of 1.7 V to 3.4 V ($\overline{\text{RESET}}$ voltage detector)
- $\overline{\text{RESET}}$ release delay: 300 μs min.
- Switching circuit for primary power supply and backup power supply configurable on one chip
- Efficient use of backup power supply possible
- Special sequence
  Backup voltage is not output when the primary power supply voltage does not reach the initial voltage at which the switch unit operates.
- Lead-free, Sn 100%, halogen-free*1

***1.** Refer to "■ **Product Name Structure**" for details.

■ Packages

- 8-Pin TSSOP
- 8-Pin SON(B)

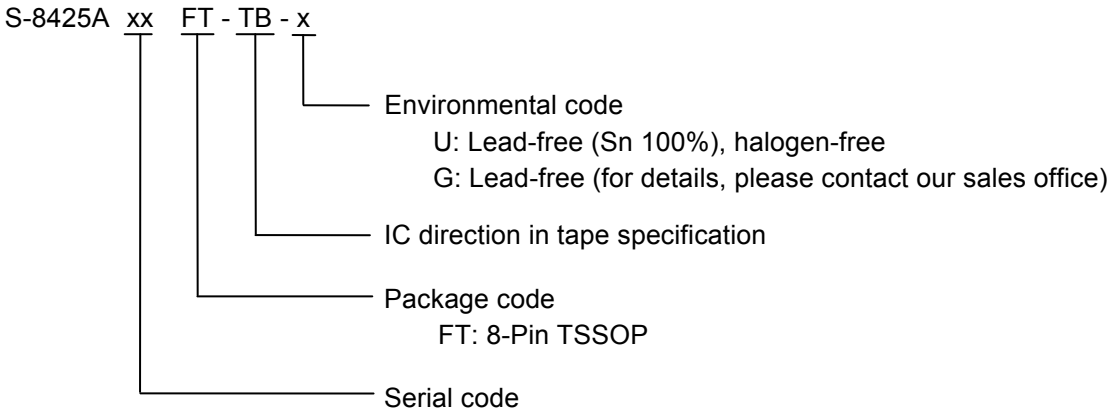
■ Applications

- Camcorders
- Digital cameras
- Memory cards
- SRAM backup equipment

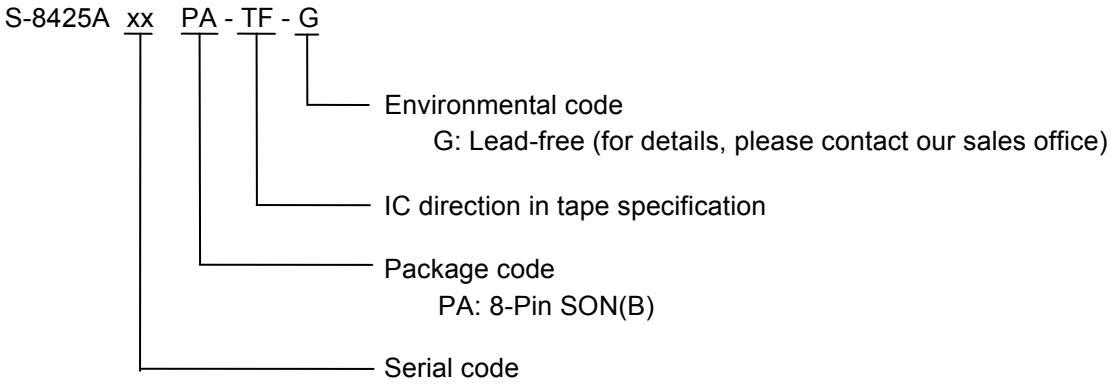
■ Product Name Structure

1. Product Name

(1) 8-Pin TSSOP



(2) 8-Pin SON(B)



2. Packages

Package Name		Drawing Code		
		Package	Tape	Reel
8-Pin TSSOP	Environmental code = G	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-SD
	Environmental code = U	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-S1
8-Pin SON(B)		PA008-B-P-SD	PA008-B-C-SD	PA008-B-R-SD

3. Product Name List

Product Name	Package	Output Voltage (V)			CS Voltage (V)		$\overline{\text{RESET}}$ Voltage (V)		Switch Voltage (V)
		V_{RO}	V_{OUT}	V_{CH}	$-V_{DET1}$	$+V_{DET1}$	$-V_{DET2}$	$+V_{DET2}$	V_{SW1}
S-8425AAAFT-TB-x	8-Pin TSSOP	3.000	3.000	3.300	3.300	3.401	2.200	2.312	$+V_{DET1} \times 0.85$
S-8425AAGFT-TB-U	8-Pin TSSOP	3.000	2.800	2.800	4.300	4.441	1.800	1.880	$+V_{DET1} \times 0.85$
S-8425AAAPA-TF-G	8-Pin SON(B)	3.000	3.000	3.300	3.300	3.401	2.200	2.312	$+V_{DET1} \times 0.85$

Caution Set the CS voltage so that the switch voltage (V_{SW1}) is equal to or greater than the $\overline{\text{RESET}}$ detection voltage ($-V_{DET2}$).

Remark 1 The selection range is as follows.

V_{RO}, V_{OUT}, V_{CH}:	2.3 to 5.4 V (0.1 V steps)
$-V_{DET1}$:	2.4 to 5.3 V (0.1 V steps)
$-V_{DET2}$:	1.7 to 3.4 V (0.1 V steps)
V_{SW1}:	$+V_{DET1} \times 0.85$ or $+V_{DET1} \times 0.77$

2. Please contact our sales office for the products with a voltage other than those specified above.

3. x: G or U

4. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ Block Diagram

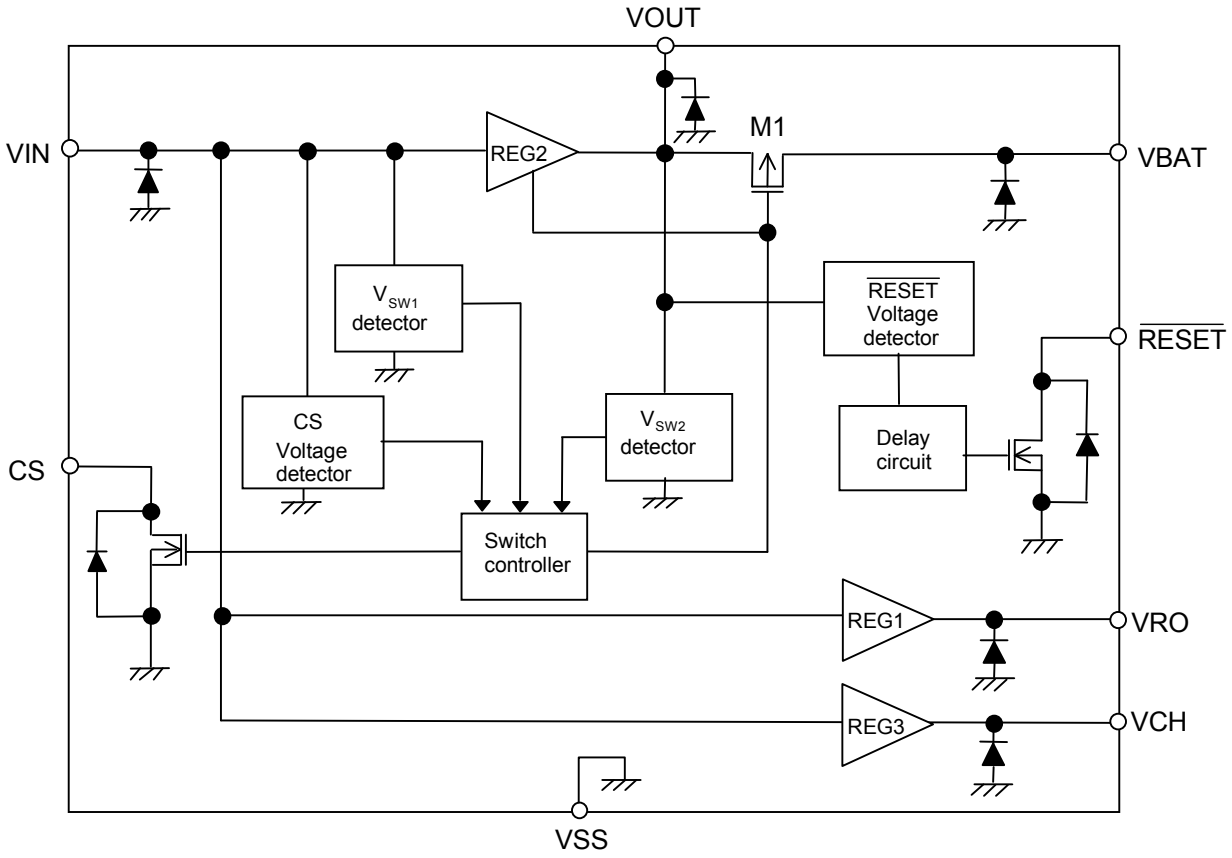
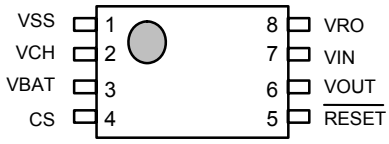


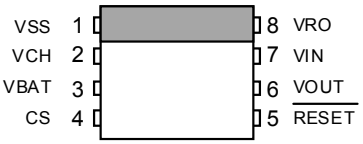
Figure 1 Block Diagram

■ Pin Configurations

8-Pin TSSOP
Top View



8-Pin SON(B)
Top View



Pin No.	Symbol	Description
1	VSS	Ground
2	VCH*1	Output pin of voltage regulator 3
3	VBAT*1	Backup power supply input pin
4	CS	Output pin of CS voltage detector
5	$\overline{\text{RESET}}$	Output pin of $\overline{\text{RESET}}$ voltage detector
6	VOUT*1	Output pin of voltage regulator 2
7	VIN*1	Primary power supply input pin
8	VRO*1	Output pin of voltage regulator 1

Figure 2 Pin Configurations

***1.** Mount capacitors between VSS (GND) and the VIN, VBAT, VOUT, VRO, and VCH pins (see the **Standard Circuit** section).

■ Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings

(Ta = 25°C, unless otherwise specified)

Item		Symbol	Absolute Maximum Rating	Unit
Primary power supply input voltage		V_{IN}	V_{SS}–0.3 to V_{SS}+18	V
Backup power supply input voltage		V_{BAT}	V_{SS}–0.3 to V_{SS}+18	V
Output voltage of voltage regulator		V_{RO}, V_{OUT}, V_{CH}	V_{SS}–0.3 to V_{IN}+0.3	V
CS output voltage		V_{CS}	V_{SS}–0.3 to V_{SS}+18	V
$\overline{\text{RESET}}$ output voltage		$V_{\overline{RESET}}$		V
Power dissipation	8-Pin TSSOP	P_D	300 (When not mounted on board)	mW
			700*1	mW
	8-Pin SON(B)		300 (When not mounted on board)	mW
			750*1	mW
Operating ambient temperature		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–40 to +125	°C

***1.** When mounted on board

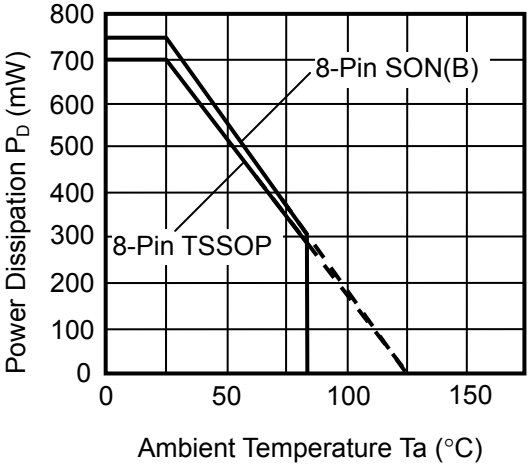
[Mounted board]

(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

(1) When mounted on board



(2) When not mounted on board

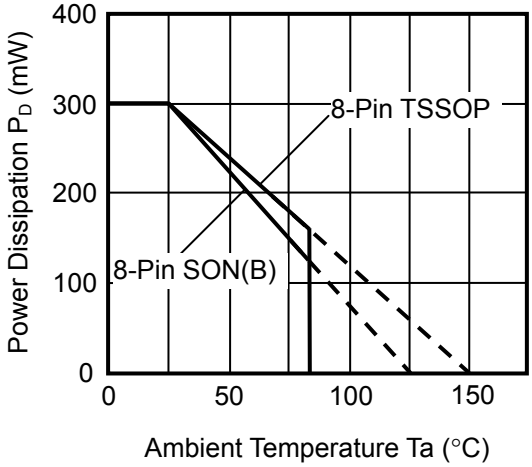


Figure 3 Power Dissipation of Package

■ Electrical Characteristics

S-8425AAAFT, S-8425AAAPA

Table 2 Electrical Characteristics

(Ta = 25°C, Unless otherwise specified)

	Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Voltage regulator	Output voltage 1	V_{RO}	V_{IN} = 7.2 V, I_{RO} = 3 mA		2.940	3.000	3.060	V	1
	Dropout voltage 1	V_{drop1}	I_{RO} = 3 mA		–	41	59	mV	
	Load stability 1	ΔV_{RO1}	V_{IN} =7.2 V, I_{RO} = 100 µA to 20 mA		–	50	100	mV	
	Input stability 1	ΔV_{RO2}	V_{IN} = 4 V to 16 V, I_{RO} = 3 mA		–	5	20	mV	
	Output voltage temperature coefficient 1	$\frac{\Delta V_{RO}}{\Delta Ta \bullet V_{RO}}$	Ta = –40°C to +85°C		–	±100	–	ppm/°C	
	Output voltage 2	V_{OUT}	V_{IN} = 7.2 V, I_{OUT} = 23 mA		2.940	3.000	3.060	V	
	Dropout voltage 2	V_{drop2}	I_{OUT} = 23 mA		–	187	252	mV	
	Load stability 2	ΔV_{OUT1}	V_{IN} = 7.2 V, I_{OUT} = 100 µA to 60 mA		–	50	100	mV	
	Input stability 2	ΔV_{OUT2}	V_{IN} = 4 V to 16 V, I_{OUT} = 23 mA		–	5	20	mV	
	Output voltage temperature coefficient 2	$\frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}$	Ta = –40°C to +85°C		–	±100	–	ppm/°C	
	Output voltage 3	V_{CH}	V_{IN} = 7.2 V, I_{CH} = 3 mA		3.234	3.300	3.366	V	
	Dropout voltage 3	V_{drop3}	I_{CH} = 3 mA		–	90	120	mV	
	Load stability 3	ΔV_{CH1}	V_{IN} = 7.2 V, I_{CH} = 100 µA to 10 mA		–	50	100	mV	
	Input stability 3	ΔV_{CH2}	V_{IN} = 4.3 V to 16 V, I_{CH} = 3 mA		–	5	20	mV	
	Output voltage temperature coefficient 3	$\frac{\Delta V_{CH}}{\Delta Ta \bullet V_{CH}}$	Ta = –40°C to +85°C		–	±100	–	ppm/°C	
	Primary power input voltage	V_{IN}	–		–	–	16	V	
Voltage detector	CS detection voltage	$-V_{DET1}$	V_{IN} voltage detection		3.234	3.300	3.366	V	2
	CS release voltage	$+V_{DET1}$	–		3.319	3.401	3.482	V	
	$\overline{\text{RESET}}$ detection voltage	$-V_{DET2}$	V_{OUT} voltage detection		2.156	2.200	2.244	V	
	$\overline{\text{RESET}}$ release voltage	$+V_{DET2}$	–		2.256	2.312	2.367	V	
	$\overline{\text{RESET}}$ release delay time	t_{DELAY}	–		0.3	0.8	–	ms	9
	Operating voltage	V_{opr}	V_{IN} or V_{BAT}		1.7	–	16	V	2
	Detection voltage temperature coefficient	$\frac{\Delta - V_{DET1}}{\Delta Ta \bullet (-V_{DET1})}$	Ta = –40°C to +85°C		–	±100	–	ppm/°C	
		$\frac{\Delta - V_{DET2}}{\Delta Ta \bullet (-V_{DET2})}$	Ta = –40°C to +85°C		–	±100	–	ppm/°C	
	Sink current	I_{SINK}	V_{DS} = 0.5 V, V_{IN} = V_{BAT} = 2.0 V	$\overline{\text{RESET}}$	1.50	2.30	–	mA	3
				CS	1.50	2.30	–	mA	
	Leakage current	I_{LEAK}	V_{DS} = 16 V, V_{IN} = 16 V		–	–	0.1	µA	
Switch unit	Switch voltage	V_{SW1}	V_{BAT} = 2.8 V, V_{IN} voltage detection		$+V_{DET1}$ × 0.83	$+V_{DET1}$ × 0.85	$+V_{DET1}$ × 0.87	V	4
	CS output inhibit voltage	V_{SW2}	V_{BAT} = 3 V, V_{OUT} voltage detection		V_{OUT} × 0.93	V_{OUT} × 0.95	V_{OUT} × 0.97	V	5
	V_{BAT} switch leakage current	I_{LEAK}	V_{IN} = 3.6 V, V_{BAT} = 0 V		–	–	0.1	µA	6
	V_{BAT} switch resistance	R_{SW}	V_{IN} = Open, V_{BAT} = 3 V, I_{OUT} = 10 µA to 500 µA		–	30	60	Ω	7
	Switch voltage temperature coefficient	$\frac{\Delta V_{SW1}}{\Delta Ta \bullet V_{SW1}}$	Ta = –40°C to +85°C		–	±100	–	ppm/°C	4
	CS output inhibit voltage temperature coefficient	$\frac{\Delta V_{SW2}}{\Delta Ta \bullet V_{SW2}}$	Ta = –40°C to +85°C		–	±100	–	ppm/°C	5
Total	Current consumption	I_{SS1}	V_{IN} = 3.6 V, Unload		–	7	15	µA	8
		I_{BAT1}	V_{BAT} = 3 V		–	–	0.1	µA	
		I_{BAT2}	V_{IN} = Open, V_{BAT} = 3 V, Unload	Ta = 25°C	–	1.0	2.1	µA	
				Ta = 85°C	–	–	3.5	µA	
	Backup power supply input voltage	V_{BAT}	–		2.0	–	4.0	V	7

Remark The number in the Test Circuit column corresponds to the circuit number in the **Test Circuits** section.

S-8425AAGFT

Table 3 Electrical Characteristics

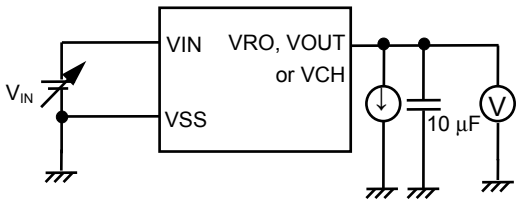
(Ta = 25°C, Unless otherwise specified)

	Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Voltage regulator	Output voltage 1	V_{RO}	V_{IN} = 7.2 V, I_{RO} = 3 mA		2.940	3.000	3.060	V	1
	Dropout voltage 1	V_{drop1}	I_{RO} = 3 mA		–	41	59	mV	
	Load stability 1	ΔV_{RO1}	V_{IN} =7.2 V, I_{RO} = 100 μA to 20 mA		–	50	100	mV	
	Input stability 1	ΔV_{RO2}	V_{IN} = 4 V to 16 V, I_{RO} = 3 mA		–	5	20	mV	
	Output voltage temperature coefficient 1	$\frac{\Delta V_{RO}}{\Delta Ta \bullet V_{RO}}$	Ta = –40°C to +85°C		–	±100	–	ppm/°C	
	Output voltage 2	V_{OUT}	V_{IN} = 7.2 V, I_{OUT} = 23 mA		2.744	2.800	2.856	V	
	Dropout voltage 2	V_{drop2}	I_{OUT} = 23 mA		–	187	252	mV	
	Load stability 2	ΔV_{OUT1}	V_{IN} = 7.2 V, I_{OUT} = 100 μA to 60 mA		–	50	100	mV	
	Input stability 2	ΔV_{OUT2}	V_{IN} = 3.8 V to 16 V, I_{OUT} = 23 mA		–	5	20	mV	
	Output voltage temperature coefficient 2	$\frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}$	Ta = –40°C to +85°C		–	±100	–	ppm/°C	
	Output voltage 3	V_{CH}	V_{IN} = 7.2 V, I_{CH} = 3 mA		2.744	2.800	2.856	V	
	Dropout voltage 3	V_{drop3}	I_{CH} = 3 mA		–	90	120	mV	
	Load stability 3	ΔV_{CH1}	V_{IN} = 7.2 V, I_{CH} = 100 μA to 10 mA		–	50	100	mV	
	Input stability 3	ΔV_{CH2}	V_{IN} = 3.8 V to 16 V, I_{CH} = 3 mA		–	5	20	mV	
	Output voltage temperature coefficient 3	$\frac{\Delta V_{CH}}{\Delta Ta \bullet V_{CH}}$	Ta = –40°C to +85°C		–	±100	–	ppm/°C	
	Primary power input voltage	V_{IN}	–		–	–	16	V	
Voltage detector	CS detection voltage	$-V_{DET1}$	V_{IN} voltage detection		4.214	4.300	4.386	V	2
	CS release voltage	$+V_{DET1}$	–		4.335	4.441	4.548	V	
	$\overline{RESET}$ detection voltage	$-V_{DET2}$	V_{OUT} voltage detection		1.764	1.800	1.836	V	
	$\overline{RESET}$ release voltage	$+V_{DET2}$	–		1.835	1.880	1.925	V	
	$\overline{RESET}$ release delay time	t_{DELAY}	–		0.3	0.8	–	ms	9
	Operating voltage	V_{opr}	V_{IN} or V_{BAT}		1.7	–	16	V	2
	Detection voltage temperature coefficient	$\frac{\Delta - V_{DET1}}{\Delta Ta \bullet (-V_{DET1})}$	Ta = –40°C to +85°C		–	±100	–	ppm/°C	
		$\frac{\Delta - V_{DET2}}{\Delta Ta \bullet (-V_{DET2})}$	Ta = –40°C to +85°C		–	±100	–	ppm/°C	
	Sink current	I_{SINK}	V_{DS} = 0.5 V	$\overline{RESET}$	1.50	2.30	–	mA	3
			V_{IN} = V_{BAT} = 2.0 V	CS	1.50	2.30	–	mA	
	Leakage current	I_{LEAK}	V_{DS} = 16 V, V_{IN} = 16 V		–	–	0.1	μA	
Switch unit	Switch voltage	V_{SW1}	V_{BAT} = 2.8 V, V_{IN} voltage detection		$+V_{DET1}$ × 0.83	$+V_{DET1}$ × 0.85	$+V_{DET1}$ × 0.87	V	4
	CS output inhibit voltage	V_{SW2}	V_{BAT} = 3 V, V_{OUT} voltage detection		V_{OUT} × 0.93	V_{OUT} × 0.95	V_{OUT} × 0.97	V	5
	V_{BAT} switch leakage current	I_{LEAK}	V_{IN} = 3.6 V, V_{BAT} = 0 V		–	–	0.1	μA	6
	V_{BAT} switch resistance	R_{SW}	V_{IN} = Open, V_{BAT} = 3 V, I_{OUT} = 10 μA to 500 μA		–	30	60	Ω	7
	Switch voltage temperature coefficient	$\frac{\Delta V_{SW1}}{\Delta Ta \bullet V_{SW1}}$	Ta = –40°C to +85°C		–	±100	–	ppm/°C	4
	CS output inhibit voltage temperature coefficient	$\frac{\Delta V_{SW2}}{\Delta Ta \bullet V_{SW2}}$	Ta = –40°C to +85°C		–	±100	–	ppm/°C	5
Total	Current consumption	I_{SS1}	V_{IN} = 3.6 V, Unload		–	7	15	μA	8
		I_{BAT1}	V_{BAT} = 3 V		–	–	0.1	μA	
		I_{BAT2}	V_{IN} = Open, V_{BAT} = 3 V Unload	Ta = 25°C	–	1.0	2.1	μA	
				Ta = 85°C	–	–	3.5	μA	
	Backup power supply input voltage	V_{BAT}	–		2.0	–	4.0	V	7

Remark The number in the Test Circuit column corresponds to the circuit number in the **Test Circuits** section.

■ Test Circuits

1.



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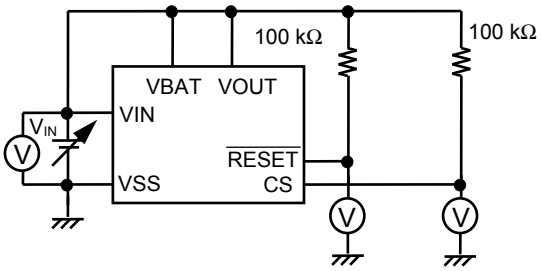

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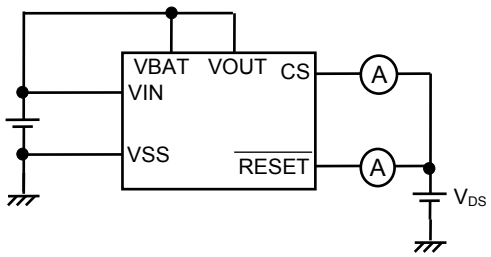

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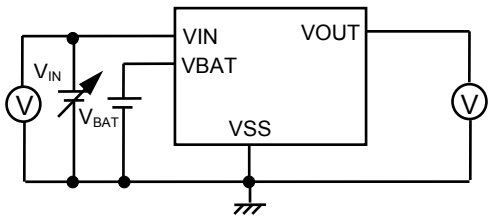
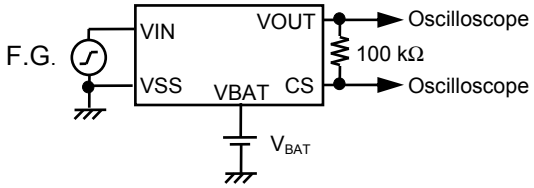


Measure the value after applying 6 V to VIN.

5.



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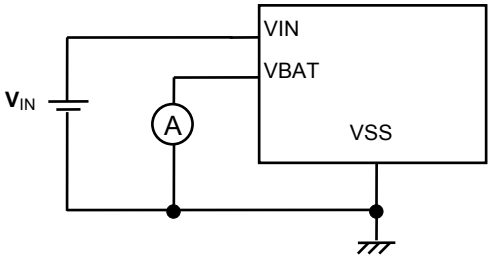
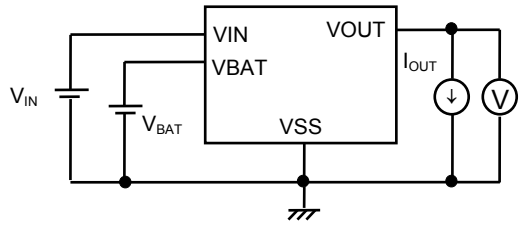
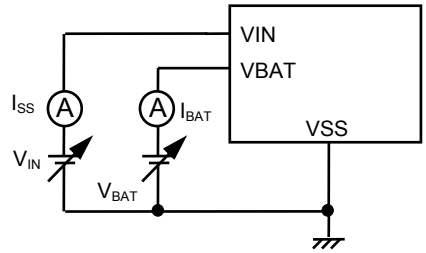


7.



Leave open and measure the value after applying 6 V to VIN.

8.



To measure I_{BAT2}, apply 6 V to VIN and then leave VIN open and measure I_{BAT}.

9.

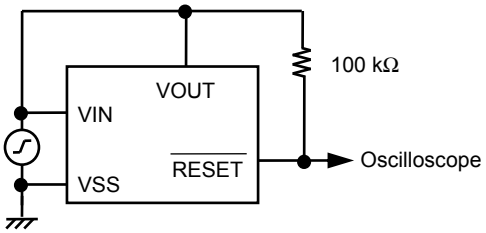
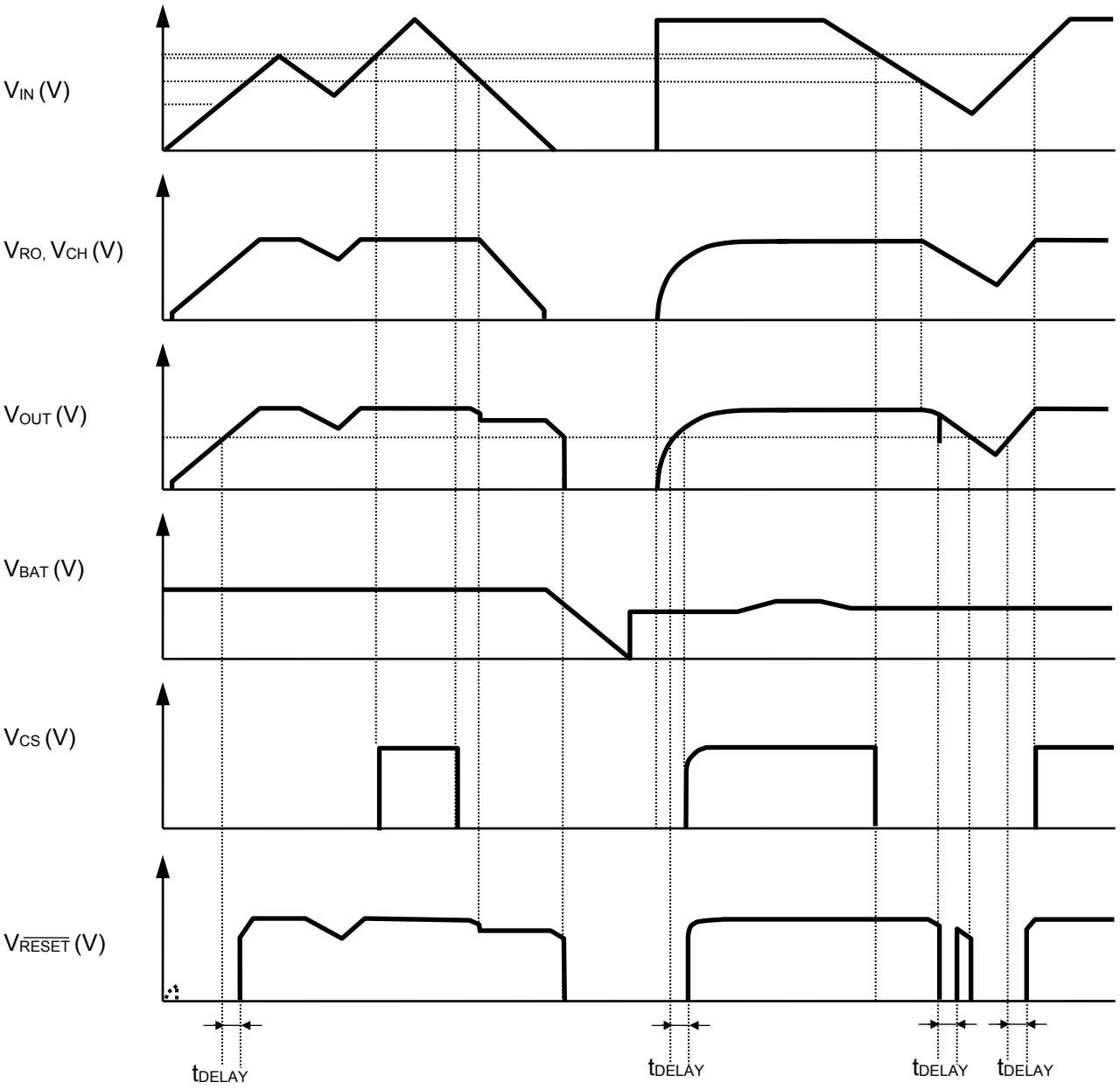


Figure 4 Test Circuits

■ Timing Chart



Remark CS and $\overline{\text{RESET}}$ are pulled up to V_{OUT}. The Y-axis is an arbitrary scale.

Figure 5 Timing Chart

■ Operation

The internal configuration of the S-8425 Series is as follows.

- Voltage regulator 1, which stabilizes input voltage V_{IN} and outputs it to V_{RO}
- Voltage regulator 2, which stabilizes input voltage V_{IN} and outputs it to V_{OUT}
- Voltage regulator 3, which stabilizes input voltage V_{IN} and outputs it to V_{CH}
- CS voltage detector, which monitors input voltage V_{IN}
- $\overline{\text{RESET}}$ voltage detector, which monitors output voltage V_{OUT}
- Switch unit

The functions and operations of the above-listed elements are described below.

1. Voltage Regulators

The S-8425 Series features on-chip voltage regulators with a small dropout voltage. The voltage of the VRO, VOUT, and VCH pins (the output pins of the voltage regulator) can separately be selected for the output voltage in 0.1 V steps between the range of 2.3 to 5.4 V.

[Dropout voltage V_{drop1}, V_{drop2}, V_{drop3}]

Assume that the voltage output from the VRO pin is $V_{RO(E)}$ under the conditions of output voltage 1 described in the electrical characteristics table. V_{IN1} is defined as the input voltage at which the output voltage from the VRO pin becomes 98% of $V_{RO(E)}$ when the input voltage V_{IN} is decreased. Then, the dropout voltage V_{drop1} is calculated by the following expression.

$$V_{drop1} = V_{IN1} - V_{RO(E)} \times 0.98$$

Similarly, assume that the voltage of the VOUT pin is $V_{OUT(E)}$, and $V_{CH(E)}$ respectively under the conditions of output voltage 2 and 3 described in the electrical characteristics table. V_{IN2} and V_{IN3} are defined as the input voltages at which the output voltage from the VOUT pin becomes 98% of $V_{OUT(E)}$ and $V_{CH(E)}$, respectively. Then, the dropout voltages V_{drop2} and V_{drop3} are calculated by the following expression.

$$V_{drop2} = V_{IN2} - V_{OUT(E)} \times 0.98$$
$$V_{drop3} = V_{IN3} - V_{CH(E)} \times 0.98$$

2. Voltage Detector

The S-8425 Series incorporates two high-precision, low power consuming voltage detectors with hysteresis characteristics. The power of the CS voltage detector is supplied from the VIN and VBAT pins. Therefore, the output is stable as long as the primary or backup power supply is within the operating voltage range (1.7 to 16 V). All outputs are Nch open-drain, and need pull-up resistors of about 100 kΩ.

2.1 CS Voltage Detector

The CS voltage detector monitors the input voltage V_{IN} (VIN pin voltage). The detection voltage can be selected from between 2.4 and 5.3 V in 0.1 V steps. The result of detection is output at the CS pin: "Low" for lower voltage than the detection level and "High" for higher voltage than the release level (however, when the VOUT pin voltage is the CS output inhibit voltage (V_{SW2}), a low level is output).

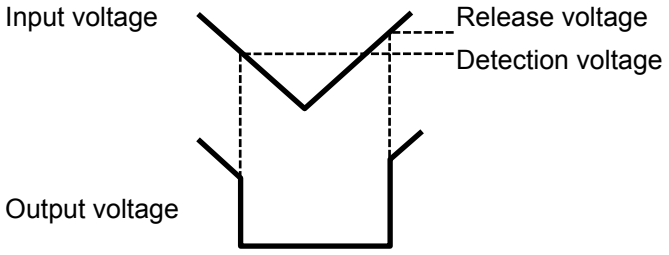


Figure 6 Definition of Detection and Release Voltages

2.2 $\overline{\text{RESET}}$ Voltage Detector

The $\overline{\text{RESET}}$ voltage detector monitors the output voltage V_{OUT} (VOUT pin voltage). The detection voltage can be selected from between 1.7 V and 3.4 V in 0.1 V steps. The result of detection is output at the $\overline{\text{RESET}}$ pin: "Low" for a lower voltage than the detection level and "High" for a higher voltage than the release level. $\overline{\text{RESET}}$ outputs the normal logic if the V_{OUT} pin voltage is 1.0 V or more.

The S-8425 Series incorporates a $\overline{\text{RESET}}$ release delay circuit.

[$\overline{\text{RESET}}$ release delay time (t_{DELAY})]

The interval from when the VOUT pin voltage exceeds the $\overline{\text{RESET}}$ release voltage value ($+V_{DET2}$) until the output of the $\overline{\text{RESET}}$ pin is actually inverted is called the $\overline{\text{RESET}}$ release delay time.

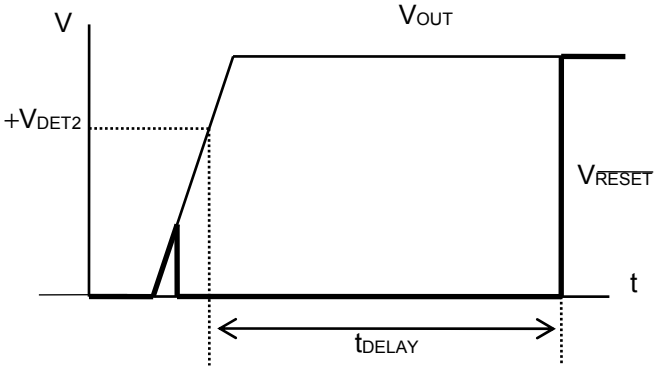


Figure 7 Definition of RESET Release Delay Time (t_{DELAY})

3. Switch Unit

The switch unit consists of the V_{SW1} and V_{SW2} detectors, a switch controller, voltage regulator 2, and switch transistor M1 (see **Figure 8 Switch Unit**).

3.1 V_{SW1} Detector

The V_{SW1} detector monitors the power supply voltage V_{IN} and sends the results of detection to the switch controller. The detection voltage (V_{SW1}) can be set to 77 ±2% or 85 ±2% of the CS release voltage $+V_{DET1}$.

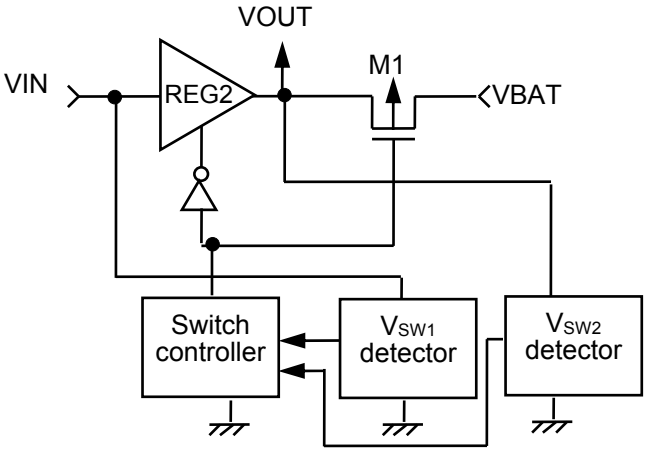


Figure 8 Switch Unit

3.2 V_{SW2} Detector

The V_{SW2} detector monitors the VOUT pin voltage and keeps the CS release voltage output low until the VOUT pin voltage rises to V_{SW2} voltage. The CS pin output then changes from low to high if the VIN pin voltage is more than the CS release voltage ($+V_{DET1}$) when the VOUT pin voltage rises to 95 ±2% of the output voltage of voltage regulator 2 (V_{OUT}). The CS pin output changes from high to low regardless of the V_{SW2} voltage when the VIN pin voltage drops to less than the CS detection voltage ($-V_{DET1}$).
The CS pin output remains high if the VIN pin voltage stays higher than the CS detection voltage ($-V_{DET1}$) when the VOUT pin voltage drops to less than the V_{SW2} voltage due to an undershoot.

3.3 Switch Controller

The switch controller controls voltage regulator 2 and switch transistor M1. There are two statuses corresponding to the power supply voltage V_{IN} (or power supply voltage V_{BAT}) sequence: a special sequence status and a normal sequence status. When the power supply voltage V_{IN} rises and becomes equal to or exceeds the CS release voltage ($+V_{DET1}$), the normal sequence status is entered, but until then the special sequence status is maintained.

(1) Special sequence status
The switch controller sets voltage regulator 2 ON and switch transistor M1 OFF from the initial status until the primary power supply voltage V_{IN} is connected and reaches more than the CS release voltage ($+V_{DET1}$) in order to prevent consumption of the backup power supply regardless of the V_{SW1} detector status. This status is called the special sequence status.

(2) Normal sequence status
The switch controller enters the normal sequence status from the special sequence status once the primary power supply voltage V_{IN} reaches more than the CS release voltage ($+V_{DET1}$).
Once the normal sequence is entered, the switch controller switches voltage regulator 2 and switch transistor M1 ON/OFF as shown in Table 4 according to the power supply voltage V_{IN}. The time required for voltage regulator 2 to be switched from OFF to ON is a few hundred μs at most. During this interval, voltage regulator 2 and switch transistor M1 may both switch OFF and the VOUT pin voltage may drop. To prevent this, connect a capacitor of 10 μF or more to the VOUT pin.
When the VOUT pin voltage becomes lower than the $\overline{\text{RESET}}$ detection voltage, the status returns to the special sequence status.

Table 4 ON/OFF Switching of Voltage Regulator 2 and Switch Transistor M1 According to Power Supply Voltage V_{IN}

Power Supply Voltage V_{IN}	Voltage Regulator 2	Switch Transistor M1	VOUT Pin Voltage
$V_{IN} > V_{SW1}$	ON	OFF	V_{OUT}
$V_{IN} < V_{SW1}$	OFF	ON	$V_{BAT} - V_{dif}$

3.4 Switch Transistor M1

Voltage regulator 2 is also used to switch from the VIN pin to the VOUT pin. Therefore, no reverse current flows from the VOUT pin to the VIN pin when voltage regulator 2 is OFF.
The output voltage of voltage regulator 2 can be selected from between 2.3 V and 5.4 V in 0.1 V steps.

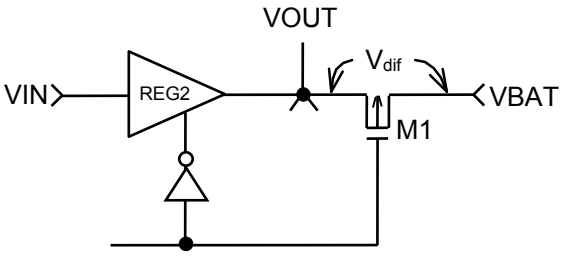


Figure 9 Definition of V_{dif}

The on-resistance of switch transistor M1 is 60 Ω or lower (I_{OUT} = 10 to 500 μA).
Therefore, when M1 is switched ON and the VOUT pin is connected to the VBAT pin, the voltage drop V_{dif} caused by M1 is 60 × I_{OUT} (output current) at maximum, and $V_{BAT} - V_{dif}$ (max.) is output to the VOUT pin at minimum.
When voltage regulator 2 is ON and M1 is OFF, the leakage current of M1 is kept below 0.1 μA max. (V_{IN} = 6 V, Ta = 25°C) with the VBAT pin grounded (VSS pin).

■ Transient Response

1. Line Transient Response Against Input Voltage Variation

The input voltage variation differs depending on whether the power supply input (0 V→10 V square wave) is applied or the power supply variation (6 V↔10 V square waves) is applied. This section describes the ringing waveforms and parameter dependency of each type. The test circuit is shown for reference.

Power supply application: 0 V→10 V square wave

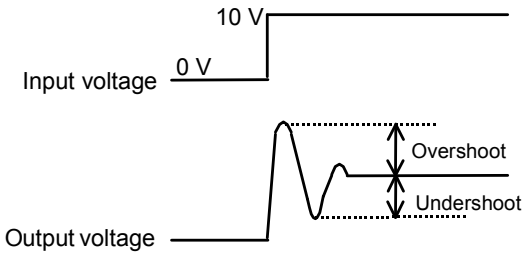


Figure 10 Power Supply Application: 0 V→10 V Square Wave

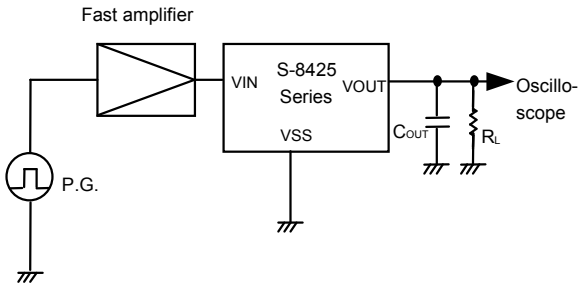


Figure 11 Test Circuit

Power Supply Application

VOUT pin

C_{OUT} = 22 μF, I_{OUT} = 50 mA, Ta = 25°C

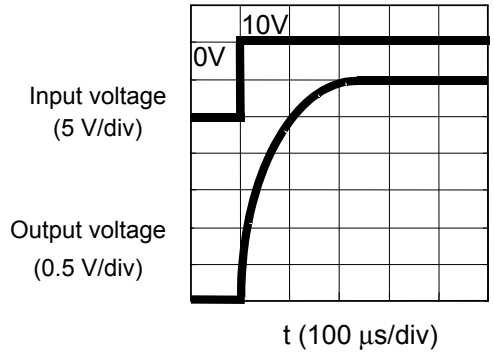


Figure 12 Ringing Waveform of Power Supply Application (VOUT Pin)

VRO pin

C_{RO} = 22 μF, I_{RO} = 30 mA, Ta = 25°C

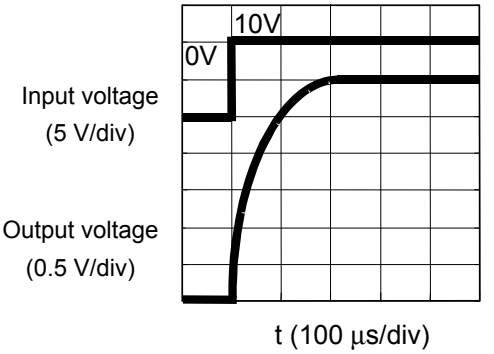


Figure 13 Ringing Waveform of Power Supply Application (VRO Pin)

VCH pin

C_{CH} = 10 μF, I_{CH} = 10 mA, Ta = 25°C

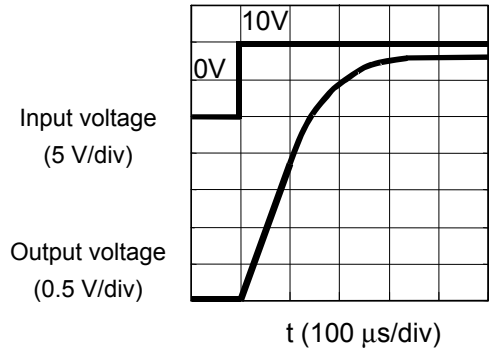


Figure 14 Ringing Waveform of Power Supply Application (VCH Pin)

Power supply variation: 6 V↔10 V square waves

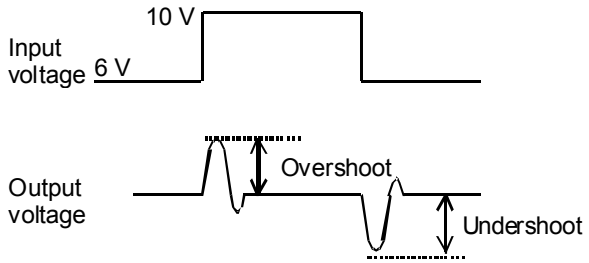


Figure 15 Power Supply Variation: 6 V↔10 V Square Waves

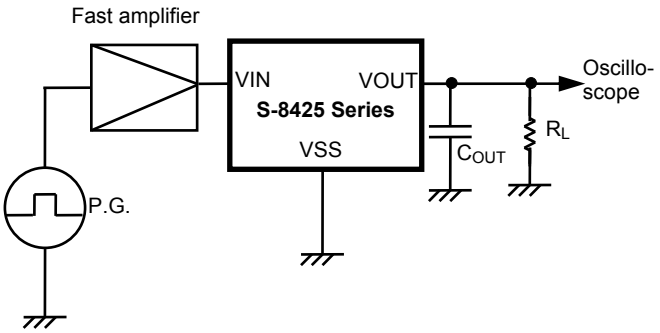


Figure 16 Test Circuit

Power Supply Variation

VOUT pin

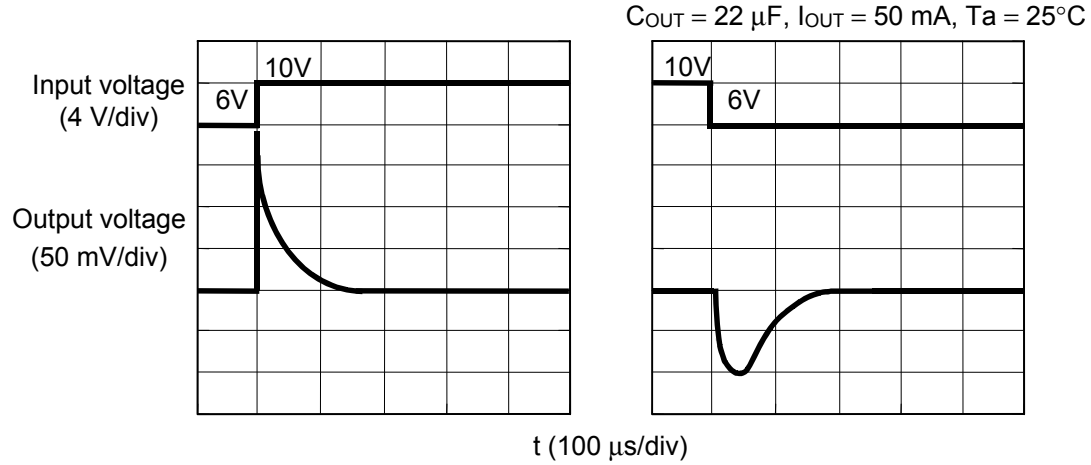


Figure 17 Ringing Waveform of Power Supply Variation (VOUT Pin)

VRO pin

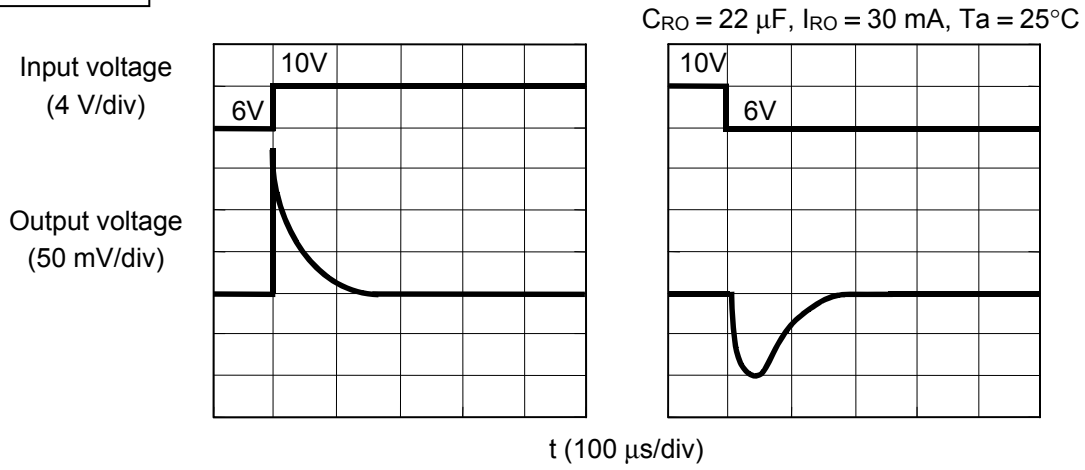


Figure 18 Ringing Waveform of Power Supply Variation (VRO Pin)

VCH pin

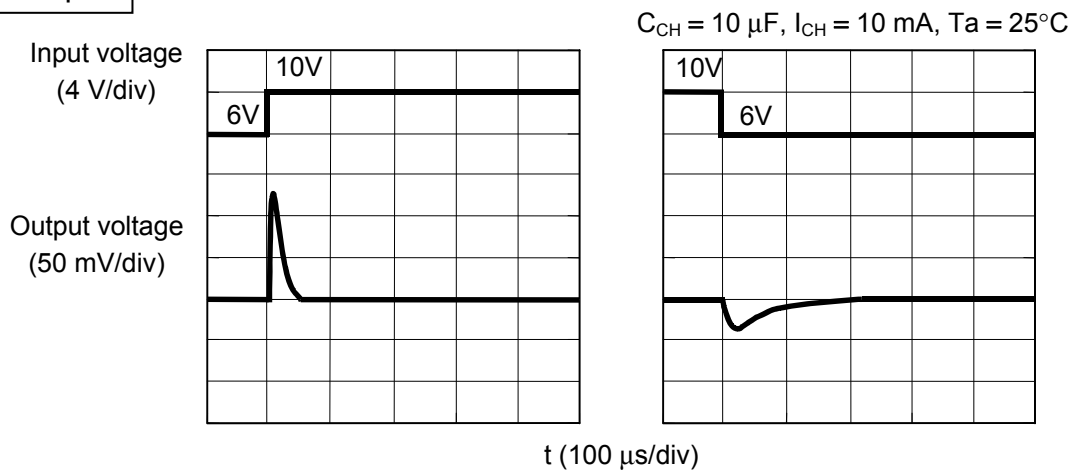


Figure 19 Ringing Waveform of Power Supply Variation (VCH Pin)

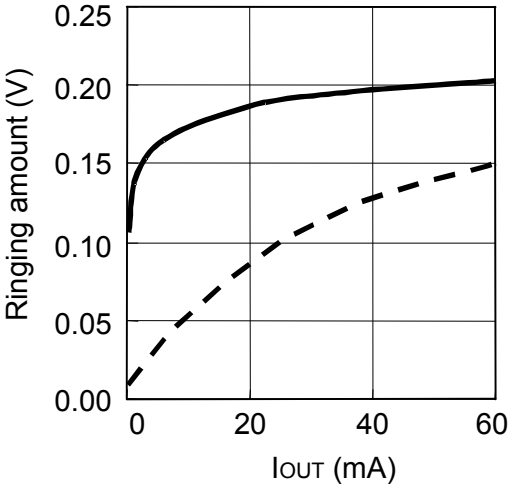
Reference data: Dependency of output current (I_{OUT}), load capacitance (C_{OUT}), input variation width (ΔV_{IN}), temperature (Ta)

For reference, the following pages describe the results of measuring the ringing amounts at the VOUT and VRO pins using the output current (I_{OUT}), load capacitance (C_{OUT}), input variation width (ΔV_{IN}), and temperature (Ta) as parameters.

1.1 I_{OUT} Dependency

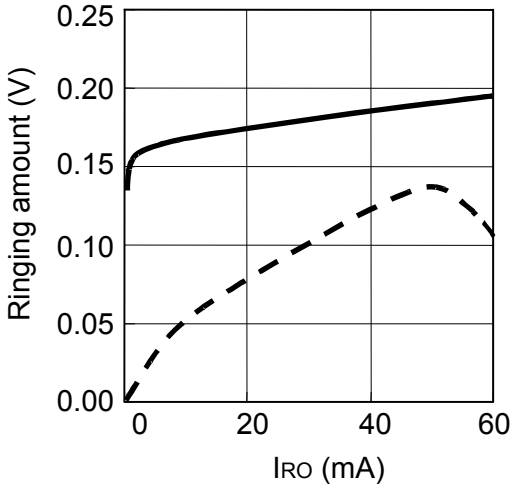
(1) VOUT pin

C_{OUT} = 22 µF, V_{IN} = 6 V↔10 V, Ta = 25°C



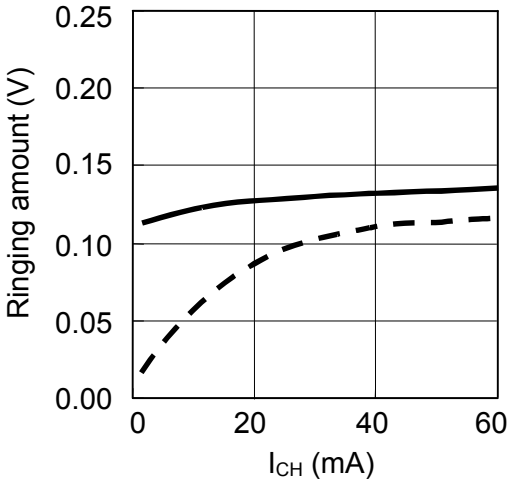
(2) VRO pin

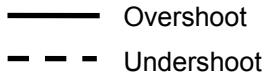
C_{RO} = 22 µF, V_{IN} = 6 V↔10 V, Ta = 25°C



(3) VCH pin

C_{CH} = 10 µF, V_{IN} = 6 V↔10 V, Ta = 25°C

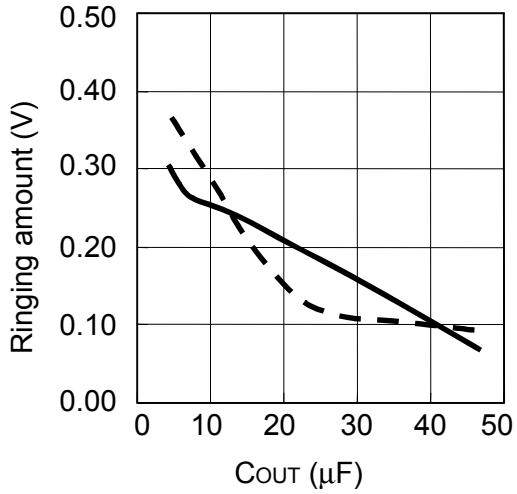




1.2 C_{OUT} Dependency

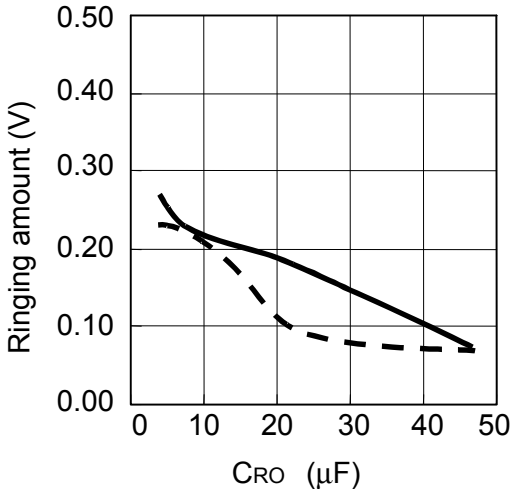
(1) VOUT pin

I_{OUT} = 50 mA, V_{IN} = 6 V↔10 V, Ta = 25°C



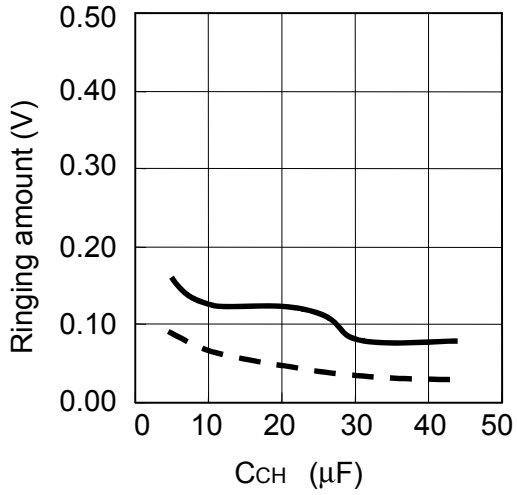
(2) VRO pin

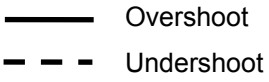
I_{RO} = 30 mA, V_{IN} = 6 V↔10 V, Ta = 25°C



(3) VCH pin

I_{CH} = 10 mA, V_{IN} = 6 V↔10 V, Ta = 25°C



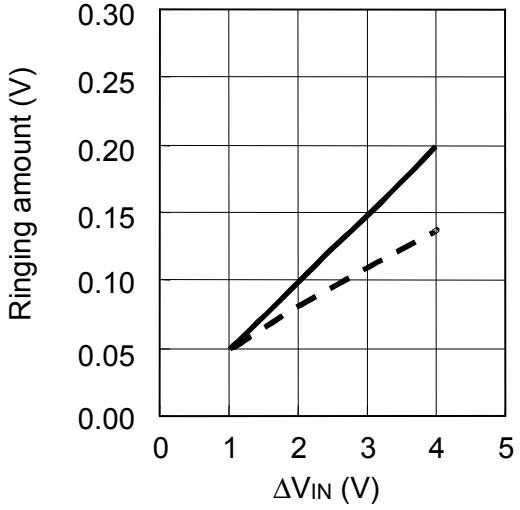


1.3 ΔV_{IN} Dependency

ΔV_{IN} shows the difference between the low voltage fixed to 6 V and the high voltage.
For example, ΔV_{IN} = 2 V means the difference between 6 V and 8 V.

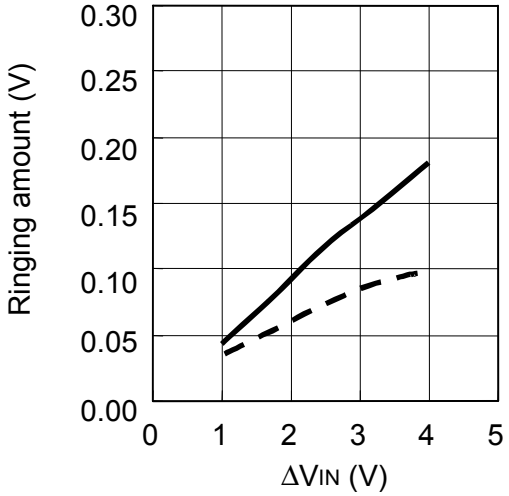
(1) VOUT pin

I_{OUT} = 50 mA, C_{OUT} = 22 µF, Ta = 25°C



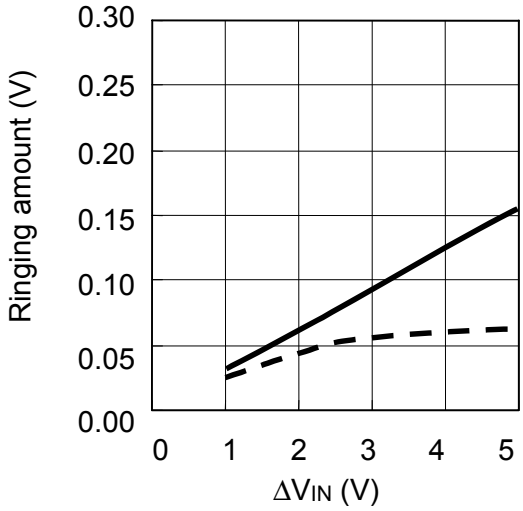
(2) VRO pin

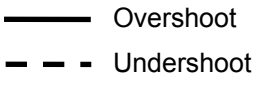
I_{RO} = 30 mA, C_{RO} = 22 µF, Ta = 25°C



(3) VCH pin

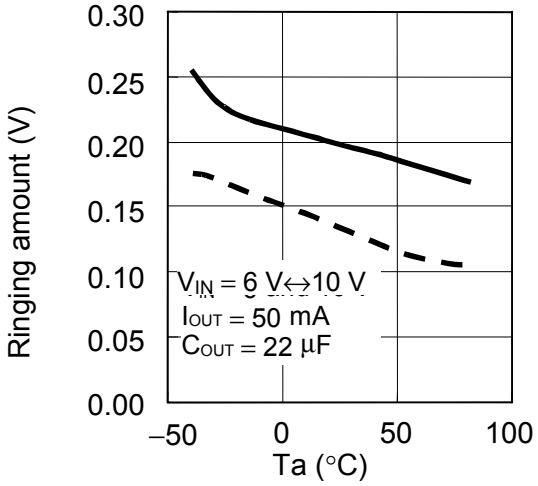
I_{CH} = 10 mA, C_{CH} = 10 µF, Ta = 25°C



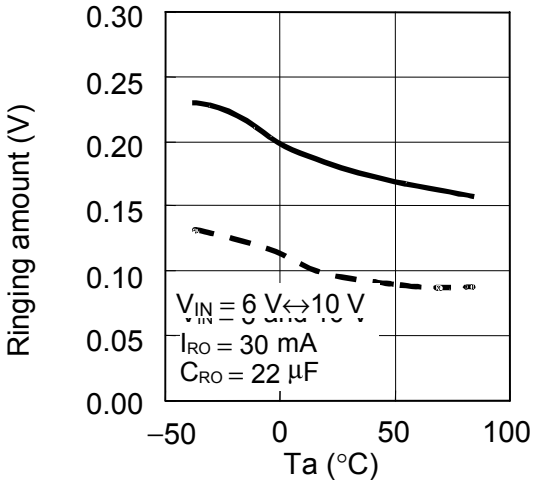


1.4 Temperature Dependency

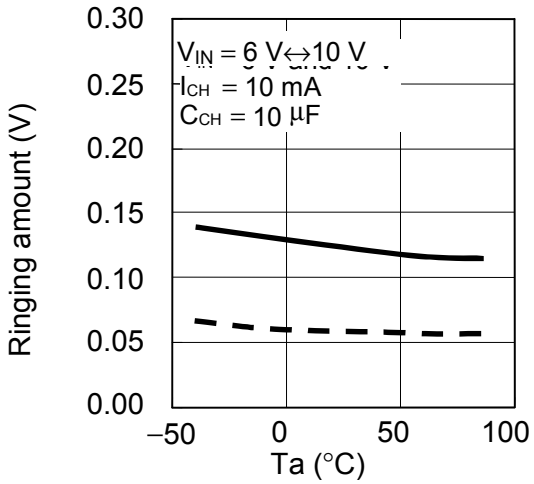
(1) VOUT pin



(2) VRO pin



(3) VCH pin



2. Load Transient Response Based on Output Current Fluctuation

The overshoot and undershoot are caused in the output voltage if the output current fluctuates between 10 μA and 50 mA (V_{RO} is between 10 μA and 30 mA, V_{CH} is between 10 μA and 10 mA) while the input voltage is constant. Figure 20 shows the output voltage variation due to the output current. Figure 21 shows the test circuit for reference. The latter half of this section describes ringing waveform and parameter dependency.

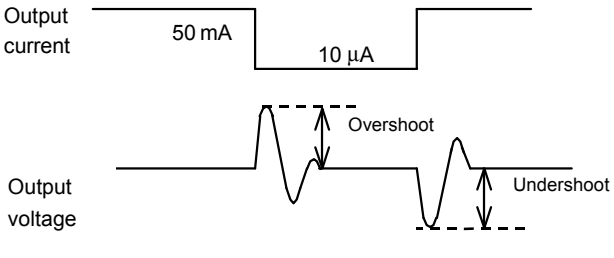


Figure 20 Output Voltage Variation due to Output Current

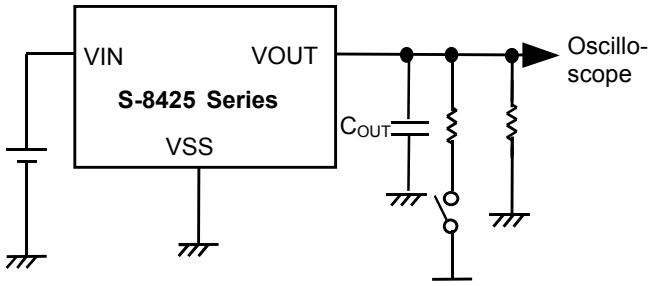


Figure 21 Test Circuit

Figures 22 to 24 show the ringing waveforms at the VOUT, VRO, and VCH pins due to the load variation.

VOUT pin

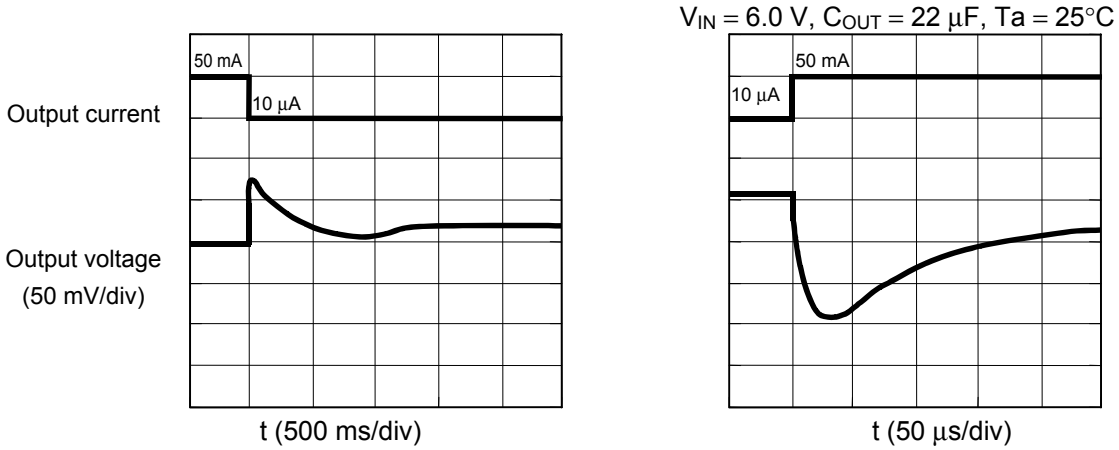


Figure 22 Ringing Waveform due to Load Variation (VOUT Pin)

VRO pin

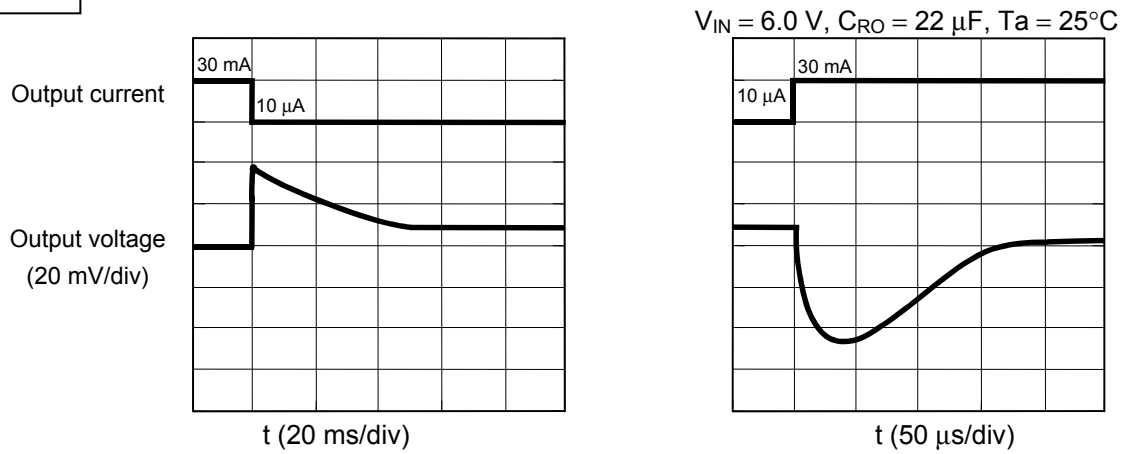


Figure 23 Ringing Waveform due to Load Variation (VRO Pin)

VCH pin

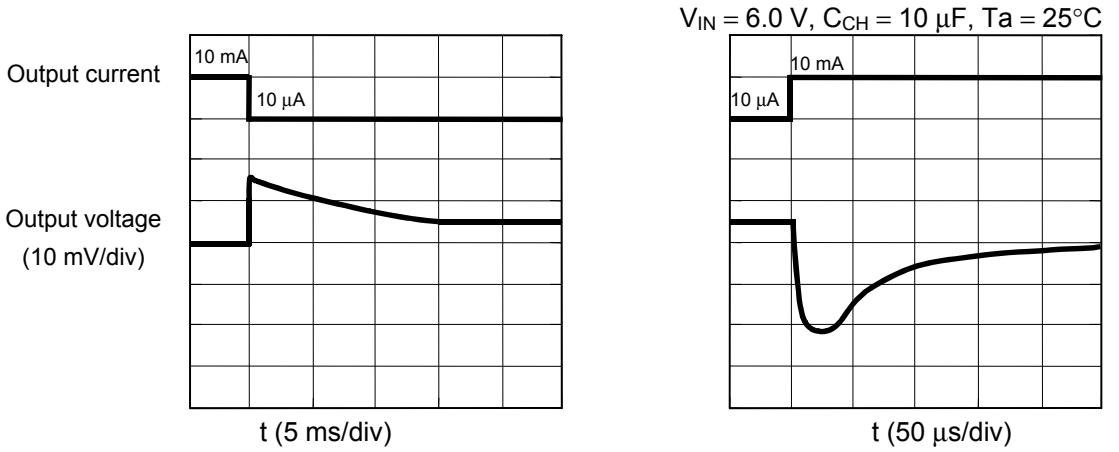


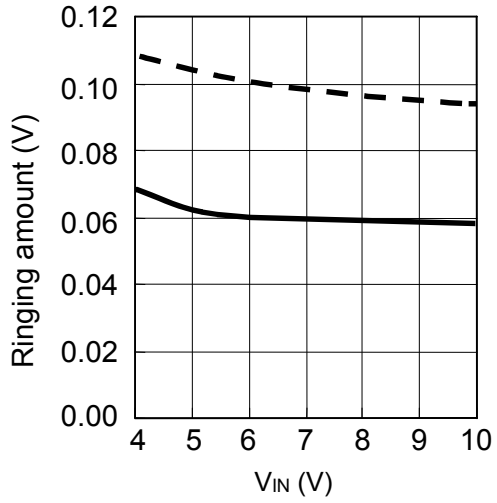
Figure 24 Ringing Waveform due to Load Variation (VCH Pin)

Reference data: Dependency of input voltage (V_{IN}), load capacitance (C_{OUT}), output variation width (ΔI_{OUT}), temperature (Ta)

2.1 V_{IN} Dependency

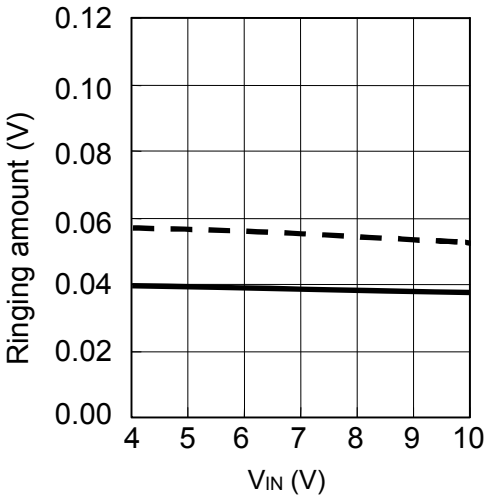
(1) VOUT pin

C_{OUT} = 22 µF, I_{OUT} = 50 mA↔10 µA, Ta = 25°C



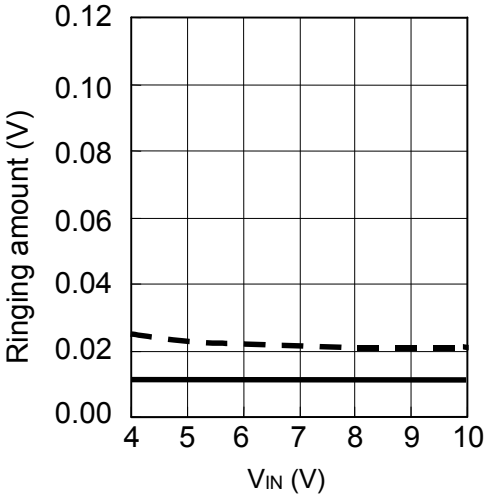
(2) VRO pin

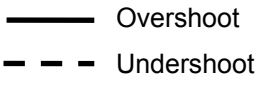
C_{RO} = 22 µF, I_{RO} = 30 mA↔10 µA, Ta = 25°C



(3) VCH pin

C_{CH} = 10 µF, I_{CH} = 10 mA↔10 µA, Ta = 25°C

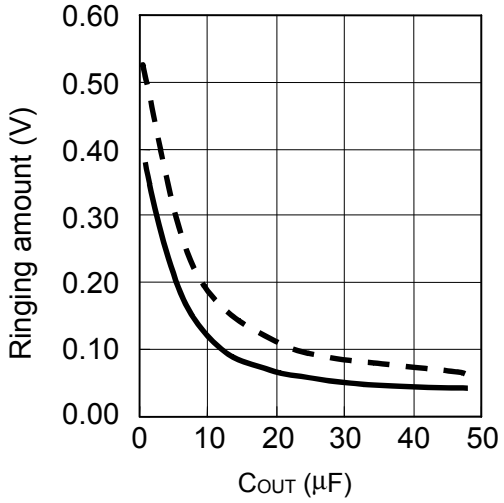




2.2 C_{OUT} Dependency

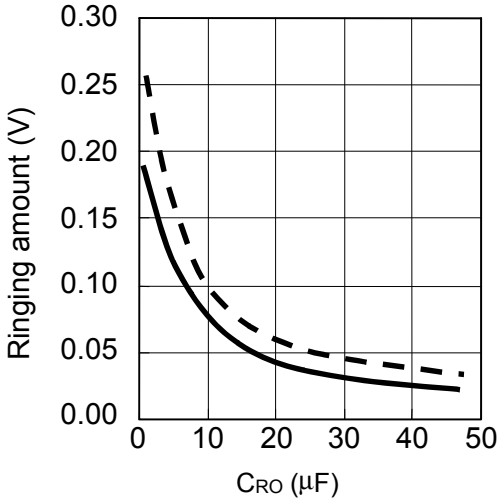
(1) VOUT pin

V_{IN} = 6.0 V, I_{OUT} = 50 mA↔10 μA, Ta = 25°C



(2) VRO pin

V_{IN} = 6.0 V, I_{RO} = 30 mA↔10 μA, Ta = 25°C



(3) VCH pin

C_{CH} = 10 μF, I_{CH} = 10 mA↔10 μA, Ta = 25°C