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Freescale Semiconductor
User's Guide

Document Number: MC9S12ZVM128MCBUG
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S12ZVM12EVB Evaluation Board User Guide

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1 Introduction

The S12ZVMx12EVB board is designed to drive 3-phase BLDC or PMSM motors, enabling implementation of motor control techniques:

- Sensor-less:
  - Back-EMF signal sensing using the MCU integrated ADC modules
  - Back-EMF zero-cross signal monitoring using MCU integrated comparators
- Sensor-based:
  - Hall sensor signal monitoring
  - Resolver sin/cos signal monitoring

The board features the S12ZVM, a 16-bit automotive microcontroller from the MagniV family. This System on Chip integrates an S12Z microcontroller with a Local Interconnect Network (LIN) physical interface, a 5-V regulator and a Gate Driver Unit (GDU). The motor power stage comprises 6 N-channel power MOSFETs that are controlled by the MCU integrated GDU.

A USB to SCI interface is available and can be used for FreeMaster PC-based application control. An integrated OSBDM debugger interface is also provided for easy programming/debugging of the S12ZVM microcontroller device.

The board is available in the following versions:

- S12ZVML12EVBLIN – Features the MC9S12ZVML12, with integrated LINPHY

- S12ZVMC12EVBCAN – Features the MC9S12ZVMC12, with a Voltage Regulator controller to supply an external CAN transceiver
- MTRCKTSBNZVM128 – Motor Control Kit integrating the S12ZVML12EVBLIN Evaluation Board with a 3-phase BLDC Motor with Hall sensor, running a sensorless control application using Back-EMF zero-crossing detection

1.1 EVB Features

- MC9S12ZVML12MKH or MC9S12ZVMC12MKH microcontroller, 64LQFP package
- BDM interface for MCU code download and debugging, via 6-pin header
- On-board OSBDM for MCU code download and debugging, via USB connector
- 6 N-channel Power MOSFETs in 3-phase half H-bridge array
- Motor Control Interface:
  - Hall Sensor
  - Resolver interface
  - SINCOS interface
- Connectivity:
  - LIN
  - CAN
  - USB-to-SCI serial port
- Phase and DC-bus current sensing circuits
- LED indicators:
  - Supply voltage indicator
  - Reset indicator
  - VDDX (MCU 5 V supply) indicator
  - FAULT indicator
- Over-voltage and over-current FAULT indicator with potentiometer adjustments
- 2 general-purpose, user configurable LEDs
- 2 general-purpose, user configurable push buttons
- 1 general-purpose, user configurable switch
- Optional 4 MHz external oscillator
- 1 general-purpose Potentiometer

1.2 Board Architecture

The S12VMx12EVB Controller Board basic building blocks are depicted in the following figure.

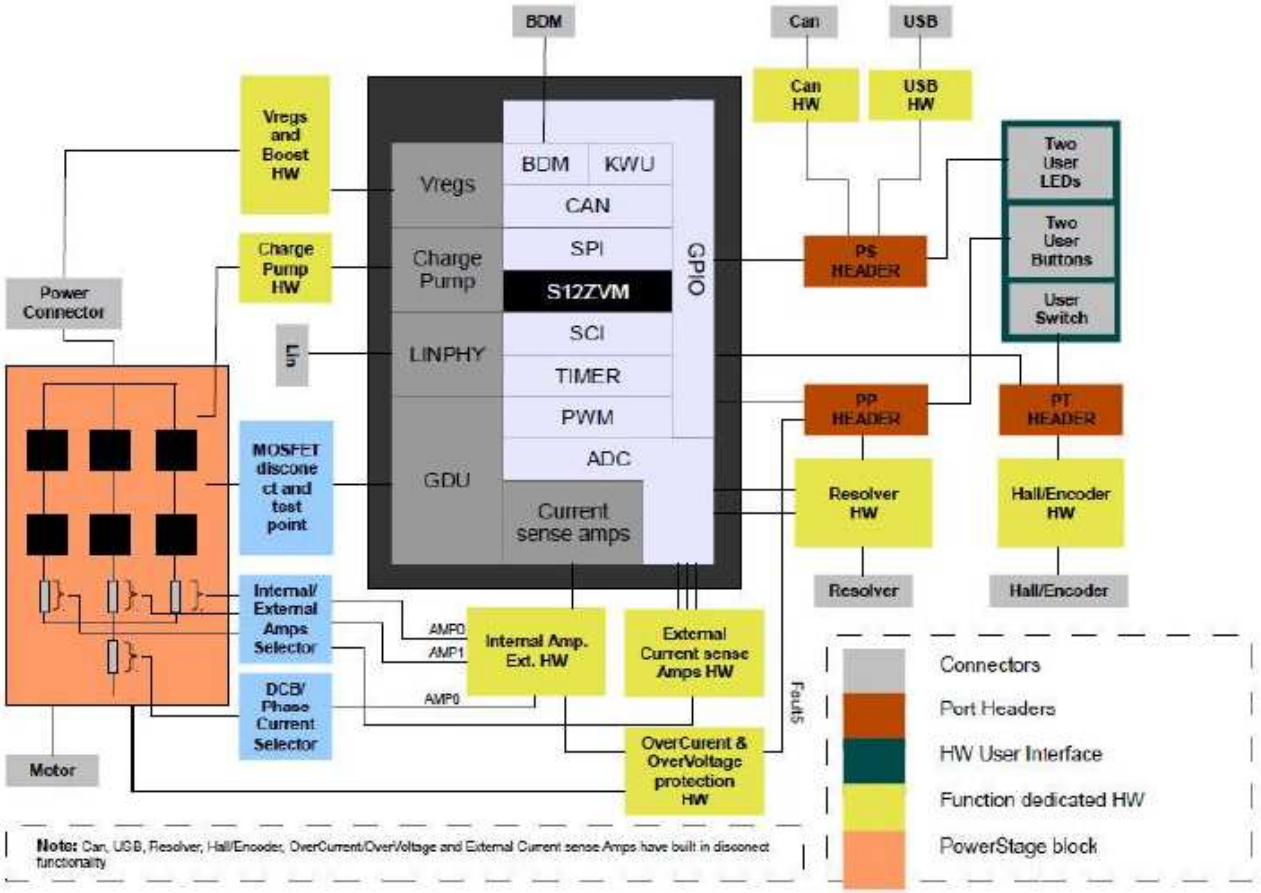

Figure 1. S12ZVMx12EVB block diagram

The board is supplied by VBAT voltage in the range from 3.5 V to 26 V. The board includes a reverse battery protection FET to the output Field Effect Transistor (FET) power bridge, as well as a reverse battery protection diode to the logic supply. A boost converter can be enabled by using the integrated boost controller and external inductor and diode components, for low voltage operation (VBAT < 7 V).

The S12ZVM microcontroller integrates the necessary regulation stages, so that VBAT is supplied directly to the microcontroller device. The VDDX regulator integrated into the S12ZVM provides 5 V to the I/O stages of the microcontroller.

The S12ZVM can supply 5 V to an external Hall sensor via the EVDD pin. Another integrated voltage regulator provides the necessary voltages to drive the power MOSFETs.

The MCU also integrates a Gate Driver Unit to drive the power MOSFETs directly from the MCU pins, using external bootstrap capacitors on the high side FETs. The GDU module includes a Charge Pump to enable 100% duty cycle driving on the high side FETs. The GDU outputs are internally controlled by the Pulse Width Modulator with Fault Protection module (PMF) inside the MCU. The PMF module can drive the different channels independently or in complementary pairs, with automatic dead time insertion.Several FAULT monitoring comparators are connected to the PMF's external FAULT pin. The settings for FAULT triggering can be configured using on-board potentiometers.

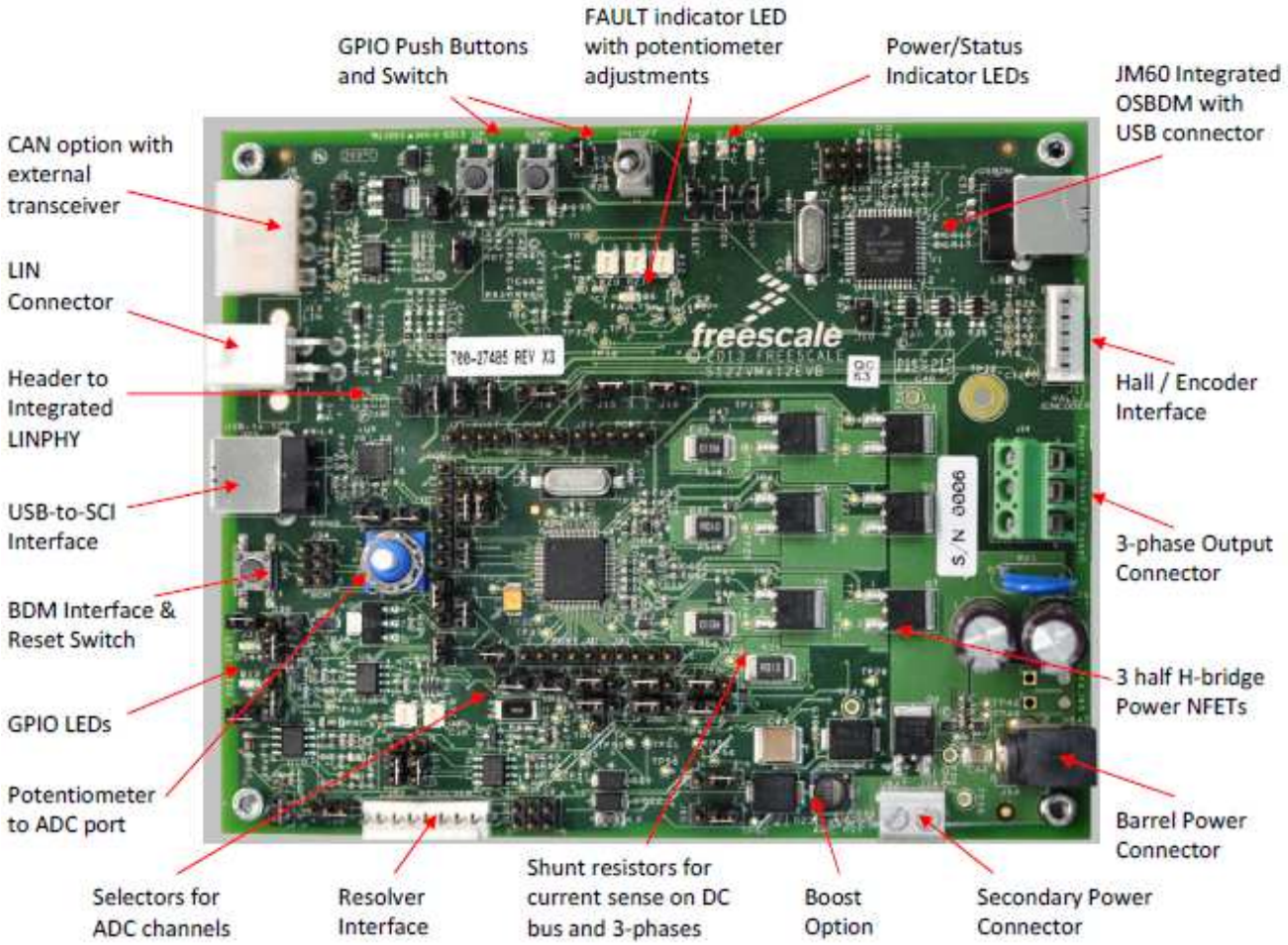

Figure 2. MC9S12ZVM128MCB controller board

2 Interface Description

2.1 Power Supply, J54 or J58

The S12VMx12EVB board can be supplied either by using the 2.1 mm DC power plug J54, or the alternate connector J58. The board can accept input voltage in the range from 3.5 V to 26 V. The board is protected against a reverse battery condition.

2.2 Alternative Power Supply, J64 and J65

The S12VMx12EVB board can also be supplied either by populating a blade terminal on both J64 (positive) and J65 (ground reference) for applications requiring higher current capabilities.

2.3 3-Phase Motor Connector, J24

Power outputs to the motor are located on connector J24. Phase outputs are labeled 0, 1, and 2. A permanent magnet synchronous (PMSM) or a brushless DC (BLDC) motor phase windings can be connected into these connectors.

Table 1. 3-phase motor connector

Connector	Signal name	Description
J24 pin 1	Phase 0	Supplies power to motor phase A
J24 pin 2	Phase 2	Supplies power to motor phase C
J24 pin 3	Phase 1	Supplies power to motor phase B

2.4 Hall Sensor Interface, J11

In Hall sensor based BLDC applications, the Hall sensor inputs are used to determine the actual motor rotor sector. The MCU is capable of providing a regulated 5 V supply to an external Hall sensor by the EVDD pin.

The signals from this connector can be routed to the timer related inputs on the MCU. The following table shows the pinout description of the Hall Sensor connector interface.

Table 2. Hall Sensor connector interface

Interface pin	Signal name	MCU signal	Description	Direction
1	EVDD	EVDD (PP0 through J14)	5 V supply to Hall sensor	Power Output
2	GND	—	Ground reference	Power Reference
3	HALL_A/PH_A	IOC1 (PT1 through J15)	Hall sensor A	Digital Input
4	HALL_B/PH_B	IOC2 (PT2 through J16)	Hall sensor B	Digital Input
5	HALL_C/Index	IOC3 (PT3)	Hall sensor C	Digital Input
6	—	—	(Not connected)	—

2.5 Resolver Interface, J62

In applications using a resolver sensor, the position of the rotor is encoded into sine and cosine signals indicating the shaft angle. A reference signal is generated out of an MCU timer pin. The sine and cosine signals can be routed to two different ADC channels, depending on the appropriate jumper configuration.

The resolver driver circuit shapes a rectangular reference signal from the timer port PT0 output to a sinusoidal waveform. It consists of an integrator that transforms the rectangular signal into a triangle. The higher harmonic components are filtered out by the following stage. The output of the filter stage drives the resolver reference winding (RES_GENP/RES_GENM).

The resolver sine and cosine signals are input into a conditioning circuitry that adjusts voltage levels down to the range acceptable to the on-chip ADC module.

The following table shows the pinout description of the resolver connector interface.

Table 3. Resolver connector interface

Interface pin	Signal name	MCU signal	Description	Direction
1	RES_GENP	(Linked to PT0)	Resolver Generator Positive Output	Analog Output
2	RES_GENM	(Linked to PT0)	Resolver Generator Negative Output	Analog Output
3	RES_SIN	AN0_0 (through J35) or AN0_3 (through J46) or AN1_2 (through J51)	Resolver Sensor SIN Input	Analog Input
4	RES_SIN_REF	—	Resolver Sensor SIN Reference	—
5	RES_COS	AN1_1 (through J50) or AN1_3 (through J52)	Resolver Sensor COS Input	Analog Input
6	RES_COS_REF	—	Resolver Sensor COS Reference	—
7	AGND	—	Analog ground reference	Power Reference
8	+5VA	—	5 V supply voltage	Power Supply

2.6 SINCOS Interface, J61

An alternative simplified resolver interface is also available on the SINCOS connector.

The following table shows the pinout description of the SINCOS interface.

Table 4. Pinouts of SINCOS interface

Interface pin	Signal name	MCU signal	Description	Direction
1	PH_A	IOC1 (PT1 through J15)	Resolver Sensor Phase A Output	Digital Input
2	RES_SIN	AN0_0 (through J35) or AN0_3 (through J46) or AN1_2 (through J51)	Resolver Sensor SIN Input	Analog Input
3	PH_B	IOC2 (PT2 through J16)	Resolver Sensor Phase B Output	Digital Input
4	RES_COS	AN1_1 (through J50) or AN1_3 (through J52)	Resolver Sensor COS Input	Analog Input
5	AGND	—	Analog ground reference	Power Reference
6	+5 VA	—	5 V supply voltage	Power Supply

2.7 CAN Connector, J8

An external CAN transceiver is available on board and can be routed to the MCU MSCAN module.

Table 5. CAN connector

Interface pin	Signal name	MCU signal	Description	Direction
1	MSCAN_H	RXCAN/TXCAN	CAN Bus H	Diff. bidirectional
2	MSCAN_L	RXCAN/TXCAN	CAN Bus L	Diff. bidirectional
3	—	—	(Not connected)	—
4	—	—	(Not connected)	—

2.8 LIN Connector, J13

The integrated LIN physical layer is used as the LIN interface.

Table 6. LIN connector

Interface pin	Signal name	MCU signal	Description	Direction
1	LGND	—	Ground reference	Power Reference
2	LGND	—	Ground reference	Power Reference
3	HD (VBAT)	—	Power Supply	—
4	LIN	LIN	LIN Bus	Digital bidirectional

2.9 LINPHY Header, J17

The LINPHY interface header provides connections to the TXD and RXD functionality of the LIN physical layer integrated into the MCU.

Table 7. LINPHY interface header

Interface pin	Signal name	MCU signal	Description	Direction
1	LPRXD	LPRXD	LIN Physical Layer RXD	Digital Output
2	LPTXD	LPTXD	LIN Physical Layer TXD	Digital Input

2.10 External BDM Connector, J34

A BDM interface for MCU code download and debugging is provided.

Table 8. External BDM connector

Interface pin	Signal name	MCU signal	Description	Direction
1	BKGD	BKGD	Background	Digital Input
2	GND	—	Ground reference	Power Reference
3	PDO	PS5/PDO	Extended DBG module data output	Digital Output
4	RESET_B	RESET	Reset	Digital Bidirectional
5	PDOCLK	PS4/PDOCLK	Extended DBG module data clock	Digital Output
6	VDDX_BDM	VDDX	5 V supply to external BDM interface	Power Supply

2.11 Extended DBG Module Header, J38

The PDO and PDOCLK signals to the DBG extended debug module are available for interfacing with dedicated debug hardware.

Table 9. Extended DBG module header

Interface pin	Signal name	MCU signal	Description	Direction
1	PDO	PS5/PDO	Extended DBG module data output	Digital Output
2	PDOCLK	PS4/PDOCLK	Extended DBG module data clock	Digital Output

2.12 BDM Connector for OSBDM Microcontroller, J1

A BDM interface is provided to load code to the OSBDM microcontroller, U1.

Table 10. BDM connector for OSBDM microcontroller

Interface pin	Signal name	OSBDM MCU signal	Description	Direction
1	U_BKGD	BKGD	Background	Digital Input
2	GND	—	Ground reference	Power Reference
3	—	—	(Not connected)	—
4	U_RESET	RESET	Reset	Digital Bidirectional
5	—	—	(Not connected)	—
6	+5 VU	VDD1	5 V supply from OSBDM USB interface	Power Supply

2.13 USB Connector for OSBDM Microcontroller, J7

This USB interface is used to communicate with a PC as an interface to load and debug code to the microcontroller. The OSBDM tool also may enable a virtual serial port that can be routed to SCI1 serial port in the MCU, at pins PS2 and PS3, by setting the appropriate registers.

Table 11. USB Connector for OSBDM microcontroller

Interface pin	Signal name	MCU signal	Description	Direction
1	+5VU	—	USB Power Supply	Power Supply
2	D-	PS2/PS3 or RESET/ BKGD	Data -	Digital Bidirectional
3	D+	PS2/PS3 or RESET/ BKGD	Data +	Digital Bidirectional
4	GND	—	Ground reference	Power Reference

2.14 USB Connector for USB-to-SCI Interface, J25

This USB interface is used to communicate with a PC as an interface to a virtual serial port.

Table 12. USB Connector for USB-to-SCI interface

Interface pin	Signal name	MCU signal	Description	Direction
1	VBUS_USB	—	USB Power Supply	Power Supply
2	D-	PS2/PS3	Data -	Digital Bidirectional
3	D+	PS2/PS3	Data +	Digital Bidirectional
4	GND_USB	—	Ground reference	Power Reference

2.15 MCU Port P Header, J21

The MCU signals from GPIO port P can be monitored using this header.

Table 13. MCU Port P header

Interface pin	MCU signal	Pin functionality
1	PP0	PP0/EVDD1/KWP0/(PWM0)/ECLK/ FAULT5/XIRQ
2	PP1	PP1/KWP1/(PWM1)/IRQ
3	PP2	PP2/KWP2/(PWM2)
4	GND	Ground reference

2.16 MCU Port E Header, J22

The MCU signals from GPIO port E can be monitored using this header.

Table 14. MCU Port E header

Interface pin	MCU signal	Pin functionality
1	PE0	PE0/EXTAL
2	PE1	PE1/XTAL
3	GND	Ground reference

2.17 MCU Port T Header, J23

The MCU signals from GPIO port T can be monitored using this header.

Table 15. MCU Port T header

Interface pin	MCU signal	Pin functionality
1	PT3	PT3/IOC3/(SS)
2	PT2	PT2/IOC2/(PWM5)/(SCK)
3	PT1	PT1/IOC1/(PWM4)/(MOSI)/(TXD0)/ LPDR1/PTURE
4	PT0	PT0/IOC0/(PWM3)/(MISO)/(RXD0)
5	GND	Ground reference

2.18 MCU Port S Header, J31

The MCU signals from GPIO port S can be monitored using this header.

Table 16. MCU Port S header

Interface pin	MCU signal	Pin functionality
1	PS0	PS0/KWS0/RXD1/RXCAN/(LPRXD)/ PTUT0
2	PS1	PS1/KWS1/TXD1/TXCAN/(LPTXD)/ PTUT1
3	PS2	PS2/KWS2/(RXD1)/MISO
4	PS3	PS3/KWS3/DBGEEV/(TXD1)/MOSI
5	PS4	PS4/KWS4/SCK/PDOCLK
6	PS5	PS5/KWS5/SS/PDO
7	GND	Ground reference

2.19 MCU Port AD Header, J41

The MCU signals from GPIO port AD can be monitored using this header.

Table 17. MCU Port AD header

Interface pin	MCU signal	Pin functionality
1	PAD0	PAD0/KWAD0/AMP0/AN0_0
2	PAD1	PAD1/KWAD1/AMPM0/AN0_1
3	PAD2	PAD2/KWAD2/AMPP0/AN0_2
4	PAD3	PAD3/KWAD3/AN0_3/
5	PAD4	PAD4/KWAD4/AN0_4/
6	PAD5	PAD5/KWAD5/AMP1/AN1_0
7	PAD6	PAD6/KWAD6/AMPM1/AN1_1/(SS)
8	PAD7	PAD7/KWAD7/AMPP1/AN1_2
9	PAD8	PAD8/KWAD8/AN1_3/VRH
10	GND	Ground reference

3 Design Considerations

This section provides additional information about the functional blocks of the S12ZVMx12EVB motor control board.

3.1 MC9S12ZVM Features

The MC9S12ZVM-Family is an automotive 16-bit microcontroller family using the 180 nm NVM + UHV technology that offers the capability to integrate 40 V analog components. The particular differentiating features of this family are the enhanced S12Z core, the combination of dual-ADC synchronized with PWM generation and the integration of “high-voltage” analog modules, including the voltage regulator (VREG), Gate Driver Unit (GDU) and a Local Interconnect Network (LIN) physical layer. These features enable a fully integrated single chip solution to drive up to 6 external power MOSFETs for BLDC or PMSM motor drive applications.

- S12Z CPU core
- Memory
  - 128, 64 or 32 KB on-chip flash with ECC
  - 512 byte EEPROM with ECC
  - 8, 4, or 2 KB on-chip SRAM with ECC
- Clock Modules
  - Phase locked loop (IPLL) frequency multiplier with internal filter
  - 1 MHz internal RC oscillator with +/-1.3% accuracy over rated temperature range
  - 4-16 MHz amplitude controlled pierce oscillator
  - Internal COP (watchdog) module
  - Autonomous periodic interrupt (API)
- Low side and high side FET pre-drivers for each phase
  - Gate drive pre-regulator
  - LDO (Low Dropout Voltage Regulator) (typically 11 V)
  - High side gate supply generated using bootstrap circuit with external diode and capacitor

    - Sustaining charge pump with two external capacitors and diodes
    - High side drain (HD) monitoring on internal ADC channel using HD/5 voltage
- 6-channel, 15-bit pulse width modulator with fault protection (PMF)
    - Independent or complementary pair operation
    - Center-aligned or edge-aligned outputs
    - Dead time insertion available for each complementary pair
- Two parallel analog-to-digital converters (ADC) with 12-bit resolution and up to 9 channels available on external pins
- Programmable Trigger Unit (PTU) for synchronization of PMF and ADC
- Connectivity
    - One on-chip LIN physical layer transceiver fully compliant with the LIN 2.1 standard (MC9S12ZVML12MKH version)
    - One serial communication interface (SCI) module with interface to internal LIN physical layer transceiver (with RX connected to a timer channel for frequency calibration purposes, if desired)
    - Up to one additional SCI (not connected to LIN physical layer)
    - MSCAN (1 Mbit/s, CAN 2.0 A, B software compatible) module
    - One serial peripheral interface (SPI) module
- 4-channel timer module (TIM) with input capture/output compare
- Voltage Regulator
    - On-chip voltage regulator (VREG) for regulation of input supply and all internal voltages
    - Optional VREG ballast control output to supply an external CAN physical layer (MC9S12ZVMC12MKH version)
    - 20 mA high-current output for use as Hall sensor supply
- Supply voltage sense with low battery warning
- Chip temperature sensor
- Two current sense circuits for over-current detection or torque measurement

3.2 Power Supply

The S12ZVMx12EVB motor control board can be supplied from three different options. It can be supplied by J54 and J58 and alternatively by populating blade terminals at locations J64 (positive supply) and J65 (ground). The battery connection to the MCU main supply, VSUP, is protected against a reverse polarity condition, through diode D19. The capacitor C43 is provided as a bulk capacitor to store energy and maintain MCU operation for a short duration upon loss of battery. The capacitor C38 is there to filter the voltage supply into the MCU pin.

3.2.1 Boost DC/DC Converter

The board also provides the external components required to enable a boost DC/DC converter, using the BOOST controller pin in the MCU, namely the inductor L7, and diodes D19 and D21. When the internal switch at the BOOST pin closes, the current builds up through L7. When the switch opens, the current flows through D19 and into the storage capacitor, C43. Diode D21 provides protection to the BOOST pin in case of a reverse battery condition. If the VBAT node shown in the figure below is already protected against a reverse battery condition, the diode D21 is not needed.

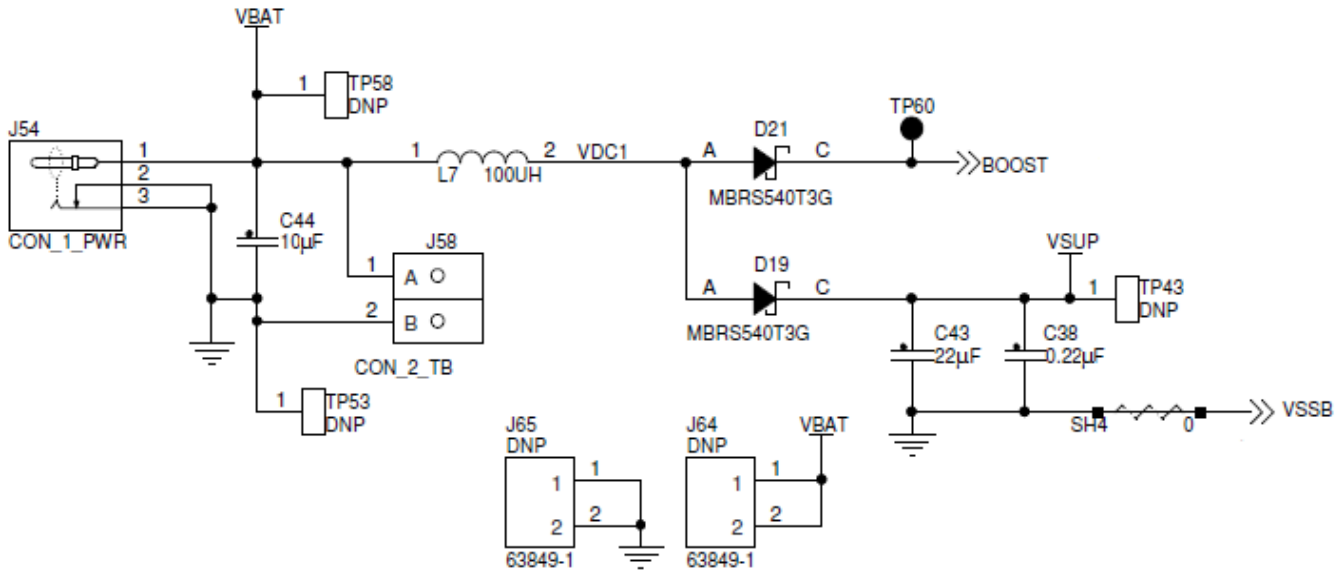

Figure 3. Boost DC/DC converter option

3.2.2 Bridge Supply (DC Link) Reverse Battery Protection

A separate reverse battery protection is provided for the FET bridge voltage supply. In this case, a power n-channel MOSFET, Q9, is provided, with its source connected to the battery input. Using external components, a charge pump driven by pin CP can be enabled to drive the reverse battery MOSFET. Additionally, a circuit is available on the board to enable a fast turn-off of the n-channel MOSFET in case of a reverse battery condition, using an external bipolar transistor. Upon a reverse battery condition, the bipolar transistor, Q10, turns on and isolates the HD pin from VBAT by opening the external MOSFET.

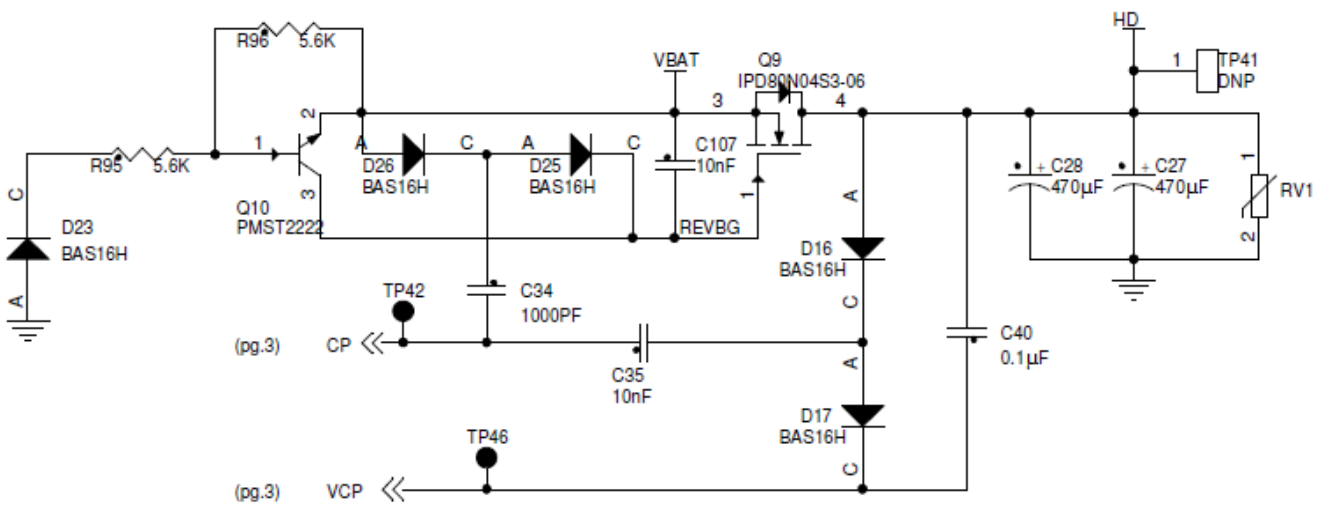

Figure 4. Reverse Battery Protection and Charge Pump circuit

3.2.3 Charge Pump for High-Side Driver Supply

In the Figure 4, there are two different implementations of charge pumps, using the same pin on the MCU. As described before, the first charge pump drives the N-channel MOSFET for reverse battery protection based on components D25, D26, C34 and C107. The second charge pump, composed of C35, C40, D16, and D17, feeds a voltage into the MCU, through the VCP pin.

3.3 Voltage Regulators

The main 5 V regulator is a linear voltage regulator integrated into the MCU. It is supplied directly from the VSUP battery input pin and delivers up to 70 mA on a regulated 5 V output on pins VDDX1, VDDX2. In case a larger current is required out of the VDDX node, an external ballast PNP transistor is provided on board, which is controlled by the BCTL pin.

To enable the ballast transistor, a couple of bits in register CPMUVREGCTL need to be adjusted by software (EXTXON = 1, INTXON = 0). Additionally, a jumper needs to be placed on header J40, shorting pins 1 and 2.

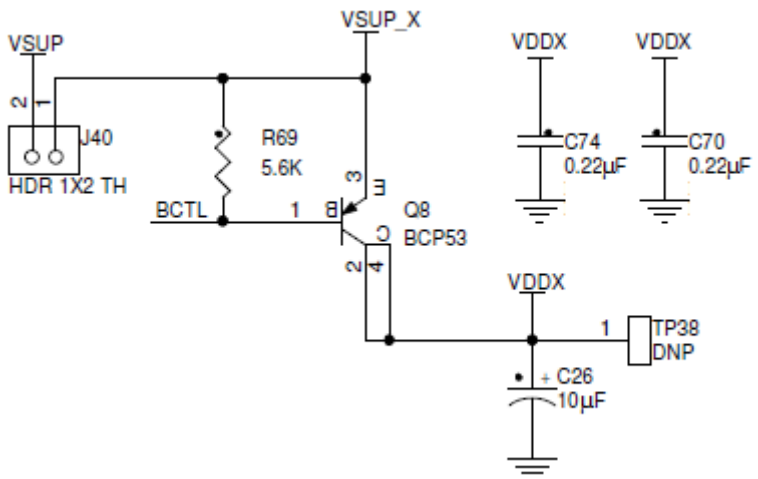

Figure 5. External ballast transistor option

The maximum current capability of the ballast transistor will be highly dependent on the operating conditions (mainly temperature and battery voltage). For example, the BCP53 PNP transistor on board is rated to 1.5 W at 25°C. At a nominal battery voltage of 12 V, the estimated current capability of the transistor would be:

I = P / V, where V = (VSUP –VDDX) = 7 V
I = 1.5 W / 7 V = 214 mA

3.4 CAN/LIN Interfaces

There are two versions of the S12ZVMx12EVB board:

- S12ZVM**L**12EVBLIN, populated with the MC9S12ZVM**L**12 device that integrates a LIN physical layer
- S12ZVM**C**12EVBCAN, populated with the MC9S12ZVM**C**12 device that integrates a controller for a second 5 V voltage regulator to supply an external CAN transceiver.

3.4.1 CAN/LIN Enablement

The EVB provides an array of 0-ohm resistors that are populated according to the variant of the S12VM device that is populated on the board. The following image shows the different resistor pairs. Only one resistor on each pair must be populated at a time.

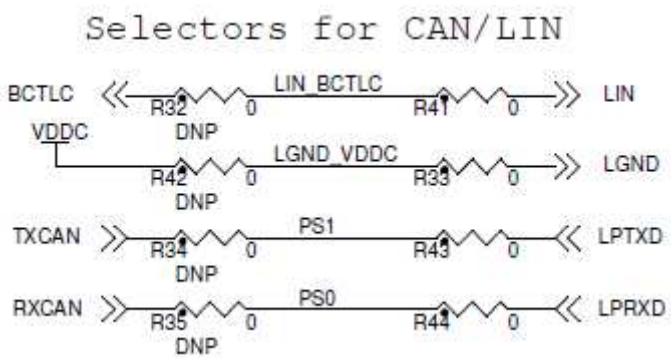

Figure 6. Resistor selection for CAN/LIN options

Table 18. Populating Resistors for CAN/LIN Enablement

	S12ZVML12MKH		S12ZVMC12MKH
MCU Pin	LIN	LIN + CAN(*)	CAN(*)
1 – LIN / BCTLC	R41	R41	R32
64 – LGND / VDDC	R33	R33	R42
4 – PS1 (LPTXD / TXCAN)	R43	R34	R34
3 – PS0 (LPRXD / RXCAN)	R44	R35	R35
Other settings			
J3 (VDDC supplied from USB, J25)	Open	Close	Open
J2 (supply to VDDC regulator)	Open	Open	Close
(*) Using external CAN transceiver			

3.4.2 LIN Physical Layer

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN Physical Layer 2.2 specification from LIN consortium.

The LIN physical interface pins (LPTXD and LPRXD) are available on a 2-pin header, J17. This can be used to interface another MCU to the LIN physical interface integrated into the S12ZVML device.

The LIN bus includes an integrated pull-up device, which can be a strong pull-up (~34 Kiloohm) or a high impedance value (~300 Kiloohm), selectable by software. A 220 pF capacitor is added at the LIN bus pin, according to the device recommendation. ESD protection is provided in the form of two back-to-back diodes in a single package, D8.

By default, the EVB is configured to operate in slave mode. It can be converted into a Master node by populating a 1 Kiloohm resistor at R45. The footprint in the PCB will hold a 0603 size surface mount resistor. This resistor is connected in series with the diode required from the battery voltage node. In this case, the battery voltage is taken from the HD node, the supply to the FET bridge high side drains.

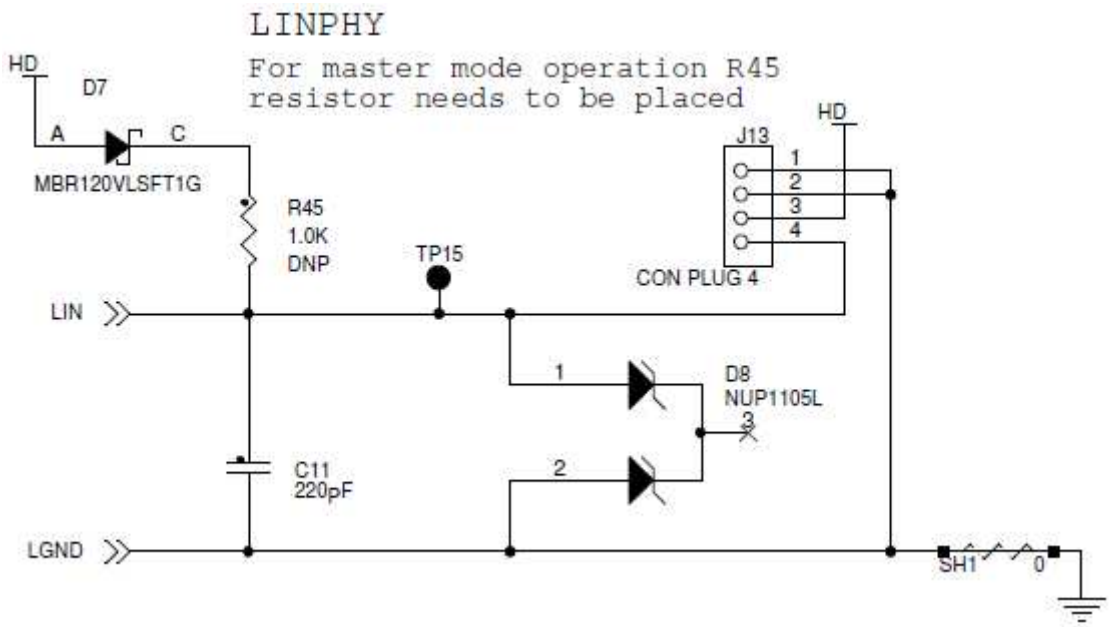

Figure 7. LIN interface

3.4.3 CAN Transceiver

The EVB includes an external CAN transceiver that can be linked to the MSCAN module of the S12ZVM device, by populating the appropriate resistors as shown in Table 18.

In the CAN version of the EVB, the external transceiver can be powered by a voltage regulator controlled by the S12ZVMC12 microcontroller. An external PNP BJT ballast transistor is required to deliver regulated 5 V to the CAN transceiver. The base of the transistor must be connected to the BCTLC base control pin on the microcontroller. The collector of the transistor must be connected to the VDDC pin on the microcontroller. A 5.6 kiloohm resistor is recommended from the base to the emitter of the transistor. The emitter terminal must be supplied from the VSUP (reverse polarity protected) battery supply. A jumper must be populated on header J2 to enable the supply to the transistor. The jumper on header J3 must not be populated in this case.

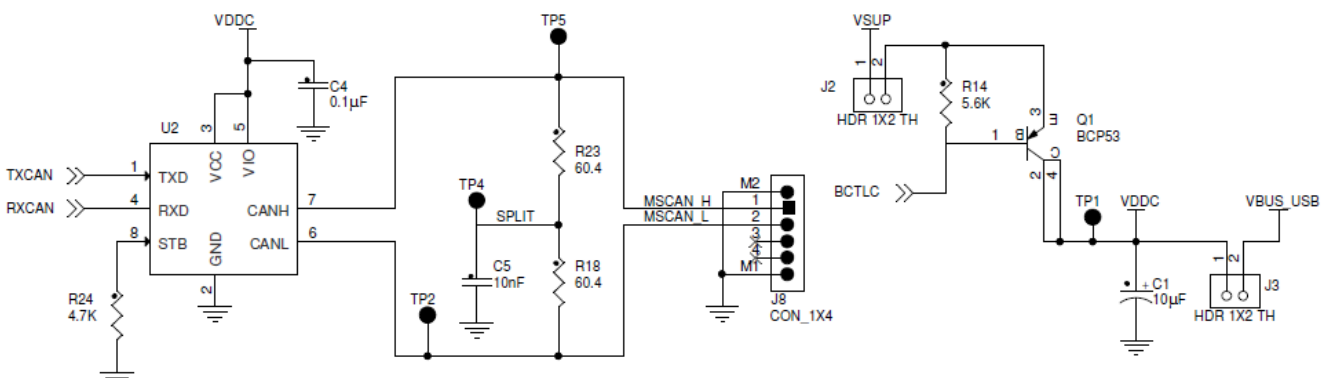

Figure 8. CAN Transceiver

In the LIN version of the EVB, the microcontroller can't control the ballast transistor, because the VDDC and BCTLC pins are replaced by the LIN and LGND pins of the LIN physical layer. However, the MSCAN module in the microcontroller can still be linked to the external CAN transceiver. The transceiver 5 V supply can be powered from the USB connector, J25, as long as a jumper is populated on header J3. In this case, the jumper on header J2 must be removed.

3.5 SCI

The S12ZVM EVB provides two different routing options to link one SCI module on the microcontroller to a USB port that could be easily connected to a personal computer.

3.5.1 SCI to USB (CP2102)

The first alternative is to use the USB interface that is provided with the CP2102 USB to UART bridge. This interface is available through a Type B USB connector, J25, and is digitally isolated. A driver needs to be installed on the host computer to create a virtual serial COM port, linked to the USB port that is connected to the USB to UART bridge.

A couple of jumpers need to be populated on headers J27 and J28 from pin 2 to pin 3 on both headers. This links the SCI1 pins from the microcontroller to the USB to UART bridge, through the digital isolator.

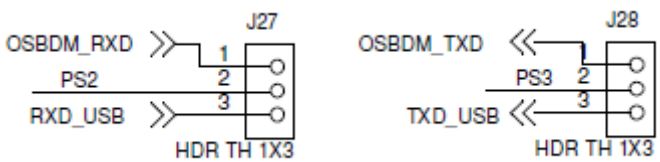

Figure 9. USB to SCI jumper options

3.5.2 SCI to USB (OSBDM)

The second option to route the SCI1 port to a USB interface is by using the on-board OSBDM programmer. This interface is available through a Type B USB connector, J7. The necessary drivers to operate the serial interface provided by the OSBDM device should install the first time the EVB is connected to the computer through a USB cable.

In this case, a couple of jumpers need to be placed on headers J27 and J28 from pin 1 to pin 2 on both headers. This will route the RXD and TXD signals from the SCI1 module, to the RXD and TXD signals from the OSBDM device.

3.6 3-Phase Power Bridge

The power stage is configured as a 3-phase Power Bridge with n-channel MOSFET transistors. The Gate Driver Unit (GDU) integrated into the MCU provides the supply voltage to the gates of the low-side and high-side MOSFETs. The GDU pins are designed to interface to external components in the automotive battery range, so they can be connected directly to the MOSFET terminals. For evaluation purposes, the connections from the GDU pins to the MOSFETs on the S12ZVM128EVB board are done through a series of 0-ohm resistors.

The drivers for the low-side MOSFET gates are driven by the internal LDO regulator (VLS_OUT). Each driver uses the pin LSx as its reference, and supplies the voltage into pin LGx to drive the MOSFET gate.

The drivers for the high-side MOSFET gates are driven by the voltage stored in a bootstrap capacitor, which is external to the MCU. This voltage is derived from the LDO regulator through an external diode and fed into the bootstrap voltage VBSx pin. Each high-side driver uses the pin HSx as its reference, and supplies the bootstrap voltage into pin HGx to drive the high-side MOSFET gate.

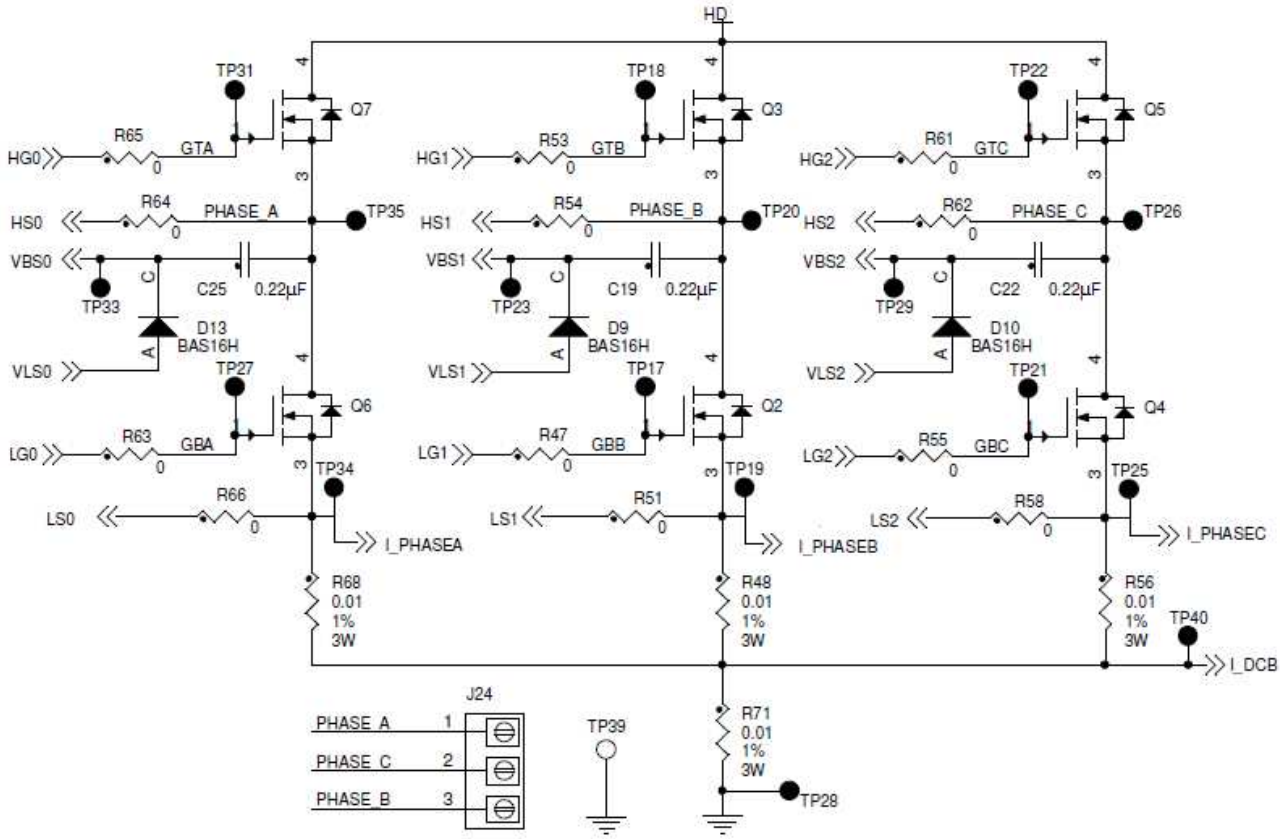

Figure 10. 3-phase output stage

3.7 Current Sense

A set of four different resistors are provided on the board for current sensing in different applications. There is one current sense resistor for each phase (R48, R56, R68), plus one resistor to sense the DC bus current (R71). The components populated on the board are 10 milliohm, 1% tolerance resistors. Several different options are provided on the board to enable current sense on multiple resistors at the same time. The MCU integrates two current sense amplifiers, and there are three additional amplifiers provided on board using external op-amps.

The two current sense amplifiers integrated into the MCU are mapped each to a different ADC module, to allow for simultaneous conversions.

Option 1) Internal Op-Amp 0:

The internal current sense amplifier 0 is mapped to the ADC pins at PAD0, PAD1, and PAD2, with the following configuration:

PAD0 = AMP0, the operational amplifier output.
PAD1 = AMPM0, the operational amplifier inverting input (minus).
PAD2 = AMPP0, the operational amplifier non-inverting input (plus).

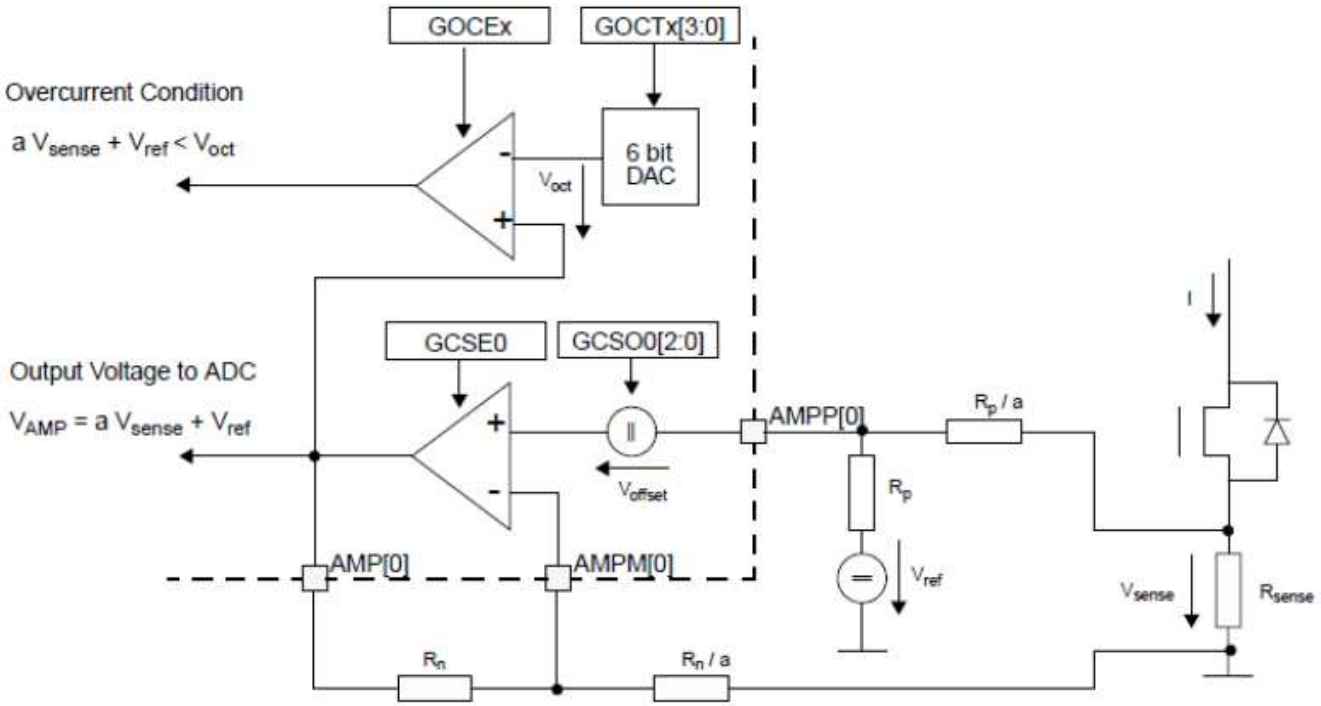

Figure 11. Integrated current sense amplifiers

On this board, two different current sense resistors can be connected to the internal operational amplifier, by selecting the appropriate configuration using jumpers in J60 and J57. To measure the current from Phase A, the jumpers must be on J60 pins 1-2 and on J57 pins 1-2. To measure the DC Bus current, the jumpers must be on J60 pins 2-3 and on J57 pins 2-3.

Table 19. Measurement of the DC Bus current

Header	Setting	Description
J60	1-2	Positive end of current sense from Phase A
	2-3	Positive end of current sense from DC Bus
J57	1-2	Negative end of current sense from Phase A
	2-3	Negative end of current sense from DC Bus

To map the operational amplifier to the AMPx pins, the following jumpers need to be placed, too: J35 pins 1-2, J44 pins 1-2, J45 pins 1-2.

The gain of the amplifier is set using external resistors where R198 = 199 = 2.2 kiloohm, and R196 = R200 = 40 kiloohm. With these resistor values, the gain of the amplifier is A = R196 / (R198 + 1K) = 40K/3.2K = 12.5. Please note the denominator considers additional 1K in series, which is the resistor before the jumper that is used to select which sense resistor is connected to the operational amplifier.

The output voltage is shifted up by 2V5_REF, a 2.5 V supply which is mid range from the full scale voltage of the ADC, 5 V, to accommodate positive and negative current swings. The voltage shift can be eliminated by removing R196 and replacing it with R197 instead.

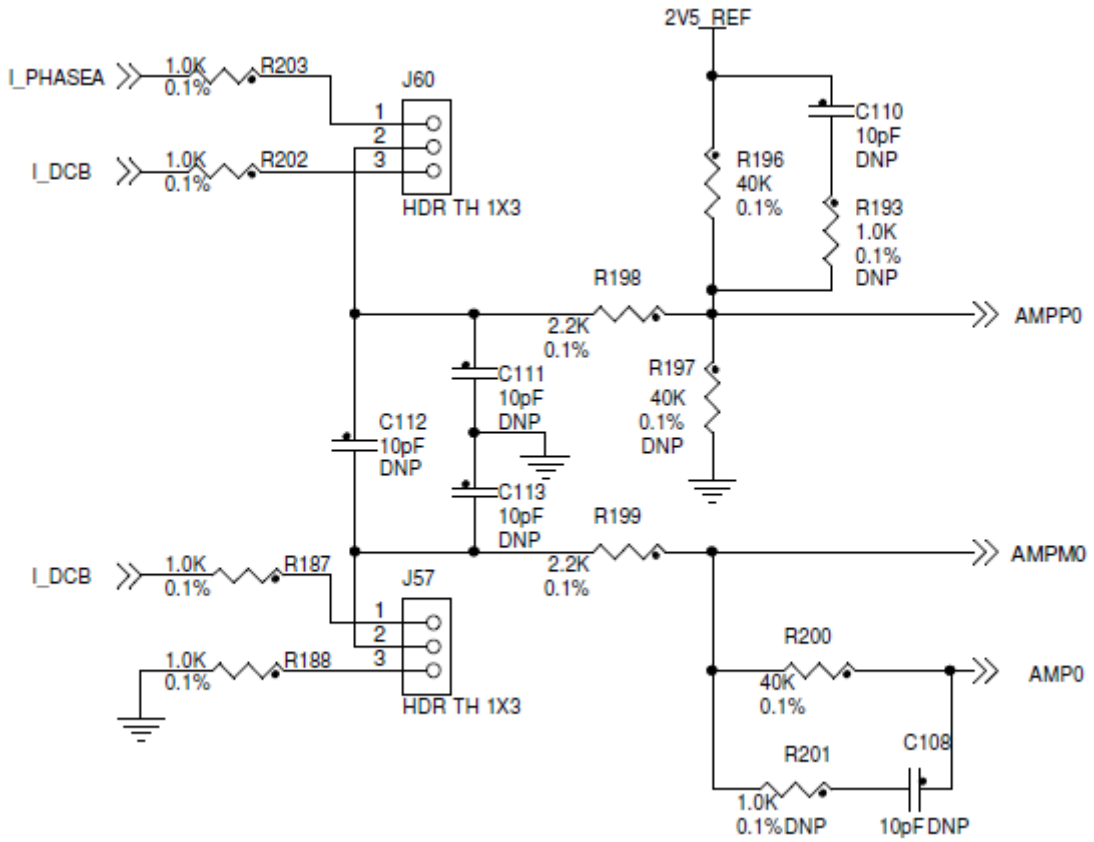

Figure 12. Phase A/DC Bus current sense option

With the sense resistor value of 10 milliohms, and the gain being 12.5, the maximum excursion of +/- 2.5 V from the mid-range voltage of 2.5 V corresponds to a sensed current of 20 A:

Vamp, max = +/-2.5 V
Vsensed, max = (Vamp, max) / Gain = (+/-2.5V) / 12.5 = 0.2 V
Isensed, max =(Vsensed, max) / Rsense = (+/-0.2V) / 0.01ohm = +/- 20 A.

Option 2) Internal Op-Amp 1:

The internal current sense amplifier 1 is mapped to the ADC pins at PAD5, PAD6, and PAD7, with the following configuration:

PAD5 = AMP1, the operational amplifier output.
PAD6 = AMPM1, the operational amplifier inverting input (minus).
PAD7 = AMPP1, the operational amplifier non-inverting input (plus).

This amplifier has fixed connections to the Phase B current sense resistor. The external gain setting resistors have the same values as described before. It is also connected to a 2.5 V reference to allow for positive and negative current swings.

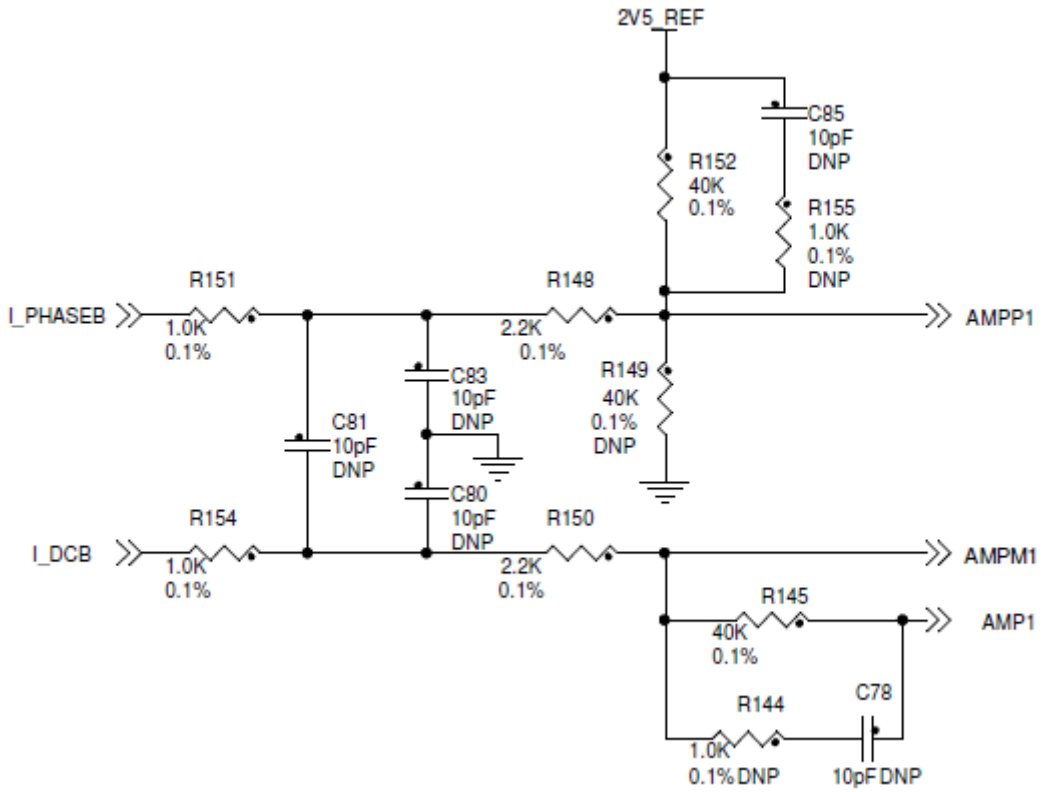

Figure 13. Phase B current sense using internal Op-Amp 1

Option 3) External Op-Amps:

There is an option to use op-amps provided on-board, external to the MCU, to sense the current from each of the three phases, routed to three different ADC channels.

The gain setting resistors have the same values as in the previous two cases, with the connection to a 2.5V reference voltage for positive and negative current swings.

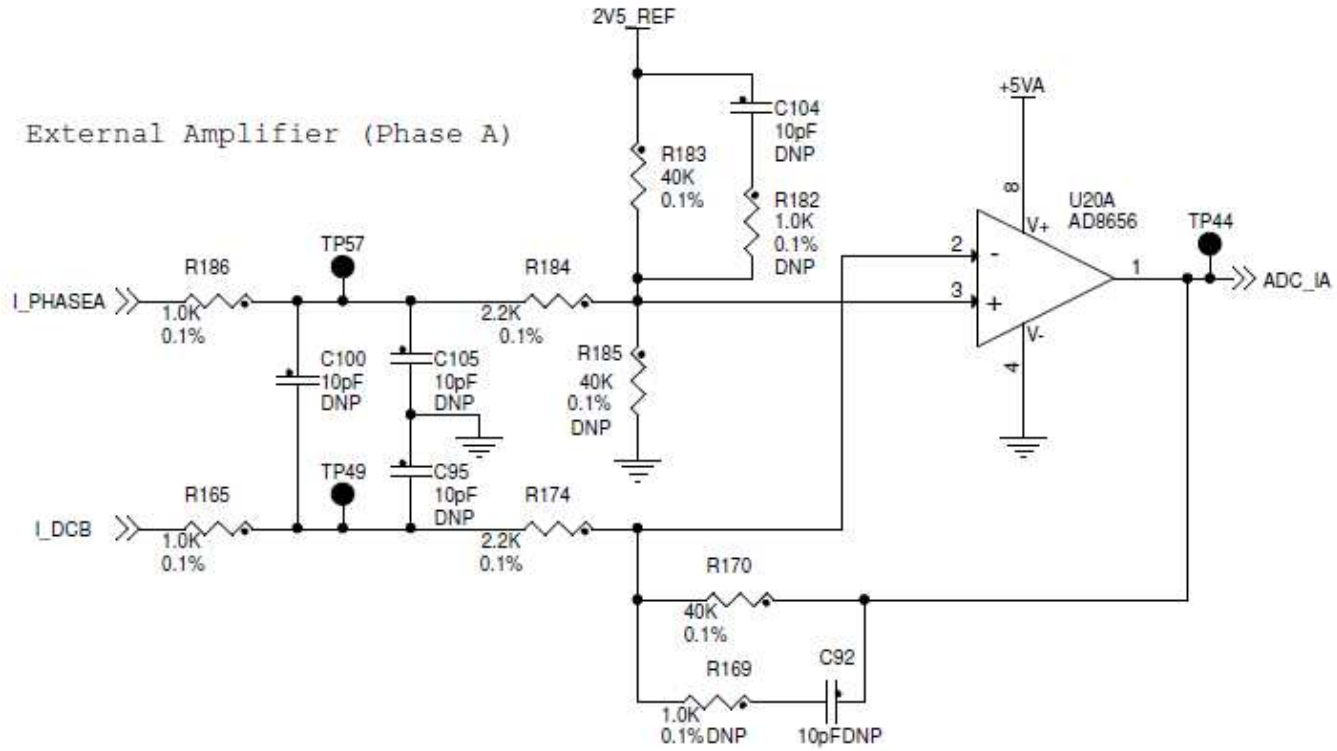

Figure 14. Phase A current sense using external Op-Amp

3.8 ADC Channel Mapping

The following figures show the jumper configurations for the different ADC external channel mapping options:

ADC Module	MCU Pin	ADC Channel	Option 1	Option 2	Option 3	Jumper
ADC 0	PAD0	AN0_0	AMP0	POS_SIN	-	J35 pins 2-3
	PAD1	AN0_1	AMPM0	-	-	-
	PAD2	AN0_2	AMPP0	-	-	-
	PAD3	AN0_3	ADC_IA	POS_SIN	-	J46 pins 1-2
	PAD4	AN0_4	ADC_IB	POT1	-	J47 pins 1-2
ADC 1	PAD5	AN1_0	AMP1	ADC_IB	-	J48 pins 2-3
	PAD6	AN1_1	AMPM1	POS_COS	-	J50 pins 2-3
	PAD7	AN1_2	AMPP1	POS_SIN	POT1	J51 pin2-J42
	PAD8	AN1_3	ADC_IC	POS_COS	-	J52 pins 1-2

Figure 15. Resolver interface plus 3-phase sensing

ADC Module	MCU Pin	ADC Channel	Option 1	Option 2	Option 3	Jumper
ADC 0	PAD0	AN0_0	AMP0	POS_SIN	-	J35 pins 1-2
	PAD1	AN0_1	AMPM0	-	-	J44 pins 1-2
	PAD2	AN0_2	AMPP0	-	-	J45 pins 1-2
	PAD3	AN0_3	ADC_IA	POS_SIN	-	J46 pins 2-3
	PAD4	AN0_4	ADC_IB	POT1	-	-
ADC 1	PAD5	AN1_0	AMP1	ADC_IB	-	-
	PAD6	AN1_1	AMPM1	POS_COS	-	J50 pins 2-3
	PAD7	AN1_2	AMPP1	POS_SIN	POT1	J51 pin2-J42
	PAD8	AN1_3	ADC_IC	POS_COS	-	-

Figure 16. Resolver interface plus 1-phase sensing

ADC Module	MCU Pin	ADC Channel	Option 1	Option 2	Option 3	Jumper
ADC 0	PAD0	AN0_0	AMP0	POS_SIN	-	J35 pins 1-2
	PAD1	AN0_1	AMPM0	-	-	J44 pins 1-2
	PAD2	AN0_2	AMPP0	-	-	J45 pins 1-2
	PAD3	AN0_3	ADC_IA	POS_SIN	-	J46 pins 2-3
	PAD4	AN0_4	ADC_IB	POT1	-	J47 pins 2-3
ADC 1	PAD5	AN1_0	AMP1	ADC_IB	-	J48 pins 1-2
	PAD6	AN1_1	AMPM1	POS_COS	-	J50 pins 1-2
	PAD7	AN1_2	AMPP1	POS_SIN	POT1	J51 pins 1-2
	PAD8	AN1_3	ADC_IC	POS_COS	-	J52 pins 2-3

Figure 17. Resolver interface plus 2-phase sensing

3.9 Hall Sensor Interface

The Hall sensor interface is used for BLDC sensor based motor control applications. The Hall sensors are used to determine the actual motor rotor sector.

The on-board interface provides the 5 V power supply voltage to supply the sensors. The Hall interface inputs are designed to support an open collector as well as push-pull Hall sensors outputs (see Figure below). A single pole RC low pass filter is present to reduce a signal noise.

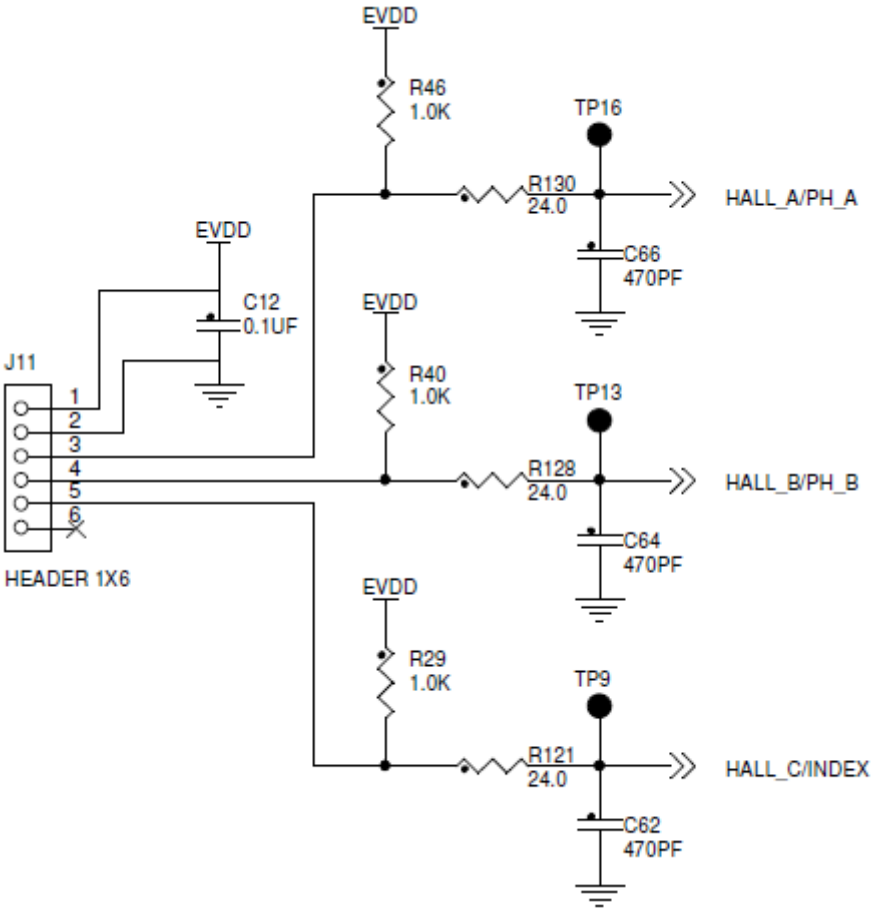

Figure 18. Hall Sensor Interface

The three signals from the Hall sensor need to be routed to the appropriate timer pins on the microcontroller. For Phase A, a jumper must be placed on pins 2-3 of header J15. For Phase B, a jumper must be placed on pins 1-2 of header J16. For phase C, there is a 0-ohm resistor that links it directly to the microcontroller pin PT3.

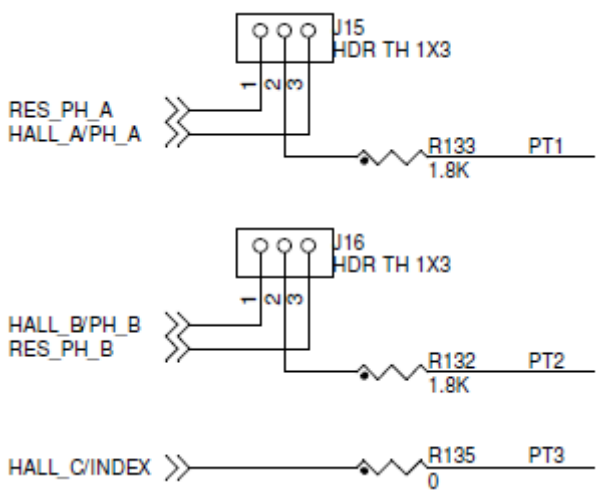

Figure 19. Hall Sensor routing options

The next figure shows the Hall sensor signal alignment to BLDC motor Back-EMF signal. The Hall sensors detect the rotor flux, so their actual state is not influenced by stator current. The Hall effect outputs in BLDC motors divide the electrical revolution into three equal sections of 120°. In this so-called 120° configuration, the Hall states 111 and 000 never occur.

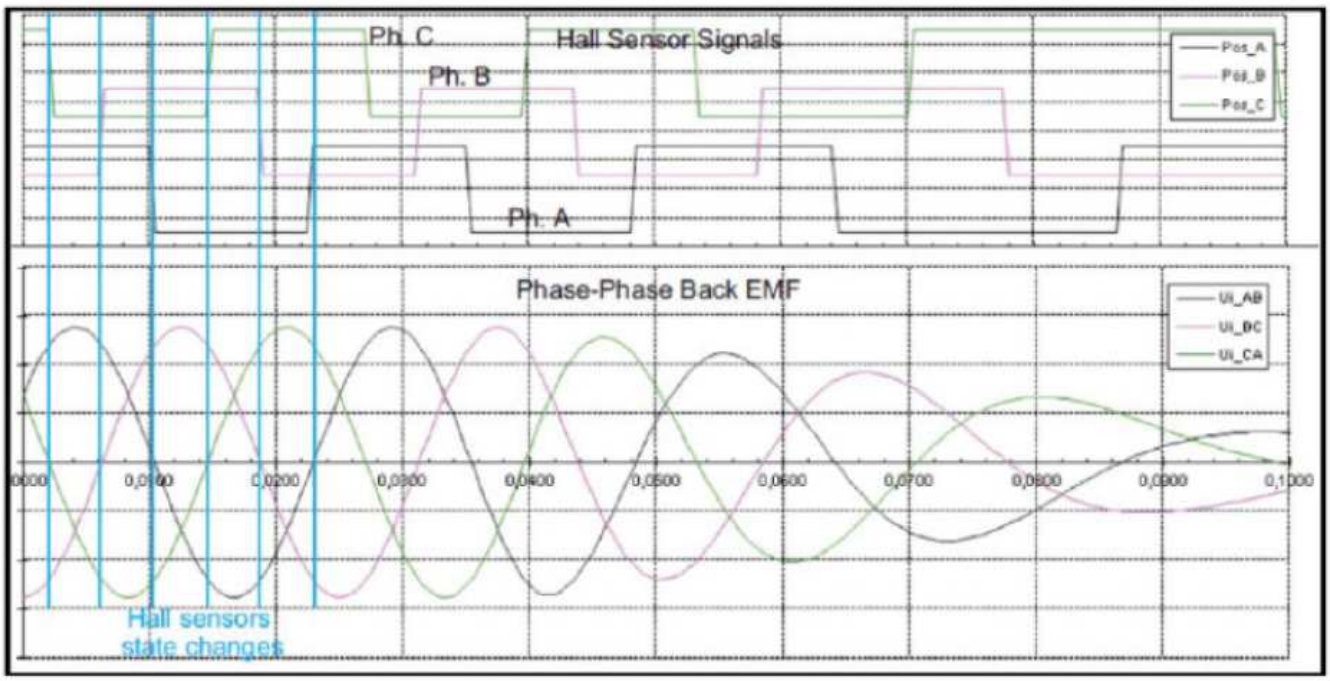

Figure 20. BLDC motor back-EMF and Hall sensor signal alignment

Based on the Hall sensor signal, the BLDC motor commutation table is developed. An example is shown in the next table. The right-hand side of the table shows the Hall sensors signal, while the left side applied phase voltage.

Table 20. BLDC motor commutation example

Commutation Vector			Vector	Hall sensor pattern definition			Hall sensor pattern result
Phase A	Phase B	Phase C		Hall Sensor C	Hall Sensor B	Hall Sensor A	
NC	$+V_{DCB}$	$-V_{DCB}$	A	1	0	1	6
$-V_{DCB}$	$+V_{DCB}$	NC	B	1	0	0	5
$-V_{DCB}$	NC	$+V_{DCB}$	C	1	1	0	4
NC	$-V_{DCB}$	$+V_{DCB}$	D	0	1	0	3
$+V_{DCB}$	$-V_{DCB}$	NC	E	0	1	1	2
$+V_{DCB}$	NC	$-V_{DCB}$	F	0	0	1	1

3.10 Resolver Interface

The resolver interface is included to observe motor rotor position. The board is populated with the hardware interface to measure motor position and speed. The resolver connector can be connected to J62.

For detailed description, see application note AN1942 or patent WO/2007/137625.