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S1C17M12/M13 (rev1.0)

EPSON
EXCEED YOUR VISION

16-bit Single Chip Microcontroller

- 16KB Flash ROM: Read/program protection function, 2KB RAM
- Supports 1.8V to 5.5V wide range operating voltage.
- Five-digit seven-segment LED controller (8SEG × 1–5COM (max.))
- Supports various kinds of interfaces (UART, SPI, I^2C)

■ DESCRIPTIONS

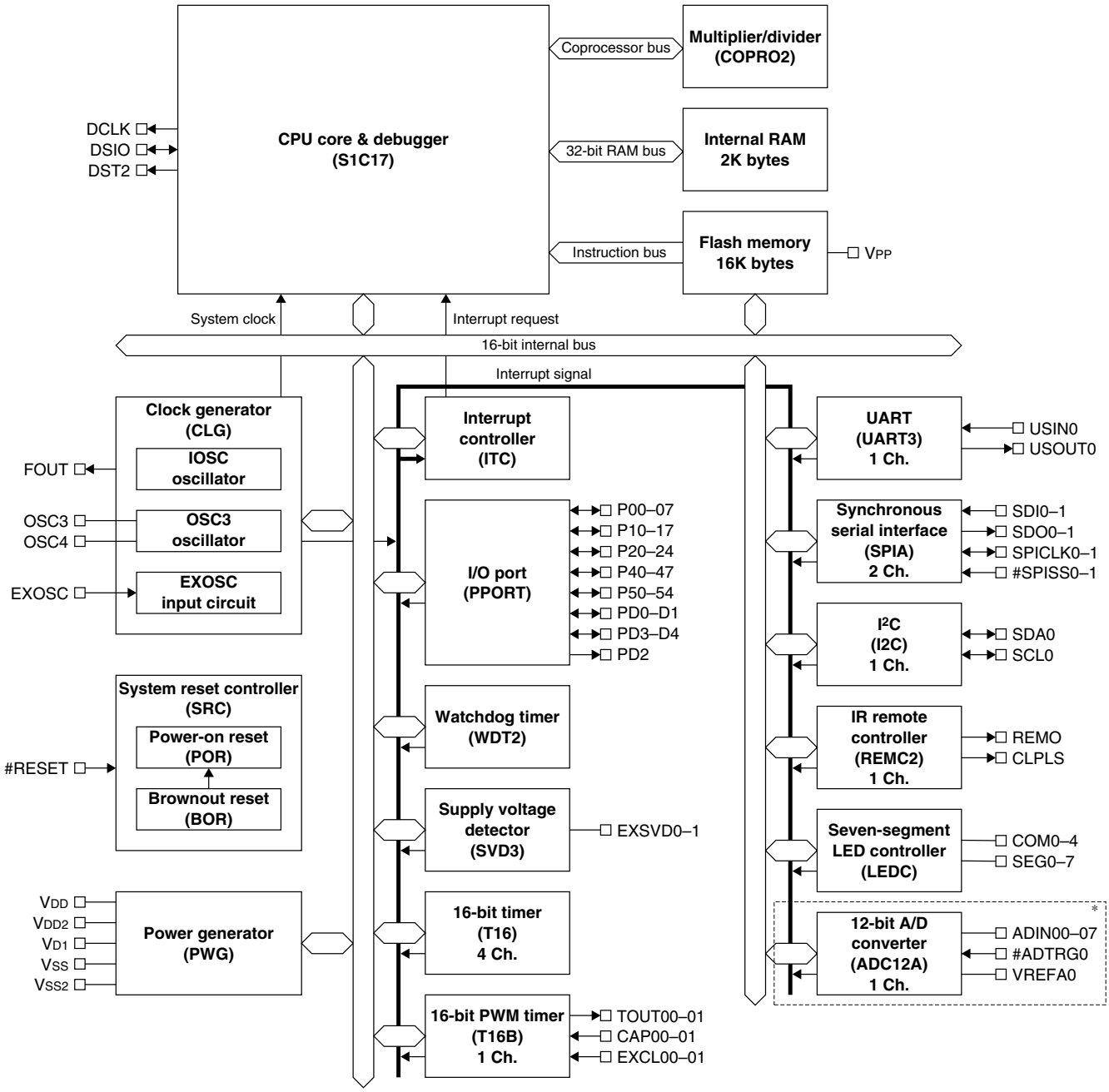
The S1C17M12/M13 is a 16-bit embedded Flash MCU that features low power consumption. It includes various serial interfaces and a seven-segment LED controller on the compact die. It is suitable for control panels with a seven-segment display for housing equipment and FA equipment.

■ FEATURES

Model	S1C17M12	S1C17M13
CPU		
CPU core	Seiko Epson original 16-bit RISC CPU core S1C17	
Other	On-chip debugger	
Embedded Flash memory		
Capacity	16K bytes (for both instructions and data)	
Erase/program count	1,000 times (min.)	
Other	Security function to protect from reading/programming by ICDmini	
	On-board programming function using ICDmini	
Embedded RAM		
Capacity	2K bytes	
Clock generator (CLG)		
System clock source	3 sources (IOSC/OSC3/EXOSC)	
System clock frequency (operating frequency)	16.8 MHz (max.)	
IOSC oscillator circuit (boot clock source)	700 kHz (typ.) embedded oscillator	
	23 µs (max.) starting time (time from cancelation of SLEEP state to vector table read by the CPU)	
OSC3 oscillator circuit	16.8 MHz (max.) crystal/ceramic oscillator	
	4, 8, 12, and 16 MHz-switchable embedded oscillator	
EXOSC clock input	16.8 MHz (max.) square or sine wave input	
Other	Configurable system clock division ratio	
	Configurable system clock used at wake up from SLEEP state	
	Operating clock frequency for the CPU and all peripheral circuits is selectable.	
I/O port (PPORT)		
Number of general-purpose I/O ports	Input/output port: 38 bits (max.)	
	Output port: 1 bit (max.)	
	Pins are shared with the peripheral I/O.	
Number of input interrupt ports	34 bits (max.)	
Number of ports that support universal port multiplexer (UPMUX)	21 bits	
	A peripheral circuit I/O function selected via software can be assigned to each port.	
Number of high drive-capability Nch outputs	8 bits (max.)	
	7 mA output (max.)	
Number of high drive-capability Pch outputs	5 bits (max.)	
	56 mA output (max., Total sum of 5 bits)	
Timers		
Watchdog timer (WDT2)	Generates NMI or watchdog timer reset.	
	Programmable NMI/reset generation cycle	
16-bit timer (T16)	4 channels	
	Generates the SPIA master clock and the ADC12A trigger signal.	
16-bit PWM timer (T16B)	1 channel	
	Event counter/capture function	
	PWM waveform generation function	
	Number of PWM output or capture input ports: 2 ports/channel	
Supply voltage detector (SVD3)		
Detection voltage	V_{DD} or external voltage (two external voltage input ports are provided.)	
Detection level	V_{DD}: 28 levels (1.8 to 5.0 V)/external voltage: 32 levels (1.2 to 5.0 V)	
Other	Intermittent operation mode	
	Generates an interrupt or reset according to the detection level evaluation.	

Model	S1C17M12	S1C17M13
Serial interfaces		
UART (UART3)	4 channels	
	Baud-rate generator included, IrDA1.0 supported	
	Open drain output, signal polarity, and baud rate division ratio are configurable.	
	Infrared communication carrier modulation output function	
Serial interfaces		
Synchronous serial interface (SPIA)	2 channels	
	2 to 16-bit variable data length	
	The 16-bit timer (T16) can be used for the baud-rate generator in master mode.	
I^2C (I2C)	1 channel	
	Baud-rate generator included	
IR remote controller (REMC2)		
Number of transmitter channels	1 channel	
Other	EL lamp drive waveform can be generated for an application example.	
Seven-segment LED controller (LEDC)		
LED control output	Seven-segment LED outputs up to five digits (8SEG × 1–5COM(max.))	
	COM time-division dynamic drive control	
	Software configurable anode/cathode common mode and off-state pin status	
	Four-level brightness adjustment function	
12-bit A/D converter (ADC12A)		
Conversion method	–	Successive approximation type
Resolution		12 bits
Number of conversion channels		1 channel
Number of analog signal inputs		8 ports/channel
Multiplier/divider (COPRO2)		
Arithmetic functions	16-bit × 16-bit multiplier	
	16-bit × 16-bit + 32-bit multiply and accumulation unit	
	32-bit ÷ 32-bit divider	
Reset		
#RESET pin	Reset when the reset pin is set to low.	
Power-on reset	Reset at power on.	
Brownout reset	Reset when the power supply voltage drops.	
Key entry reset	Reset when the P00 to P01/P02/P03 keys are pressed simultaneously (can be enabled/disabled using a register).	
Watchdog timer reset	Reset when the watchdog timer overflows (can be enabled/disabled using a register).	
Supply voltage detector reset	Reset when the supply voltage detector detects the set voltage level (can be enabled/disabled using a register).	
Interrupt		
Non-maskable interrupt	4 systems (Reset, address misaligned interrupt, debug, NMI)	
Programmable interrupt	External interrupt: 1 system (8 levels)	
	Internal interrupt: 14 systems (8 levels)	
Power supply voltage		
V_{DD} operating voltage	1.8 to 5.5 V	
V_{DD} operating voltage for Flash programming	1.8 to 5.5 V (V_{PP} = 7.5 V external power supply is required.)	
Operating temperature		
Operating temperature range	-40 to 85 °C	
Current consumption (Typ. value)		
SLEEP mode	0.5 µA (TBD) IOSC = OFF, OSC3 = OFF	
HALT mode	180 µA (TBD) OSC3 = 4 MHz (internal oscillator)	
RUN mode	600 µA (TBD) OSC3 = 4 MHz (internal oscillator), CPU = OSC3 (1 wait cycle)	
	1,700 µA (TBD) OSC3 = 16 MHz (internal oscillator), CPU = OSC3 (2 wait cycles)	
Shipping form		
1	TQFP12-48pin (Lead pitch: 0.5 mm)	

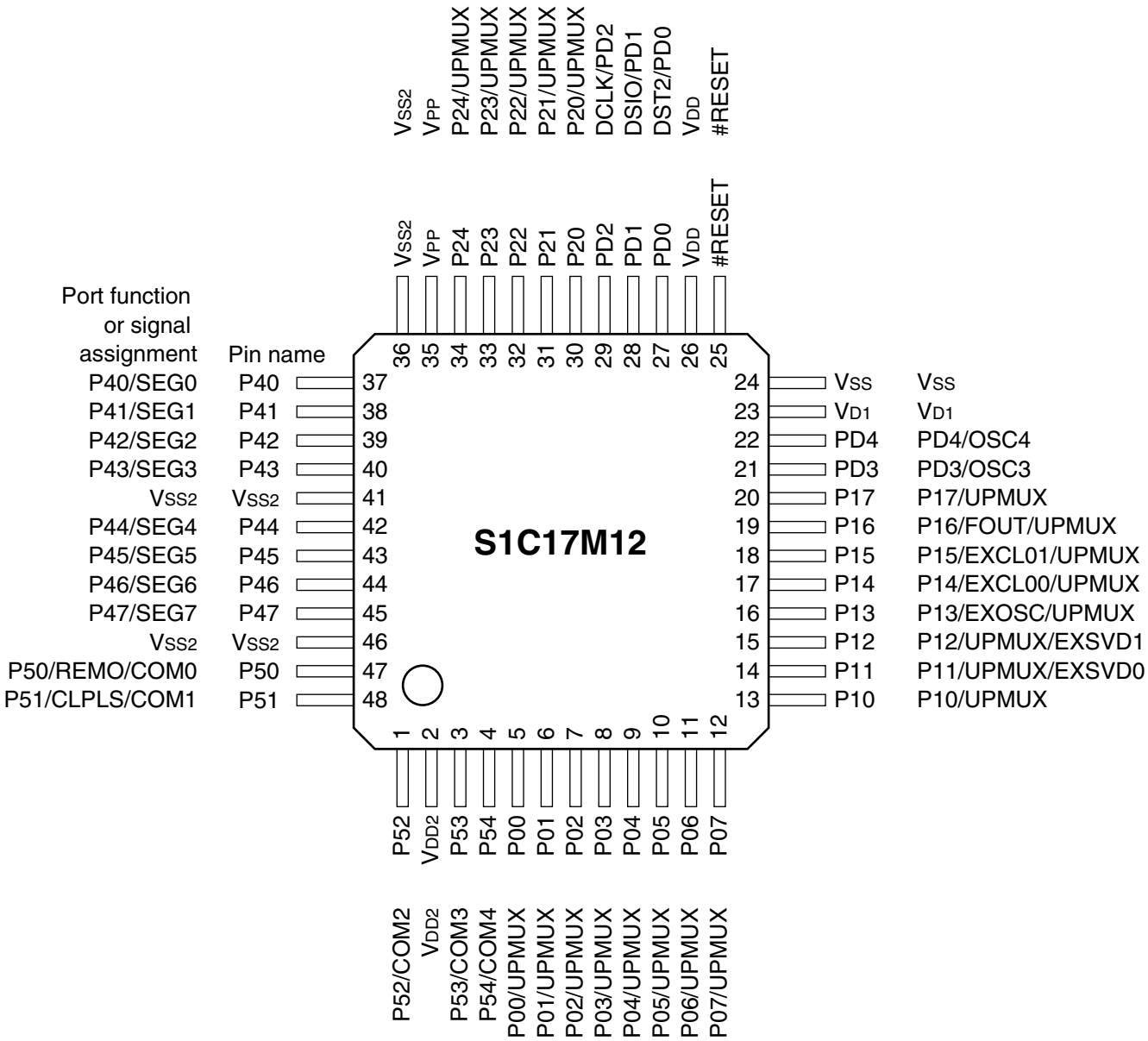
■ BLOCK DIAGRAM



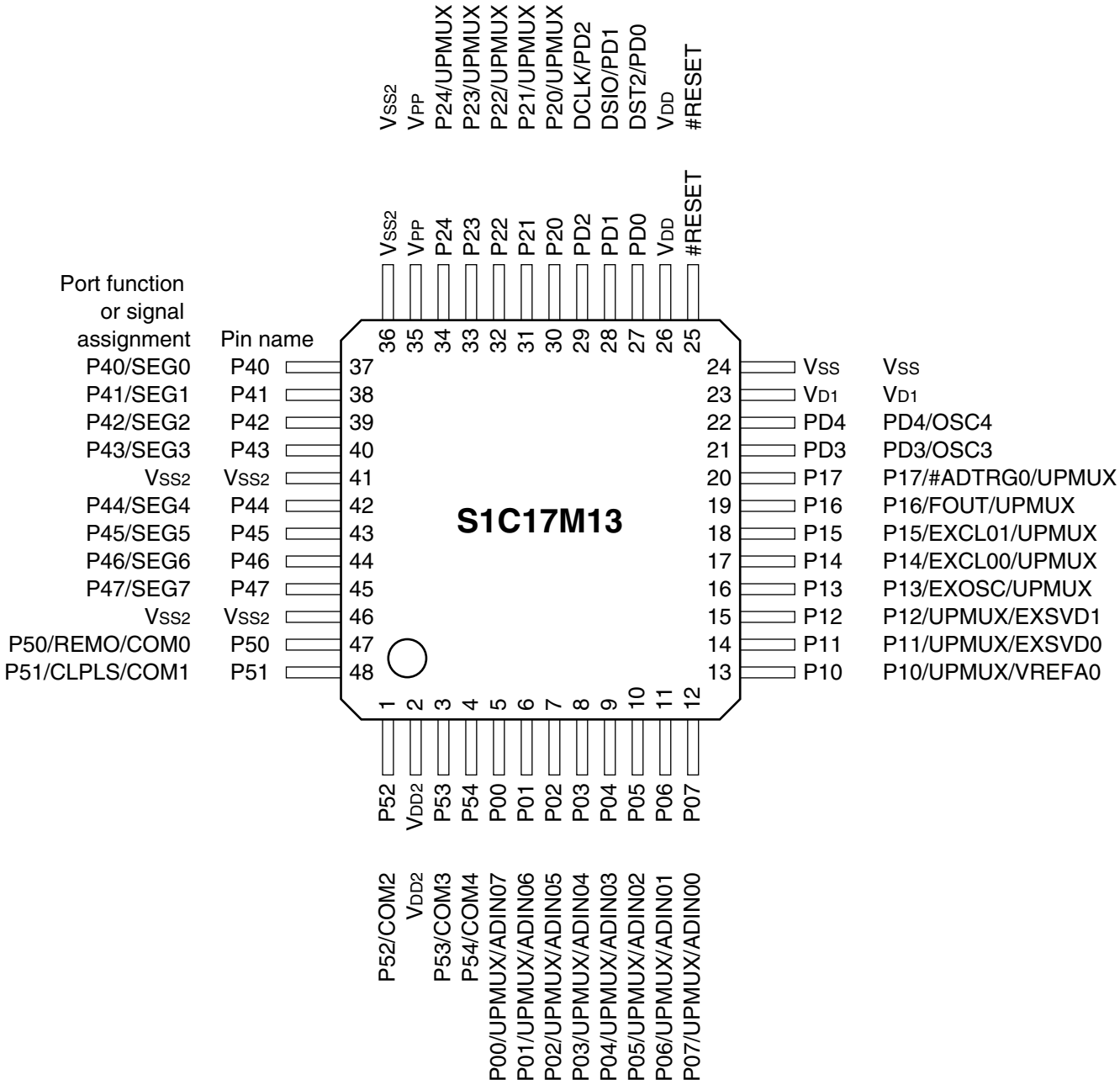
* Not available in the S1C17M12.

■ PIN CONFIGURATION DIAGRAMS

S1C17M12 pin configuration diagram (TQFP12-48pin)



S1C17M13 pin configuration diagram (TQFP12-48pin)



■ PIN DESCRIPTIONS

Symbol meanings

Assigned signal: The signal listed at the top of each pin is assigned in the initial state. The pin function must be switched via software to assign another signal (see the "I/O Ports" chapter).

I/O:
- I = Input
- O = Output
- I/O = Input/output
- P = Power supply
- A = Analog signal
- Hi-Z = High impedance state

Initial state:
- I (Pull-up) = Input with pulled up
- I (Pull-down) = Input with pulled down
- Hi-Z = High impedance state
- O (H) = High level output
- O (L) = Low level output

Tolerant fail-safe structure:
- ✓ = Over voltage tolerant fail-safe type I/O cell included (see the "I/O Ports" chapter)
  The over voltage tolerant fail-safe type I/O cell allows interfacing without passing unnecessary current even if a voltage exceeding V_{DD} is applied to the port. Also unnecessary current is not consumed when the port is externally biased without supplying V_{DD}.

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	S1C17M12	S1C17M13
V_{DD}	V_{DD}	P	–	–	Power supply (+), I/O power supply (except for P50–54)	✓	✓
V_{DD2}	V_{DD2}	P	–	–	I/O power supply (P50–54)	✓	✓
V_{SS}	V_{SS}	P	–	–	GND (except for P40–47, P50–54)	✓	✓
V_{SS2}	V_{SS2}	P	–	–	GND (P40–47, P50–54)	✓	✓
V_{PP}	V_{PP}	P	–	–	Power supply for Flash programming	✓	✓
V_{D1}	V_{D1}	A	–	–	V_{D1} regulator output	✓	✓
#RESET	#RESET	I	I (Pull-up)	–	Reset input	✓	✓
P00	P00	I/O	Hi-Z	–	I/O port	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓
	ADIN07	A			12-bit A/D converter Ch.0 analog signal input 7	–	✓
P01	P01	I/O	Hi-Z	–	I/O port	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓
	ADIN06	A			12-bit A/D converter Ch.0 analog signal input 6	–	✓
P02	P02	I/O	Hi-Z	–	I/O port	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓
	ADIN05	A			12-bit A/D converter Ch.0 analog signal input 5	–	✓
P03	P03	I/O	Hi-Z	–	I/O port	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓
	ADIN04	A			12-bit A/D converter Ch.0 analog signal input 4	–	✓
P04	P04	I/O	Hi-Z	–	I/O port	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓
	ADIN03	A			12-bit A/D converter Ch.0 analog signal input 3	–	✓
P05	P05	I/O	Hi-Z	–	I/O port	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓
	ADIN02	A			12-bit A/D converter Ch.0 analog signal input 2	–	✓
P06	P06	I/O	Hi-Z	–	I/O port	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓
	ADIN01	A			12-bit A/D converter Ch.0 analog signal input 1	–	✓
P07	P07	I/O	Hi-Z	–	I/O port	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓
	ADIN00	A			12-bit A/D converter Ch.0 analog signal input 0	–	✓
P10	P10	I/O	Hi-Z	–	I/O port	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓
	VREFA0	A			12-bit A/D converter Ch.0 reference voltage input	–	✓
P11	P11	I/O	Hi-Z	–	I/O port	✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)	✓	✓
	EXSVD0	A			External power supply voltage detection input Ch.0	✓	✓

Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function		S1C17M12	S1C17M13
P12	P12	I/O	Hi-Z	–	I/O port		✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		✓	✓
	EXSVD1	A			External power supply voltage detection input Ch.1		✓	✓
P13	P13	I/O	Hi-Z	–	I/O port		✓	✓
	EXOSC	I			Clock generator external clock input		✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		✓	✓
P14	P14	I/O	Hi-Z	–	I/O port		✓	✓
	EXCL00	I			16-bit PWM timer Ch.0 event counter input 0		✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		✓	✓
P15	P15	I/O	Hi-Z	–	I/O port		✓	✓
	EXCL01	I			16-bit PWM timer Ch.0 event counter input 1		✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		✓	✓
P16	P16	I/O	Hi-Z	–	I/O port		✓	✓
	FOUT	O			Clock external output		✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		✓	✓
P17	P17	I/O	Hi-Z	–	I/O port		✓	✓
	#ADTRG0	I			12-bit A/D converter Ch.0 trigger input		–	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		✓	✓
P20	P20	I/O	Hi-Z	–	I/O port		✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		✓	✓
P21	P21	I/O	Hi-Z	–	I/O port		✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		✓	✓
P22	P22	I/O	Hi-Z	–	I/O port		✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		✓	✓
P23	P23	I/O	Hi-Z	–	I/O port		✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		✓	✓
P24	P24	I/O	Hi-Z	–	I/O port		✓	✓
	UPMUX	I/O			User-selected I/O (universal port multiplexer)		✓	✓
P40	P40	I/O	Hi-Z	–	I/O port	High drive-capability	✓	✓
	SEG0	O			LED segment output	Nch output	✓	✓
P41	P41	I/O	Hi-Z	–	I/O port	High drive-capability	✓	✓
	SEG1	O			LED segment output	Nch output	✓	✓
P42	P42	I/O	Hi-Z	–	I/O port	High drive-capability	✓	✓
	SEG2	O			LED segment output	Nch output	✓	✓
P43	P43	I/O	Hi-Z	–	I/O port	High drive-capability	✓	✓
	SEG3	O			LED segment output	Nch output	✓	✓
P44	P44	I/O	Hi-Z	–	I/O port	High drive-capability	✓	✓
	SEG4	O			LED segment output	Nch output	✓	✓
P45	P45	I/O	Hi-Z	–	I/O port	High drive-capability	✓	✓
	SEG5	O			LED segment output	Nch output	✓	✓
P46	P46	I/O	Hi-Z	–	I/O port	High drive-capability	✓	✓
	SEG6	O			LED segment output	Nch output	✓	✓
P47	P47	I/O	Hi-Z	–	I/O port	High drive-capability	✓	✓
	SEG7	O			LED segment output	Nch output	✓	✓
P50	P50	I/O	Hi-Z	–	I/O port	High drive-capability	✓	✓
	REMO	O			IR remote controller transmit data output	Pch output	✓	✓
	COM0	O			LED common output		✓	✓
P51	P50	I/O	Hi-Z	–	I/O port	High drive-capability	✓	✓
	CLPLS	O			IR remote controller clear pulse output	Pch output	✓	✓
	COM1	O			LED common output		✓	✓
P52	P50	I/O	Hi-Z	–	I/O port	High drive-capability	✓	✓
	COM2	O			LED common output	Pch output	✓	✓
P53	P50	I/O	Hi-Z	–	I/O port	High drive-capability	✓	✓
	COM3	O			LED common output	Pch output	✓	✓
P54	P50	I/O	Hi-Z	–	I/O port	High drive-capability	✓	✓
	COM4	O			LED common output	Pch output	✓	✓
PD0	DST2	O	O (L)	–	On-chip debugger status output		✓	✓
	PD0	I/O			I/O port		✓	✓
PD1	DSIO	I/O	I (Pull-up)	–	On-chip debugger data input/output		✓	✓
	PD1	I/O			I/O port		✓	✓
PD2	DCLK	O	O (H)	–	On-chip debugger clock output		✓	✓
	PD2	O			Output port		✓	✓

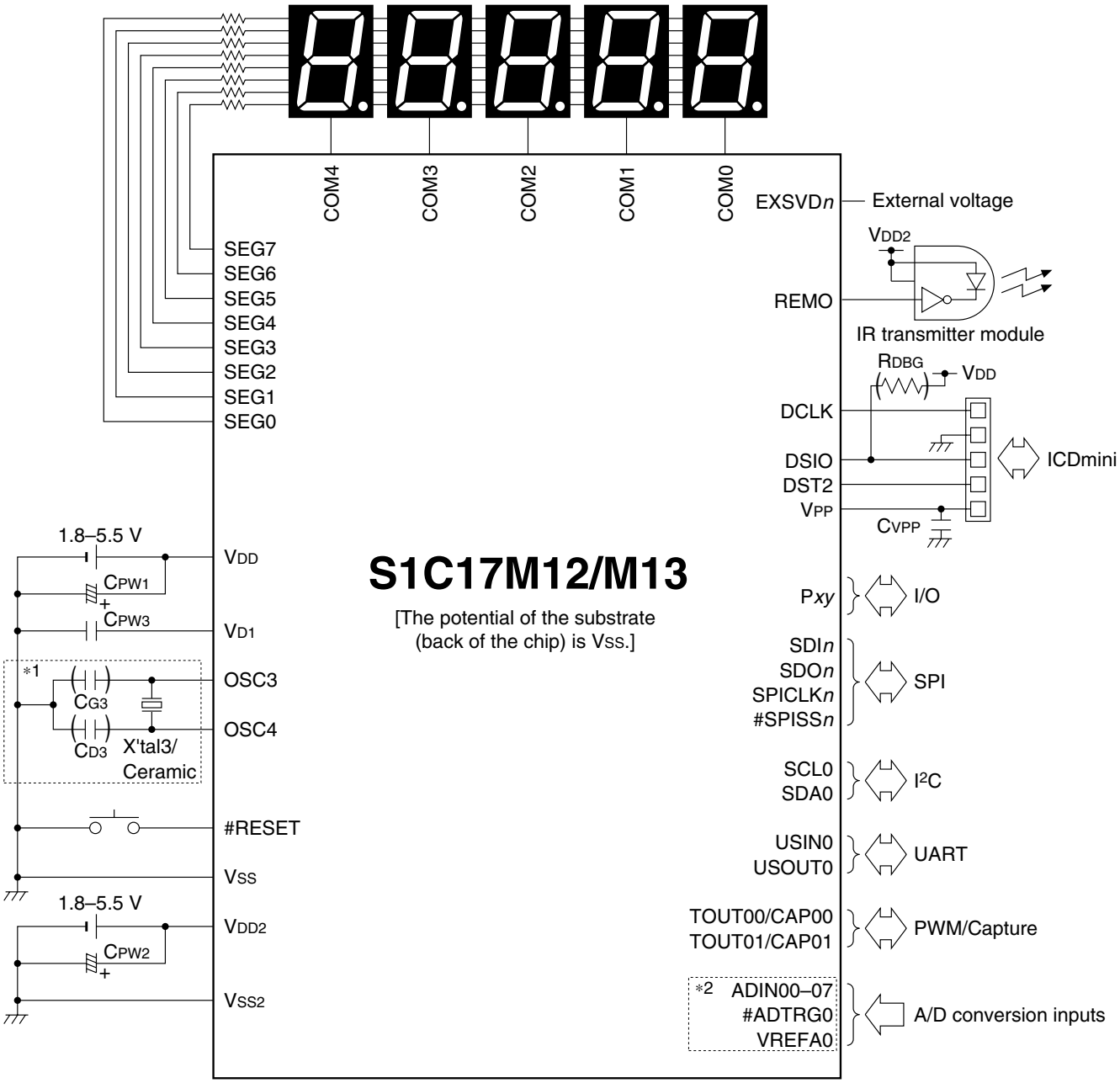
Pin/pad name	Assigned signal	I/O	Initial state	Tolerant fail-safe structure	Function	S1C17M12	S1C17M13
PD3	PD3	I/O	Hi-Z	–	I/O port	✓	✓
	OSC3	A			OSC3 oscillator circuit input	✓	✓
PD4	PD4	I/O	Hi-Z	–	I/O port	✓	✓
	OSC4	A			OSC3 oscillator circuit output	✓	✓

Universal port multiplexer (UPMUX)

The universal port multiplexer (UPMUX) allows software to select the peripheral circuit input/output function to be assigned to each pin from those listed below. Note, however, that a function cannot be assigned to two or more pins simultaneously.

Peripheral circuit	Signal to be assigned	I/O	Channel number *n*	Function
Synchronous serial interface (SPIA)	SDI*n*	I	*n* = 0, 1	SPIA Ch.*n* data input
	SDO*n*	O		SPIA Ch.*n* data output
	SPICLK*n*	I/O		SPIA Ch.*n* clock input/output
	#SPISS*n*	I		SPIA Ch.*n* slave-select input
I^2C (I2C)	SCL*n*	I/O	*n* = 0	I2C Ch.*n* clock input/output
	SDA*n*	I/O		I2C Ch.*n* data input/output
UART (UART3)	USIN*n*	I	*n* = 0	UART3 Ch.*n* data input
	USOUT*n*	O		UART3 Ch.*n* data output
16-bit PWM timer (T16B)	TOUT*n*0/CAP*n*0	I/O	*n* = 0	T16B Ch.*n* PWM output/capture input 0
	TOUT*n*1/CAP*n*1	I/O		T16B Ch.*n* PWM output/capture input 1

■ Basic External Connection Diagram



*1:When OSC3 crystal/ceramic oscillator is selected
*2:Available only in the S1C17M13
( ): Do not mount components if unnecessary.

Sample external components

Symbol	Name	Recommended components
X'tal3	Crystal resonator	CA-301 (4 MHz) manufactured by Seiko Epson Corporation
Ceramic	Ceramic resonator	CSBLA_J (1 MHz) manufactured by Murata Manufacturing Co., Ltd.
C_{G3}	OSC3 gate capacitor	Ceramic capacitor
C_{D3}	OSC3 drain capacitor	Ceramic capacitor
C_{PW1}	Bypass capacitor between V_{SS} and V_{DD}	Ceramic capacitor or electrolytic capacitor
C_{PW2}	Bypass capacitor between V_{SS2} and V_{DD2}	Ceramic capacitor or electrolytic capacitor
C_{PW3}	Capacitor between V_{SS} and V_{D1}	Ceramic capacitor
R_{DBG}	DSIO pull-up resistor	Thick film chip resistor
C_{VPP}	Capacitor between V_{SS} and V_{PP}	Ceramic capacitor

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