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EPSON
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S1D13515 / S2D13515 Display Controller

Hardware Functional Specification

SEIKO EPSON CORPORATION

Rev. 1.7

NOTICE

Table Of Contents

Chapter 1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13515/S2D13515 Display Controller. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

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We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

1.2 Overview Description

The S1D13515/S2D13515 is a highly integrated color LCD graphics controller with external memory interface. The architecture is designed to meet the needs of automotive and embedded markets requiring a flexible LCD solution. For automotive applications, the S2D13515 has three primary target placements within a vehicle.

1. Heads-Up Display
2. Instrument Cluster
3. Center Console

The S1D13515/S2D13515 advances on the successes of other Epson LCD controllers by embedding a proprietary 32-bit RISC CPU and associated accelerator blocks to achieve an increase in flexibility and functionality over previous designs. Routines are provided allowing for audio playback, 2D BitBLT operations, warp and filtering before display operations, and the ability to offer OpenGL-ES 1.1 support. In particular, the warp functions make this an ideal solution for the automotive Heads-Up Display (HUD) market, or pseudo 3D navigation displays.

The S1D13515/S2D13515 is an affordable, low power device which uses a flexible external SDRAM memory interface to provide its frame buffer. It supports a wide variety of CPU interfaces and LCD panel types, including Double Display panels, which makes it an excellent choice for instrumentation or center cluster applications. While focusing on the automotive market, the S1D13515/S2D13515's impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of other markets.

The S1D13515/S2D13515 design includes some of the following key features:

1. Warp engine for HUD projection correction
2. Embedded 32-bit proprietary RISC CPU
3. Support for two TFT Displays simultaneously
4. Support for Double Display LCD panels from Epson and Sharp
5. The ability to provide OpenGL-ES library functionality
6. The ability to playback audio
7. The ability to reset and display an image without the Host CPU involvement

Chapter 2 Features

2.1 Memory

- Uses external SDRAM which is:
  - Accessible by both the internal and Host CPUs
  - Used for executable code, data, and the frame buffer
  - Addressable through direct or indirect access modes
  - Accessible linearly in configurable 4M byte paging windows (direct access mode)
- SDRAM Interface:
  - SDRAM Clock Frequency: 100Mhz (typical)
  - Supports x16 and x32 SDRAM interfaces (x32 is strongly recommended in most cases)
  - Supports 8/16/32/64M bytes of 4 bank SDRAM
  - Low power design

2.2 CPU Interfaces

Note
The S1D/S2D13515 supports Little Endian interface only.

- Direct and indirect interface support for the following CPU interfaces:
  - Intel 80 Types 1 and 2 (8/16-bit)
  - Renesas SH-4 (8/16-bit)
  - FreeScale MPC555 PowerPC bus interface with burst and non-burst modes (16-bit Little Endian configuration only)
  - NEC V850 Types 1 and 2 (8/16-bit)
  - Texas Instruments TMS470 with burst mode (16-bit only)
  - Marvell PXA3xx (16-bit Direct only)
- Serial Host Interface
  - SPI
  - I2C

2.3 Panel Interface Support

- Single or Dual panels (dual panel implementations can have independent images)
  - LCD1 supports:
    - 12/16/18-bit interface for Generic TFT/TFD
    - Optionally, LCD1 pins can be used for a second Camera / RGB data stream
  - LCD2 supports:
    - 12/16/18/24-bit interface for Generic TFT/TFD
    - EID Double Screen panel
    - Sharp DualView panel
  - Optional Serial Command interface supports:
    - a-Si TFT interface (8-bit)
    - TFT w/u-Wire interface (16-bit)
    - EPSON ND-TFD 4 pin interface (8-bit)
    - EPSON ND-TFD 3 pin interface (9-bit)
    - 24-bit serial
- Panel Resolution Examples:
  - 800x480 + 320x240 @ 32 bpp, 60Hz
  - 1024x768 @ 32 bpp, 60Hz
- TV-Out can be achieved by connecting an external TV encoder, such as the S1D13746, to the LCD outputs

2.4 Display Features

- Four input window sources can be stored in SDRAM (Main/Aux/OSD/LCD Fetcher) and support:
  - 8/16/24 bpp color depths
  - Hardware / Software Double Buffer Frame Control
  - Horizontal Flip
  - Virtual Width
  - Alpha Blending for the OSD
- Blending Engine can combine various input window sources for output
  - Three input sources
  - Input sources can be blended in four different ways
- Warp logic for HUD projection correction or other distortion compensation
  - Processed image can be sent back to SDRAM
- Camera1 or Camera2 image can be stored in SDRAM and used for Main/Aux/OSD/LCD Fetcher/Warp/Sprite
- Interrupt
  - Maskable Non-Display (Vsync) Interrupt support
  - Delayed version of Vsync Interrupt support
  - All interrupts are sent to the internal CPU, but can also be redirected to the HOST

2.5 Embedded CPU

- Embedded CPU Speed: 50MHz (typical)
- 32-bit RISC CPU with the following routines:
  - Audio decode (supported codecs: MP3, AAC, WAV, ADPCM, Ogg Vorbis)
  - 2D BitBLT Acceleration with API
    Some functions will be embedded in mask ROM, others will be provided as optional.
  - OpenGL-ES Assist (OpenGL-ES v1.1 compliant)
  - OEM defined functions

2.6 Sprite Engine

- 2D Sprite Engine
  - Up to Eight Sprites
  - Image rotation and mirror functions
  - Alpha Blending
  - Typical usage: Instrument Cluster, Simple GUI composition, etc.

2.7 Video / Camera Input

- Video / Camera input port supporting one of the following configurations:
  - up to two 8-bit cameras
  - up to two RGB data streams
  - one 8-bit camera and one RGB data stream
  - Note: When the second camera input is used, only a single panel is available.
- Supports ITU-R BT.656 YUV format
- Supports Interlaced or Progressive input
- Supports down-scaling of the video input stream
- Captures YUV Data into SDRAM as RGB format

2.8 Clock Source

- Flexible Clock Structure:
  - Two embedded PLLs
  - Built-in crystal input
  - Digital clock input
- Clocks are dynamically turned off when modules are not needed

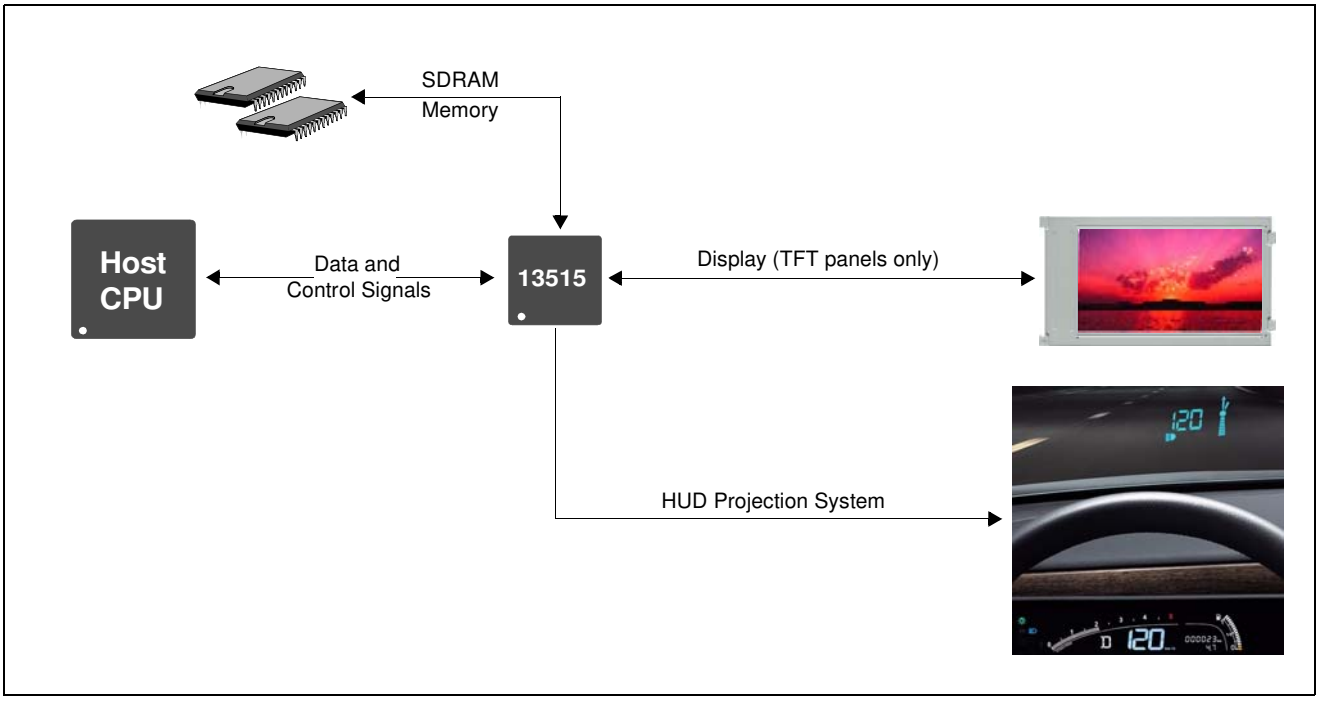
2.9 Miscellaneous

- Internal System Clock Speed: 50MHz (typical)
- IRQ output pin
  - Multiple interrupt sources (LCD1 / LCD2 / DMA / Timer / Keypad / etc.)
- I2C interface (typically used for camera)
- I2S interface (typically used for audio output)
- PWM: 2 channel for backlight control
- SPI Flash Memory interface
- Keypad Interface
  - 5 x 5 matrix support
- Software initiated power save mode
- General Purpose Input/Output pins are available
- IO operates at 3.3 volts ± 0.3v
- Core operates at 1.8 volts ± 0.15v
- Packages:
  - S1D13515B00B - PBGA1U 256-pin package (Body Size: 17 x 17 x 1.7 mm, Ball pitch: 1.0 mm)
  - S2D13515B00B - PBGA1U 256-pin package (Body Size: 17 x 17 x 1.7 mm, Ball pitch: 1.0 mm)
  - S1D13515F00A - QFP22 256-pin package (Body Size: 28 x 28 x 1.4 mm, Pin pitch: 0.4 mm)
  - S2D13515F00A - QFP22 256-pin package (Body Size: 28 x 28 x 1.4 mm, Pin pitch: 0.4 mm)
- Temperature Range:
  - S1D13515; -40° C to +85° C
  - S2D13515; -40° C to +105° C

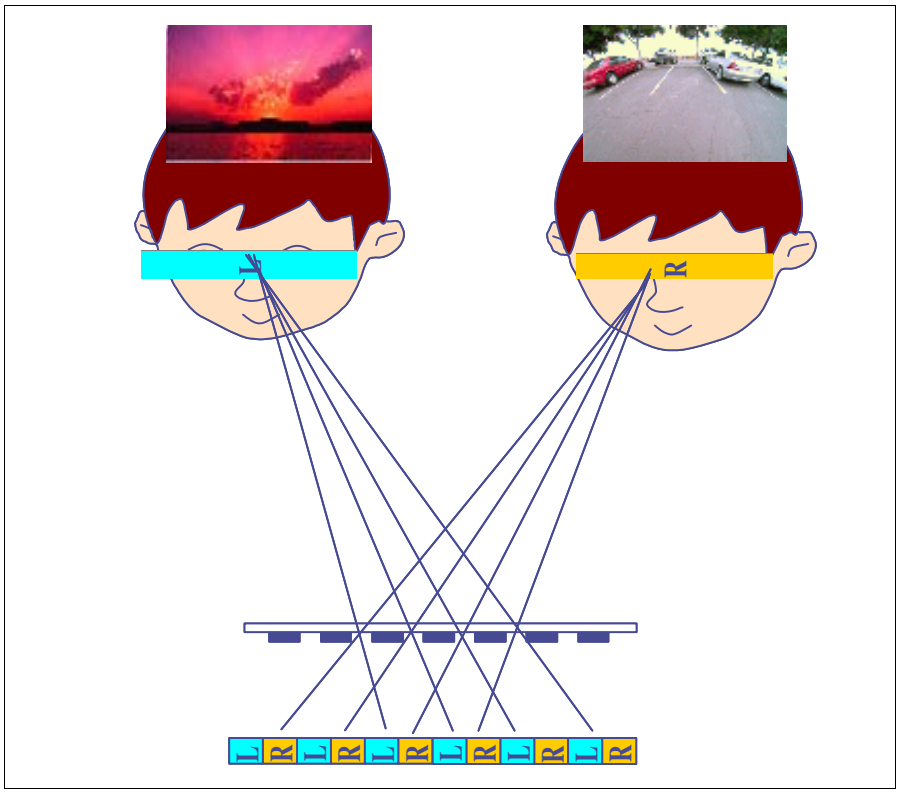
Chapter 3 Typical Implementation Use Cases

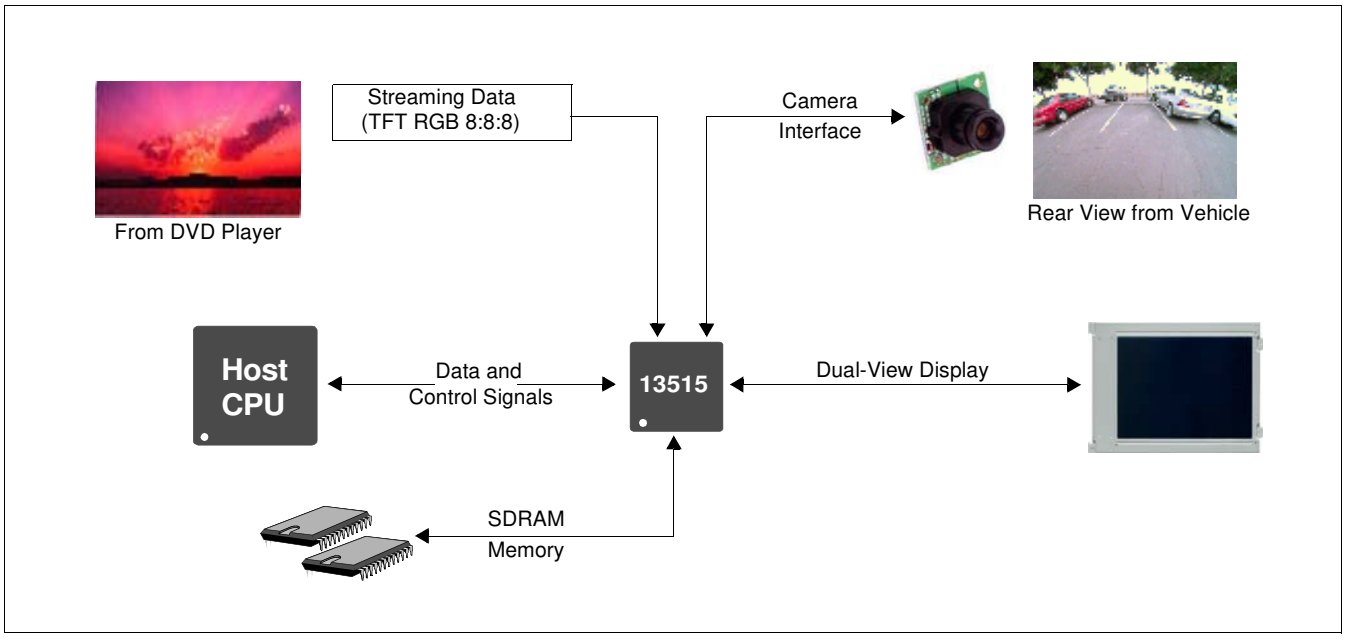
The following are generic Use Cases. For specific implementations of the S1D13515 and S2D13515, please see the Application Notes.

3.1 Use Case 1 - Heads-Up Display (HUD) with LCD Panel



3.2 Use Case 2 - Dual-View Panel with Streaming Data and Camera Input





Chapter 4 Block Diagram

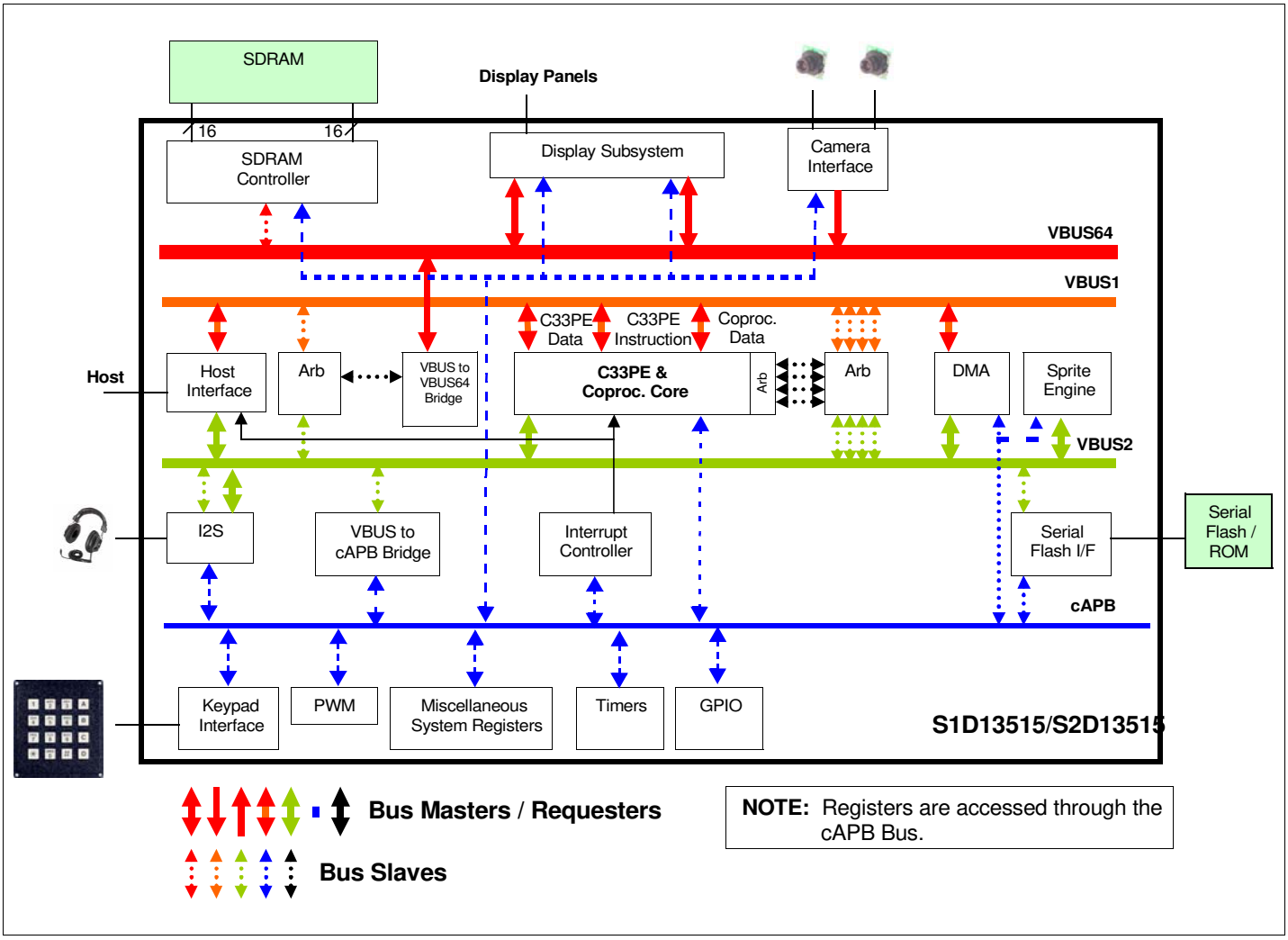


Figure 4-1: Block Diagram

Chapter 5 Pins

5.1 Pinout Diagram (QFP22 256-pin)

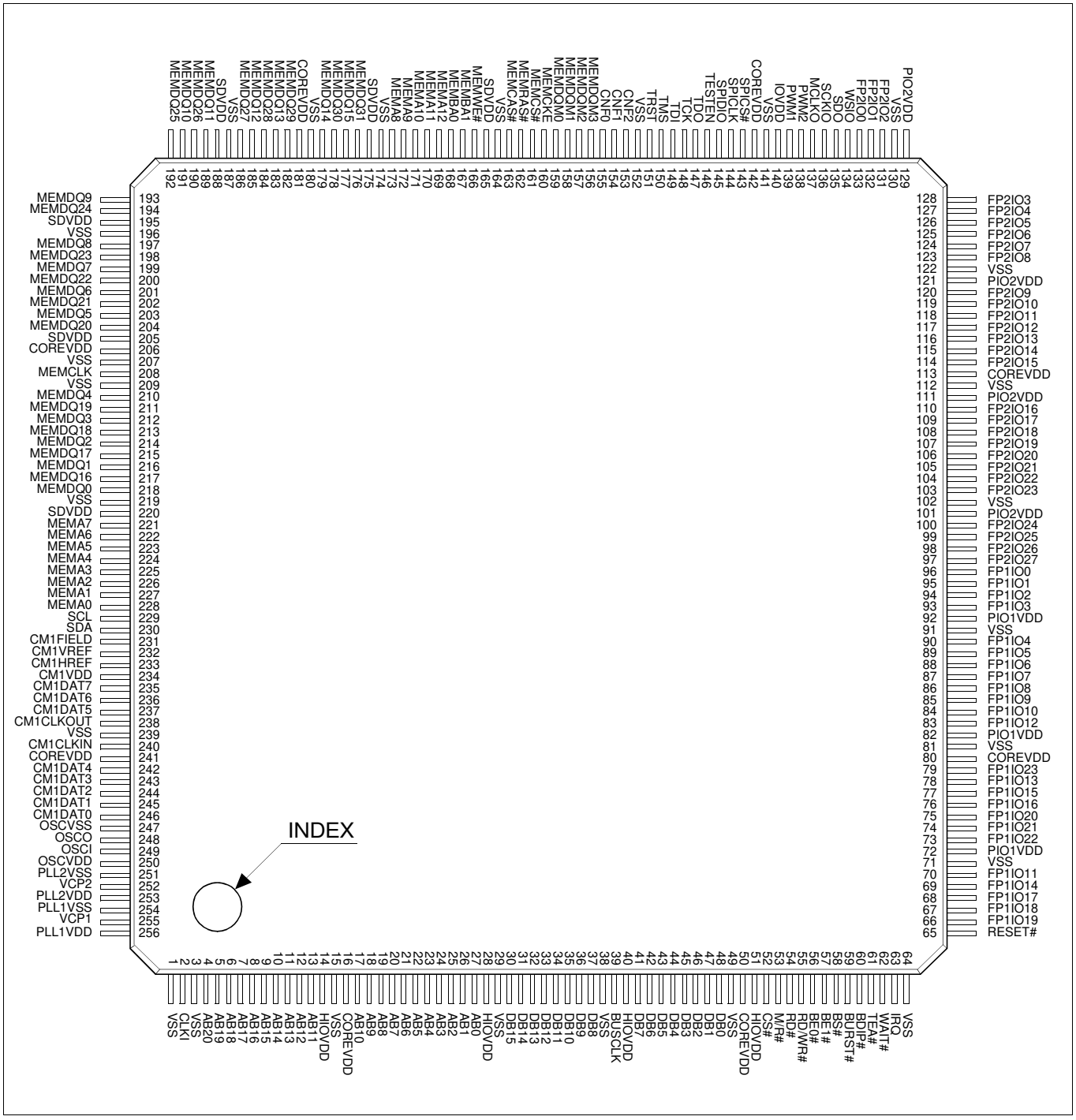


Figure 5-1: QFP22-256 Pin Mapping

5.2 Pinout Diagram (PBGA 256-pin)

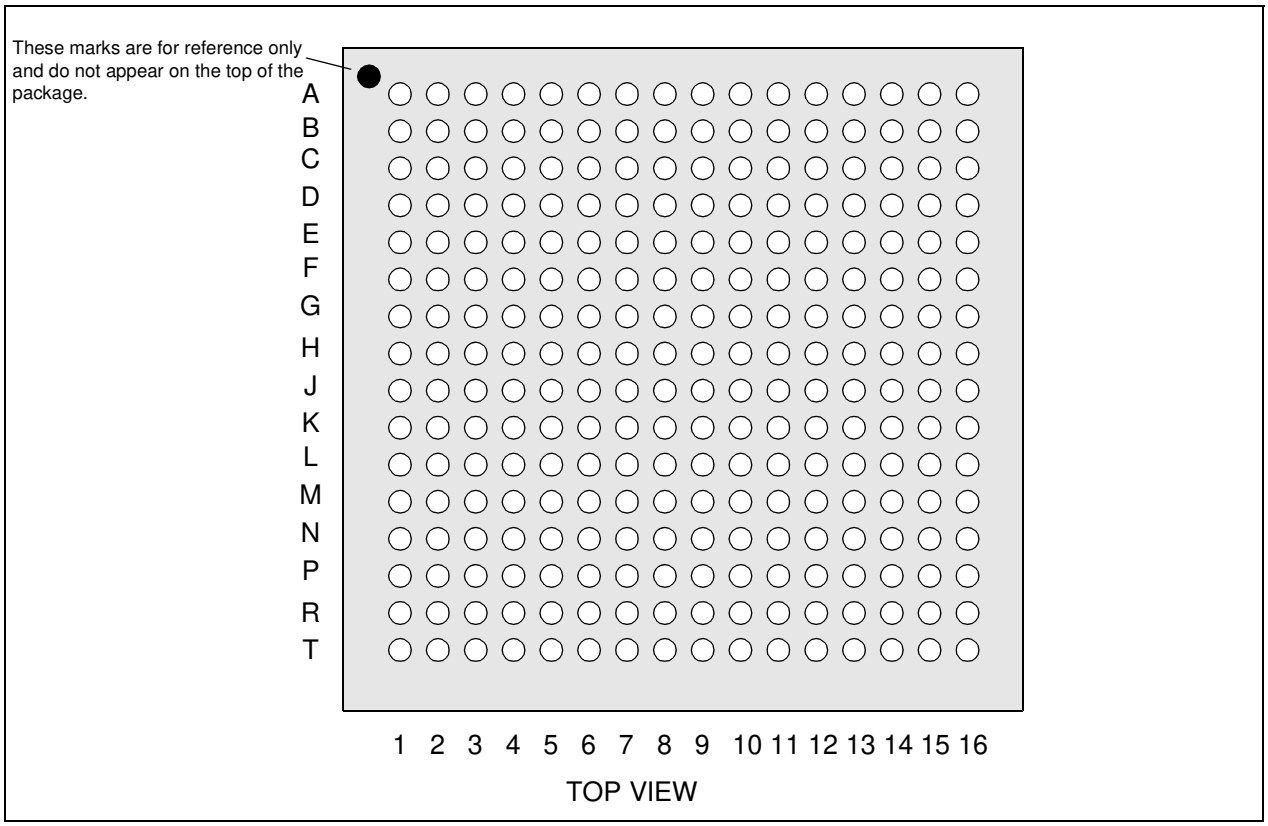


Figure 5-2: PBGA1U-256 Pin Mapping

Table 5-1: PBGA1U-256 Pin Mapping

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	VCP1	PLL2VDD	VCP2	OSCI	OSCO	CM1CLKOUT	CM1DAT5	MEMA0	MEMA6	MEMDQ1	MEMCLK	MEMDQ21	MEMDQ23	SDVDD	VSS	A
B	CLKI	PLL1VDD	PLL1VSS	PLL2VSS	OSCVDD	OSCVSS	CM1CLKIN	CM1VREF	MEMA1	SDVDD	MEMDQ18	VSS	MEMDQ6	MEMDQ8	MEMDQ25	MEMDQ10	B
C	AB20	VSS	CM1DAT0	CM1DAT1	CM1DAT2	CM1DAT3	VSS	CM1FIELD	MEMA3	MEMDQ0	MEMDQ4	COREVDD	MEMDQ22	MEMDQ9	MEMDQ26	MEMDQ11	C
D	AB15	AB16	AB18	AB19	CM1DAT4	COREVDD	CM1DAT6	SDA	MEMA5	MEMDQ16	VSS	MEMDQ20	MEMDQ24	SDVDD	MEMDQ27	MEMDQ12	D
E	COREVDD	HIOVDD	AB13	AB14	AB17	CM1DAT7	CM1VDD	SCL	MEMA7	MEMDQ2	SDVDD	MEMDQ7	VSS	MEMDQ28	VSS	COREVDD	E
F	AB6	AB7	AB10	VSS	AB11	AB12	CM1HREF	MEMA2	MEMDQ17	MEMDQ19	MEMDQ5	MEMDQ29	MEMDQ14	MEMDQ30	MEMA8	SDVDD	F
G	HIOVDD	AB2	AB3	AB4	AB5	AB8	AB9	MEMA4	MEMDQ3	MEMDQ13	MEMDQ15	MEMDQ31	VSS	MEMA9	MEMA10	MEMA12	G
H	DB12	DB15	DB13	DB14	VSS	AB0	AB1	VSS	VSS	MEMA11	MEMBA0	MEMBA1	MEMWE#	SDVDD	MEMRAS#	MEMCAS#	H
J	BUSCLK	DB8	DB9	HIOVDD	DB7	DB10	DB11	VSS	VSS	CNF0	MEMDQM3	MEMDQM2	MEMDQM1	MEMDQM0	MEMCS#	MEMCKE	J
K	DB3	DB2	DB4	DB5	DB6	DB1	FP1IO10	FP2IO26	FP2IO18	FP2IO10	TCK	TMS	TRST	VSS	CNF1	CNF2	K
L	DB0	COREVDD	CS#	VSS	HIOVDD	FP1IO16	FP1IO9	FP1IO0	FP2IO21	FP2IO13	SPIDIO	SPICLK	VSS	TESTEN	TDO	TDI	L
M	M/R#	RD#	RD/WR#	BE0#	BS#	FP1IO15	FP1IO8	FP1IO1	FP2IO22	VSS	FP2IO6	PWM2	PWM1	IOVDD	SPICS#	COREVDD	M
N	BE1#	BURST#	BDIP#	VSS	FP1IO21	COREVDD	FP1IO7	VSS	PIO2VDD	FP2IO17	FP2IO14	FP2IO8	WSIO	SDO	SCKIO	MCLKO	N
P	WAIT#	TEA#	FP1IO19	FP1IO14	FP1IO20	VSS	FP1IO4	FP1IO2	FP2IO24	FP2IO19	FP2IO15	FP2IO9	FP2IO7	FP2IO0	FP2IO2	FP2IO1	P
R	IRQ	RESET#	FP1IO17	FP1IO22	FP1IO13	FP1IO12	FP1IO5	FP1IO3	FP2IO25	FP2IO20	PIO2VDD	FP2IO12	VSS	FP2IO4	VP2IO3	PIO2VDD	R
T	VSS	FP1IO18	FP1IO11	PIO1VDD	FP1IO23	PIO1VDD	FP1IO6	PIO1VDD	FP2IO27	FP2IO23	FP2IO16	COREVDD	FP2IO11	PIO2VDD	FP2IO5	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

5.3 Pin Descriptions

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin

RESET# States

H	=	High level output
L	=	Low level output
Z	=	High Impedance (Hi-Z)
1	=	Pull-up resistor on input
0	=	Pull-down resistor on input
#	=	Active low level

Table 5-2: Cell Descriptions

Cell	Description
ILTR	Low voltage transparent input
OLTR	Low voltage transparent output
IC	LVCMOS input
ICS	LVCMOS schmitt input
ICD1T	LVCMOS input with pull-down resistor (50kΩ@3.3V) with Test Function
ICSU1T	LVCMOS schmitt input with pull-up resistor (50kΩ@3.3V) with Test Function
ICSU2T	LVCMOS schmitt input with pull-up resistor (100kΩ@3.3V) with Test Function
ICSD1T	LVCMOS schmitt input with pull-down resistor (50kΩ@3.3V) with Test Function
IOC2P1T	Low noise LVCMOS IO buffer (2mA/4mA@3.3V) with pull-up resistor (50kΩ@3.3V) with Test Function
IOC2P2T	Low noise LVCMOS IO buffer (2mA/4mA@3.3V) with pull-up resistor (100kΩ@3.3V) with Test Function
IOC2D1T	Low noise LVCMOS IO buffer (2mA/4mA@3.3V) with pull-down resistor (50kΩ@3.3V) with Test Function
IOC2D2T	Low noise LVCMOS IO buffer (2mA/4mA@3.3V) with pull-down resistor (100kΩ@3.3V) with Test Function
IOCS2D1T	Low noise LVCMOS schmitt IO buffer (2mA/4mA@3.3V) with pull-down resistor (50kΩ@3.3V) with Test Function
OLT2T	Low noise 3-state Output buffer (2mA/4mA@3.3V) with Test Function
OLT3	Low noise 3-state Output buffer (8mA@ 3.3V)
OLT3T	Low noise 3-state Output buffer (8mA@ 3.3V) with Test Function
P	Power

5.3.1 Host Interface

Many of the host interface pins have different functions depending on the host bus interface that is selected. For a summary of the possible host bus interface configurations and associated pin mapping details, see Section 5.4, “Configuration Pins” on page 32 and Section 5.5, “Host Interface Pin Mapping” on page 34. To determine the RESET# state for each pin, refer to Section 11.1, “Hard Reset State” on page 433.

Table 5-3: Host Interface Pin Descriptions

Pin Name	Type	QFP Pin#	PBGA Pin#	Cell	Power	Description
AB[20:19]	IO	4, 5	C1, D4	IOCS2D1T	HIOVDD	These input/output pins are the host address bus pins 20-19. For a summary of which pins are used for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
AB18	I	6	D3	ICSD1T	HIOVDD	This input pin is the host address pin 18. For a summary of which pins are used for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
AB[17:8]	IO	7, 8, 9, 10, 11, 12, 13, 17, 18, 19	E5, D2, D1, E4, E3, F6, F5, F3, G7, G6	IOCS2D1T	HIOVDD	These input/output pins are the host address bus pins 17-6. For a summary of which pins are used for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
AB7	IO	20	F2	IOCS2D1T	HIOVDD	This input/output pin is the host address bus pin 7. For a summary of which pins are used for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
AB6	IO	21	F1	IOCS2D1T	HIOVDD	This input/output pin is the host address bus pin 6. For a summary of which pins are used for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
AB[5:0]	I	22-27	G5, G4, G3, G2, H7, H6	ICSD1T	HIOVDD	These input pins are the host address bus pins 5-0. For a summary of which pins are used for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
DB[15:10]	IO	30, 31, 32, 33, 34, 35, 36	H2, H4, H3, H1, J7, J6	IOC2D1T	HIOVDD	These input/output pins are the host data bus pins 15-10. For a summary of which pins are used for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
DB9	IO	36	J3	IOC2D1T	HIOVDD	This input/output pin is the host data bus pin 9. For a summary of which pins are used for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
DB[8:0]	IO	37, 41, 42, 43, 44, 45, 46, 47, 48	J2, J5, K5, K4, K3, K1, K2, K6, L1	IOC2D1T	HIOVDD	These input/output pins are the host data bus pins 8-0. For a summary of which pins are used for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
CS#	I	52	L3	ICD1T	HIOVDD	This input pin is Chip Select.
M/R#	IO	53	M1	IOCS2D1T	HIOVDD	This input/output pin has multiple functions. For a summary of the pin functions for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.

Table 5-3: Host Interface Pin Descriptions

Pin Name	Type	QFP Pin#	PBGA Pin#	Cell	Power	Description
RD#	I	54	M2	ICD1T	HIOVDD	This input pin has multiple functions. For a summary of the pin functions for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
RD/WR#	I	55	M3	ICD1T	HIOVDD	This input pin has multiple functions. For a summary of the pin functions for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
BE0#	I	56	M4	ICD1T	HIOVDD	This input pin has multiple functions. For a summary of the pin functions for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
BE1#	IO	57	N1	IOC2D1T	HIOVDD	This input/output pin has multiple functions. For the Intel 80 Type 2 Indirect 8-bit Host Interface, this pin must be connected to HIOVDD. For a summary of the pin functions for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
BS#	IO	58	M5	IOC2P2T	HIOVDD	This input/output pin has multiple functions. For a summary of the pin functions for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
BURST#	I	59	N2	IC	HIOVDD	This input pin is Burst Transfer for the MPC555 and TI TMS470 Host interfaces and is used for burst support. For all other host bus interfaces, it is used in combination with the CNF[2:1] pins for selecting the host bus interface. For a summary of all possible host bus interfaces, see Section 5.4, “Configuration Pins” on page 32.
BDIP#	I	60	N3	IC	HIOVDD	This input pin is used for the MPC555 and TI TMS470 Host interfaces and indicates a burst transfer is in progress. For all other host bus interfaces, it is used in combination with the CNF[2:1] pins for selecting the host bus interface. For a summary of all possible host bus interfaces, see Section 5.4, “Configuration Pins” on page 32.

Table 5-3: Host Interface Pin Descriptions

Pin Name	Type	QFP Pin#	PBGA Pin#	Cell	Power	Description
TEA#	IO	61	P2	IOC2D1T	HIOVDD	This input/output pin is Transfer Error Acknowledge and is used for burst support for the MPC555 and TI TMS470 Host interfaces. This signal indicates that a bus error occurred in the current transaction. The MCU asserts this signal when the bus monitor does not detect a bus cycle termination within a reasonable amount of time. The assertion of TEA# causes the termination of the current bus cycle, regardless of the state of TEA#. An external pull-up device is required to negate TEA# quickly, before a second error is detected. That is, the pin must be pulled up within one clock cycle of the time it was tri-stated by the MPC555 / TI TMS470. For all other host bus interfaces, it is used in combination with the CNF[2:1] pins for selecting the host bus interface. For a summary of all possible host bus interfaces, see Section 5.4, “Configuration Pins” on page 32.
WAIT#	IO	62	P1	IOC2P2T	HIOVDD	During a data transfer, this output pin is driven active to force the system to insert wait states. It is driven inactive to indicate the completion of a data transfer. WAIT# is released to a high impedance state after the data transfer is complete. For a summary of the pin functions for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
BUSCLK	I	39	J1	ICD1T	HIOVDD	This input clock is typically used for an external clock source for the Host CPU bus interface. For a summary of the pin functions for each host bus interface configuration, see Section 5.5, “Host Interface Pin Mapping” on page 34.
IRQ	O	63	R1	OLT2T	HIOVDD	This output pin is the IRQ output from the S1D13515/S2D13515.