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S1D13709
Embedded Memory Graphics LCD Controller

Hardware Functional Specification

Document Number: XA8A-A-001-01

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NOTICE

Table of Contents

1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13709. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This document is updated as appropriate. Please check the Epson Electronics America Website at **vdc.epson.com** for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@eea.epson.com.

1.2 Overview Description

The S1D13709 is the LCD controller compatible with the S1D13700. It supports TFT LCD interface in addition to the S1D13700 function. The S1D13709 has flexible up-scaler and it can use WVGA TFT LCD with this function.

The S1D13709 can display both text and graphics on an LCD panel. The S1D13709 allows layered text and graphics, scrolling of the display in any direction, and partitioning of the display into multiple screens. It includes 32K bytes of embedded SRAM display memory which is used to store text, character codes, and bit-mapped graphics. The S1D13709 handles display controller functions including: transferring data from the controlling micro-processor to the buffer memory, reading memory data, converting data to display pixels, and generating timing signals for the LCD panel.

The S1D13709 is designed with an internal character generator which supports 160, 5x7 pixel characters in internal mask ROM (CGROM) and 64, 8x8 pixel characters in character generator RAM (CGRAM). When the CGROM is not used, up to 256, 8x16 pixel characters are supported in CGRAM.

2 Features

2.1 Internal Memory

- Embedded 32K bytes of SRAM display memory

2.2 Host CPU Interface

- Direct Address Bus support for:
  - Generic Bus (Z80 family) microprocessor interface
  - MC68K family microprocessor interface
- Indirect Address Bus support for:
  - Generic Bus (Z80 family) microprocessor interface
  - MC68K family microprocessor interface
  - M6800 family microprocessor interface
- 8-bit CPU data bus interface

2.3 Display Support

- STN-LCD
  - 4-bit monochrome LCD interface
  - Maximum resolutions supported:
    640x240 at 1 bpp
    320x240 at 2 bpp
    240x160 at 4 bpp
  - 1/2-duty to 1/256-duty LCD drive
- TFT-LCD
  - 4-bit monochrome LCD interface
  - 6-bit color palette LCD interface
  - Maximum resolutions supported:
    800x480
  - Up-scaler adjusts output image size for various LCD's

2.4 Display Modes

- 1/2/4 bit-per-pixel color depth support
- Text, graphics and combined text/graphics display modes
- Three overlapping screens in graphics mode
- Programmable cursor control
- Smooth horizontal scrolling of all or part of the display in monochrome mode
- Smooth vertical scrolling of all or part of the display in all modes
- Color Palette mode for the TFT interface

2.5 Character Generation

- 160, 5x7 pixel characters in embedded mask-programmed character generator ROM (CGROM)
- Up to 64, 8x8 pixel characters in character generator RAM (CGRAM)
- Up to 256, 8x16 pixel characters in embedded character generator RAM (when CGROM is not used)

2.6 Power

- Software initiated power save mode
- Low power consumption
- CORE V_{DD} 3.0 to 5.5 volts
- PLL V_{DD} 3.0 to 5.5 volts
- IO V_{DD} 3.0 to 5.5 volts

2.7 Clock Source

- Two terminal crystal or Single Oscillator input
  Input Clock (maximum 66 MHz)
  STN-Clock (XSCL) (maximum 15 MHz)
  TFT-Clock (FPSHIFT) (maximum 35MHz)

2.8 Package

- TQFP14 - 80-pin Pb-free package (lead free)

3 System Diagrams

3.1 Host Interface Connections

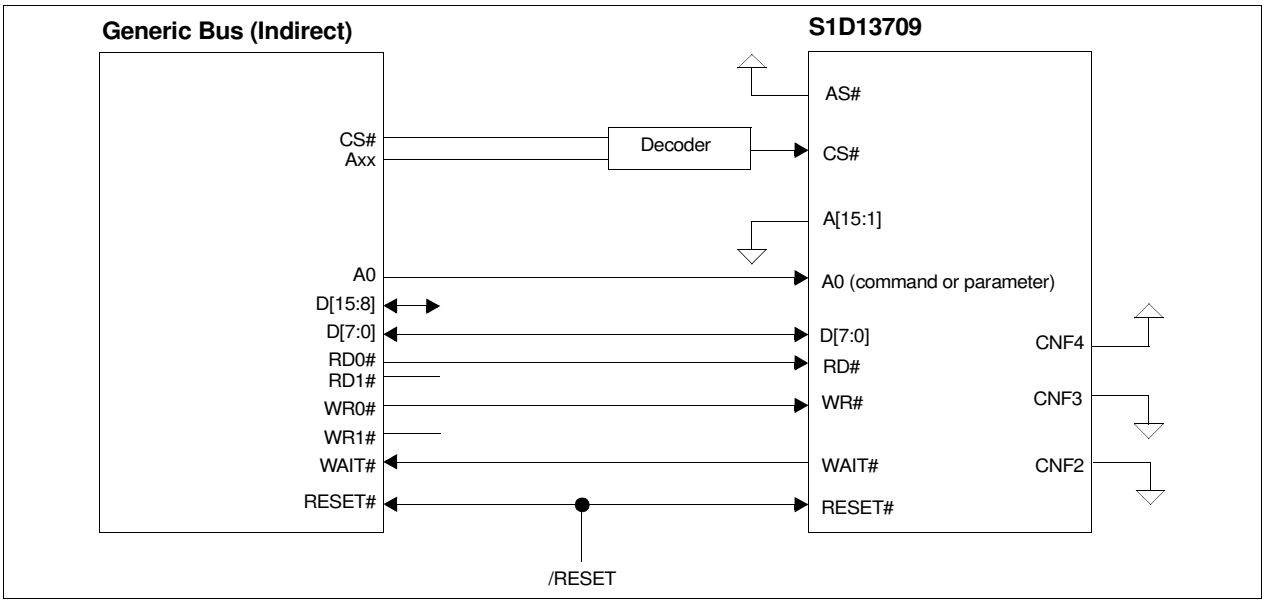

Figure 3-1 Indirect Generic to S1D13709 Interface Example

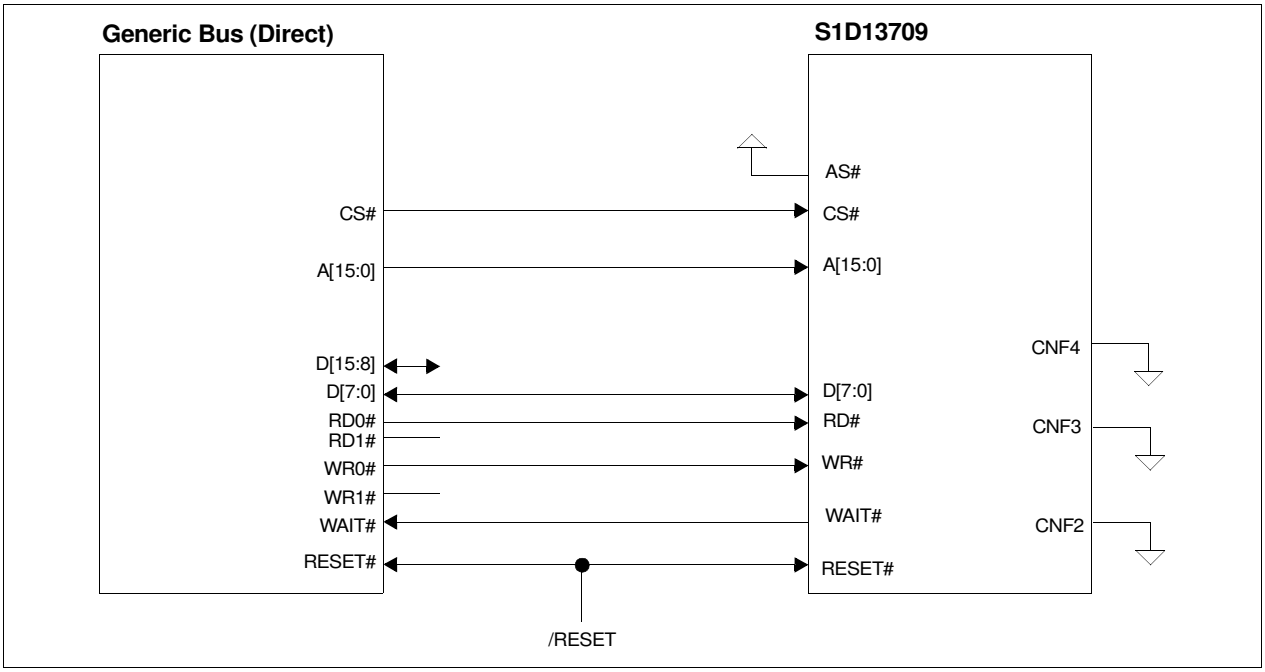

Figure 3-2 Direct Generic to S1D13709 Interface Example

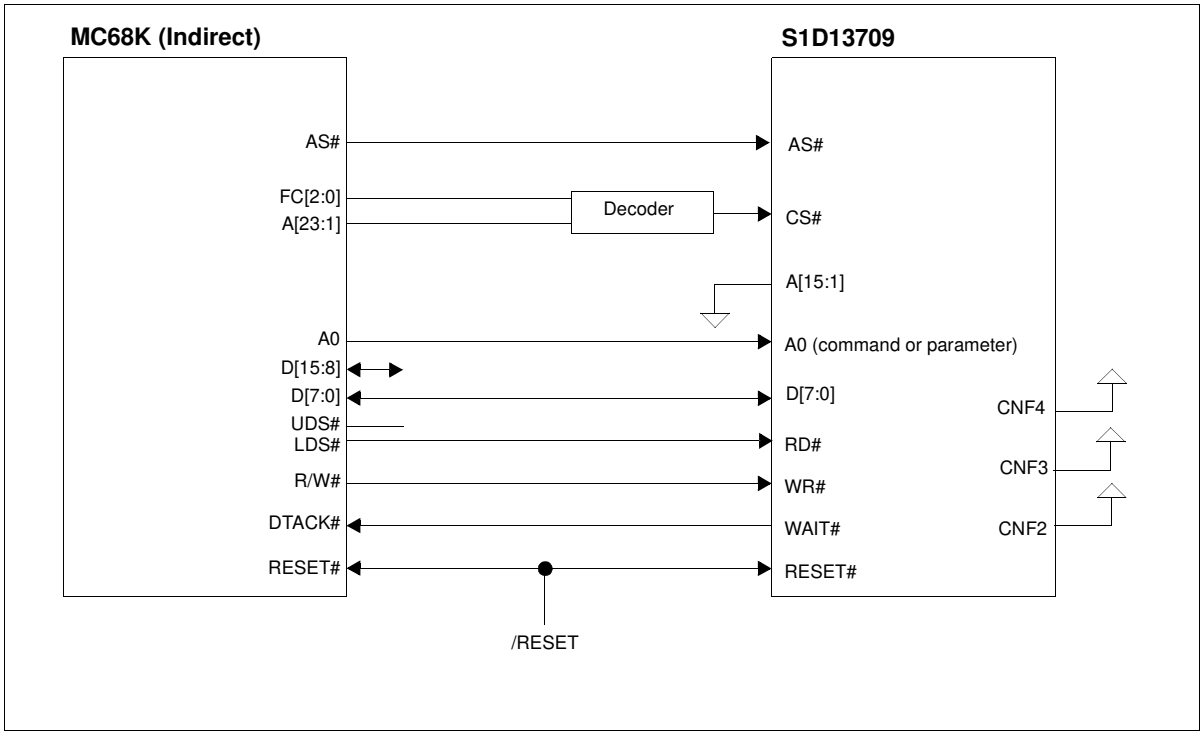

Figure 3-3 Indirect MC68K to S1D13709 Interface Example

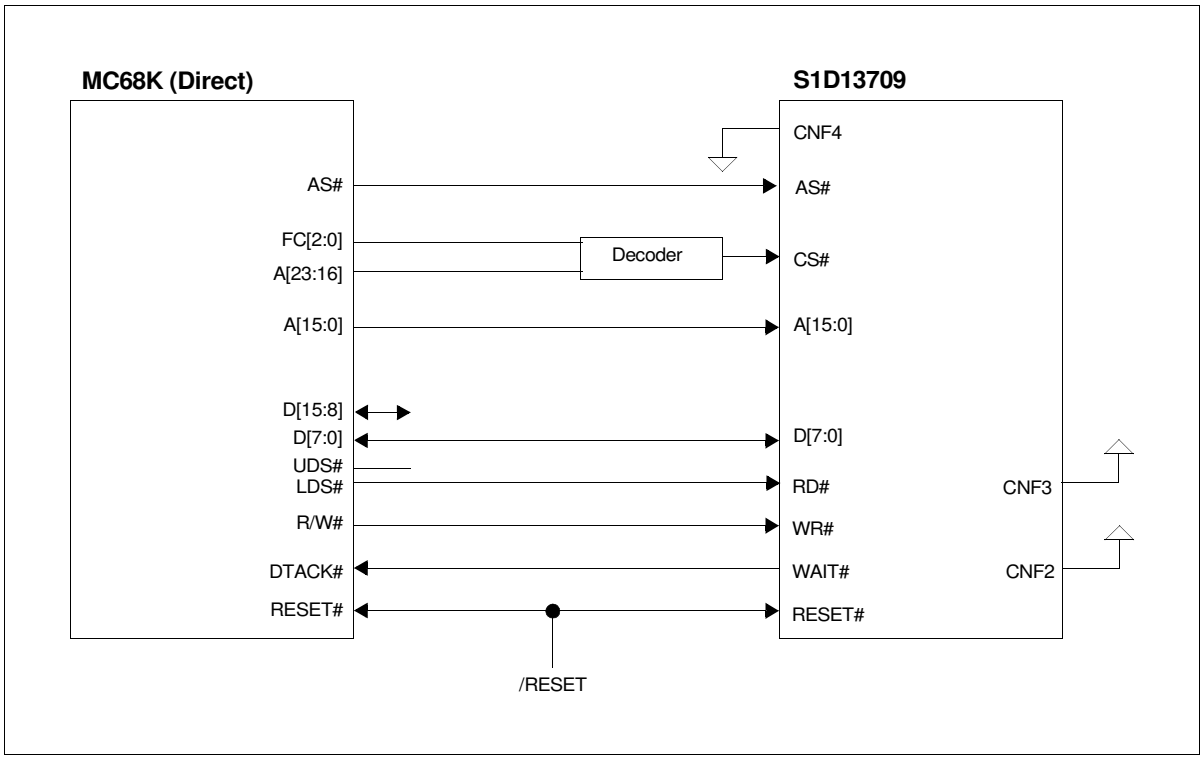

Figure 3-4 Direct MC68K to S1D13709 Interface Example

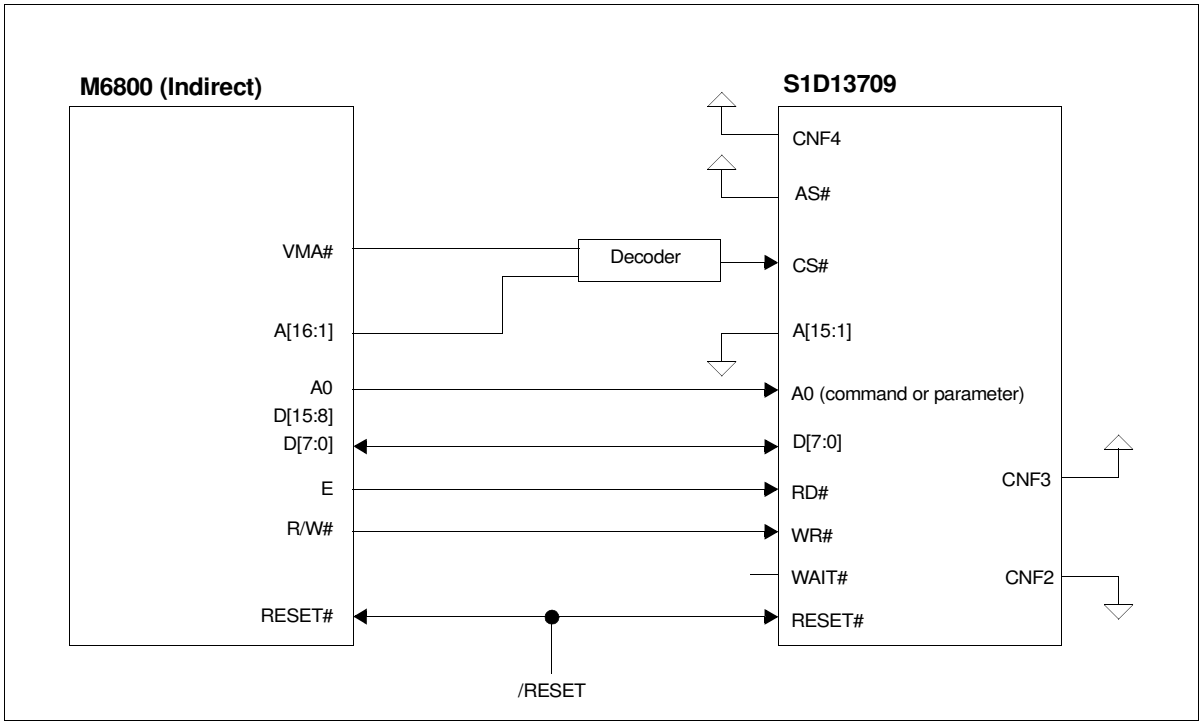

Figure 3-5 Indirect M6800 to S1D13709 Interface Example

3.2 LCD Interface Connections

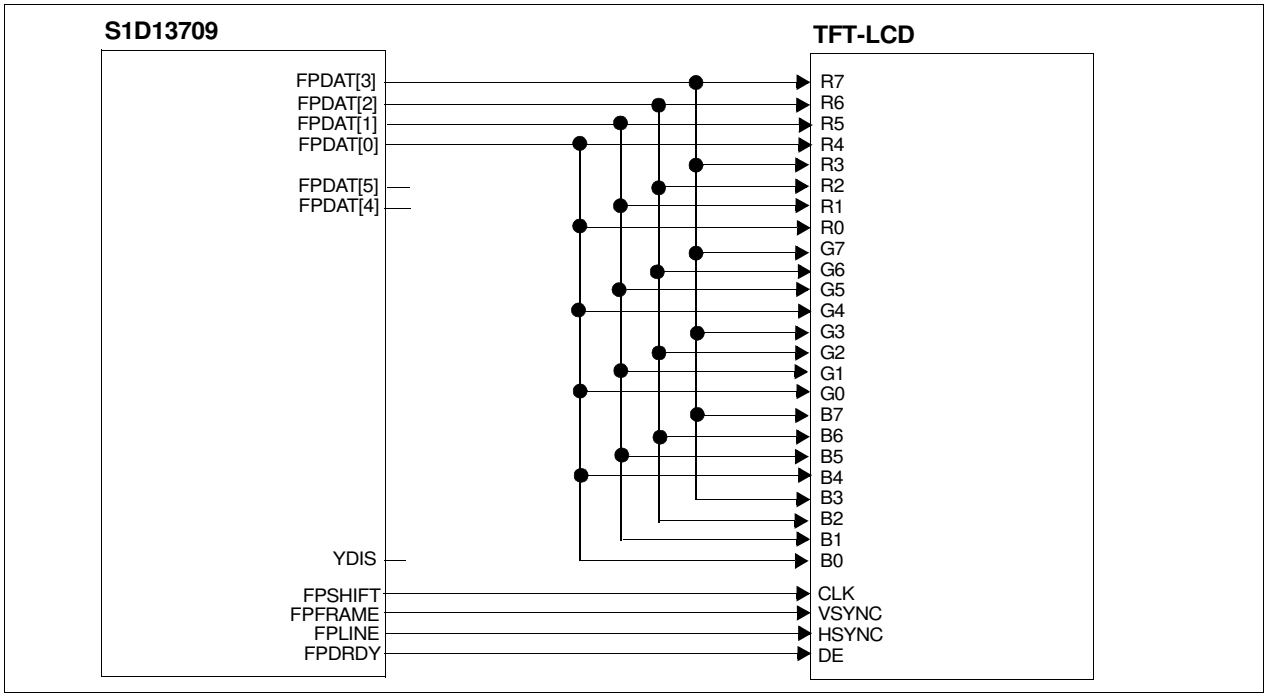

Figure 3-6 S1D13709 to TFT-LCD Example (Gray Scale Mode, REG[34h]bit1 = 0)

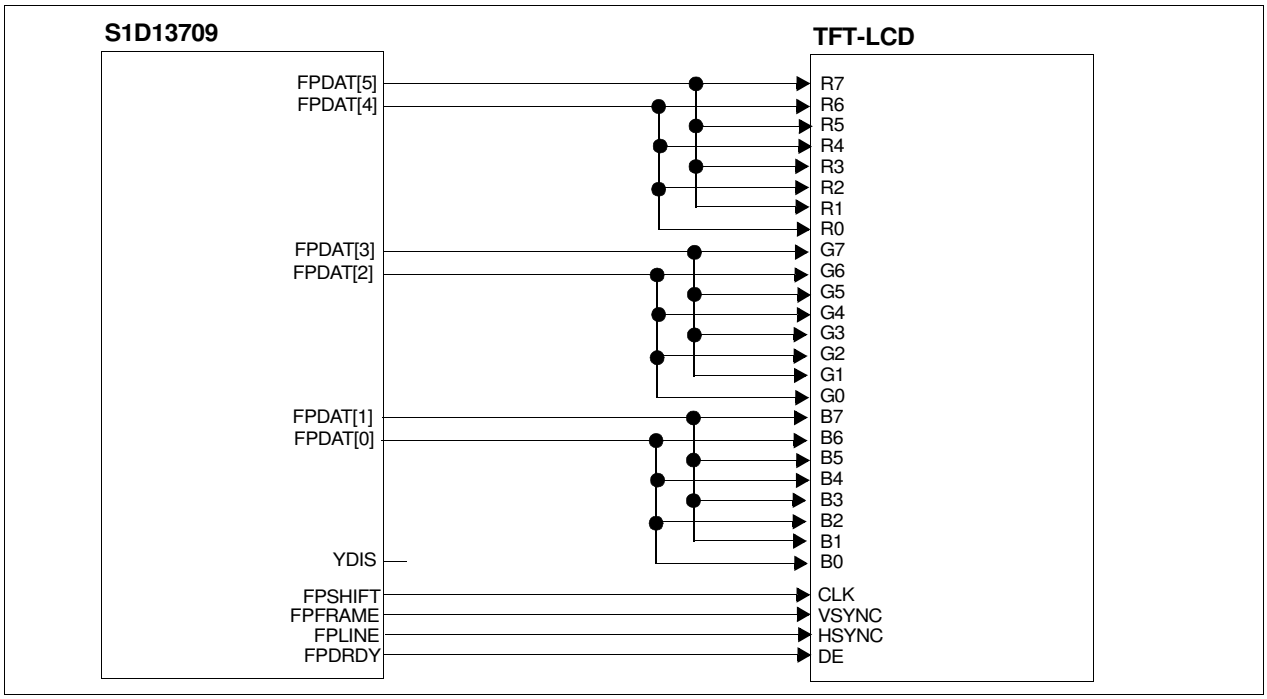

Figure 3-7 S1D13709 to TFT-LCD Example (Color Palette Mode, REG[34h]bit1 = 1)

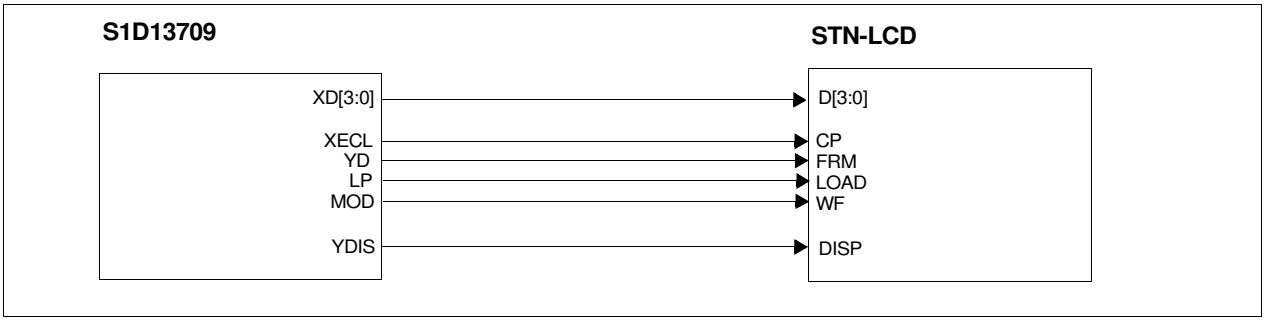

Figure 3-8 S1D13709 to STN-LCD Example

4 Functional Block Diagram

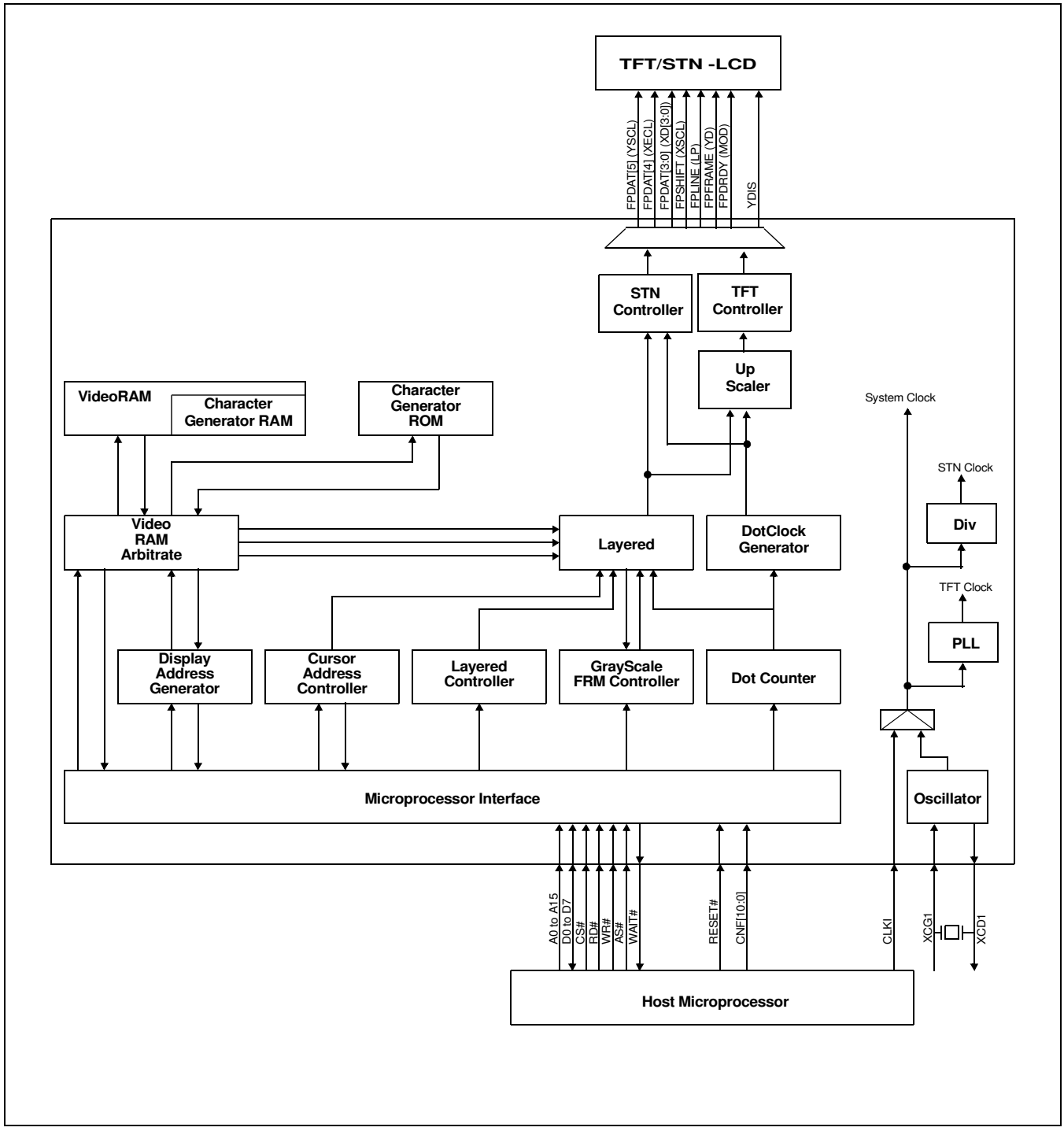

Figure 4-1 Functional Block Diagram

5 Pins

5.1 Pinout Diagram

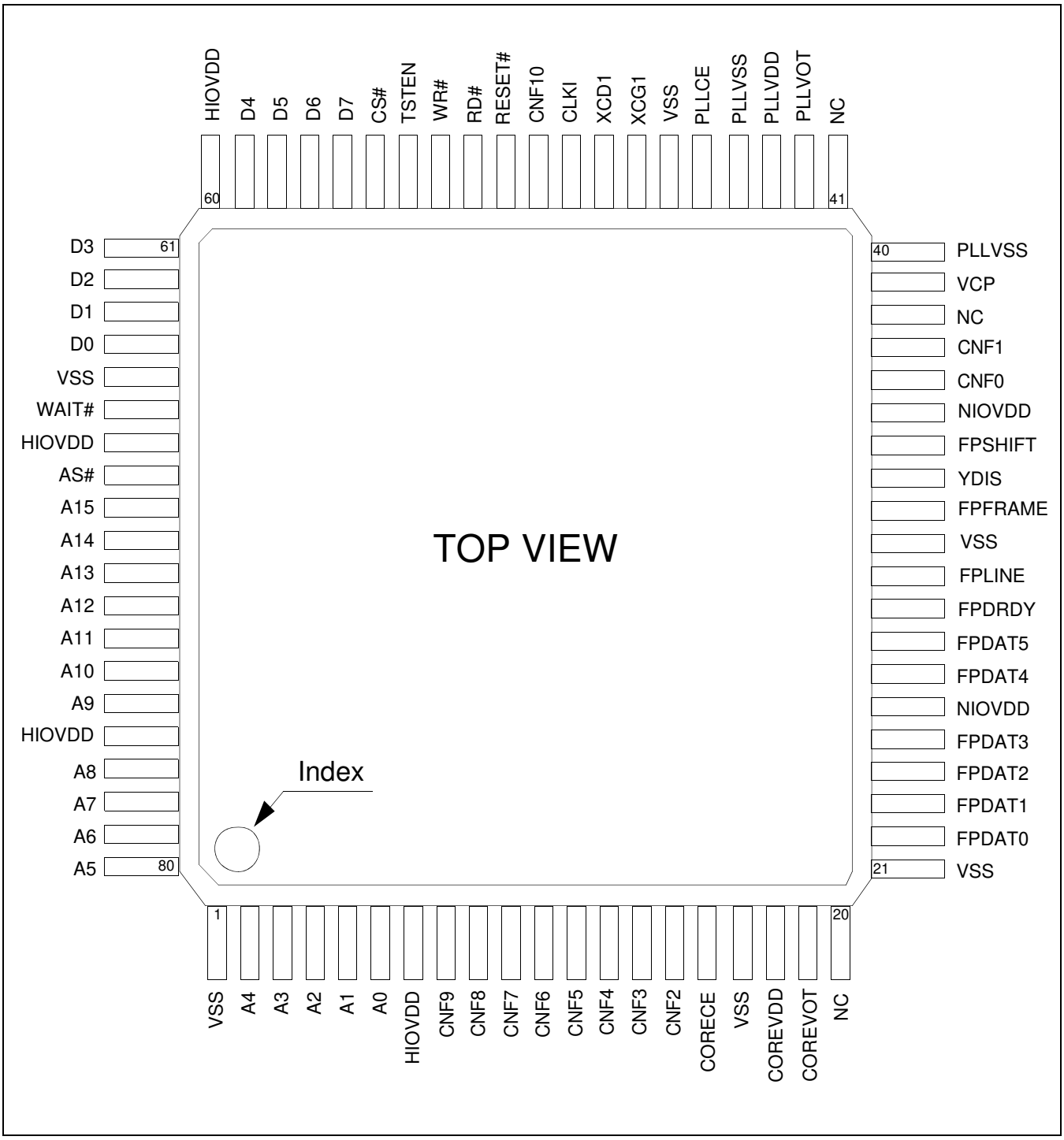

Figure 5-1 Pinout Diagram (TQFP14 - 80 pin)

5.2 Pin Descriptions

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin

RESET# and Power On States

Z	=	High Impedance (Hi-Z)
L	=	Low level output
H	=	High level output
0	=	Pull-down control on input
1	=	Pull-up control on input
X	=	Undetermined
—	=	Not applicable

Table 5-1: Cell Descriptions

Item	Description
CI	CMOS input
SI	CMOS Schmitt input
OBSEL	CMOS output buffer with Drive Selector (2mA or 6mA@3.3V, 3mA or 8mA@5V)
IOB	CMOS Input/Output buffer (6mA@3.3V, 8mA@5V)
TOB	Tri-state output buffer (6mA@3.3V, 8mA@5V)
LIN	Transparent input
LOT	Transparent output

5.2.1 Host Interface

Many of the host interface pins have different functions depending on the selection of the host bus interface (see configuration of CNF[4:2] pins in Table 5-7: "Summary of Configuration Options 1," on page 26). For a summary of host interface pins, see Table 5-10: "Host Interface Pin Mapping," on page 28.

Table 5-2 Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
A15	I	69	CI	HIOVDD	—	System Address pins 15-1. • For Direct addressing mode, these pins are used for the system address bits 15-1. • For Indirect addressing mode, these pins must be connected to ground (VSS).
A14	I	70	CI	HIOVDD	—	
A13	I	71	CI	HIOVDD	—	
A12	I	72	CI	HIOVDD	—	
A11	I	73	CI	HIOVDD	—	
A10	I	74	CI	HIOVDD	—	
A9	I	75	CI	HIOVDD	—	
A8	I	77	CI	HIOVDD	—	
A7	I	78	CI	HIOVDD	—	
A6	I	79	CI	HIOVDD	—	
A5	I	80	CI	HIOVDD	—	
A4	I	2	CI	HIOVDD	—	
A3	I	3	CI	HIOVDD	—	
A2	I	4	CI	HIOVDD	—	
A1	I	5	CI	HIOVDD	—	
A0	I	6	CI	HIOVDD	—	System Address pin 0. • For Direct addressing mode, this pin is used for system address bit 0. • For Indirect addressing mode, this pin in conjunction with RD# and WR# determines the type of data present on the data bus.
D7	IO	56	IOB	HIOVDD	Z	System data bus pins 7-0. These tristate input/output data pins must be connected to the microprocessor data bus.
D6	IO	57	IOB	HIOVDD	Z	
D5	IO	58	IOB	HIOVDD	Z	
D4	IO	59	IOB	HIOVDD	Z	
D3	IO	61	IOB	HIOVDD	Z	
D2	IO	62	IOB	HIOVDD	Z	
D1	IO	63	IOB	HIOVDD	Z	
D0	IO	64	IOB	HIOVDD	Z	

Table 5-2 Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
CNF10	I	50	SI	HIOVDD	—	These input pins select the TFT-LCD Automatic Setting Mode and must be connected to either HIOVDD or VSS. For further information, see Section 5.3, “Summary of Configuration Options” on page 26.
CNF9	I	8	SI	HIOVDD	—	
CNF8	I	9	SI	HIOVDD	—	
CNF7	I	10	SI	HIOVDD	—	
CNF6	I	11	SI	HIOVDD	—	
CNF5	I	12	SI	HIOVDD	—	
CNF4	I	13	SI	HIOVDD	—	This input pin selects the microprocessor addressing mode and must be connected to either HIOVDD or VSS. The S1D13709 supports both Direct and Indirect addressing modes. For further information, see Section 5.3, “Summary of Configuration Options” on page 26.
CNF3	I	14	SI	HIOVDD	—	These input pins select the host bus interface (microprocessor interface) and must be connected to either HIOVDD or VSS. The S1D13709 supports Generic processors (such as the 8085 and Z80®), the MC68K family of processors (such as the 68000) and the M6800 family of processors (such as the 6800). For further information, see Section 5.3, “Summary of Configuration Options” on page 26.
CNF2	I	15	SI	HIOVDD	—	
CNF1	I	37	SI	NIOVDD	—	These input pins are used for configuration of the XSCL clock cycle time and must be connected to either NIOVDD or VSS. For further information, see Section 5.3, “Summary of Configuration Options” on page 26.
CNF0	I	36	SI	NIOVDD		
RD#	I	52	SI	HIOVDD	—	This input pin has multiple functions. • When the Generic host bus interface is selected, this pin is the active-LOW read strobe (RD#). The S1D13709 data output buffers are enabled when this signal is low. • When the M6800 host bus interface is selected, this pin is the active-high enable clock (E). Data is read from or written to the S1D13709 when this clock goes high. • When the MC68K host bus interface is selected, this pin is the active-low lower data strobe (LDS#). Data is read from or written to the S1D13709 when this signal goes low.
WR#	I	53	SI	HIOVDD	—	This input pin has multiple functions. • When the Generic host bus interface is selected, this signal is the active-low write strobe (WR#). The bus data is latched on the rising edge of this signal. • When the M6800 host bus interface is selected, this signal is the read/write control signal (R/W#). Data is read from the S1D13709 if this signal is high, and written to the S1D13709 if it is low. • When the MC68K host bus interface is selected, this signal is the read/write control signal (RD/WR#). Data is read from the S1D13709 if this signal is high, and written to the S1D13709 if it is low.

Table 5-2 Host Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
CS#	I	55	SI	HIOVDD	—	Chip select. This active-low input enables the S1D13709. It is usually connected to the output of an address decoder device that maps the S1D13709 into the memory space of the controlling microprocessor.
WAIT#	O	66	TOB	HIOVDD	Z	This output pin has multiple functions. • When the Generic host bus interface is selected, this pin is WAIT#. During a data transfer, WAIT# is driven active-low to force the system to insert wait states. It is driven inactive to indicate the completion of a data transfer. WAIT# is released to a high impedance state after the data transfer is complete. For indirect addressing mode, the WAIT# pin can be used to handshake with the Host. • When the MC68K host bus interface is selected, this pin is DTACK#. During a data transfer, DTACK# is driven active-high to force the system to insert wait states. It is driven inactive to indicate the completion of a data transfer. DTACK# is released to a high impedance state after the data transfer is complete. For indirect addressing mode, the DTACK# pin can be used to handshake with the Host. • When the M6800 host bus interface is selected, this pin must be left unconnected and floating.
AS#	I	68	CI	HIOVDD	—	This input pin has multiple functions. • When the Generic host bus interface is selected, this pin must be connected to VDD (pulled high). • When the MC68K host bus interface is selected, this pin is the address strobe (AS#). • When the M6800 host bus interface is selected, this pin must be connected to VDD (pulled high).
RESET#	I	51	SI	HIOVDD	—	This active-low input performs a hardware reset of the S1D13709 which sets all internal registers to their default states and forces all signals to their inactive states. Note: Do not trigger a RESET# when the supply voltage is lowered.

5.2.2 LCD Interface

In order to provide effective low-power drive for LCD matrixes, the S1D13709 can directly control both the X and Y-drivers using an enable chain.

Table 5-3 LCD Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
FPDAT5 (YSCL)	O	28	OBSEL	NIOVDD	L	When the TFT interface is selected (REG[34h] bit 0 =1), this pin is TFT data output. (FPDAT5) When the STN interface is selected (REG[34h] bit 0 =0), this pin is STN control signal output (YSCL). The falling edge of YSCL latches the data on YD into the input shift registers of the Y-drivers. YSCL is not used with driver ICs which use LP as the Y-driver shift clock.
FPDAT4 (XECL)	O	27	OBSEL	NIOVDD	L	When the TFT interface is selected (REG[34h] bit 0 =1), this pin is TFT data output. (FPDAT4) When the STN interface is selected (REG[34h] bit 0 =0), this pin is STN control signal output (XECL). The falling edge of XECL triggers the enable chain cascade for the X-drivers. Every 16th clock pulse is output to the next X-driver.
FPDAT3 (XD3)	O	25	OBSEL	NIOVDD	L	When the TFT interface is selected (REG[34h] bit 0 =1), this pin is TFT data output. (FPDAT[3:0]) When the STN interface is selected (REG[34h] bit 0 =0), this pin is STN data output (XD[3:0]). XD[3:0] are the 4-bit X-driver (column drive) data outputs and must be connected to the inputs of the X-driver chips.
FPDAT2 (XD2)	O	24	OBSEL	NIOVDD	L	
FPDAT1 (XD1)	O	23	OBSEL	NIOVDD	L	
FPDAT0 (XD0)	O	22	OBSEL	NIOVDD	L	
FPDRDY (MOD)	O	29	OBSEL	NIOVDD	L	When the TFT interface is selected (REG[34h] bit 0 =1), this pin is TFT data enable output. (FPDRDY) When the STN interface is selected (REG[34h] bit 0 =0), this pin is STN control signal output (MOD). MOD is the LCD panel backplane bias signal. The MOD period is selected using the SYSTEM SET command.

Table 5-3 LCD Interface Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
FPLINE (LP)	O	30	OBSEL	NIOVDD	L	When the TFT interface is selected (REG[34h] bit 0 =1), this pin is TFT HSYNC output. (FPLINE) When the STN interface is selected (REG[34h] bit 0 =0), this pin is STN control signal output (LP). LP latches the signal in the X-driver shift registers into the output data latches. LP is a falling edge triggered signal, and pulses once every display line. LP must be connected to the Y-driver shift clock on LCD modules.
FPFRAME (YD)	O	32	OBSEL	NIOVDD	L	When the TFT interface is selected (REG[34h] bit 0 =1), this pin is TFT VSYNC output. (FPFRAME) When the STN interface is selected (REG[34h] bit 0 =0), this pin is STN control signal output (YD). YD is the data pulse output for the Y drivers. It is active during the last line of each frame, and is shifted through the Y drivers one by one (by YSCL), to scan the display's common connections.
FPSHIFT (XSCL)	O	34	OBSEL	NIOVDD	L	When the TFT interface is selected (REG[34h] bit 0 =1), this pin is TFT clock output. (FPSHIFT) When the STN interface is selected (REG[34h] bit 0 =0), this pin is STN clock output (XSCL). The falling edge of XSCL latches the data on FPDAT[3:0] into the input shift registers of the X-drivers. As XSCL is generated to synchronize with XECL, the total output of the XSCL clock for one line is a multiple of 16. To conserve power, this clock is stopped between LP and the start of the following display line.
YDIS	O	33	OBSEL	NIOVDD	L	This pin is used for the STN interface only (REG[34h] bit 0 =0). This output pin is the power-down output signal. YDIS is high while the display drive outputs are active. YDIS goes low one or two frames after the power save command is written to the S1D13709. All Y-driver outputs are forced to an intermediate level (de-selecting the display segments) to blank the display. In order to implement power-down operation in the LCD unit, the LCD power drive supplies must also be disabled when the display is disabled by YDIS. When the TFT interface is selected (REG[34h] bit 0 =1), this pin must be left unconnected.

5.2.3 Clock Input

Table 5-4 Clock Input Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
XCG1	I	47	LIN	HIOVDD	—	This input pin is the crystal connection for use with the internal oscillator. This pin must be pulled down when using an external clock source (CLKI). For further information on the use of the internal oscillator, see Section 9.3, “Oscillator Circuit” on page 62.
XCD1	O	48	LOT	HIOVDD	—	This output pin is the crystal connection for use with the internal oscillator. This pin must be left unconnected when using an external clock source (CLKI). For further information on the use of the internal oscillator, see Section 9.3, “Oscillator Circuit” on page 62.
CLKI	I	49	SI	HIOVDD	—	This is the external clock input. This pin must be pulled down when using a crystal with the internal oscillator. For further information on clocks, see Section 9, “Clocks” on page 61.

5.2.4 Miscellaneous

Table 5-5 Miscellaneous Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
TSTEN	I	54	CI	HIOVDD	—	This pin is used for production test only and must be connected to ground (VSS).
COREVOT	O	19	LOT	COREVDD	—	This pin is used for production test only and must be connected to VSS via a 1uF capacitor.
CORECE	I	16	LIN	COREVDD	—	This pin is used for production test only and must be connected to COREVDD.
PLLVOT	O	42	LOT	PLLVDD	—	This pin is used for production test only and must be connected to PLLVSS via a 1uF capacitor.
PLLCE	I	45	LIN	PLLVDD	—	This pin is used for production test only and must be connected to PLLVDD.
VCP	O	39	LOT	PLLVDD	—	This pin is used for production test only and must be left unconnected.

5.2.5 Power And Ground

Table 5-6 Power And Ground Pin Descriptions

Pin Name	Type	Pin #	Cell	Power	RESET#/ Power On State	Description
HIOVDD	P	7,67,76	P	—	—	IO power supply for the Host (MPU) interface, 3.3/5.0 volts. A 0.1uF bypass capacitor is necessary between each HIOVDD and VSS.
NIOVDD	P	26,35	P	—	—	IO power supply for the LCD interface, 3.3/5.0 volts. A 0.1uF bypass capacitor is necessary between each NIOVDD and VSS.
COREVDD	P	18	P	—	—	Core power supply, 3.3/5.0 volts. A 1uF bypass capacitor is necessary between COREVDD and VSS.
PLLVDD	P	43	P	—	—	PLL power supply, 3.3/5.0 volts. A 1uF bypass capacitor is necessary between PLLVDD and PLLVSS.
VSS	P	1,17,21 ,31,46, 65	P	—	—	Ground for HIOVDD, NIOVDD and COREVDD
PLLVSS	P	40,44	P	—	—	Ground for PLLVDD

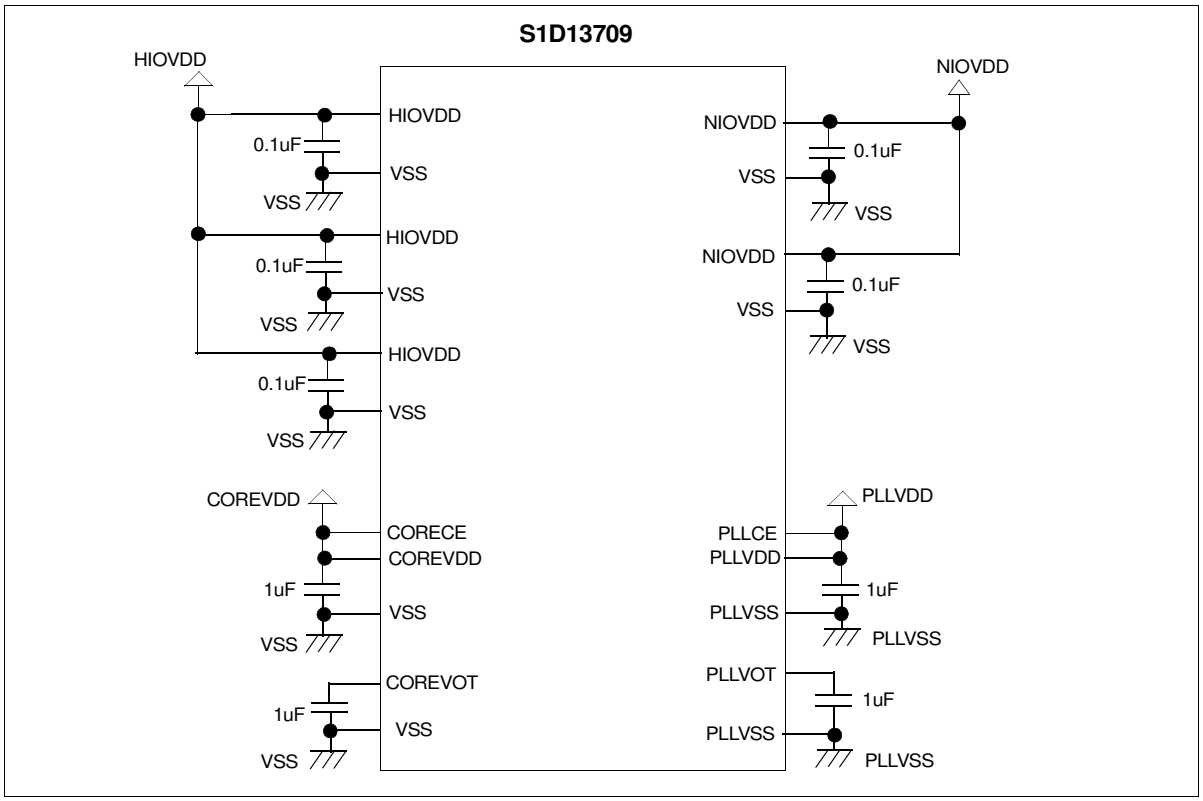

Figure 5-2 Power and Ground Connection