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S1D13715
Mobile Graphics Engine with Megapixel Support

Hardware Functional Specification

Document Number: X52A-A-001-07.4

SEIKO EPSON CORPORATION

Rev. 7.4

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Table of Contents

1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13715 Mobile Graphics Engine. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This document is updated as appropriate. Please check for the latest revision of this document before beginning any development. The latest revision can be downloaded at vdc.epson.com.

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1.2 General Description

The S1D13715 is an Mobile Graphics Engine solution designed with support for the digital video revolution in mobile products. The S1D13715 contains an integrated dual port camera interface, hardware JPEG encoder/decoder and can be interfaced to an external MPEG codec. Seamlessly connecting to both direct and indirect CPU interfaces, it provides support for up to two LCD panels. The Mobile Graphics Engine supports all standard TFT panel types and many extended TFT types, eliminating the need for an external timing control IC. The S1D13715, with it's 320K bytes of embedded SRAM and rich feature set, provides a low cost, low power, single chip solution to meet the demands of embedded markets requiring Digital Video, such as Mobile Communications devices and Palm-size PDAs.

Additionally, products requiring a rotated display can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory, transparent to the software application. The S1D13715 also provides support for "Picture-in-Picture Plus" (a variable size window with overlay functions). Higher performance is provided by the Hardware Acceleration Engine which provides 2D BitBLT functions.

The S1D13715 provides impressive support for cellular and other mobile solutions requiring Digital Video support. However, its impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

1.3 Internal Memory

The S1D13715 contains 320K bytes of internal SRAM memory. This internal memory is divided into three physical SRAM banks that contain independent arbitration logic. The boundaries between the memory banks are transparent to the user. Memory Bank1 is 64K bytes, Bank2 is 128K bytes, and Bank3 is 128K bytes.

The internal memory can be used in 5 main ways:

1. **Main Window Display Only**: 320K bytes available. If the JPEG functions and the PIP$^+$ window are not required (therefore disabled), the entire 320K bytes of memory is available for main window image storage. In this case, the image written to the main display window can either come from the Host (RGB data) over the host interface, and/or input by the camera (YUV or RGB data) through the camera interface. The Main Window Display Start Address registers (REG[0212h]-[0214h]) determines where the main window image is stored in memory. Additionally, if the main window image is being updated by a camera, the YUV/RGB Converter Write Start Address registers (REG[0242h]-[0244h]) determines where the camera data is written and typically equals the address of the Main Window Display Start Address.

2. **Main Window and PIP$^+$ Window Display Only**: 320K bytes available. If the JPEG functions are not required (therefore disabled), the entire 320K bytes of memory is available for image storage and must be shared between the Main Window Display Image and the PIP$^+$ Window Display Image. It is recommended that the Main Window and the PIP$^+$ Window be located in different memory banks for improved performance. Since the PIP$^+$ Window is typically smaller than the Main Window, it is recommended that the PIP$^+$ Window Display Image be set to Bank1 using the PIP$^+$ Display Start Address registers (REG[0218h]-[021Ah]), and the Main Window Display Image be set to Bank2 and/or Bank3 using the Main Window Display Start Address registers (REG[0212h]-[0214h]). As in option 1, the image data for either of these windows can come from the Host or from the camera. Typically, in this setup the camera will input image data to the PIP+ Window and the YUV/RGB Converter Write Start Address registers (REG[0242h]-[0244h]) will equal the PIP$^+$ Display Start Address.

3. **JPEG Functions Enabled**: 288K bytes - JPEG FIFO size available. If either the JPEG Encoder or Decoder is used, segments of Bank1 and Bank3 are automatically reserved for JPEG use only. The JPEG FIFO uses Bank1 and its size is configurable from 4K bytes to 64K bytes using the JPEG FIFO Size bits (REG[09A4h] bits 3-0). The JPEG FIFO starts at address 0 of Bank1 and is accessed using the JPEG FIFO Read/Write register (REG[09A6h]). The JPEG FIFO is used as an interface between the JPEG module and the HOST. When the S1D13715 is encoding a JPEG image, the JPEG FIFO stores JPEG data for the HOST to read. When the S1D13715 is decoding a JPEG file, the JPEG FIFO stores incoming JPEG data from the HOST. The size of the JPEG FIFO should be set to optimize performance based on the HOST operating speed, S1D13715 operating speed, and the size of the JPEG image. The JPEG Line Buffer uses the upper 32K bytes of Bank3, from 48000h - 4FFFFh. During an encode operation, the JPEG Line Buffer is used to organize incoming YUV data from the

camera and send it to the JPEG Encoder. During a decode operation, the JPEG Line Buffer organizes the YUV data output of the JPEG decoder to be sent to the View Resizer and YUV/RGB Converter for display on the LCD panel.

4. **YUV Data Output**: 288K bytes - JPEG FIFO size available. If YUV data from the camera is directly sent to the HOST, the JPEG Codec is bypassed, however the JPEG FIFO and JPEG Line Buffer are still utilized. The JPEG FIFO and JPEG Line Buffer are used as described for the decode operation in option 3 (JPEG Functions Enabled).

5. **YUV Data Input**: 288K bytes available. If YUV data from the Host is sent directly to the S1D13715, the JPEG Codec and JPEG FIFO are bypassed. YUV data is written directly to the JPEG Line Buffer. In this mode, the JPEG Line Buffer is accessed using the JPEG Line Buffer Write Port register (REG[09E0h]). The JPEG Line Buffer then sends the YUV data to the View Resizer and the YUV/RGB Converter for display on the LCD panel.

All data stored in the internal memory that is intended for display on the LCD panel, must be stored in RGB format. YUV data from the camera interface or from the HOST must be converted to RGB by the YUV/RGB Converter. Color depth data formats of 8/16/32 bit-per-pixel are supported.

1.4 Host CPU Interface

The S1D13715 supports four CPU Host interfaces with 16-bit wide data buses. Each interface can support little or big endian data formats, direct or indirect addressing, and the option to use a wait signal or not. See Section 5.4, “Summary of Configuration Options” on page 43 for a description on how to configure the S1D13715 for these various options. In addition to these four CPU Host interfaces, the S1D13715 also has a serial CPU port which allows the CPU Host to directly control a serial LCD panel connected to the S1D13715.

The Host CPU that is used to connect to the S1D13715 must meet all specified timing parameters for the Host interface being used, as shown in Section 7.3, “Host Interface Timing” on page 60.

It is recommended that the WAIT# signal be used for all host interfaces as this will ensure that the highest performance is achieved when accessing the S1D13715. When this mode is selected, the WAIT# signal is only asserted when needed (i.e. the S1D13715 cannot accept or present data immediately). If the WAIT# signal is not used, the CPU must guarantee that all cycles meet the maximum cycle length as shown in Table 7-46: “Wait Length,” on page 91.

1.4.1 Direct Addressing Host Interfaces

The direct addressing host interfaces (Direct 80 Type 1, Direct 80 Type 2, Direct 80 Type 3, and Direct 68) are generic asynchronous CPU interfaces that provide addressing along with the data in one transfer. These interfaces only differ in the signals used to interpret the read/write and byte enable command signals. Typically, these interfaces are used to connect to the external memory bus of the host CPU and offer the highest performance when accessing the S1D13715.

The direct addressing host interfaces also have the ability to combine the S1D13715 registers and internal memory into one contiguous memory segment or into separate memory segments. In the contiguous mode (1 CS# mode), only one chip select is used to select the S1D13715 on the host bus. Memory and register accesses are differentiated by the M/R# pin which is typically connected to address pin A19 of the host CPU bus. In the separate memory mode (2 CS# mode), two chip selects select the S1D13715. One chip select is used for memory accesses and the other is used for register accesses. In this mode, the host CPU can be programmed to assign different memory spaces for the memory and registers of the S1D13715.

1.4.2 Indirect Addressing Host Interfaces

The indirect addressing host interfaces (Indirect 80 Type 1, Indirect 80 Type 2, Indirect 80 Type 3, and Indirect 68) are generic asynchronous CPU interfaces that provide addressing and data in two separate transfers. These interfaces only differ in the signals used to interpret the read/write and byte enable command signals. Typically, these interfaces are used when the address and data lines of the host CPU are multiplexed together and two transfers are needed to complete a data transfer.

1.4.3 Serial Port Interface for Serial LCD Control

The S1D13715 also supports a Serial Host Interface that is used to directly control a serial LCD panel connected to the S1D13715. This bypass mode is controlled by the Serial Port Bypass Enable bit (REG[0032h] bit 8). Typically, this interface is used when the S1D13715 is in power save mode and a serial LCD panel is required to show an image such as a status display.

1.5 LCD Controller

The S1D13715 Mobile Graphics Engine contains a versatile LCD controller which supports many LCD panel types and offers a rich feature set. The S1D13715 has three LCD interface modes where either one or two LCD panels (referred to as LCD1 and LCD2) can be connected to the S1D13715. These modes are selected using the Panel Interface bits (REG[0032h] bits 1-0). LCD1 and LCD2 each have their own vertical and horizontal LCD panel size setting and other specific features, in order to easily switch from the LCD1 panel display to the LCD2 panel display or vice versa.

In Mode 1, LCD1 is defined as a TFT RGB type LCD panel. The various TFT LCD panel types supported are listed in Table 10-12: "RGB Panel Type Selection," on page 151 and are selected using the RGB Panel Type bits (REG[0032h] bits 15-10). LCD2 is defined as a serial interface type LCD panel with integrated RAM to store the image data.

In Mode 2, LCD1 is defined as a parallel interface LCD panel with integrated RAM to store the image data. LCD2 is defined as a serial interface type LCD panel with integrated RAM to store the image data.

In Mode 3, LCD1 and LCD2 are both defined as parallel interface LCD panels with integrated RAM to store the image data.

In Mode 4, LCD1 is defined as a TFT RGB type LCD panel. The various LCD panel types supported are listed in Table 10-12: "RGB Panel Type Selection," on page 151 and are selected using the RGB Panel Type bits (REG[0032h] bits 15-10). LCD2 is defined as a parallel interface LCD panel with integrated RAM to store the image data.

In each mode, only one display (LCD1 or LCD2) at a time can be the active display. A typical application for using two separate LCD panels would be a clamshell type cellular phone where there is a main display and a smaller status display on the outside of the phone. LCD1 would be the main display and LCD2 would be the small status display, typically a serial interface LCD panel. Two images would be stored in the internal memory of the S1D13715 for each LCD display. When each display is selected as active, (LCD1 when the cellular phone is open and LCD2 when the cellular phone is closed) the correct image to be displayed is selected using the Main Window Display Start Address registers (REG[0210h]-[0212h]).

For LCD Interface Pin Mapping refer to Table 5-12: "LCD Interface Pin Mapping for Mode 1," on page 46 and Table 5-13: "LCD Interface Pin Mapping for Modes 2/3," on page 47.

1.5.1 RGB LCD Interface

The RGB LCD interface supports a wide range of TFT panels. TFT panels that can be programmed via various serial type interface are also supported and are selected with the LCD1 Serial Data Type bits (REG[0054h] bits 7-5). If this type of panel is connected to LCD1, the RGB Panel Type must be set to the General TFT, ND-TFT setting.

The RGB LCD panel data bus width is selectable to support 9/12/16/24-bit panels using the RGB Interface Panel Data Bus Width bits (REG[0032h] bits 6-4). Other configurable options include non-display period times and polarity, width, and position of control signals.

1.5.2 Parallel LCD Interface

The Parallel LCD Interface supports multiple output data formats, providing the flexibility to support various RAM integrated Parallel Interface LCD panels. If a parallel panel is connected to LCD1, the LCD1 Parallel Data Format bits (REG[0056h] bits 2-0) are used to program the output data format, otherwise the LCD2 Parallel Data Format bits (REG[005Eh] bits 2-0) are used.

The LCD panel image can be updated in three different ways. Manual Transfer is accomplished by setting REG[003Ah] bit 1 = 1 which sends one frame of panel data to the Parallel LCD panel. LCD Module VSYNC Manual Transfer mode synchronizes a manual frame transfer to an external VSYNC signal sent by the parallel LCD panel. The VSYNC Input Enable bit for either LCD1 or LCD2 (REG[0056h] bit 7 or REG[005Eh] bit 7) must be set to enable this mode. The last transfer method is Automatic Transfer which sends frames to the LCD panel whenever a camera vertical sync signal is detected. If the VYSNC Input mode is also enabled, an external LCD panel VSYNC must also be detected. Automatic Transfer mode is enabled by setting REG[003Ch] bit 1 = 1. Automatic Transfer mode is intended for displaying a camera image on a serial or parallel interface LCD panel without the need to manually update the panel display.

1.5.3 Serial LCD Interface

The Serial LCD Interface supports serial type LCD panels only on LCD2. Serial Data Type, Data Direction, Data Format, and Serial Clock Phase and Polarity are all selectable and are controlled in the LCD2 Serial Interface Setting register (REG[005Ch]). Serial Interface Panels are updated with image data as described in Section 1.5.2, “Parallel LCD Interface” on page 16.

1.6 Display Features

The S1D13715 contains display features that enhance the functionality of the Mobile Graphics Engine. These features are Picture-in-Picture Plus (PIP$^+$), Overlay, SwivelView, Mirror, and Pixel Doubling.

PIP$^+$ is a sub-window within the Main Window and typically is used to display the camera image or a decoded JPEG image. PIP$^+$ can be used with the overlay functions so that only the part of the PIP$^+$ window that overlaps the overlay color in the Main Window is displayed (according to the overlay function selected). Various overlay functions can be employed such as transparency, averaging, ANDing, ORing, and Inverting. Multiple overlay functions can be enabled, but only the overlay function with the highest priority is processed.

SwivelView is a hardware rotation of the display image by either 90, 180, or 270 degrees. By processing the rotation of the image in hardware, SwivelView offers a performance advantage over software rotation. SwivelView can be used to support portrait sized panels mounted in a landscape orientation or vice versa.

Mirror can be used to mirror the image in either the PIP$^+$ window display, Main Window display, or both. A typical application for mirroring is to support swivelling on a clamshell phone. When the large display is on the outside of the phone and the camera is pointing at the user, mirroring allows the camera image to be displayed properly.

Pixel Doubling is a feature that can be used to double the size of an image in either the PIP$^+$ window display, Main Window display or both. Typical applications for pixel doubling include increasing the displayed size of a decoded JPEG image or using a larger panel size than is supported natively by an operating system. For example, if a 320x320 resolution panel is used with an OS that supports only a main display of 160x160 (such as in many PDAs), pixel doubling can be enabled to utilize the whole display.

1.7 Camera Interface

The S1D13715 supports two 8-bit parallel Camera Interfaces. Only one camera interface can be active at a given time. The input data format supported is YUV 4:2:2. Embedded sync signals, as defined by the ITU-R BT656 standard, are also supported. A clock is supplied to the camera from the camera interface (CM1CLKOUT or CM2CLKOUT) and the camera in turn outputs YUV data, horizontal and vertical sync signals, and a pixel clock that the S1D13715 camera interface uses to sample the incoming YUV data. The CMxCLKOUT frequencies are controlled by the Camera1 Clock Divide Select bits (REG[0100h] bits 3-0) and Camera2 Clock Divide Select bits (REG[0104h] bits 3-0). The output control of these two clocks is controlled by REG[0110h] bit 0. The camera interface supports various types of YUV cameras by allowing the selection of different formats of YUV 4:2:2 signals. Features such as YUV Data Format, YUV Data Range, HSYNC and VSYNC polarity, and Camera Pixel Clock Input Polarity are all selectable.

Since the Camera Pixel Clock can be, at most, 1/3 the S1D13715 System Clock , the frames per second of the camera image displayed on the LCD display is dependant on the internal speed of the S1D13715. For example, a setting of 54MHz for the System Clock results in the camera returning a Pixel Clock of 6.5MHz when the S1D13715 Camera Clock Out Divide is set to a divide of 4 (typical cameras use a divide by 2 of the input clock to generate the pixel clock). For CIF resolutions (352x288), this translates into 29 fps. For a Camera Clock Out Divide of 2 and VGA resolutions (640x480), 21 fps is achieved.

In addition to the main function of the two camera interfaces, other video functions are supported. For the Camera Interface Pin Mappings refer to Section 5.7.1, “Camera1 Interface Pin Mapping” on page 52 and Section 5.7.2, “Camera2 Interface Pin Mapping” on page 52.

1.8 Resizers and YUV/RGB Converter

There are two resizers in the S1D13715: the view resizer and the capture resizer. Both resizers can be used to resize (crop) and/or scale incoming YUV data from the camera interface, from the JPEG Decoder, or from the Host CPU in YUV bypass mode. Once the YUV data has been resized and scaled, it gets converted to RGB data by the YUV/RGB Converter (YRC), so that it can be displayed on the LCD panel. The location in memory where the YRC writes the RGB data is defined by the YUV/RGB Converter Write Start Address registers (REG[0242h]-[0244h]). The output bpp of the YRC must match either the Main Window color depth (bpp) or the PIP^{+} Window color depth (bpp) setting, depending on which window the image is being displayed in. The YRC color depth (bpp) output is controlled by the YRC Output Bpp Select bits (REG[0240h] bits 11-10). The resizers can support a maximum image size up to 2048 x 2048 pixels.

Although each resizer can be configured to be the source for the YRC using the Output Source Select bit (REG[0940h] bit 3), typically the view resizer is set as the source since only the capture resizer can be the source for the JPEG Encoder or for YUV bypass mode to the Host CPU. A typical application has the view resizer resizing the camera data and has the YRC converting it for display on the LCD panel, while the capture resizer is used to send camera YUV data for JPEG encoding or for raw storage by the Host CPU. When the desired viewed camera image is the same dimensions as the desired captured JPEG or YUV image, only the capture resizer needs to be used.

Note

Only the view resizer can be used to resize YUV data from the JPEG Decoder or from the Host CPU.

1.9 JPEG Encoder / Decoder

The S1D13715 contains a full JPEG Codec capable of encoding an incoming camera data stream or decoding a JPEG image sent from the Host CPU.

1.9.1 Encoder

Either the YUV data stream from the camera interface or the display buffer memory via the RGB to YUV Converter can be encoded into a JPEG image. The YUV data from the capture resizer is organized into 8 x 8 blocks in the JPEG Line Buffer, as required for JPEG processing, and then sent to the JPEG Encoder. As the JPEG Encoder is encoding the YUV data, it starts filling up the JPEG FIFO with JPEG data. This data must be read by the Host CPU before the JPEG FIFO overflows. Status flags and interrupts can be used to determine how full the JPEG FIFO is becoming. The JPEG FIFO is accessed through the JPEG FIFO Read/Write register (REG[09A6h]). The JPEG FIFO can be set as large as 128K bytes and typically this will be large enough to contain the whole JPEG image. A smaller JPEG file size can be achieved using the capture resizer's trimming and scaling functions or a higher JPEG compression ratio can be achieved by using different Quantization and Huffman Tables.

As mentioned in Section 1.3, "Internal Memory" on page 12, when the JPEG functions are enabled, 32K bytes of the internal memory is used for the JPEG Line Buffer and from 4K bytes to 64K bytes is used for the JPEG FIFO. The JPEG Encoder can encode YUV 4:2:2, YUV 4:2:0, and YUV 4:1:1 data formats and will convert the incoming YUV data to the desired format. This encoding option is set by the YUV Format Select bits (REG[1000h] bits 1-0). The JPEG file size can be reduced if a smaller UV:Y ratio format is used.

The intended use of the JPEG Encoder is to "take a snapshot" of the currently viewed camera image or display image, or to encode YUV data sent by the Host CPU. This JPEG image is then downloaded to the Host CPU through the JPEG FIFO and stored as a JPEG file.

1.9.2 Decoder

The S1D13715 contains a JPEG Decoder which allows the Host CPU to send a JPEG image file for conversion and display on the LCD panel, or to send the resulting YUV decoded data back to the Host CPU. The incoming JPEG data is written to the JPEP FIFO and then goes to the JPEG Decoder for decoding into YUV format. The YUV format output is based on the original format the JPEG file was encoded from and is reported in the YUV Format Select bits (REG[1000h] bits 1-0). The output of the JPEG Decoder goes to the JPEG Line Buffer which then organizes the 8 x 8 blocks of YUV data into the correct YUV format and sends this data to the view resizer. The view resizer can trim and scale the image and then it is converted by the YRC to be displayed on the LCD panel or sent to the Host CPU.

While writing the JPEG data to the JPEG FIFO, the Host CPU may be interrupted. When this happens, the JPEG Decoder completes decoding the data stored in the JPEG FIFO and the waits for more data from the Host CPU. The decode operation will continue until the

JPEG Decoder detects the End-of-File Marker. The JPEG FIFO must not be overflowed by the Host CPU. Status flags and interrupts can be used to determine how full the JPEG FIFO is becoming. The JPEG FIFO is accessed through the JPEG FIFO Read/Write register (REG[09A6h]).

As mentioned in Section 1.3, “Internal Memory” on page 12, when the JPEG functions are enabled, 32K bytes of the internal memory is used for the JPEG Line Buffer and from 4K bytes to 64K bytes is used for the JPEG FIFO. The JPEG Decoder can decode YUV 4:4:4, YUV 4:2:2, YUV 4:2:0, and YUV 4:1:1 data formats.

1.10 2D BitBLT Engine

The purpose of the 2D BitBLT Engine is to improve the overall system performance by off-loading the work of the Host CPU in moving display data between the CPU and display memory. There are five BitBLTs (Bit Block Load Transfer) that can move display data from one location to another. Additionally, data functions can be performed that manipulate the source and/or destination data. For more information on the 2D BitBLT Engine, see Section 16, “2D BitBLT Engine” on page 344.

2 Features

2.1 Internal Memory

- Embedded 320K byte SRAM memory used for:
  - Display Buffer
  - JPEG FIFO
  - JPEG Line Buffer

2.2 Host CPU Interface

- Four generic asynchronous CPU interfaces
- 16-bit data bus
  - 16-bit register and FIFO access
  - 8/16-bit display buffer access
- Direct / Indirect addressing
- Little / Big endian support
- Registers are memory-mapped
  - M/R# input selects between memory and register address space
  - M/R# and CS# inputs select between memory and register address space in 2 CS# mode
- CPU serial port for direct control of a serial LCD
- CPU parallel port for direct control of a parallel LCD

2.3 Display Support

- Active Matrix TFT displays: 9/12/18/24-bit interface
  - Extended TFT interface (Type 2 and Type 5)
  - TFT with u-Wire interface
  - a-Si TFT interface
  - Epson ND-TFD interface
- ‘Direct’ support for the Casio TFT LCD (or compatible interfaces)
- ‘Direct’ support for a-TFT Samsung TFT LCD (or compatible interfaces)
- ‘Direct’ support for the Sharp HR-TFT LCD (or compatible interfaces)

- 'Direct' support for Toshiba low power LCDs. Contact your Epson sales representative for details.
- 8/9-bit serial interface LCDs with integrated RAM
- 8/16/18/24-bit MPU parallel interface LCDs with integrated RAM
- Supports a maximum of 2 panels (LCD1 and LCD2 can't be refreshed simultaneously)

2.4 Display Modes

- Supports three panel interface modes which each allow two LCDs (LCD1 and LCD2) to be connected to the S1D13715. Only one LCD can be active at a time.
  - Mode 1:
    - LCD1: RGB type panel
    - LCD2: Serial interface panel
  - Mode 2:
    - LCD1: Parallel interface panel
    - LCD2: Serial interface panel
  - Mode 3:
    - LCD1: Parallel interface panel
    - LCD2: Parallel interface panel
  - Mode 4:
    - LCD1: RGB type panel
    - LCD2: Parallel interface panel
- Host CPU can directly control serial interface panels on LCD2
- Host CPU can directly control parallel interface panels on LCD1 or LCD2
- 8/16/32 bit-per-pixel (bpp) color depths
- Separate Look-up Tables (LUTs) for the Main Window and the PIP$^+$ Window
- LUTs can be bypassed

2.5 Display Features

- Overlay functions
- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of display image
- Mirror Display: provides a "mirror" image of the display
- Virtual display support: displays images larger than the panel size through the use of panning and scrolling
- Picture-in-Picture Plus (PIP$^+$): displays a variable size window overlaid over background image
- Pixel Doubling
- Video Invert: Data output to the LCD is inverted

2.6 Camera Interface

- 2-port Camera Interface (only one camera interface can be used at a time)
- Supports YUV 4:2:2 format
- Supports ITU-R BT.656 format
- 8-bit data bus (YUV Multi Out)
- MPU type interface camera support on Camera1 interface
- MPEG Codec input interface support on Camera2 interface
- Strobe control function

2.7 Digital Video Features

- Hardware JPEG codec based on the JPEG baseline standard
  - JPEG Encode supports YUV 4:2:2, YUV 4:2:0, YUV4:1:1 formats
  - JPEG Decode supports YUV 4:4:4, YUV 4:2:2, YUV 4:2:0, YUV4:1:1 formats
  - Arithmetic accuracy satisfies the compatibility test of JPEG Part-2
  - Software control of image size
  - Maximum horizontal image size for JPEG encoding (YUV 4:2:2 format: up to 2880 pixels)
- Two resizers: View resizer receives YUV data from the camera interface, or from the JPEG decoder, or from the Host CPU. Capture resizer receives YUV data only from the camera interface.
  - YUV Data can be resized (trimmed and scaled) then:
    - Converted to RGB data for display on the LCD
    - Converted to JPEG data and read by the CPU Host via the JPEG FIFO
    - Read by the Host CPU directly (YUV format)
- YUV to RGB Converter (YRC): YUV data from the View Resizer or Capture Resizer is converted to RGB format to be displayed on the LCD.

2.8 Picture Input / Output Functions

- The YUV data (YUV 4:2:2 format) from Camera Interface can be:
  - Stored in the display buffer after resizing and conversion to RGB format.
  - Transferred to the Host CPU via the JPEG FIFO after resizing and encoding to JPEG format.
  - Transferred to the Host CPU via the JPEG FIFO after resizing and conversion to YUV (format 4:2:2 or 4:2:0).

- The JPEG file downloaded from the Host CPU can be:
  - Decoded by the internal JPEG decoder, resized, scaled, converted to RGB and stored in the display buffer memory for display on the LCD.
  - Decoded by the internal JPEG decoder, resized, scaled, and downloaded to the Host CPU via the JPEG FIFO.
- YUV data (format 4:2:2 or 4:2:0) downloaded from the Host CPU can be:
  - Resized, scaled, converted to RGB and stored in the display buffer memory for display on the LCD.
  - Encoded by the internal JPEG encoder, resized, scaled, and downloaded to the Host CPU via the JPEG FIFO.
- RGB data in the display buffer can be:
  - Converted to YUV, then transferred to the Host CPU via the JPEG FIFO after resizing and encoding to JPEG format.

2.9 2D BitBLT Acceleration

- 2D BitBLT engine including: (this function does not support 32bpp modes)

Move BitBLT	Transparent Move BitBLT
Solid Fill BitBLT	Read BitBLT
Pattern Fill BitBLT	

2.10 Clock

- Internal PLL driven by a single external reference clock, 32.768KHz
- 40 - 55MHz PLL output
- PLL bypass mode for external clock input

2.11 Power Save

- Software initiated power save mode
- Software initiated display blank

2.12 Miscellaneous

- General Purpose Input/Output pins are available

3 System Diagrams

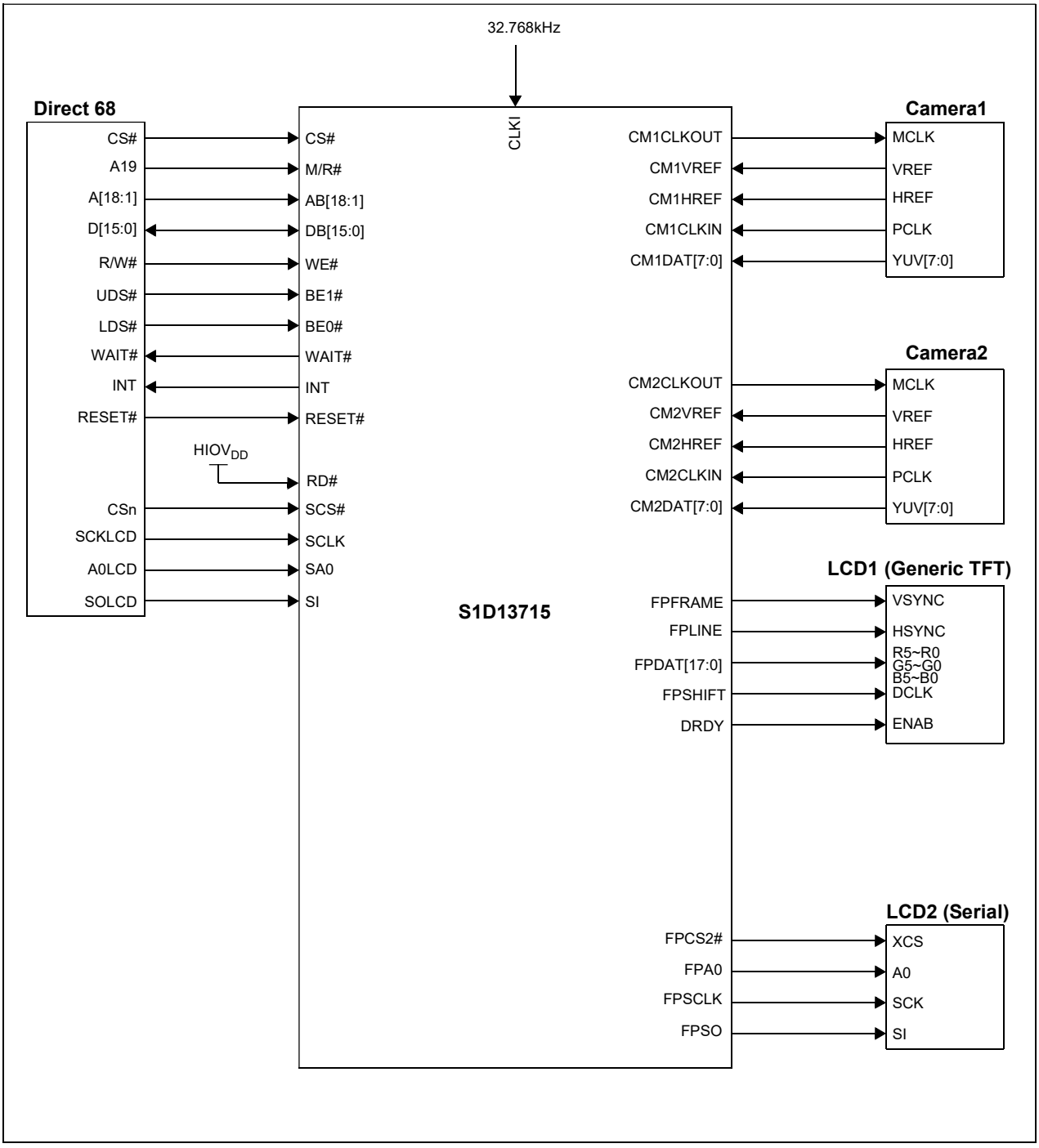

Figure 3-1: S1D13715 System Diagram 1