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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



S1D13715

S1D13715 QVGA LCD Controller

The S1D13715 is a QVGA LCD Controller designed to support digital video in products for embedded markets. The S1D13715 contains an integrated dual port camera interface, hardware JPEG encoder/decoder and can be interfaced to an external MPEG codec. Seamlessly connecting to both direct and indirect CPU interfaces, it provides support for TFT panels. The S1D13715, with its 320 KB of embedded SRAM and rich feature set, provides a low cost, low power, single chip solution to meet the demands of embedded markets requiring digital video.

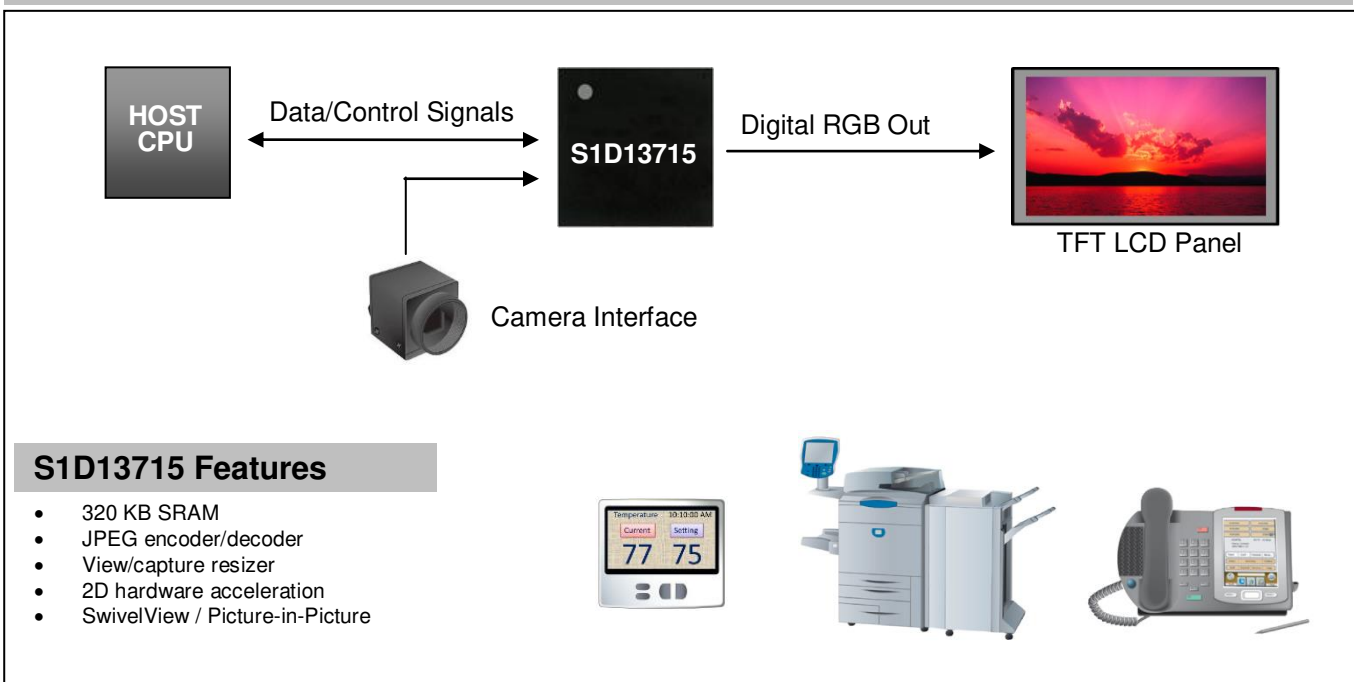
Additionally, products requiring a rotated display can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory transparent to the software application. The S1D13715 also provides support for "Picture-in-Picture" (a variable size window with overlay functions). Higher performance is provided by the hardware acceleration engine which provides 2D BitBLT functions.

The S1D13715 provides impressive solutions for embedded markets requiring digital video support. Its impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

FEATURES

- Embedded 320 KB SRAM display buffer
- Low operating voltage
- Direct and indirect CPU interfaces
- Programmable resolutions and color depths
- Support for TFT panels
- 9/12/18/24-bit RGB interface
- Extended TFT interfaces including HR-TFT
- Internal PLL or digital clock input
- Dual port camera interface with resize function
- Hardware JPEG encoder/decoder
- YUV to RGB converter
- SwivelView™ 90°, 180°, 270° hardware for rotation of displayed image
- Picture-in-Picture
- 2D hardware acceleration engine
- Software initiated power save mode

SYSTEM BLOCK DIAGRAM



DESCRIPTION

Display Buffer

- 320 KB of embedded SRAM
- Addressable as a single linear address space

Panel Support

- Supports TFT panels
 - 9/12/18/24-bit RGB interface
- Typical resolutions:
 - up to 320x480@16bpp
 - up to 320x240@32bpp

Display Features

- 8/16/32 bpp support
- Picture-in-Picture: displays a variable size window overlaid over the background image
- Overlay functions
- Pixel doubling: doubles the effective resolution
- Video invert: inverts display data

Acceleration

- 2D BitBLT engine
- SwivelView: 90°, 180°, 270° hardware rotation of display image
- Mirror display: hardware "mirror" image of display

CPU Interface

- 16-bit generic asynchronous CPU interface
- Direct and indirect addressing

Digital Video

- Dual port camera interface (YUV 4:2:2)
- Hardware JPEG encoder (YUV 4:2:2, 4:1:1, 4:2:0)
- Hardware JPEG decoder (YUV 4:4:4, 4:2:2, 4:1:1, 4:2:0)
- YUV display/capture (YUV 4:2:2, 4:2:0)
- Memory image JPEG encode (YUV 4:2:2, 4:1:1, 4:2:0)
- View and capture hardware resizer with trimming and reduction functions
- YUV to RGB and RGB to YUV converters
- Support for external MPEG codec interface

Miscellaneous

- Internal programmable PLL. or digital clock input
- Software initiated power save mode
- Multiple general purpose input/output pins
- COREVDD 1.8 volts and IOVDD 3.0 volts
- PFBGA 160-pin and QFP 176-pin packages

JAPAN SEIKO EPSON CORPORATION IC Sales & Marketing Department 421-8 Hino, Hino-shi, Tokyo 191-8501, JAPAN Phone: +81-42-587-5816 FAX: +81-42-587-5117	CHINA EPSON (CHINA) CO., LTD 4 th Floor, Tower 1 of China Central Place, 81 Jianguo Road, Chaoyang District, Beijing 100025, CHINA Phone: +86-10-8522-1199 FAX: +86-10-8522-1120	TAIWAN EPSON TAIWAN TECHNOLOGY & TRADING LTD. 14F, No. 7, Song Ren Road, Taipei 110, TAIWAN Phone: +886-2-8786-6688 FAX: +886-2-8786-6660
AMERICA EPSON ELECTRONICS AMERICA, INC. 214 Devcon Drive, San Jose, CA 95112, USA Phone: +1-800-228-3964 FAX: +1-408-922-0238	CHINA SHANGHAI Branch Room 01 & 04 17F, Greenland Center II, 562 Dong An Road, Shanghai 200032, CHINA Phone: +86-21-5423-5577 FAX: +86-21-5423-4677	SINGAPORE EPSON SINGAPORE PTE., LTD. 1 HarbourFront Place, #03-02 HarbourFront Tower One, SINGAPORE 098633 Phone: +65-6586-5500 FAX: +65-6271-3182
EUROPE EPSON EUROPE ELECTRONICS GmbH Riesstrasse 15, 80992 Munich, GERMANY Phone: +49-89-14005-0 FAX: +49-89-14005-110	CHINA SHENZHEN Branch Room 804-805, 8 th Floor, Tower 2, Ali Center, No.3331 Keyuan South RD (Shenzhen bay), Nanshan District, Shenzhen 518054, CHINA Phone: +86-10-3299-0588 FAX: +86-10-3299-0560	KOREA SEIKO EPSON CORP. 19F, KLI 63 Bldg., 60 Yoido-dong, Youngdeungpo-Ku, Seoul 150-763, KOREA Phone: +82-2-784-6027 FAX: +82-2-767-3677

<http://global.epson.com/products/semicon>



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