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S1D13719
Mobile Graphics Engine

Hardware Functional Specification

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Table of Contents

1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13719 Mobile Graphics Engine. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

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1.2 General Description

The S1D13719 is a Mobile Graphics Engine solution designed with support for the digital video revolution in mobile products. The S1D13719 contains an integrated dual port camera interface, hardware JPEG encoder/decoder and can be interfaced to an external MPEG codec. Seamlessly connecting to both direct and indirect CPU interfaces, it provides support for up to two LCD panels. The Mobile Graphics Engine supports all standard TFT panel types and many extended TFT types, eliminating the need for an external timing control IC. The S1D13719, with it's 512K bytes of embedded SRAM and rich feature set, provides a low cost, low power, single chip solution to meet the demands of embedded markets requiring Digital Video, such as Mobile Communications devices and Palm-size PDAs.

Additionally, products requiring a rotated display can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory, transparent to the software application. The S1D13719 also provides support for "Picture-in-Picture Plus" (a variable size window with overlay functions). Higher performance is provided by the Hardware Acceleration Engine which provides 2D BitBLT functions.

The S1D13719 provides impressive support for cellular and other mobile solutions requiring Digital Video support. However, its impartiality to CPU type or operating system makes it an ideal display solution for a wide variety of applications.

2 Features

2.1 Internal Memory

- Embedded 512K byte SRAM used for:
  - Display Buffer
  - JPEG FIFO (up to 512K bytes)
  - JPEG Line Buffer (up to 96K bytes)
- SRAM consists of 5 physical banks (64K/128K/128K/128K/64K bytes)

2.2 Registers

- Registers are memory-mapped
- Asynchronous/synchronous registers (asynchronous registers are accessible during power save mode)
- Special register ports:
  - JPEG FIFO Port (used for JPEG encode/decode/bypass)
  - JPEG Line Buffer Port (used for JPEG encode/decode/bypass)

2.3 Host CPU Interface

- Five Generic Asynchronous CPU interfaces (Mode 80 Type 1, 2, 3 and Mode 68)
- 16-bit serial CPU interface
- 16-bit data bus
  - 16-bit register and FIFO access (when M/R# = 0)
  - 8/16-bit memory access (for direct interface only, when M/R# = 1)
- Hardware configurable at RESET# (using CNF[7:0] pins)
- Indirect / Direct addressing
- Little / Big endian support for parallel interfaces
- Two chip select modes (1CS# or 2CS#) for parallel interfaces
- Memory Rectangular Access for indirect interfaces
- Serial clock polarity mode for serial interface
- Parallel LCD bypass function is not supported when serial interface is selected
  - Bus time-out reset function (interrupt/reset)
  - Cycle time-out function (terminate cycle generation/interrupt)

- Interrupt output
- LCD Bypass Mode (direct control of LCD input by the host CPU)
  - Available for both LCD1/LCD2
  - Supports serial/parallel interface LCD panels
  - Parallel interface LCD panels can be read when LCD panel is bypassed
  - Host CPU control during power save mode

2.4 Display Support

- 9/12/16/18/24-bit RGB Interface Active Matrix TFT displays:
  - Generic TFT interface
  - a-Si TFT interface
  - TFT with u-Wire interface
  - Epson ND-TFD interface
  - Extended TFT interface (Type 2)
- "Direct" support for the Casio TFT LCD (or compatible interfaces)
- "Direct" support for a-TFT Samsung TFT LCD (or compatible interfaces)
- "Direct" support for the Sharp HR-TFT LCD (or compatible interfaces)
  - "Direct" support for Toshiba low power LCDs. Contact your Epson sales representative for details.
- 8/16/18/24-bit Parallel Interface LCD panels with integrated RAM
- 8/9/16/18-bit Serial Interface LCD panels with integrated RAM
- Supports a maximum of 2 panels (LCD1 and LCD2 cannot be refreshed simultaneously)

2.5 Display Modes

- Supports four panel interface modes which each allow two LCDs (LCD1 and LCD2) to be connected to the S1D13719. Only one LCD can be active at a time.
  - Mode 1:
    - LCD1: RGB type panel
    - LCD2: Serial interface panel
  - Mode 2:
    - LCD1: Parallel interface panel
    - LCD2: Serial interface panel
  - Mode 3:
    - LCD1: Parallel interface panel
    - LCD2: Parallel interface panel
  - Mode 4:
    - LCD1: RGB type panel
    - LCD2: Parallel interface panel
- Color Depths:
  - RGB format: 8 bpp/16 bpp/24bpp (can be displayed on Main window or PIP$^+$ window)
  - YUV format: 16bpp (can be displayed only on PIP$^+$ window)
- Look-up table (LUT):
  - LUT1 (for main window): 256 word x 8-bit x 3pcs
  - LUT2 (for PIP$^+$ window): 64 word x 8-bit x 3pcs
  - LUTs can be bypassed

2.6 Display Features

- SwivelView: 90°/180°/270° counter-clockwise hardware rotation of display image
- Mirror Function: Horizontal flip of the display image
- Virtual Display: Displays an image that is larger than the size of the panel using panning and scrolling
- Picture-In-Picture-Plus (PIP$^+$): displays a variable size window overlaid over background image
- Overlay Functions: Average/AND/OR/INV operations using the transparency/key color of PIP$^+$ window
- Overlay can be combined
- Pixel Doubling: Doubles the size of the display image (independent horizontal/vertical)
- Fractional Zoom: Image can be reduced up 1/2x original size or expanded up to 2x original size (Only available for YUV 4:2:2 format)

- Fractional Shrink: Image can be reduced up n/128 (n=1-128) original size (for Capture/View Resizer)
- Video Invert: Data output to the LCD is inverted

2.7 Camera Interface

- Camera interface supports resolution up to a maximum of WUXGA (1920 x 1200) depending on the AC characteristics
- Supports YUV 4:2:2 format
- Supports ITU-R BT.656 format
- 8-bit/16-bit data bus interface
- MPEG Codec interface support on Camera2 interface
- Programmable capture frame
- Timing signal output for strobe control
  - Pulse is programmable and can be output synchronous to the camera input

2.8 JPEG Codec

- Hardware JPEG codec based on the JPEG baseline standard
  - JPEG Encode supports YUV 4:2:2, YUV 4:1:1 formats
  - JPEG Decode supports YUV 4:4:4, YUV 4:2:2, YUV 4:1:1 formats
  - Arithmetic accuracy satisfies the compatibility test of JPEG Part-2 (ISO/IEC10918-2)
  - Software control of image size to maximum of SXGA (1280 x 1024)
  - No gray scale marker support
- JPEG Encode
  - Image data from the camera can be resized and encoded
  - Image data from the LCD can be resized and encoded
  - YUV data from the Host can be encoded
  - Encoded JPEG file is read from the JPEG FIFO
- JPEG Decode
  - Decoded JPEG data is written to the JPEG FIFO
  - JPEG image data can be decoded, resized and then written to the display buffer

2.9 Resizer Functions

- Capture Resizer
  - Resizes image data from the camera
  - Resizes image data for the LCD
  - UV clip function
  - Available trimming and scaling functions (1/2-1/32)
- View Resizer
  - Resizes image data from the camera
  - Resizes JPEG decoded image data
  - UV clip function
  - Available trimming and scaling functions (1/2 - 1/32)
- Pixel Doubling
  - Doubles the image size (i.e. 160x120 can be doubled to 320x240)
  - Independent control of horizontal and vertical
  - Supports both RGB and YUV 4:2:2 formats
- Fractional Capture/View Resizer
  - Camera image data can be reduced from 1x to ½x size in 128 steps
  - JPEG decode data can be reduced from 1x to ½x size in 128 steps
  - Reduction ratios independent of view resize size
- Fractional Zoom
  - YUV 4:2:2 image data can be expanded from 1x to 2x size in 128 steps
  - YUV 4:2:2 image data can be reduced from 1x to 1/2x size in 128 steps
  - Expansion/reduction ratios independent of PIP^{+} window size

2.10 Image Data I/O Functions

- YUV data input from camera can be:
  - Resized and written to the display buffer in RGB 5:6:5 format
  - Resized and written to the display buffer in YUV 4:2:2 format
  - Resized, encoded to a JPEG file (YUV 4:2:2, YUV 4:1:1 format), and then output though the JPEG FIFO
  - Resized, converted to YUV 4:2:2 format, and then output through the JPEG FIFO
- JPEG file from the Host CPU can be:

- Input through the JPEG FIFO and decoded by the JPEG codec
- Decoded, resized, and written to the display buffer in RGB 5:6:5 format
- Decoded, resized, and written to the display buffer in YUV 4:2:2 format
- Decoded and output through the JPEG Line Buffer

- LCD Display data (specified rectangular area of display data) can be:
  - Converted to YUV format data
  - Resized, encoded to a JPEG file, and then output through the JPEG FIFO
- YUV data from the Host CPU can be:
  - Input through the JPEG line buffer, resized, and written to the display buffer in RGB 5:6:5 format
  - Input through the JPEG line buffer, resized, and written to the display buffer in YUV 4:2:2 format
  - Input through the JPEG line buffer, encoded, and output through the JPEG FIFO

2.11 Image Data Conversion Functions

- YUV/RGB Converter 1 can:
  - Convert resized image data to RGB 5:6:5 or 8:8:8 format
  - Convert resized image data to YUV 4:2:2 format
  - Use fixed UV data (UV clip)
  - Write a specified rectangular area to the display buffer
  - Set a write prohibit color (RGB)
- YUV/RGB Converter 2 can:
  - Convert YUV 4:2:2 format data in the display buffer to RGB 8:8:8 format
  - Use fixed UV (UV clip)
- RGB/YUV Converter can:
  - Convert RGB format data in a specified area of the display buffer to YUV format
  - Output to LCD panel stop when RGB/YUV converter operates (Parallel/Serial interface LCD panel)
  - Output blank data when RGB/YUV converter operates (RGB interface LCD panel)

2.12 2D BitBLT Accelerator

- Move BitBLT
- Transparent Move BitBLT
- Solid Fill BitBLT
- Read BitBLT (Direct Interface Mode Only)
- Pattern Fill BitBLT

2.13 SD Memory Card Interface

- SD Memory Card interface compatible with the SD Memory Card Physical Layer version 1.0 specification
  - 4-bit or 1-bit interface
  - No security functions
  - Card Detect and Write Protect inputs

2.14 General Purpose I/O Ports

- 22 General Purpose I/O Pins
  - Configurable as inputs or outputs (inputs at reset)
  - Pull-down resistance control for inputs (pull-down resistance is enabled at reset)
  - GPIO pins can be controlled during power save mode

2.15 Clocks

- PLL (requires clock input of 32.768kHz)
  - PLL output range: 48-55MHz
  - PLL output clock period jitter: 3%
  - PLL output stabilization time: 50ms
- PLL bypass mode available

2.16 Power Save Functions

- Software initiated power save mode (internal system clock is stopped)
- Clock supply control for each module
- LCD frame transfer (serial/parallel interface LCD panel)
- LCD auto frame transfer synchronized to camera input (serial/parallel interface LCD panel)
- Pull-down resistance control of general purpose I/O port (default is off for output mode)
- Bypass mode from Host CPU to LCD panel
- The power supply of Camera1 I/F and Camera2 I/F is independent. Only Camera I/F can stop the power supply when the Camera module unused

2.17 Power Supply Voltage

- Logic voltage: 1.95V - 1.65V
- PLL voltage: 1.95V - 1.65V
- Host Interface voltage: 3.25V - 2.75V
- LCD Interface voltage: 3.25V - 2.75V
- Camera Interface voltage: 3.25V - 2.75V
- SD Memory Card Interface voltage: 3.25V - 2.75V

2.18 Package

- PFBGA 180-pin package

3 System Diagrams

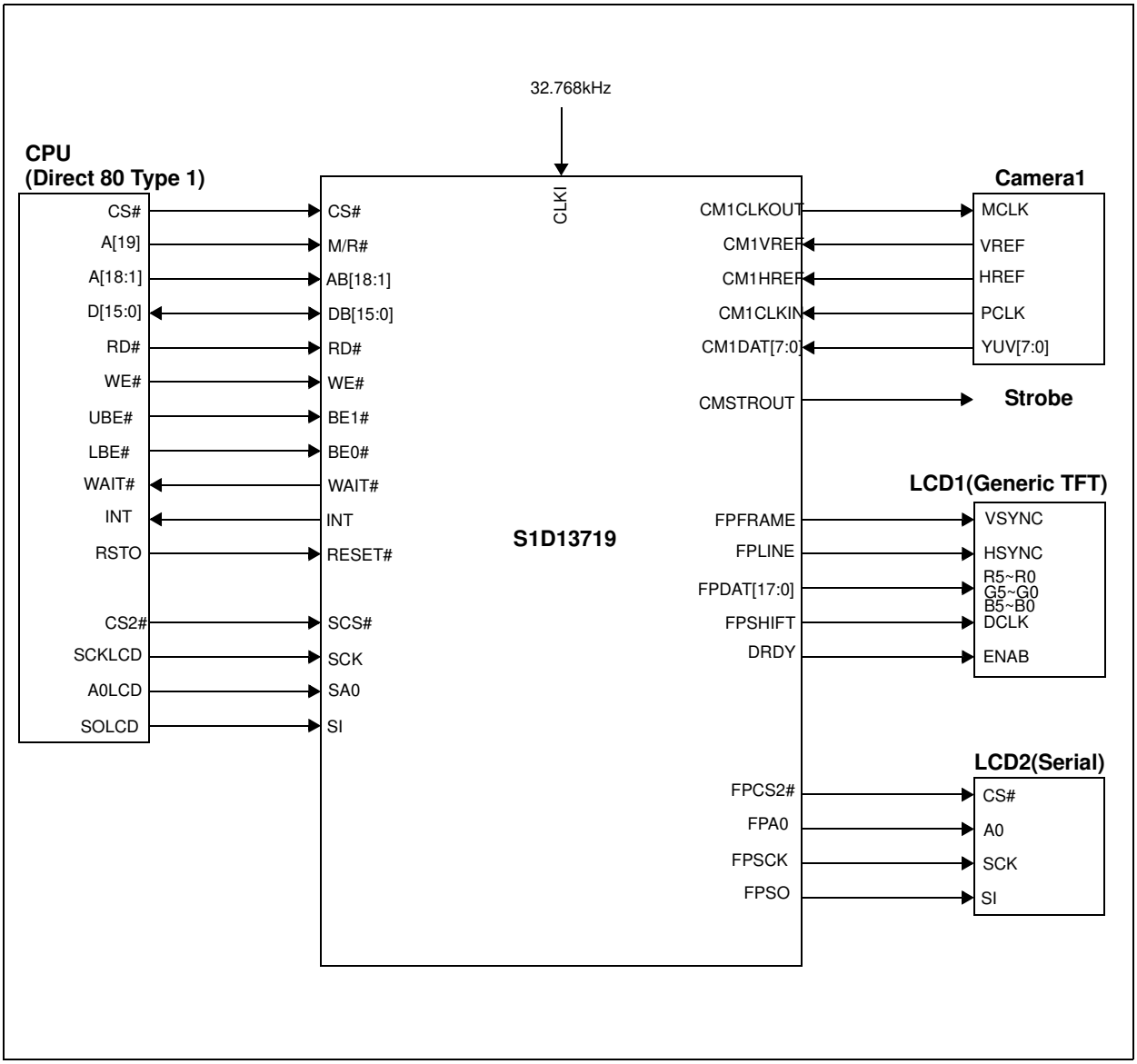

Figure 3-1: Example System Diagram 1

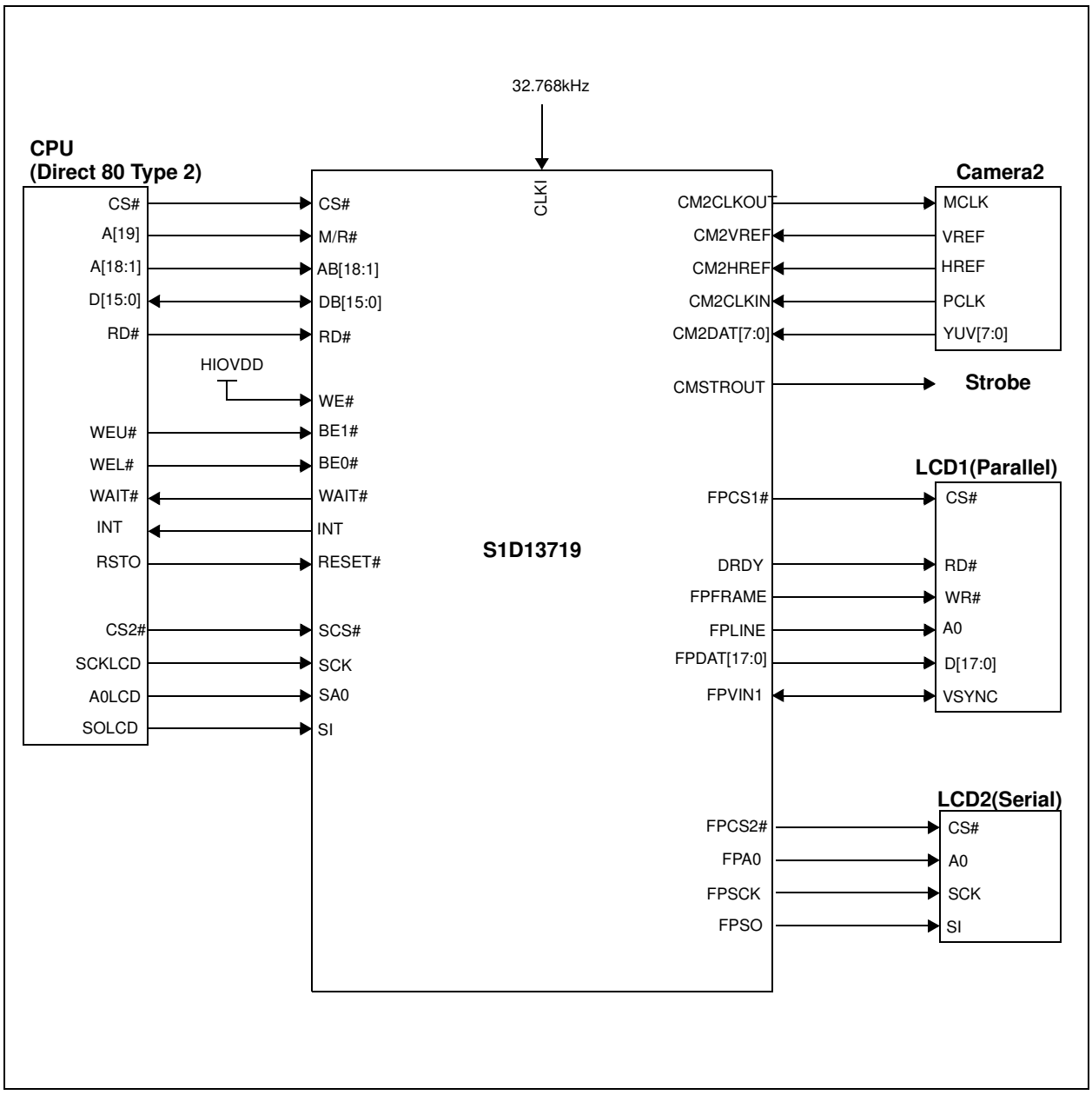

Figure 3-2: Example System Diagram 2

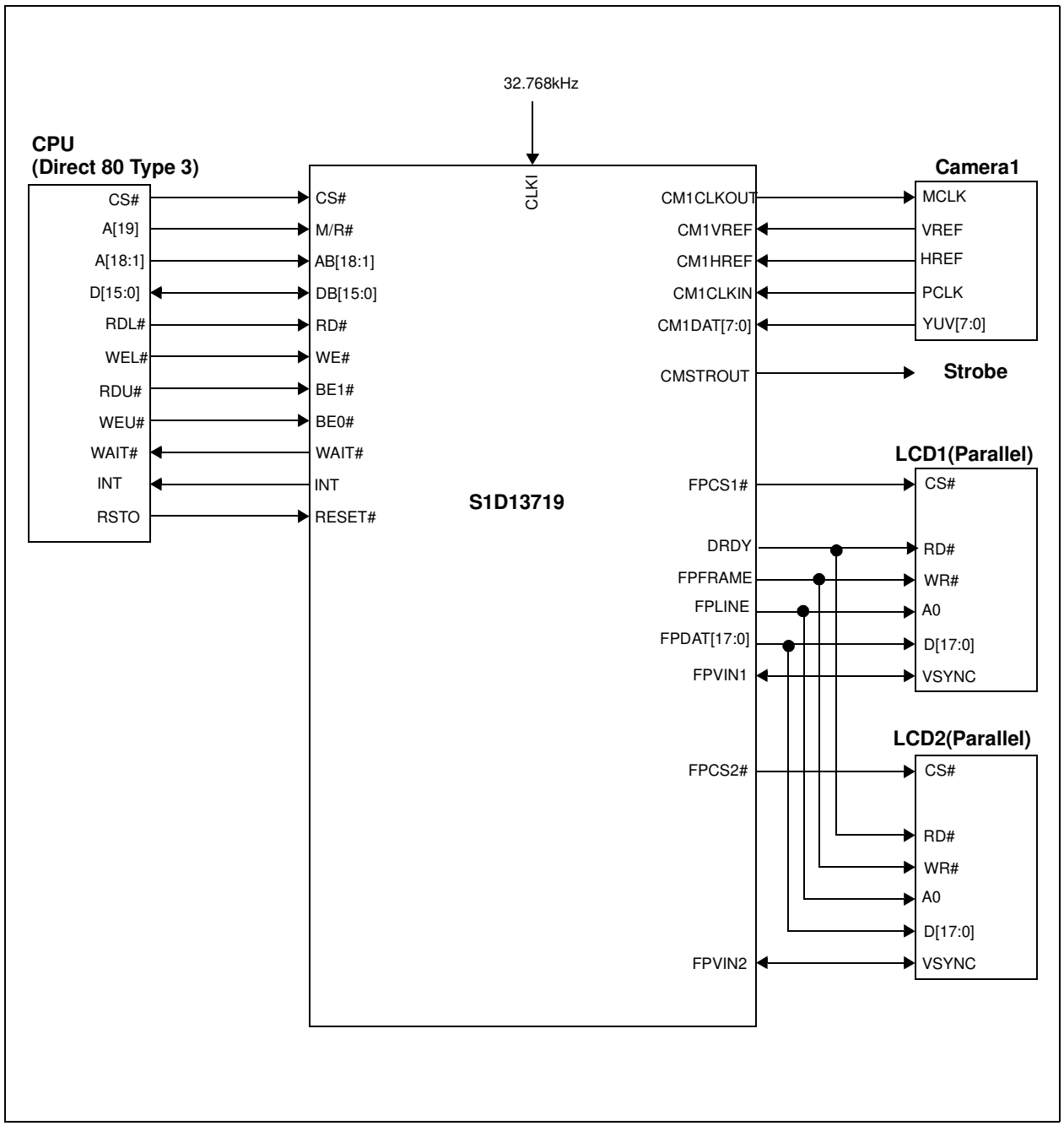

Figure 3-3: Example System Diagram 3

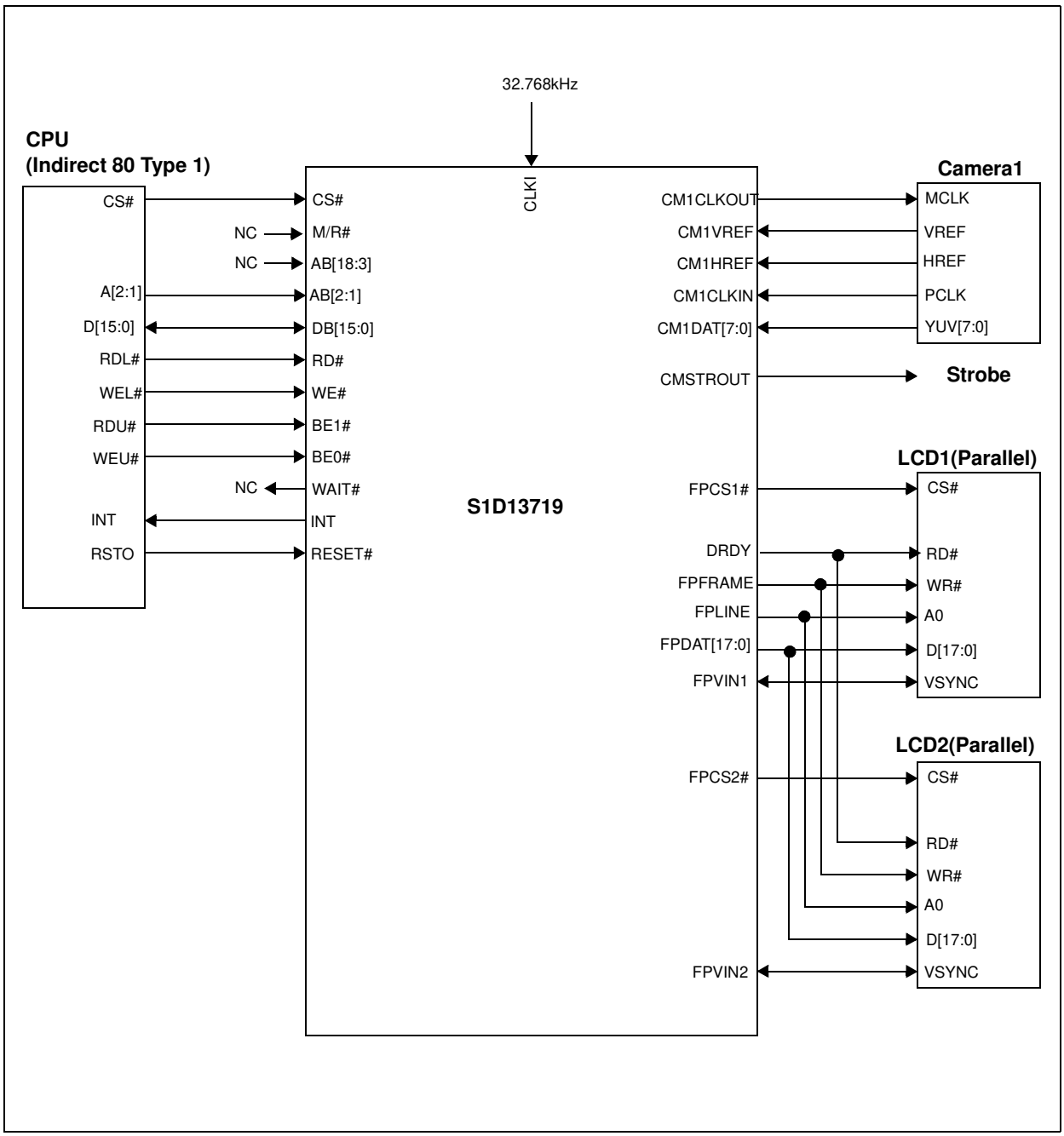

Figure 3-4: Example System Diagram 4

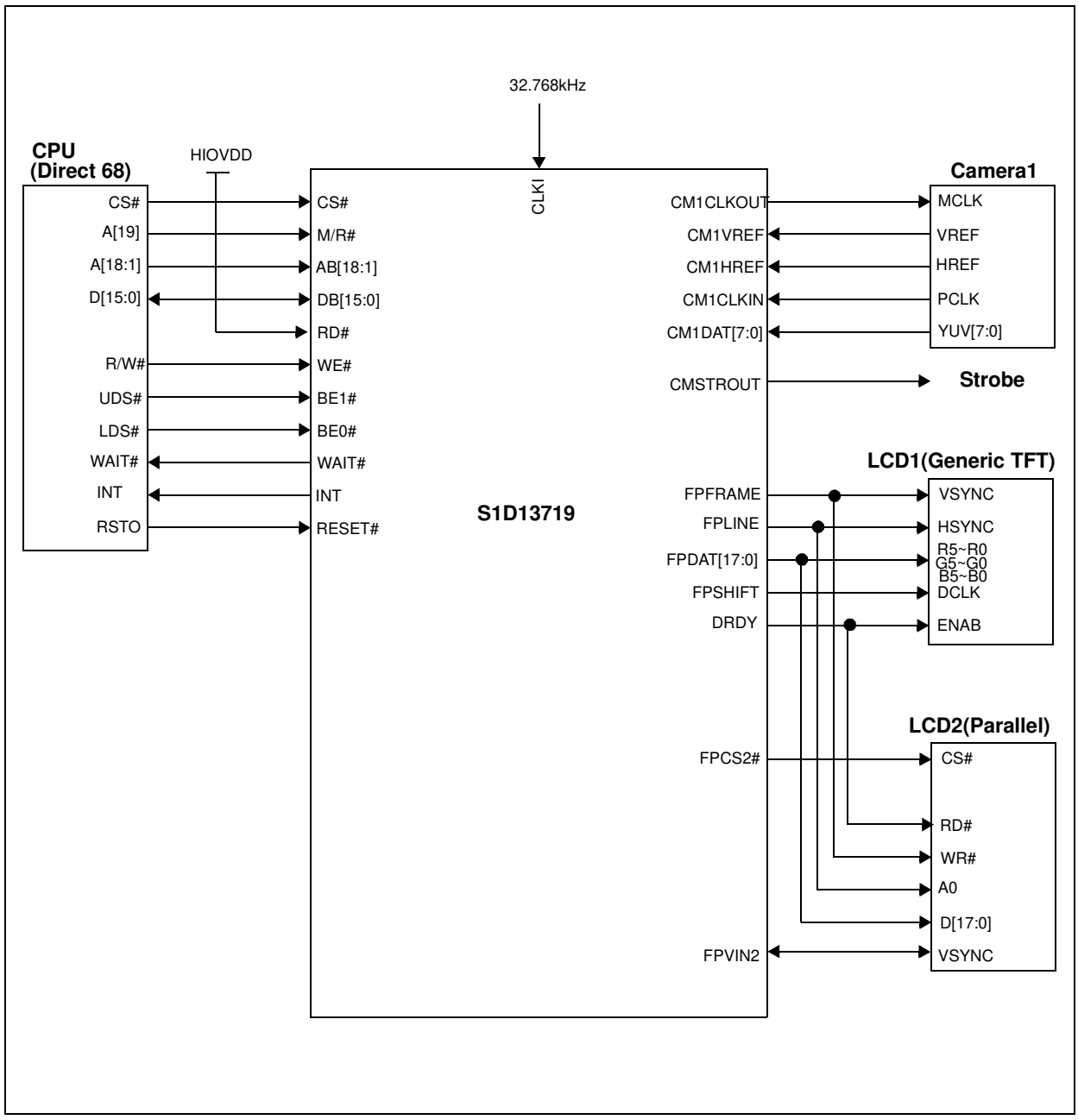

Figure 3-5: Example System Diagram 5

4 Block Diagram

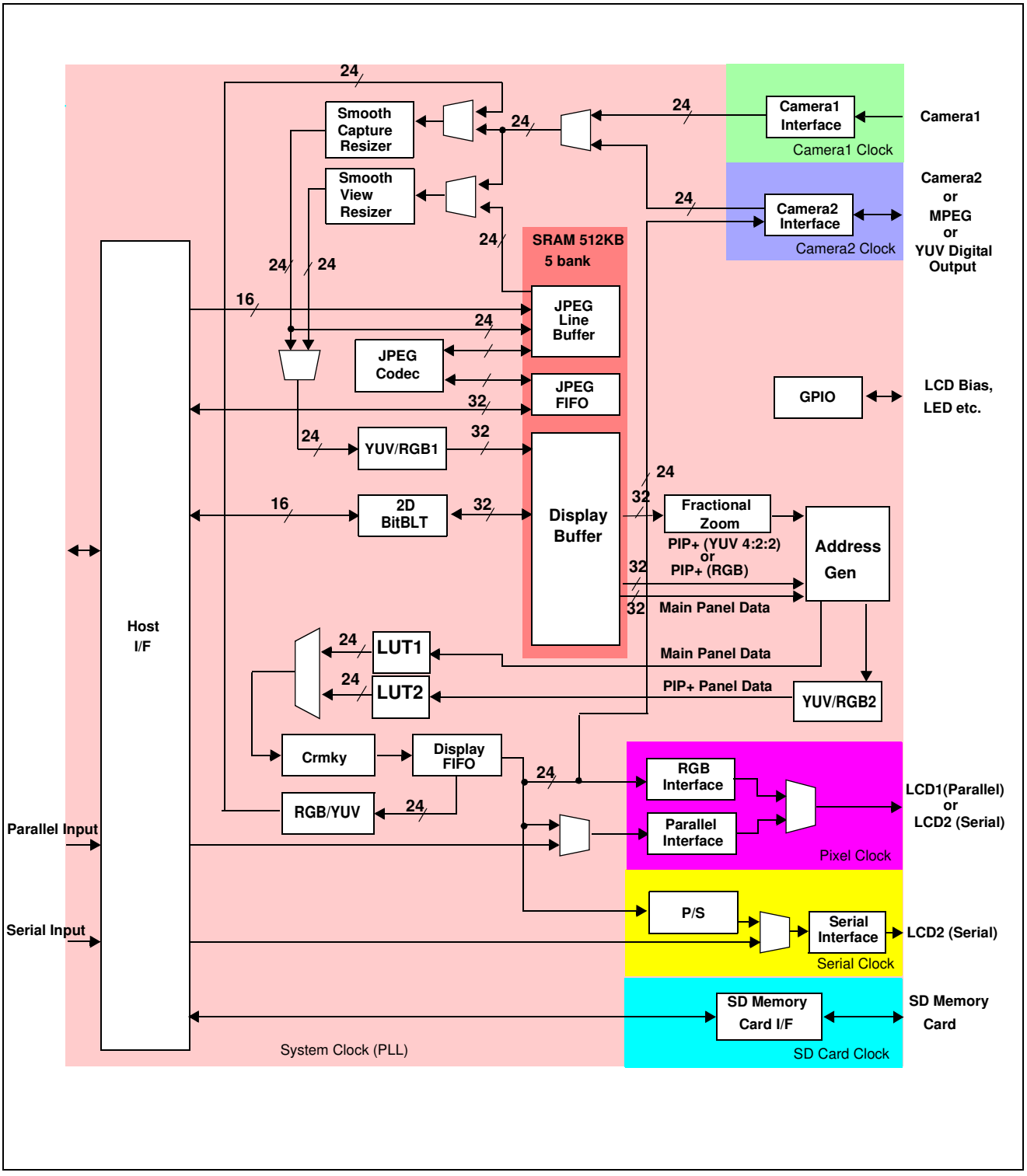

Figure 4-1: S1D13719 Block Diagram