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S1D13742 Mobile Graphics Engine

Hardware Functional Specification

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Table of Contents

1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13742 Embedded Memory LCD Controller. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This document is updated as appropriate. Please check the Epson Research and Development Website at **www.erd.epson.com** for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

1.2 Overview Description

The S1D13742 is a color LCD graphics controller with an embedded 768K byte display buffer. The S1D13742 supports a 8/16-bit Intel 80 CPU architecture while providing high performance bandwidth into display memory allowing for fast screen updates.

Products requiring a rotated display image can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory transparent to the software application. Resolutions supported include 800x480 single buffered and 352x416 double buffered.

The S1D13742 uses a double-buffer architecture to prevent any visual tearing during streaming video screen updates.

2 Features

2.1 Integrated Frame Buffer

- Embedded 768K byte SRAM display buffer.

2.2 CPU Interface

- 8/16-bit Intel 80 interface (used for display or register data).
- Chip select is used to select device. When inactive, any input data/command will be ignored.

2.3 Input Data Formats

- RGB: 8:8:8, 6:6:6, 5:6:5 (8:8:8 will be truncated to 16 or 18 bpp).
- YUV 4:2:2, 4:2:0 (Internal YUV to RGB Converter stored as 16 or 18 bpp).

Note
All input data must be internally converted to the same format before being stored in the display buffer. Different data types can not be mixed within a common display buffer.

2.4 Display Support

- Active Matrix TFT interface.
  - 18/36-bit interface.
  - Supports resolutions up to 800x480.

2.5 Display Modes

- 16/18 bit-per-pixel (bpp) color depths.
- 16 bpp to 18 bpp conversion: Input data can be converted from 16 bpp to 18 bpp in one of three ways.
  1. RGB (5:6:5) msb copying to create new lsb for the Red and Blue components. This conversion is done prior to storing in memory, as this allows for 16 bpp and 18 bpp input data to be mixed.
  2. Gamma Correction Look-Up-Tables: there are three, 64 position, 8-bit wide LUT's. The data stored in memory can be used as an index into these tables. The LUT's are placed on the display side and therefore do not affect the data stored in memory.
  3. RGB (5:6:5) stored in memory: LUT is by-passed. Copy msb to lsb for red and blue during the display read from memory.

2.6 Display Features

- All display writes will be handled by window apertures/position for complete or partial display updates. All window coordinates are referenced to top left corner of the displayed image (even in a rotated display, the top-left corner is maintained and no host side translation need take place).
- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of display image. All displayed windows can have independent rotation. No additional programming necessary when enabling these modes.
- Double-Buffer available to prevent image tearing during streaming input. Resolutions supported must fit inside 384K bytes (½ of total available display buffer). Typical resolution of 352x416.
- Pixel Doubling: Horizontal and Vertical averaging for smooth doubling of a single window.
- Pixel Halving: no limitation on number of windows.

2.7 Clock Source

- Internal programmable PLL.
- Single MHz clock input: CLKI.
- CLKI available as CLKOUT (separate CLKOUTEN pin associated with output).
  - output state = 0 when disabled.

2.8 Miscellaneous

- Hardware / Software Power Save mode.
- Input pin to Enable/Disable Power Save Mode.
- General Purpose Input/Output pins are available (GPIO[7:0]).
  - INT pin associated with selectable GPIO inputs.
- Package: QFP20 144-pin package

3 Block Diagram

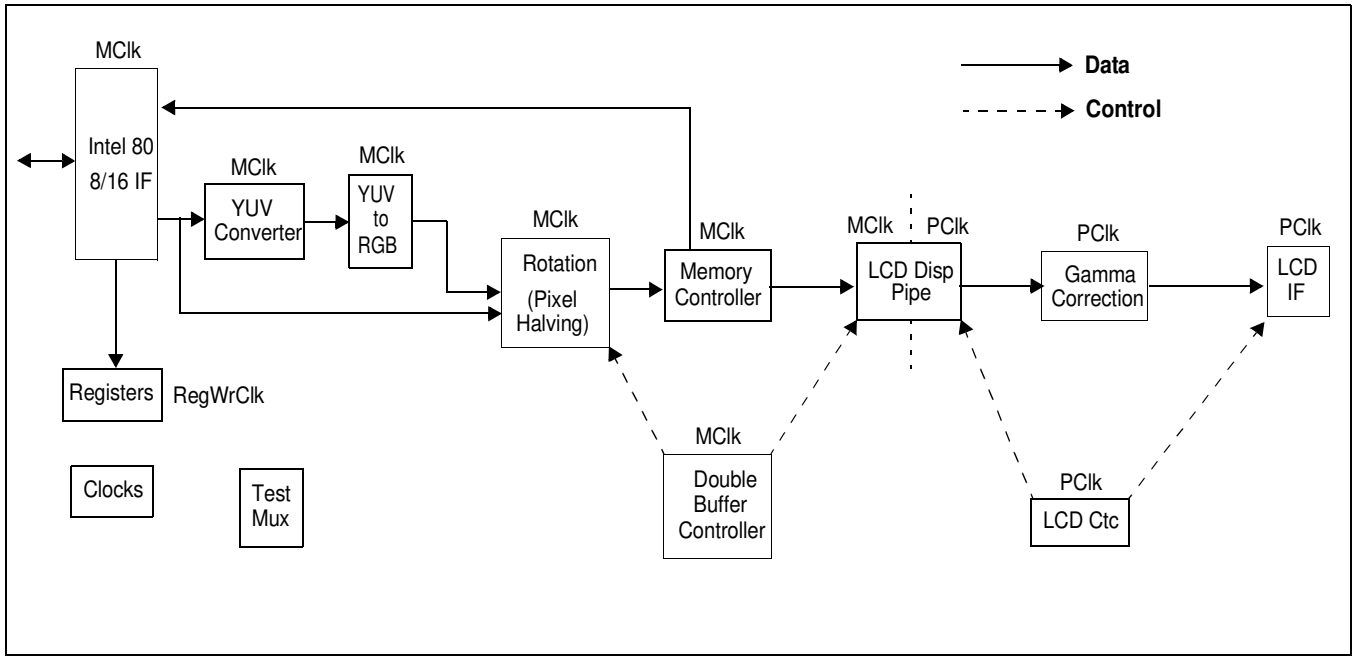

Figure 3-1: Block Diagram

4 Pinout Diagram

4.1 Pin-Out

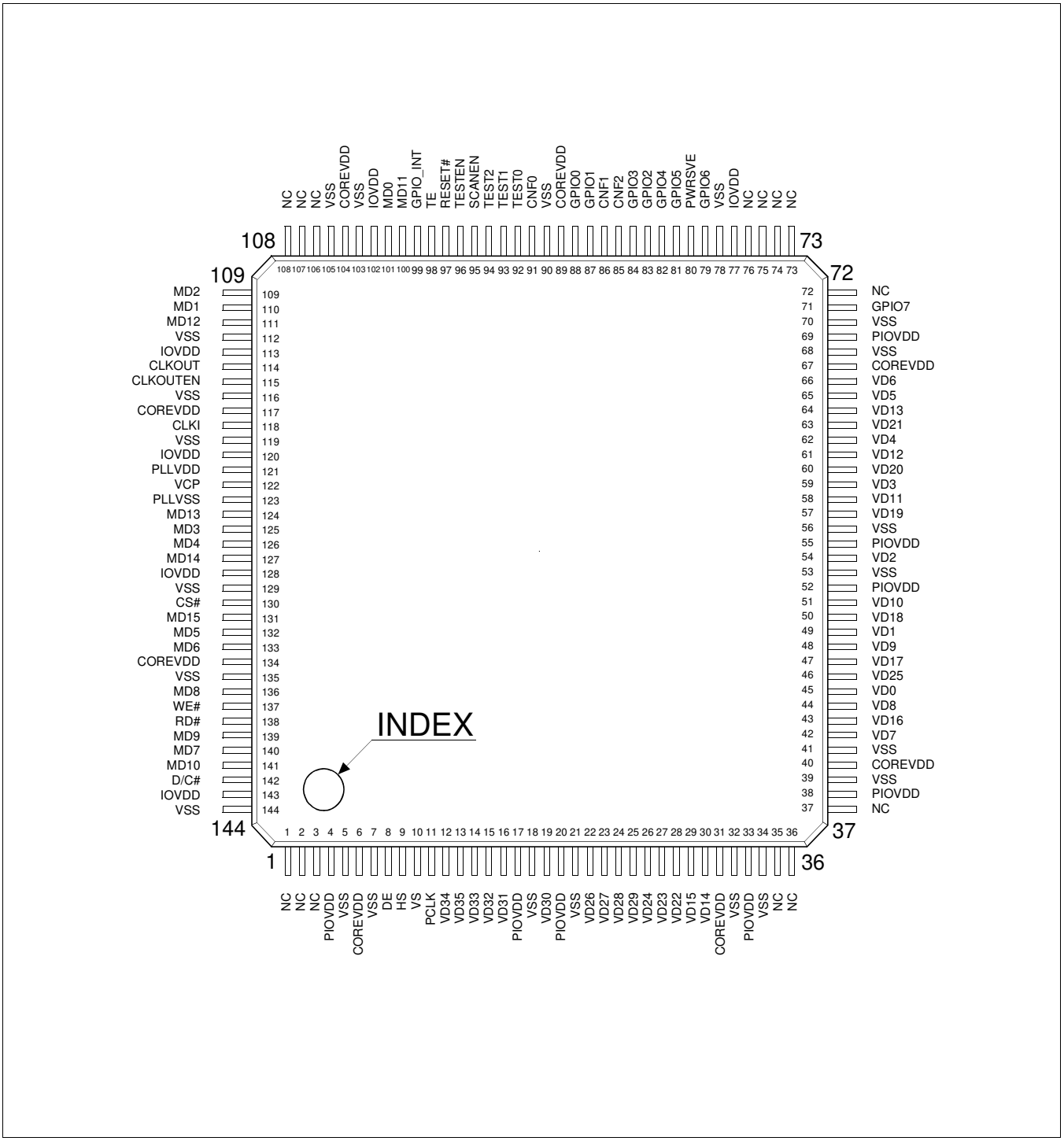

Figure 4-1: S1D13742 QFP20 Pinout (Top View)

4.2 Pin Descriptions

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin

RESET# / Power Save Status

H	=	High level output
L	=	Low level output
Hi-Z	=	High Impedance

Table 4-1: Cell Description

Item	Description
HI	H System[1] LVCMOS[3] Input Buffer
HIS	H System LVCMOS Schmitt Input Buffer
HID	H System LVCMOS Input Buffer with pull-down resistor
HO	H System LVCOMOS Output buffer
HB	H System LVCMOS Bidirectional Buffer
HBD	H System LVCMOS Bidirectional Buffer with pull-down resistor
HB_DSEL	H System LVCMOS Bidirectional Buffer with Drive Selector
LIDS	L System[2] LVCMOS Schmitt Input Buffer with pull-down resistor
LITR	L System Transparent Input Buffer

[1] H System is IOVDD and PIOVDD (see Section 6, “D.C. Characteristics”).
[2] L System is COREVDD (see Section 6, “D.C. Characteristics”).
[3] LVCMOS is Low Voltage CMOS (see Section 6, “D.C. Characteristics”).

4.2.1 Intel 80 Host Interface

Table 4-2: Host Interface Pin Descriptions

Pin Name	Type	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
MD[15:0]	IO	131,127, 124,111, 100,141, 139,136, 140,133, 132,126, 125,109, 110,101	HB	IOVDD	Hi-Z	Hi-Z	Intel 80 Data lines. • For the S1D13742B00, when the 8-bit bus interface is selected by CNF1, MD[15:8] are pulled low by internal resistors. • For the S1D13742B01, when the 8-bit bus interface is selected by CNF1, MD[15:8] should be connected to VSS. **Note:** The Host Data lines can be swapped (i.e. MD15 = MD0) using the CNF0 pin. For details, see Section 4.3, “Summary of Configuration Options” on page 17.
WE#	I	137	HI	IOVDD	Input	Input	This input pin is the Write Enable signal.
RD#	I	138	HI	IOVDD	Input	Input	This input pin is the Read Enable signal.
CS#	I	130	HI	IOVDD	Input	Input	This input pin is the Chip Select signal.
D/C#	I	142	HI	IOVDD	Input	Input	This input pin is used to select between Intel 80 address and data
TE	O	98	HO	IOVDD	L	L	Tearing Effect: this pin will reflect the VSYNC, HSYNC or the OR’d combination status of the display.
GPIO_INT	O	99	HO	IOVDD	L	Output	This interrupt pin is associated with selected GPIO pins when configured as inputs or outputs. Interrupt functionality is not affected by Power Save. See Section 9.3.10, “General Purpose IO Pins Registers” on page 71 for operational description.
RESET#	I	97	HI	IOVDD	Input	Input	Active low input to set all internal registers to the default state and to force all signals to their inactive states.

4.2.2 LCD Interface

Table 4-3: LCD Interface Pin Descriptions

Pin Name	Type	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
VD[35:0]	IO	13,12,14,15, 16,19,25,24, 23,22,46,26, 27,28,63,60, 57,50,47,43, 29,30,64,61, 58,51,48,44, 42,66,65,62, 59,54,49,45	HB_ DSEL	PIOVDD	L	L	Panel Data bits 35-0. VD[35:0] are used for all modes. In 2 pixels/clock mode, VD[17:0] represent the 1st pixel sent in a 2 pixel/clock operation. **Note:** The Panel Data Lines can be swapped (i.e. VD23 = VD0) using the VD Data Swap bit, REG[14h] bit 7. **Note:** The VD output drive is selectable between 2.5mA and 6.5mA using the CNF2 pin. For details, see Section 4.3, "Summary of Configuration Options" on page 17.
VS	O	10	HO	PIOVDD	H	L	This output pin is the Vertical Sync pulse
HS	O	9	HO	PIOVDD	H	L	This output is the Horizontal Sync pulse
PCLK	O	11	HO	PIOVDD	CLKI	L	This output pin is the Data Clock
DE	O	8	HO	PIOVDD	L	L	This output pin is the Data Enable

Note
The LCD interface requires a separate power rail (PIOVDD) to support the configurable IO drive. For details, see the CNF2 description in Section 4.3, "Summary of Configuration Options" on page 17.

Note
Input of VD[35:0] is used for production test only.

4.2.3 Clocks

Table 4-4: Clock Input Pin Descriptions

Pin Name	Type	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
CLKI	I	118	HIS	IOVDD	Input	Input	MHz input for PLL operation or MHz input if PLL is bypassed Input frequency range: 1MHz ~ 33MHz
CLKOUT	O	114	HO	IOVDD	L	CLKI	This output pin represents the CLKI pin if enabled by CLKOUTEN. When disabled the output is low. **Note:** this output is not affected by the various power save modes
CLKOUTEN	I	115	HI	IOVDD	Input	Input	This pin enables/disables the CLKOUT pin.

4.2.4 Miscellaneous

Table 4-5: Miscellaneous Pin Descriptions

Pin Name	Type	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
CNF[2:0]	I	85,86,91	HI	IOVDD	Input	Input	These inputs are used for power-up configuration. For details, see Section 4.3, "Summary of Configuration Options" on page 17. **Note: These pins must be connected directly to IOVDD or VSS.**
TESTEN	I	96	LIDS	IOVDD	—	—	Test Enable input used for production test only This pin should be left unconnected for normal use.
GPIO[7:0]	IO	71,79,81, 82,84,83, 87,88	HBD	IOVDD	L	Pull Down Active	These pins are general purpose input/output pins. These pins have internal pull-down resistors which can be controlled using REG[64h].
PWRSVE	I	80	HI	IOVDD	Input	Input	This pin enables/disables the Standby Power Save Mode When unused this pin must be connected to VSS.
TEST[2:0]	I	94,93,92	HID	IOVDD	—	—	These are Test Function pins and are used for production test only. These pins should be left unconnected for normal operation.
SCANEN	I	95	HID	IOVDD	—	—	This is the Test Scan Enable input and is used for production test only. This pin should be left unconnected for normal operation.
VCP	I	122	LITR	PLLVDD	—	—	This is the PLL VCP Test pin and is used for production test only. This pin should be left unconnected for normal operation.
NC	—	1,2,3, 35,36, 37,72, 73,74, 75,76, 106,107, 108	—	—	—	—	These pins are not connected.

4.2.5 Power And Ground

Table 4-6: Power And Ground Pin Descriptions

Pin Name	Type	QFP Pin #	Cell	Description
COREVDD	P	6,31,40,67,89, 104,117,134	P	Core power supply
IOVDD	P	77,102,113, 120,128,143	P	IO power supply for the host interface
PIOVDD	P	4,17,20,33,38, 52,55,69	P	IO power supply for the panel interface
PLLVDD	P	121	P	PLL power supply
PLLVSS	P	123	P	GND for PLL
VSS	P	5,7,18,21,32, 34,39,41,53, 56,68,70,78, 90,103,105, 112,116,119, 129, 135,144	P	GND

4.3 Summary of Configuration Options

These pins are used for power-up configuration and must be connected directly to IOVDD or VSS. The state of CNF[2:0] may be changed at any time.

Table 4-7: Summary of Power-On/Reset Options

Configuration Input	Power-On/Reset State	
	1 (connected to IOVDD)	0 (Connected to VSS)
CNF0	Host Data Lines are normal: If CNF1 = 1, then D15 = D15, etc. If CNF1 = 0, then D7 = D7, etc.	Host Data Lines are swapped: If CNF1 = 1, then D15 = D0, etc. If CNF1 = 0, then D7 = D0, etc.
CNF1	Host Data is 16-bit	Host Data is 8-bit
CNF2	PIOVDD output current (I_{OL2}) = 6.5mA	PIOVDD output current (I_{OL2}) = 2.5mA

Note

When CNF1=0, all Register access is 8-bit only.

When CNF1 =1 (16-bit): All Register access is 8-bit ONLY (the most significant byte on the data bus is ignored) except the Memory Data Port. Access to the Memory Data Port is 16-bit.

5 Pin Mapping

5.1 Intel 80 Data Pins

This function is controlled by CNF [1:0]

Table 5-1: S1D13742B00 Intel 80 Data Pin Mapping

Pin Name	16-Bit Data No Swap (CNF1=1, CNF0=1)	16-Bit Data Swapped (CNF1=1, CNF0=0)	8-Bit Data No Swap (CNF1=0, CNF0=1)	8-Bit Data Swapped (CNF1=0, CNF0=0)
MD15	MD15	MD0	Pulled Low by Internal Resistor	Pulled Low by Internal Resistor
• • •	• • •	• • •	• • •	• • •
MD8	MD8	MD7	Pulled Low by Internal Resistor	Pulled Low by Internal Resistor
MD7	MD7	MD8	MD7	MD0
• • •	• • •	• • •	• • •	• • •
MD0	MD0	MD15	MD0	MD7

Table 5-2: S1D13742B01 Intel 80 Data Pin Mapping

Pin Name	16-Bit Data No Swap (CNF1=1, CNF0=1)	16-Bit Data Swapped (CNF1=1, CNF0=0)	8-Bit Data No Swap (CNF1=0, CNF0=1)	8-Bit Data Swapped (CNF1=0, CNF0=0)
MD15	MD15	MD0	Hi-Z	Hi-Z
• • •	• • •	• • •	• • •	• • •
MD8	MD8	MD7	Hi-Z	Hi-Z
MD7	MD7	MD8	MD7	MD0
• • •	• • •	• • •	• • •	• • •
MD0	MD0	MD15	MD0	MD7

5.2 LCD Interface Pin Mapping

Table 5-3: LCD Interface Pin Mapping for Mode 1 and Mode 2

Pin Name	16bpp				18bpp			
	Single (18-bit)		Double (36-bit)		Single (18-bit)		Double (36-bit)	
	Normal	Swap	Normal	Swap	Normal	Swap	Normal	Swap
VS	Vertical Sync							
HS	Horizontal Sync							
PCLK	Pixel Clock							
DE	Data Enable							
VD0	B4	R4	B4	R4	B0	R5	B0	R5
VD1	B0	R3	B0	R3	B1	R4	B1	R4
VD2	B1	R2	B1	R2	B2	R3	B2	R3
VD3	B2	R1	B2	R1	B3	R2	B3	R2
VD4	B3	R0	B3	R0	B4	R1	B4	R1
VD5	B4	R4	B4	R4	B5	R0	B5	R0
VD6	G0	G5	G0	G5	G0	G5	G0	G5
VD7	G1	G4	G1	G4	G1	G4	G1	G4
VD8	G2	G3	G2	G3	G2	G3	G2	G3
VD9	G3	G2	G3	G2	G3	G2	G3	G2
VD10	G4	G1	G4	G1	G4	G1	G4	G1
VD11	G5	G0	G5	G0	G5	G0	G5	G0
VD12	R4	B4	R4	B4	R0	B5	R0	B5
VD13	R0	B3	R0	B3	R1	B4	R1	B4
VD14	R1	B2	R1	B2	R2	B3	R2	B3
VD15	R2	B1	R2	B1	R3	B2	R3	B2
VD16	R3	B0	R3	B0	R4	B1	R4	B1
VD17	R4	B4	R4	B4	R5	B0	R5	B0
VD18	driven 0	driven 0	B4	R4	driven 0	driven 0	B0	R5
VD19	driven 0	driven 0	B0	R3	driven 0	driven 0	B1	R4
VD20	driven 0	driven 0	B1	R2	driven 0	driven 0	B2	R3
VD21	driven 0	driven 0	B2	R1	driven 0	driven 0	B3	R2
VD22	driven 0	driven 0	B3	R0	driven 0	driven 0	B4	R1
VD23	driven 0	driven 0	B4	R4	driven 0	driven 0	B5	R0
VD24	driven 0	driven 0	G0	G5	driven 0	driven 0	G0	G5
VD25	driven 0	driven 0	G1	G4	driven 0	driven 0	G1	G4
VD26	driven 0	driven 0	G2	G3	driven 0	driven 0	G2	G3
VD27	driven 0	driven 0	G3	G2	driven 0	driven 0	G3	G2
VD28	driven 0	driven 0	G4	G1	driven 0	driven 0	G4	G1
VD29	driven 0	driven 0	G5	G0	driven 0	driven 0	G5	G0
VD30	driven 0	driven 0	R4	B4	driven 0	driven 0	R0	B5
VD31	driven 0	driven 0	R0	B3	driven 0	driven 0	R1	B4
VD32	driven 0	driven 0	R1	B2	driven 0	driven 0	R2	B3
VD33	driven 0	driven 0	R2	B1	driven 0	driven 0	R3	B2
VD34	driven 0	driven 0	R3	B0	driven 0	driven 0	R4	B1
VD35	driven 0	driven 0	R4	B4	driven 0	driven 0	R5	B0

5.3 LCD Interface Data Pins

This function is controlled by REG[14h] bit 7.

Table 5-4: LCD Interface Data Pin Mapping

Pin Name	36-Bit Data No Swap REG[14] b7=0	36-Bit Data Swapped REG[14] b7=1	18-Bit Data No Swap REG[14] b7=0	18-Bit Data Swapped REG[14] b7=1
VD35	VD35	VD0	Driven Low	Driven Low
• • •	• • •	• • •	• • •	• • •
VD18	VD18	VD17	Driven Low	Driven Low
VD17	VD17	VD18	VD17	VD0
• • •	• • •	• • •	• • •	• • •
VD0	VD0	VD35	VD0	VD17

6 D.C. Characteristics

6.1 Absolute Maximum Ratings

Table 6-1: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
Core V_{DD}	Core Supply Voltage	VSS - 0.3 ~ 2.0	V
PLL V_{DD}	PLL Supply Voltage	VSS - 0.3 ~ 2.0	V
IO V_{DD}	Host IO Supply Voltage	COREVDD ~ 4.0	V
PIO V_{DD}	Panel IO Supply Voltage	COREVDD ~ 4.0	V
V_{IN}	Input Signal Voltage	VSS - 0.3 ~ IOVDD + 0.3	V
V_{OUT}	Output Signal Voltage	VSS - 0.3 ~ IOVDD + 0.3	V
I_{OUT}	Output Signal Current	±10	mA

6.2 Recommended Operating Conditions

Table 6-2: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
Core V_{DD}	Core Supply Voltage	VSS = 0 V	1.40	1.50	1.60	V
PLL V_{DD}	PLL Supply Voltage	VSS = 0 V	1.40	1.50	1.60	V
IO V_{DD}	Host IO Supply Voltage	VSS = 0 V	1.65	—	3.6	V
PIO V_{DD}	Panel IO Supply Voltage	VSS = 0 V	1.65	—	3.6	V
V_{IN}	Input Voltage	—	VSS	—	IOVDD	V
T_{OPR}	Operating Temperature	—	-40	+25	+85	°C
T_{stg}	Storage Temperature	—	-65		+150	°C

Note

There are no special Power On/Off requirements with respect to sequencing the various VDD pins. There are also no special requirements for the IO signals, however Inputs should not be floating. If the input signals were to power up in a valid cycle, the S1D13742 would decode the cycle.

6.3 Electrical Characteristics

The following characteristics are for: IOVDD. VSS = 0V, T_{OPR} = -40 to +85°C.

Table 6-3: Electrical Characteristics for IOVDD or PIOVDD = 1.8V ± 0.15V

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{QALL}	Quiescent Current	CLKI stopped (grounded), Sleep Mode enabled, all power supplies active	—	100	—	µA
I_{PLL}	PLL Current	f_{PLL} = 54MHz	—	500	1000	µA
I_{CORE}	Operation Peak Current	COREVDD Power Pin	—	—	62	mA
P_{CORE}	Core Typical Operating Power	see Note 1	—	9.15	—	mW
P_{PLL}	PLL Typical Operating Power		—	0.7	—	mW
P_{PIO}	PIO Typical Operating Power		—	2.8	—	mW
P_{HIO}	HIO Typical Operating Power		—	0.018	—	mW
P_{CORE}	Core Typical Operating Power	see Note 2	—	10.9	—	mW
P_{PLL}	PLL Typical Operating Power		—	0.77	—	mW
P_{PIO}	PIO Typical Operating Power		—	2.124	—	mW
P_{HIO}	HIO Typical Operating Power		—	0.001	—	mW
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA
IOV_{OH2}	High Level Output Voltage	IOV_{DD} = min I_{OH2} = -2.5mA	IOVDD - 0.40	—	IOVDD	V
$PIOV_{OH2}$	High Level Output Voltage	PIOVDD = min I_{OH2} = -2.5mA	PIOVDD - 0.40	—	PIOVDD	V
$PIOV_{OH4}$	High Level Output Voltage	PIOVDD = min I_{OH2} = -6.5mA	PIOVDD - 0.40	—	PIOVDD	V
IOV_{OL2}	Low Level Output Voltage	IOVDD = min I_{OL2} = 2.5mA	VSS	—	0.40	V
$PIOV_{OL2}$	Low Level Output Voltage	PIOVDD = min I_{OL2} = 2.5mA	VSS	—	0.40	V
$PIOV_{OL4}$	Low Level Output Voltage	PIOVDD = min I_{OL2} = 6.5mA	VSS	—	0.40	V
IOV_{IH}	High Level Input Voltage	CMOS Input	1.27	—	—	V
$PIOV_{IH}$	High Level Input Voltage	CMOS Input	1.27	—	—	V
IOV_{IL}	Low Level Input Voltage	CMOS Input	—	—	0.57	V
$PIOV_{IL}$	Low Level Input Voltage	CMOS Input	—	—	0.57	V
IOV_{T+}	Positive Trigger Voltage	CMOS Schmitt	0.57	—	1.56	V
IOV_{T-}	Negative Trigger Voltage	CMOS Schmitt	0.33	—	1.27	V
IO V_H	Hysteresis Voltage	CMOS Schmitt	0.24	—	—	V
R_{PU1}	Pull-Up Resistance Type1	V_I = VSS	40	100	240	kΩ
R_{PD1}	Pull-Down Resistance Type1	V_I = VDD	40	100	240	kΩ
R_{PU2}	Pull-Up Resistance Type2	V_I = VSS	80	200	480	kΩ
R_{PD2}	Pull-Down Resistance Type2	V_I = VDD	80	200	480	kΩ
C_{IO}	Pin Capacitance	f = 1MHz, VDD = 0V	—	—	8	pF

Note

1. Typical Operating Current Environment:
   352x416 K2 TFT panel with PCLK divide by 4. SYSCLK=48.5MHz from PLL, PLL Source from 19.2MHz CLKI input. 18bpp memory storage.
   COREVDD and PLLVDD to 1.5V, HIOVDD, PIOVDD to 1.8V
2. Typical Operating Current Environment:
   800 x 480 TFT panel with PCLK divide by 3. SYSCLK= 59MHz from PLL, PLL Source from 12MHz CLKI input. 16bpp memory storage.
   COREVDD and PLLVDD to 1.5V, HIOVDD, PIOVDD to 1.8V

The following characteristics are for: IOVDD. VSS = 0V, T_{OPR} = -40 to +85°C.

Table 6-4: Electrical Characteristics for IOVDD or PIOVDD = 2.8V ± 0.14V

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{QALL}	Quiescent Current	CLKI stopped (grounded), Sleep Mode enabled, all power supplies active	—	120	—	µA
I_{PLL}	PLL Current	f_{PLL} = 54MHz	—	500	1000	µA
I_{CORE}	Operation Peak Current	COREVDD Power Pin	—	—	62	mA
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA
IOV_{OH2}	High Level Output Voltage	IOV_{DD} = min I_{OH2} = -3.6mA	IOVDD - 0.40	—	IOVDD	V
$PIOV_{OH2}$	High Level Output Voltage	PIOVDD = min I_{OH2} = -3.6mA	PIOVDD - 0.40	—	PIOVDD	V
$PIOV_{OH4}$	High Level Output Voltage	PIOVDD = min I_{OH2} = -10.8mA	PIOVDD - 0.40	—	PIOVDD	V
IOV_{OL2}	Low Level Output Voltage	IOVDD = min I_{OL2} = 3.6mA	VSS	—	0.40	V
$PIOV_{OL2}$	Low Level Output Voltage	PIOVDD = min I_{OL2} = 3.6mA	VSS	—	0.40	V
$PIOV_{OL4}$	Low Level Output Voltage	PIOVDD = min I_{OL2} = 10.8mA	VSS	—	0.40	V
IOV_{IH}	High Level Input Voltage	CMOS Input	1.75	—	—	V
$PIOV_{IH}$	High Level Input Voltage	CMOS Input	1.75	—	—	V
IOV_{IL}	Low Level Input Voltage	CMOS Input	—	—	0.70	V
$PIOV_{IL}$	Low Level Input Voltage	CMOS Input	—	—	0.70	V
IOV_{T+}	Positive Trigger Voltage	CMOS Schmitt	0.93	—	2.36	V
IOV_{T-}	Negative Trigger Voltage	CMOS Schmitt	0.53	—	1.92	V
IO V_H	Hysteresis Voltage	CMOS Schmitt	0.40	—	—	V
R_{PU1}	Pull-Up Resistance Type1	V_I = VSS	24	60	144	kΩ
R_{PD1}	Pull-Down Resistance Type1	V_I = VDD	24	60	144	kΩ
R_{PU2}	Pull-Up Resistance Type2	V_I = VSS	48	120	288	kΩ
R_{PD2}	Pull-Down Resistance Type2	V_I = VDD	48	120	288	kΩ
C_{IO}	Pin Capacitance	f = 1MHz, VDD = 0V	—	—	8	pF

Note

1. Typical Operating Current Environment:
   352x416 K2 TFT panel with PCLK divide by 4. SYSCLK=48.5MHz from PLL, PLL Source from 19.2MHz CLKI input. 18bpp memory storage.
   COREVDD and PLLVDD to 1.5V, HIOVDD, PIOVDD to 2.8V
2. Typical Operating Current Environment:
   800 x 480 TFT panel with PCLK divide by 3. SYSCLK= 59MHz from PLL, PLL Source from 12MHz CLKI input. 16bpp memory storage.
   COREVDD and PLLVDD to 1.5V, HIOVDD, PIOVDD to 2.8V

The following characteristics are for: IOVDD, VSS = 0V, T_{OPR} = -40 to +85°C.

Table 6-5: Electrical Characteristics for IOVDD or PIOVDD = 3.3V ± 0.3V

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{QALL}	Quiescent Current	Quiescent Conditions	—	160	—	µA
I_{PLL}	PLL Current	f_{PLL} = 54MHz	—	500	1000	µA
I_{CORE}	Operation Peak Current	COREVDD Power Pin	—	—	62	mA
I_{IZ}	Input Leakage Current	—	-5	—	5	µA
I_{OZ}	Output Leakage Current	—	-5	—	5	µA
IOV_{OH2}	High Level Output Voltage	IOV_{DD} = min I_{OH2} = -4.0mA	IOVDD - 0.40	—	IOVDD	V
$PIOV_{OH2}$	High Level Output Voltage	PIOVDD = min I_{OH2} = -4.0mA	PIOVDD - 0.40	—	PIOVDD	V
$PIOV_{OH4}$	High Level Output Voltage	PIOVDD = min I_{OH2} = -12.0mA	PIOVDD - 0.40	—	PIOVDD	V
IOV_{OL2}	Low Level Output Voltage	IOVDD = min I_{OL2} = 4.0mA	VSS	—	0.40	V
$PIOV_{OL2}$	Low Level Output Voltage	PIOVDD = min I_{OL2} = 4.0mA	VSS	—	0.40	V
$PIOV_{OL4}$	Low Level Output Voltage	PIOVDD = min I_{OL2} = 12.0mA	VSS	—	0.40	V
IOV_{IH}	High Level Input Voltage	CMOS Input	2.20	—	—	V
$PIOV_{IH}$	High Level Input Voltage	CMOS Input	2.20	—	—	V
IOV_{IL}	Low Level Input Voltage	CMOS Input	—	—	0.80	V
$PIOV_{IL}$	Low Level Input Voltage	CMOS Input	—	—	0.80	V
IOV_{T+}	Positive Trigger Voltage	CMOS Schmitt	1.40	—	2.70	V
IOV_{T-}	Negative Trigger Voltage	CMOS Schmitt	0.60	—	1.80	V
IO V_H	Hysteresis Voltage	CMOS Schmitt	0.45	—	—	V
R_{PU1}	Pull-Up Resistance Type1	V_I = VSS	20	50	120	kΩ
R_{PD1}	Pull-Down Resistance Type1	V_I = VDD	20	50	120	kΩ
R_{PU2}	Pull-Up Resistance Type2	V_I = VSS	40	100	240	kΩ
R_{PD2}	Pull-Down Resistance Type2	V_I = VDD	40	100	240	kΩ
C_{IO}	Pin Capacitance	f = 1MHz, VDD = 0V	—	—	8	pF

7 A.C. Characteristics

Conditions:

IOVDD = PIOVDD = 1.8V ± 0.15V or 2.8V ± 0.14V
T_A = -40° C to 85° C
T_{rise} and T_{fall} for all inputs except Schmitt and CLKI must be ≤ 50 ns (10% ~ 90%)
T_{rise} and T_{fall} for all Schmitt must be ≤ 5 ms (10% ~ 90%)
C_L = 8pF ~ 30pF (MD[15:0])
C_L = 15pF (TE, GPIO_INT, CLKOUT)
C_L = 30pF (LCD Panel/GPIO Interface)

7.1 Clock Timing

7.1.1 Input Clocks

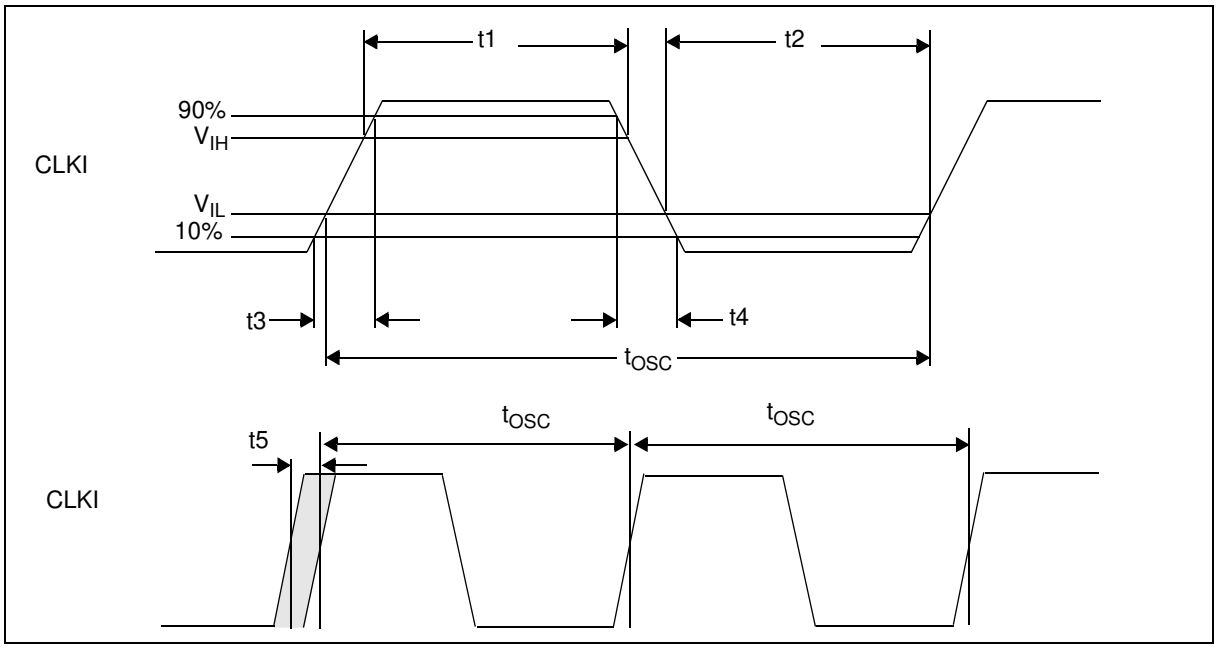

Figure 7-1 Clock Input Required (CLKI)