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S1D13746 TV Out Mobile Graphics Engine

Hardware Functional Specification

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Table of Contents

1 Introduction

1.1 Scope

This is the Hardware Functional Specification for the S1D13746, TV-Out Embedded Memory Mobile Graphics Engine. Included in this document are timing diagrams, AC and DC characteristics, register descriptions, and power management descriptions. This document is intended for two audiences: Video Subsystem Designers and Software Developers.

This document is updated as appropriate. Please check the Epson Research and Development Website at **www.erd.epson.com** for the latest revision of this document before beginning any development.

We appreciate your comments on our documentation. Please contact us via email at documentation@erd.epson.com.

1.2 Abbreviations and Acronyms

The following abbreviations and acronyms are used in this document:

All numbers are in decimal unless marked otherwise (b for binary, h for hexadecimal)
k = 2^{10} = 1024 when used with regards to memory
b = bit
B = Byte
bpp = bits-per-pixel
msb = Most Significant bit
lsb = Least Significant bit
IO = Input/Output
LUT = Look-Up Table
NC = No Connection
YYC = YUV to YUV Converter
YRC = YUV to RGB Converter
RYC = RGB to YUV Converter
VDP = Vertical Display Period
VNDP = Vertical Non-display Period
DDS = Digital Direct Synthesis
POUT = PLL Output

1.3 S1D13746 TV-Out Mobile Graphics Engine Family

The S1D13746 TV-Out Mobile Graphics Engine family currently includes the S1D13746B00 and the S1D13746B01/S1D13746F01. The following table describes the differences between these devices.

Table 1-1 S1D13746B0x Comparison

Device	Feature Differences
S1D13746B00	Base Design
S1D13746B01	All features of the S1D13746B00 plus: • GPIO interrupt and registers are asynchronous and fully functional in SLEEP mode. • Chrominance and Luminance filters for TV output improved from 11-TAP to 15-TAP to enhance Composite output. • Dot-Crawl elimination circuitry added for NTSC Composite mode. • Input and output scalers improved to provide sharper output image. • Input pre-scaler (decimation scaler) added to allow input image size of up to 3072x4092. • TV block changed to operate with flexible frequency range of 18MHz to 27MHz, and changed clock source for TV block to be selectable between CLKI/OSCI and PLL output divided by 2. This allows the possibility of running CLKI/OSCI from 1MHz to 54MHz range. • Square Pixel Correction Enable bit added to auto-scale the output window width to display square pixels. • Two more pin functions added to the TE (Tearing Effect) signal. • IO cells changed to Fail-Safe type. • Pull-Down resistor on the PWRSVE input removed.
S1D13746F01	All features of the S1D13746B01 in a QFP15 128-pin package.

2 Operational Overview

The S1D13746 is a Mobile Graphics Engine offering direct TV-output capability allowing for the display of multiple windows and orientations.

The S1D13746 contains a 312k byte display buffer. Input resolutions exceeding the memory space are automatically scaled down to fit. The final display output can be scaled-up and bordered to fit the standard TV resolutions as defined by PAL or NTSC.

TV output can be double-buffered to prevent image tearing during streaming video and also act as a frame-rate converter, allowing slow input video streaming while still maintaining PAL or NTSC output timing.

Input Data can come from a Host processor using an Intel 80 protocol or from a standard TFT display output (Parallel RGB Interface). The S1D13746 can be connected directly to a standard TFT display output. In this case, the registers are programmed using a Serial Interface and the S1D13746 converts the TFT output data appropriately for display on a TV.

All image data uses the Input/Output Window Size/Position registers and is accesses using the Display Memory Data Port. Subsequent windows are considered destructive overlays. Each window can have independent rotation and position characteristics.

The S1D13746 is designed to accept DMA burst accesses from an Intel 80 CPU interface. All accesses to the display buffer are handled through a Display Memory Data Port.

2.1 TV Support

The S1D13746 conforms to both the PAL and NTSC output standards with respect to resolution and output format. Both Composite and S-Video outputs formats are supported. The S1D13746 supports multiple RGB, YUV 4:2:2 and YUV 4:2:0 input formats. All data is converted and stored as YUV 4:2:0.

2.1.1 Writing Window Data

Window data can either be written by a Host processor via the Intel 80 Interface or input by the Parallel RGB Interface. For the Intel 80 processor, the windows can vary in size, For the Parallel RGB Interface, the window size is automatically determined by the horizontal and vertical input timings.

2.1.2 Scaling Features

- Host Input Data can be scaled-down to fit within the available memory.
  - The Input Scaler logic requires an input size, either programmed by the Host or calculated automatically if using the Parallel RGB Interface. The available memory is either the entire display buffer (312k bytes) or 156k bytes if the double buffer feature is enabled. The required scaling ratio from Input Size to memory is automatically calculated.
- Memory Output Data (intended for display on the TV) can be scaled-up for display on the TV (Display Output Scaler).
  - if the resulting scale-up does not equal full resolution as defined by the PAL or NTSC standards, then an automatic border is generated and the resulting image is centered within the border.
  - If displaying multiple images on the TV, the initial background image determines both the Scale-down ratio to memory and the Scale-up ratio to the display. These ratios are used by all other windows.
  - If displaying multiple images on the TV, all subsequent windows are referenced to the top-left of the (auto-centered) background image for position.

2.1.3 Window Rotation

SwivelView™ provides 90°, 180°, 270° counter-clockwise hardware rotation of the image window as written by the host. All windows can have independent rotation when writing to memory. No additional programming is necessary when enabling these modes.

2.1.4 Multiple TV Windows

Multiple “windows” can be destructively written to the TV display. If multiple windows are required, the first window written is considered the “background”. All subsequent windows are stored in memory “on-top” of the background image and are therefore considered destructive.

Multiple TV Windows with Transparency

Any destructive window can have a transparent color associated with it. Only those pixels that are not transparent are actually written to memory. The window is first scaled-down (if necessary) to fit in memory. After the scaler the pixels are compared to the 24-bit YUV value programmed for the transparent color.

There are three modes in which to use the transparent feature.

1. Normal Mode: if the resulting scaled pixels equal the transparent color, they are not written to memory. In this mode there will be color artifacts surrounding the non-transparent color.

2. Black/White Mode: in this mode, the transparent color is limited to black or white with the visible color being the opposite. In this mode any color artifacts are minimized by forcing all pixels to be either transparent or not.

3. Text Mode: in this mode, the transparent color intensity range calculated from the Transparency Color Registers determines if the pixel is transparent or not. This mode is similar to Black/White mode with the effect of removing more color artifacts.

2.1.5 Single TV Window

If only a single window is required, The S1D13746 can scale-down the input data to fit within the memory, scale-up for display on the TV, auto-center and Auto Border if the final output is not full screen.

2.1.6 TV Window Border Support

S1D13746 automatically generates a programmable border color around a window where the resulting image size (after scale-up) does not equal the TV output resolution (PAL or NTSC). The window is centered within the border.

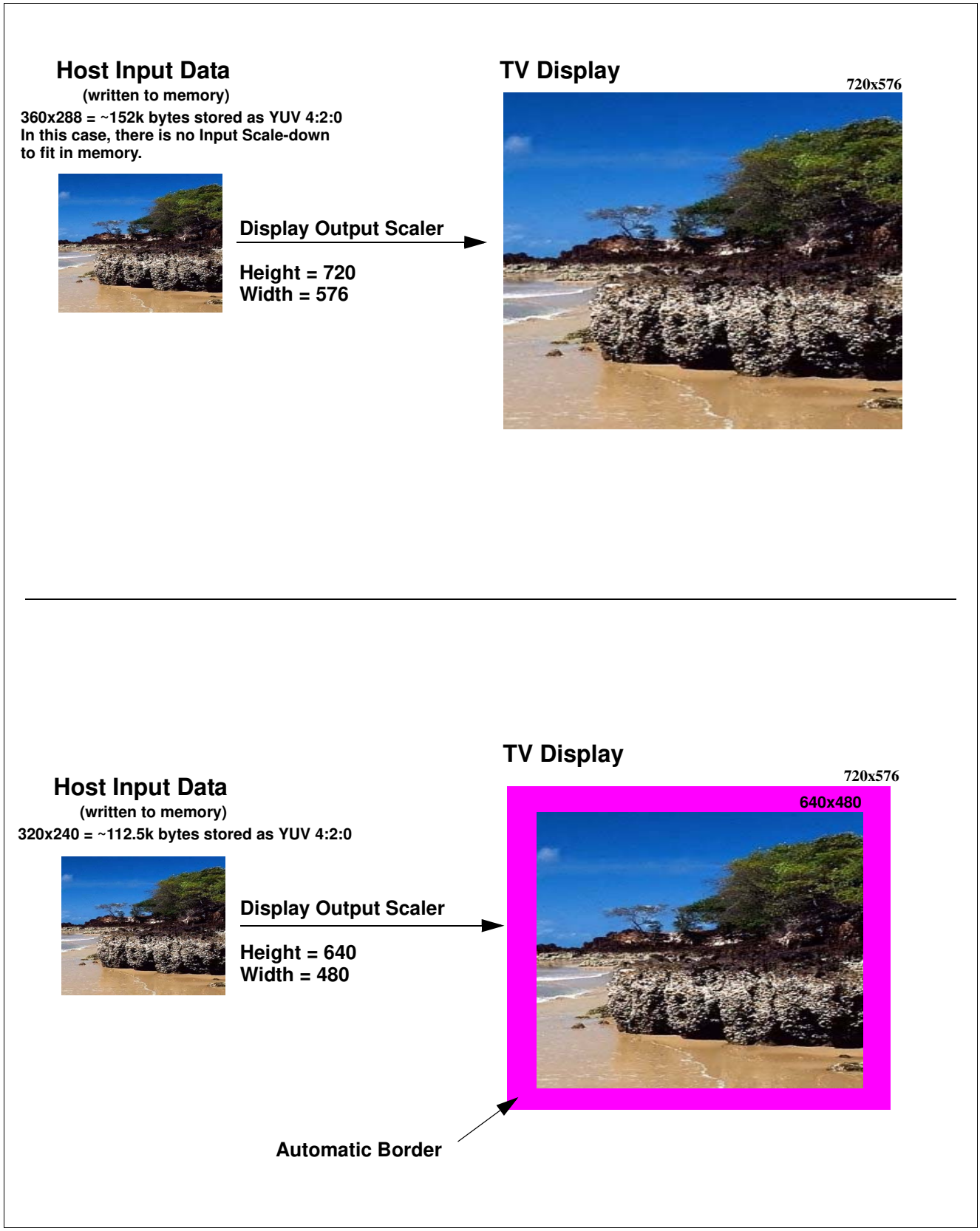
2.1.7 Double Buffered TV Window

A single TV window can be double buffered to prevent any visual tearing from a streaming input. This window can be the entire screen resolution or a just a portion.

When configuring a window for streaming video, the S1D13746 automatically double buffers the input data based on the window coordinates. If this window is only a portion of the screen, Buffer #1 is used for the “background” static portion and one of the buffered windows data. Buffer #2 is used only for the other double buffered window data and does not contain any static data from the background.

Interrupting a streaming window to update static information on the screen is permitted since the TV display pipe only uses data from a buffer that has been completely written. Therefore, a single buffer may be repeatedly displayed until the next buffer is ready. If the display pipe is currently using Buffer #2 when the Double Buffer is disabled, the display pipe reverts to using Buffer #1 since it is the only buffer containing the background information. Double-buffering supports the maximum resolutions as defined by the PAL and NTSC standard.

When Double Buffering is enabled, the memory is split into 2 banks of 156k bytes and the scale ratio from the input image to memory is increased to allow the image to fit inside 1/2 the previously available memory.


Host Input Data
(written to memory)
360x288 = ~152k bytes stored as YUV 4:2:0
In this case, there is no Input Scale-down
to fit in memory.
Display Output Scaler
Height = 720
Width = 576
TV Display
720x576
Host Input Data
(written to memory)
320x240 = ~112.5k bytes stored as YUV 4:2:0
Display Output Scaler
Height = 640
Width = 480
TV Display
720x576
640x480
Automatic Border

Host Input Data

(written to memory, Single Buffered)

720x576 = 607.5k bytes @ 4:2:0

Scaled-down to fit inside 312k bytes

514x412 = ~310k bytes @ 4:2:0

Host Input Data

(written to memory)

720x576

514x412 = ~312k bytes @ 4:2:0

Scaled-down to fit inside 312k bytes

Host Input Data (destructive window)

352x416

Scaled-down to fit inside background image

720x576

Memory Output Data

Scaled-up and Bordered

Host Input Data
(written to memory)

Scaled-down to fit inside 312k bytes

Host Input Data
(transparency enabled = black)

720x576

Memory Output Data

Scaled-up and Bordered

3 Features

3.1 Integrated Display Buffer

- Embedded 312k byte SRAM display buffer.

3.2 CPU Interface

- 8/16-bit Intel 80 interface (used for display or register data).
- Parallel RGB Interface (display data only).
- Three Wire Serial Interface (register data only).
- Chip select is used to select the S1D13746. When inactive, input data/commands are ignored.

3.3 Input Data Formats

- RGB: 8:8:8, 6:6:6, 5:6:5, 3:3:2.
  - all RGB input data is converted and stored as YUV 4:2:0.
- YUV: 4:2:2, 4:2:0.
  - all YUV input data is converted and stored as YUV 4:2:0.

3.4 TV Display Support

- Composite Output for both PAL and NTSC TV standards.
- S-Video Output for both PAL and NTSC TV standards.
- Programmable 15-tap Chrominance / Luminance Filters.
- Wide-Screen Signalling support (ITU-R BT.1119-2, ETSI EN 300 294, IEC 61880, compliant).
- Closed Caption Support (CEA-608-B).

3.5 TV Display Features

- Input Data can:
  - be scaled-down to fit within available memory
  - be rotated.
  - have an associated transparent color
- Memory Output Data can be scaled-up for display on the TV
- TV image is automatically “bordered” to fit the output resolution, if not scaled to fit.
  - programmable YUV border color
  - auto-center
  - independent aspect ratio is available for Display Output Height/Width scaling factors
- Square pixel correction output width scaling

3.6 Image Enhancement Engine

- 3x3 Pixel Filter
- User defined coefficients
  - individual control for each YUV component
- Display effects include:
  - smooth, sharpen, blur, detail, edge enhance, emboss, contour, flicker filter, sepia

3.7 Clock Source

- Internal programmable PLL
- Single oscillator input: CLKI (determined by CNF2)

or

- Two-terminal Crystal support: OSCI, OSCO (determined by CNF2)

Note
An 18MHz to 27MHz clock is required by internal TV DDS logic in order to derive appropriate PAL and NTSC output timings. For any clock source other than 27MHz, the PLL should be programmed for 54MHz.

- CLKI available as CLKOUT (separate CLKOUTEN pin associated with output)
  - output state = 0 when disabled

3.8 Miscellaneous

- Hardware / Software Power Save mode
  - Input pin to Enable/Disable Power Save Mode
- General Purpose Input/Output pins are available (GPIO[7:0])
  - INT pin associated with selectable GPIO inputs
- Package:

S1D13746B01B	PFBGA 100 pin (7mm x 7mm)
S1D13746F01A	QFP15 128 pin

4 Block Diagram

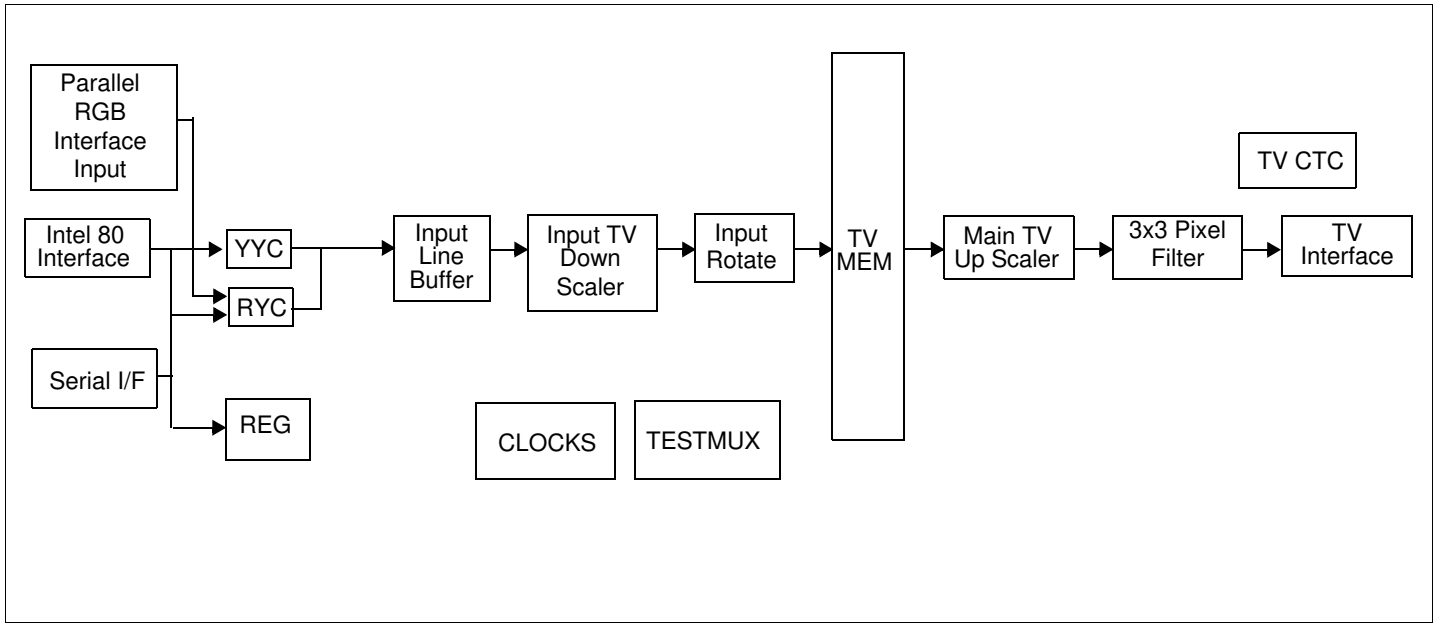


Figure 4-1: S1D13746 Block Diagram

5 Pinout

5.1 Package Pin Mapping

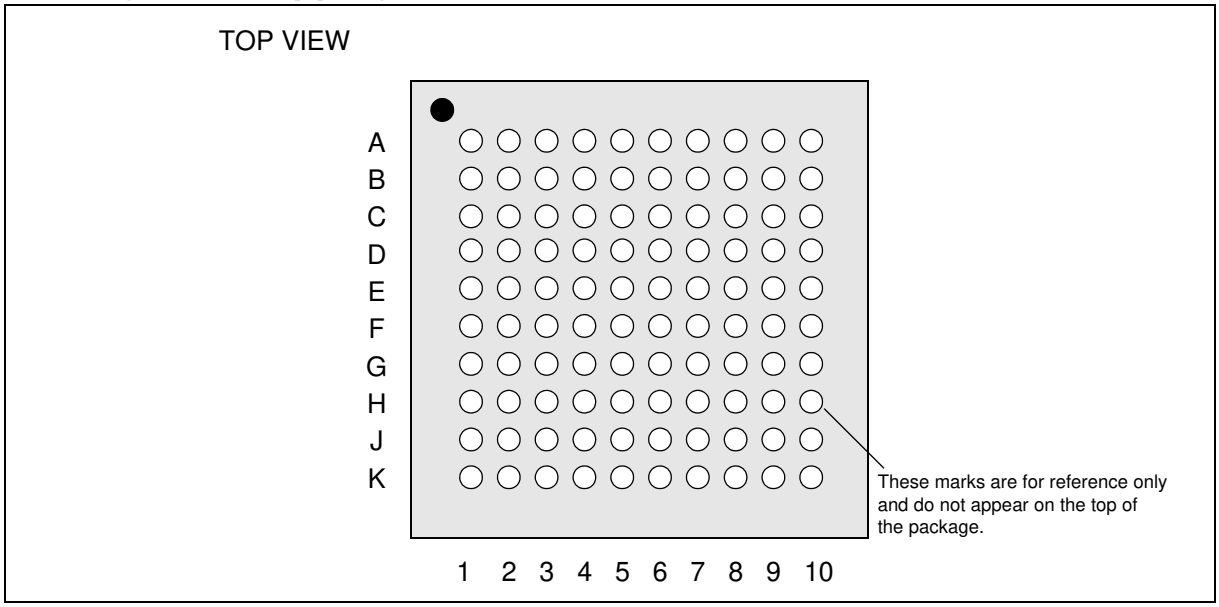


Figure 5-1: S1D13746 PFBGA 100-pin Pinout Diagram (Top View)

Table 5-1: S1D13746 PFBGA 100-pin Pinout (Top View)

	1	2	3	4	5	6	7	8	9	10
A	NC	COREVDD	SCLK	SO	SI	VSS	PCLK	DE	VSS	NC
B	PWRSVE	TESTEN	GPIO7	CS#	GPIO1	GPIO0	TE	D/C#	COREVDD	MD15
C	SCANEN	TEST0	GPIO6	GPIO5	GPIO2	GPIO_INT	GPIO4	WE#	VSS	MD13
D	DACVEE	DACVCC	TEST2	SIOVDD	GPIO3	RESET#	IOVDD	MD11	MD12	MD9
E	BOUT	DACVCC	DACVEE	TEST1	CNF0	RD#	MD10	MD8	MD7	MD6
F	DACVEE	VADJ	DACVCC	VSS	CNF1	IOVDD	MD14	MD5	MD4	MD3
G	DACVEE	VREF	DACVEE	VSS	CNF3	CNF2	MD0	MD1	MD2	COREVDD
H	AOUT	DACVCC	DACVCC	VSS	VSS	IOVDD	VSS	IOVDD	CLKOUTEN	CLKOUT
J	DACVEE	DACVEE	DACVCC	IOVDD	COREVDD	OSCVSS	OSCVDD	VCP	VSS	CLKI
k	NC	NC	DACVEE	VSS	VSS	OSCI	OSCO	PLLVDD	PLLVSS	NC

Note

Pins marked as NC are not used and must be left unconnected.

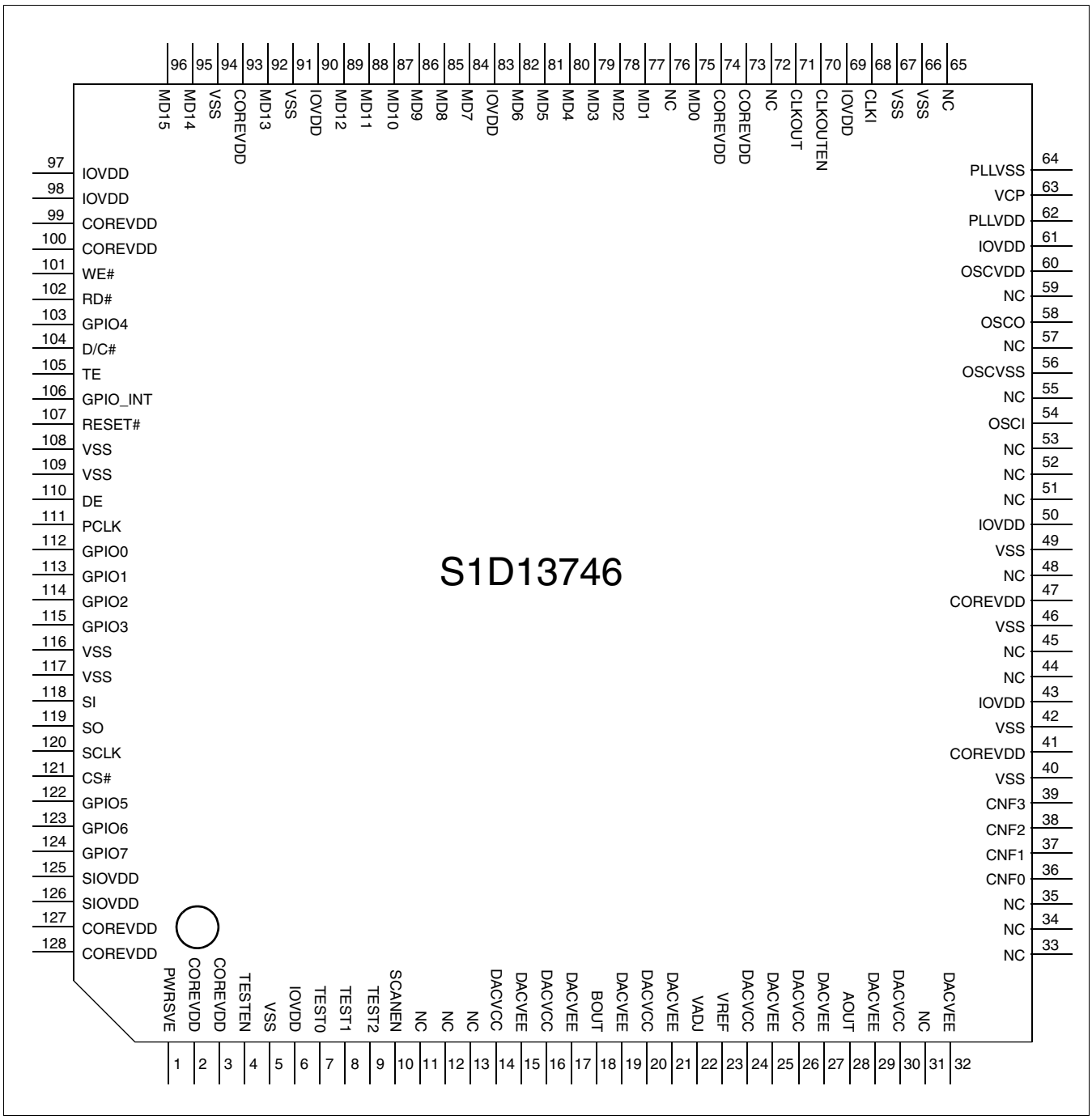


Figure 5-2: S1D13746 QFP15 128-pin (Top View)

Note

Pins marked as NC are not used and must be left unconnected.

5.2 Pin Descriptions

Key:

Pin Types

I	=	Input
O	=	Output
IO	=	Bi-Directional (Input/Output)
P	=	Power pin
AP	=	Analog power pin
G	=	Ground pin
AG	=	Analog ground pin

RESET# / Power Save Status

H	=	High level output
L	=	Low level output
Hi-Z	=	High Impedance

Table 5-3 Cell Description

Item	Description
HI	H System[1] LVCMOS[3] Input Buffer with Fail Safe
HIS	H System LVCMOS Schmitt Input Buffer with Fail Safe
HID	H System LVCMOS Input Buffer with pull-down resistor and Fail Safe
HO	H System LVCOMOS Output buffer with Fail Safe
HB	H System LVCMOS Bidirectional Buffer with Fail Safe
HBD	H System LVCMOS Bidirectional Buffer with pull-down resistor and Fail Safe
LIDS	L System[2] LVCMOS Schmitt Input Buffer with pull-down resistor
LITR	L System Transparent Input Buffer
LOTR	L System Transparent Output Buffer
AIO	Analog

[1] H System is IOVDD and PIOVDD (see Section 7, “D.C. Characteristics” on page 31).
[2] L System is COREVDD (see Section 7, “D.C. Characteristics” on page 31).
[3] LVCMOS is Low Voltage CMOS (see Section 7, “D.C. Characteristics” on page 31).

5.2.1 Intel 80 Host Interface

Table 5-2: Host Interface Pin Descriptions

Pin Name	Type	PFBGA Pin #	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
MD[15:0]	IO	B10, F7, C10, D9, D8, E7, D10, E8, E9, E10, F8, F9, F10, G9, G8, G7	96, 95, 92, 89, 88, 87, 86, 85, 84, 82, 81, 80, 79, 78, 77, 75	HB	IOVDD	Hi-Z	Hi-Z	This pin has multiple functions. • For the Intel 80 Interface these pins are the data lines MD[15:0], see Section 6.1, “Intel 80 Data Pins” on page 30. • For the Parallel RGB Interface these pins are the input data bits VD[17:2], see Section 6.2, “Parallel RGB Data Pins” on page 30
WE#	I	C8	101	HI	IOVDD	—	—	This pin has multiple functions. • For the Intel 80 Interface this input pin is the Write Enable signal (WE#) • For the Parallel RGB Interface this input pin is the data bit 1 (VD1)
RD#	I	E6	102	HI	IOVDD	—	—	This pin has multiple functions. • For the Intel 80 Interface this input pin is the Read Enable signal • For the Parallel RGB Interface this input pin is the data bit 0 (VD0)
CS#	I	B4	121	HI	SIOVDD	—	—	This input pin is the Chip Select signal for both the Intel 80 Host Interface as well as the Serial Interface.
D/C#	I	B8	104	HI	IOVDD	—	—	This pin has multiple functions. • For the Intel 80 Interface this input pin selects between address and data (D/C#) • For the Parallel RGB Interface this input pin is the Horizontal Sync (HS)
TE	IO	B7	105	HB	IOVDD	L	L	This pin has multiple functions. • For the Intel 80 Interface this pin is Tearing Effect. This pin reflects the VSYNC status of the display and can be used to indicate when it is safe to write new data from the Host in order to prevent visual tearing of an image. • For the Parallel RGB Interface this input pin is the Vertical Sync (VS)
PCLK	I	A7	111	HIS	IOVDD	—	—	This input pin is the Parallel RGB Interface PCLK input. If the Parallel RGB Interface is not used (CNF[1:0] = 01b or 11b) this pin should be connected to VSS.
DE	I	A8	110	HI	IOVDD	—	—	This input pin is the Parallel RGB Interface DE input. If the Parallel RGB Interface is not used (CNF[1:0] = 01b or 11b) this pin should be connected to VSS.

Table 5-2: Host Interface Pin Descriptions (Continued)

Pin Name	Type	PFBGA Pin #	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
GPIO_INT	O	C6	106	HO	IOVDD	L	L	This pin is the interrupt output associated with GPIO pins when they are configured as inputs. When a GPIO interrupt occurs, this output pin is driven high. For details see the register descriptions for REG[F0h] ~ REG[FAh], in Section 11.3.9, “General Purpose IO Pins Registers” on page 117
RESET#	I	D6	107	HIS	IOVDD	—	—	This active low input sets all internal registers to the default state and forces all signals to their inactive states.

5.2.2 Serial Peripheral Interface (SPI)

Table 5-3: SPI Pin Descriptions

Pin Name	Type	PFBGA Pin #	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
SO	IO	A4	119	HB	SIOVDD	Hi-Z	Hi-Z	This pin is the Serial Output. If the serial interface is not used (CNF[1:0] = 01b or 11b), this pin should be connected to either SIOVDD or VSS through a resistor .
SI	I	A5	118	HI	SIOVDD	—	—	This pin is the Serial Input. If the serial interface is not used (CNF[1:0] = 01b or 11b), this pin should be connected to VSS.
SCLK	I	A3	120	HIS	SIOVDD	—	—	This pin is the Serial Clock. If the serial interface is not used (CNF[1:0] = 01b or 11b), this pin should be connected to VSS.

5.2.3 TV Interface

Note
If unused, these pins should be left unconnected.

Table 5-4: TV Interface Pin Descriptions

Pin Name	Type	PFBGA Pin #	QFP Pin #	Cell	IO Voltage	RESET# State	Power Save Status	Description
AOUT, BOUT	O	H1, E1	28, 18	AIO	DAC	—	—	These are the TV analog output pins. The TV outputs are designed to drive a double terminated 75Ω load (37.5 ohms). For further details, see Section 24.1, “DAC External Components” on page 184. When using Composite Video, AOUT is used and BOUT is left unconnected. When using S-Video, AOUT is the luminance signal and BOUT is the chrominance signal.
VREF	IO	G2	23	AIO	DAC	—	—	This input/output pin is the reference voltage for the DAC. The VREF Enable bit (REG[9Eh] bit 0) is used to determine whether external or internal VREF mode is selected. When REG[9Eh] bit 0 = 0b, external VREF mode is selected and 1.23 volts should be applied to this pin. When REG[9Eh] bit 0 = 1b, internal VREF mode is selected and this pin can be used during testing to confirm the output level is 1.23V. However, for normal operations, this pin should be left unconnected.
VADJ	IO	F2	22	AIO	DAC	—	—	This input/output is the reference current generation pin for the DAC. Connect a 2.06kΩ resistor (Rset) between VADJ and DACVEE. For further details, see Section 24.1, “DAC External Components” on page 184. When the IREF Enable bit = 0b (REG[9Eh] bit 1 = 0b), the internal generation of the reference current is disabled, and VADJ does not control reference current. There should be no problems with leaving the resistor connected.