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EPSON

S1F75510

Charge-pump DC/DC Converter & Voltage Regulator

Preliminary

■ DESCRIPTION

The S1F75510 is a power IC designed for use with medium or small capacity TFT–LCD panel modules.
A single chip of this IC is capable of generating three different levels of positive and negative output voltages simultaneously, which are necessary to drive the LCD, by use of a single input power of +2.7 through +3.6V.
Since the S1F75510 does not require external transistors nor diodes as its voltage conversion circuit, its built-in CMOS transistors constituting a complete charge pump type DC/DC converter, it is most suitable for the purpose of reducing the current consumption levels of the LCD modules.
Moreover, the charge pump type DC/DC converter of the S1F75510 can be operated upon the frequencies, which are to be switched over by the mode changing signals, using either of the built-in clock signals or external clock signals optimal to respective cases.
This function can drastically suppress the current consumption of this IC while under light load state, thus exhibiting very high power conversion efficiencies.

■ FEATURES

- Supply voltage ····· 2.7V to 3.6V single power input
- Self consumption current (normal mode/blank mode) ···· 300μA / 30μA (TBD)
  Normal mode: Boosting by use of the internal clock
  Blank mode: Selectable between boosting by use of the internal clock or by use of the external clock.
- Conversion efficiency of the charge pump ····· 90% or more respectively
- Built-in voltage conversion circuits constituted by charge pump type DC/DC converter,
  - ×2 boosting circuit in the positive direction
  - ×3 boosting circuit in the positive direction
  - ×3 boosting circuit in the negative direction
- Built-in voltage stabilizing circuit
- Capable of outputting the positive supply voltage V_{OUT2} for the source driver
  - ×2 boosting circuit in the positive direction + voltage stabilizing circuit
    Output voltage: +5.0V ±3% (TBD)
- Capable of outputting the positive supply voltage V_{OUT3} for the gate driver
  - ×3 boosting circuit in the positive direction
    Output voltage: +15V
    $V_{OUT3} = V_{OUT2} \times 3$
- Capable of outputting the negative supply voltage V_{OUT4} for the gate driver
  - ×3 boosting circuit in the negative direction
    Output voltage: –10V
    $V_{OUT4} = V_{OUT2} \times -2$
- Built-in electric charge discharging circuit
- Built-in shut down function
- Shipping state ····· SSOP3–24pin
- This IC is not of the radiation resistant design nor of the light resistance design.

■ BLOCK DIAGRAM

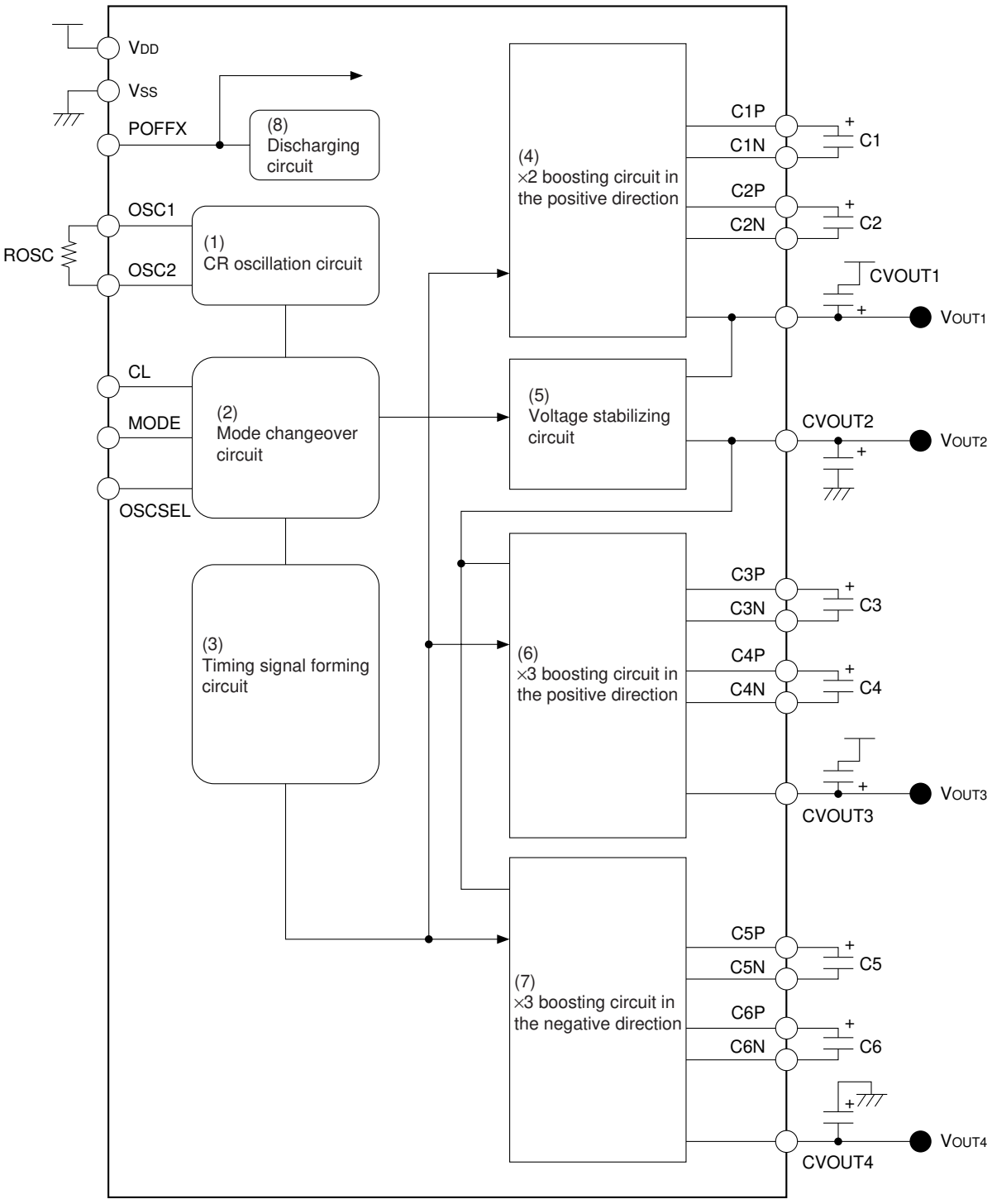


Fig. 1 Block diagram

■ DESCRIPTIONS FOR THE BLOCK DIAGRAM

(1) CR oscillation circuit

The oscillation circuit is constituted by connecting a resistor between the OSC1 pin and the OSC2 pin. The clock signals being generated by this oscillation circuit will become effective as boosting clock signals while the mode changeover signal MODE is on the V_{DD} level (normal mode) or while the mode changeover signal MODE is on the V_{SS} level and, at the same time, when the internal/external clock selection signal OSCSEL is on the V_{DD} level (blank mode · internal clock). When the MODE is set to the V_{SS} level and, at the same time, when the OSCSEL is set to the V_{SS} level (blank mode · external clock), the oscillation will be interrupted.

(2) Mode changeover circuit

The operation modes of the boosting circuit and voltage stabilizing circuit are being switched over by the mode changeover signal MODE. Also, it selects the clock signals to feed to the timing signal forming circuit from either of the external clock signals or internal clock signals.

(3) Timing signal forming circuit

This circuit generates the charge pump boosting clock signals. This circuit outputs timing signals of the clock type (internal clock or external clock) having been selected by the mode changeover circuit to drive respective boosting circuits. When the shut down signal POFFX is set to the V_{SS} level, the timing signal stops to interrupt the boosting operation.

(4) ×2 boosting circuit in the positive direction

This circuit makes ×2 boosting in the positive direction by charge pump boosting upon the inputted supply voltage $V_{DD} – V_{SS}$ using the V_{SS} potential as the reference voltage. The ×2 boosted output will enter into the voltage stabilizing circuit.

(5) Voltage stabilizing circuit

This circuit generates the positive supply voltage V_{OUT2} for the source driver. ON the basis of the built-in reference, this circuit stabilizes the output from the above "(4) ×2 boosting circuit in the positive direction" by use of the series regulator.

(6) ×3 boosting circuit in the positive direction

This circuit generates the positive supply voltage V_{OUT3} for the gate driver. This circuit effects ×3 boosting in the positive direction by charge pump boosting upon the voltage $V_{OUT2} – V_{SS}$ using the V_{SS} potential as the reference voltage.

(7) ×3 boosting circuit in the negative direction

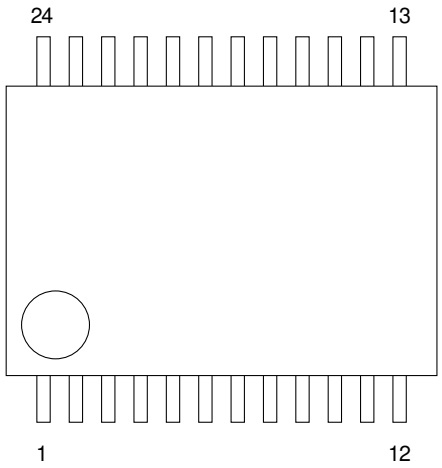
This circuit generates the negative supply voltage V_{OUT4} for the gate driver. This circuit effects ×3 boosting in the negative direction by charge pump boosting upon the voltage $V_{OUT2} – V_{SS}$ using the V_{OUT2} potential as the reference voltage.

(8) Electric charge discharging circuit

This circuit discharges the electric charge remaining in the V_{OUT3} pin and V_{OUT4} pin to the V_{SS} level. This circuit will work when the POFFX pin is set to the V_{SS} level.

■ PIN ASSIGNMENT

SSOP3–24pin S1F75510M0A0



Pin No.	Pin name	Pin No.	Pin name
1	C3N	13	MODE
2	C3P	14	CL
3	C4P	15	POFFX
4	C4N	16	OSC1
5	V_{OUT3}	17	OSC2
6	V_{DD}	18	OSCSEL
7	C1N	19	V_{OUT2}
8	C1P	20	V_{OUT4}
9	V_{OUT1}	21	C6P
10	C2P	22	C6N
11	C2N	23	C5N
12	V_{SS}	24	C5P

■ PIN DESCRIPTION

(1) CR oscillation circuit · Mode changeover circuit · Timing signal forming circuit · Electric charge discharging circuit

<table>
<tr><th>Pin name</th><th>I/O</th><th>Pin No.</th><th>Function</th></tr>
<tr><td>POFFX</td><td>I</td><td>15</td><td>This is the shut down pin. Set it to the VDD level while the IC is in operation. When this signal is set to the VSS level, operations of all the circuits will be interrupted bringing the IC into the shut down state. The electric charge discharging circuit discharges the electric charge remaining in the VOUT3 pin and VOUT4 pin to the VSS level.</td></tr>
<tr><td>OSC1</td><td>I</td><td>16</td><td>This is the CR oscillation circuit gate input pin. This is the pin to connect the oscillation resistor. Fix it to the VSS level in case the built-in oscillation circuit will not be used.</td></tr>
<tr><td>OSC2</td><td>O</td><td>17</td><td>This is the CR oscillation circuit drain input pin. Connect the oscillation resistor between this pin and the OSC1 pin.</td></tr>
<tr><td>CL</td><td>I</td><td>14</td><td>This is the boosting external clock signal input pin. Input the charge pump clock signals under the blank mode into this pin.</td></tr>
<tr><td>MODE
OSCSEL</td><td>I
I</td><td>13
18</td><td>This is the mode changeover pin.
This is the pin for selection between the internal clock and external clock signals.
<table>
<tr><th>MODE</th><th>OSCSEL</th><th>Function</th></tr>
<tr><td>HIGH(VDD)</td><td>HIGH(VDD)</td><td>Normal mode</td></tr>
<tr><td></td><td>LOW(VSS)</td><td>The boosting clock signals are being generated through the internal oscillation.
The built-in oscillation circuit will operate and the voltage stabilizing circuit will operate.</td></tr>
<tr><td>LOW(VSS)</td><td>HIGH(VDD)</td><td>Blank mode (internal oscillation)
The boosting clock signals are being generated through the internal oscillation.
The built-in oscillation circuit will operate and the voltage stabilizing circuit will operate under low current consumption state.</td></tr>
<tr><td></td><td>LOW(VSS)</td><td>Blank mode (external oscillation)
The boosting clock signals are being generated by the external clock.
The built-in oscillation circuit will be interrupted and the voltage stabilizing circuit will operate under low current consumption state.</td></tr>
</table></td></tr>
</table>

(2) ×2 boosting circuit in the positive direction

Pin name	I/O	Pin No.	Function
V_{OUT1}	O	9	This is the output pin of the ×2 boosting circuit in the positive direction.
C1P	(O)	8	This is the pin to connect the positive side of the V_{OUT1} output voltage generating flying capacitor C1.
C1N	(O)	7	This is the pin to connect the negative side of the V_{OUT1} output voltage generating flying capacitor C1.
C2P	(O)	10	This is the pin to connect the positive side of the V_{OUT1} output voltage generating flying capacitor C2.
C2N	(O)	11	This is the pin to connect the negative side of the V_{OUT1} output voltage generating flying capacitor C2.

(3) Voltage stabilizing circuit

Pin name	I/O	Pin No.	Function
V_{OUT1}	I	9	This is the input power pin (+) for the voltage stabilizing circuit. This pin is being connected to the output pin of the ×2 boosting circuit in the positive direction internally, inside this IC.
V_{OUT2}	O	19	This is the output pin of the voltage stabilizing circuit.

(4) ×3 boosting circuit in the positive direction

Pin name	I/O	Pin No.	Function
V_{OUT3}	O	5	This is the output pin of the ×3 boosting circuit in the positive direction.
C3P	(O)	2	This is the pin to connect the positive side of the V_{OUT3} output voltage generating flying capacitor C3.
C3N	(O)	1	This is the pin to connect the negative side of the V_{OUT3} output voltage generating flying capacitor C3.
C4P	(O)	3	This is the pin to connect the positive side of the V_{OUT3} output voltage generating flying capacitor C4.
C4N	(O)	4	This is the pin to connect the negative side of the V_{OUT3} output voltage generating flying capacitor C4.

(5) ×3 boosting circuit in the negative direction

Pin name	I/O	Pin No.	Function
V_{OUT4}	O	20	This is the output pin of the ×3 boosting circuit in the negative direction.
C5P	(O)	24	This is the pin to connect the positive side of the V_{OUT4} output voltage generating flying capacitor C5.
C5N	(O)	23	This is the pin to connect the negative side of the V_{OUT4} output voltage generating flying capacitor C5.
C6P	(O)	21	This is the pin to connect the positive side of the V_{OUT4} output voltage generating flying capacitor C6.
C6N	(O)	22	This is the pin to connect the negative side of the V_{OUT4} output voltage generating flying capacitor C6.

(6) Power pins

Pin name	I/O	Pin No.	Function
V_{DD}	I	6	This is the input power pin (+).
V_{SS}	I	12	This is the input power pin (–).

■ FUNCTIONAL DESCRIPTION

● Operational description

Generating voltage levels are:

· Positive boosting supply voltage necessary for the voltage stabilizing circuit (V_{OUT1})

· Positive stabilized supply voltage necessary for the source driver (V_{OUT2})

· Positive and negative boosting supply voltages necessary for the gate driver (V_{OUT3} and V_{OUT4})

The V_{OUT1} supply voltage is being generated by the charge pump type DC/DC converter (×2 boosting circuit in the positive direction). It makes ×2 boosting in the positive direction of the potential difference occurring between the V_{DD} – V_{SS} using the V_{SS} potential as the reference voltage.

The V_{OUT2} supply voltages is being generated by the series regulator stabilizing the potential difference occurring between the V_{OUT1} – V_{SS} using the V_{SS} potential as the reference voltage.

The V_{OUT3} supply voltage is being generated by the charge pump type DC/DC converter (×3 boosting circuit in the positive direction). It makes ×3 boosting in the positive direction of the potential difference occurring between the V_{OUT2} – V_{SS} using the V_{SS} potential as the reference voltage.

The V_{OUT4} supply voltage is being generated by the charge pump type DC/DC converter (×3 boosting circuit in the negative direction). It makes ×3 boosting in the negative direction of the potential difference occurring between the V_{OUT2} – V_{SS} using the V_{OUT2} potential as the reference voltage.

Indicated below is the system configuration diagram for the power circuit.

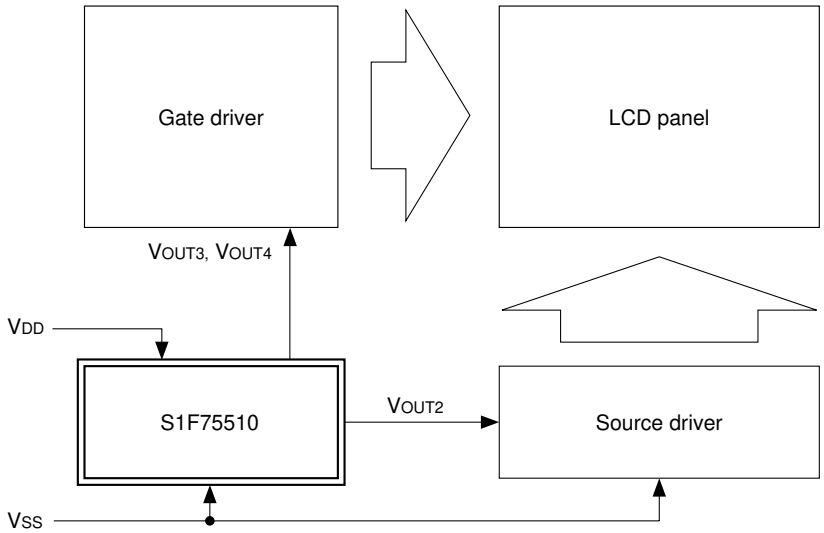


Fig. 2 System configuration diagram

Indicated below is the potential correlation diagram inside the system as is shown in Fig. 2.

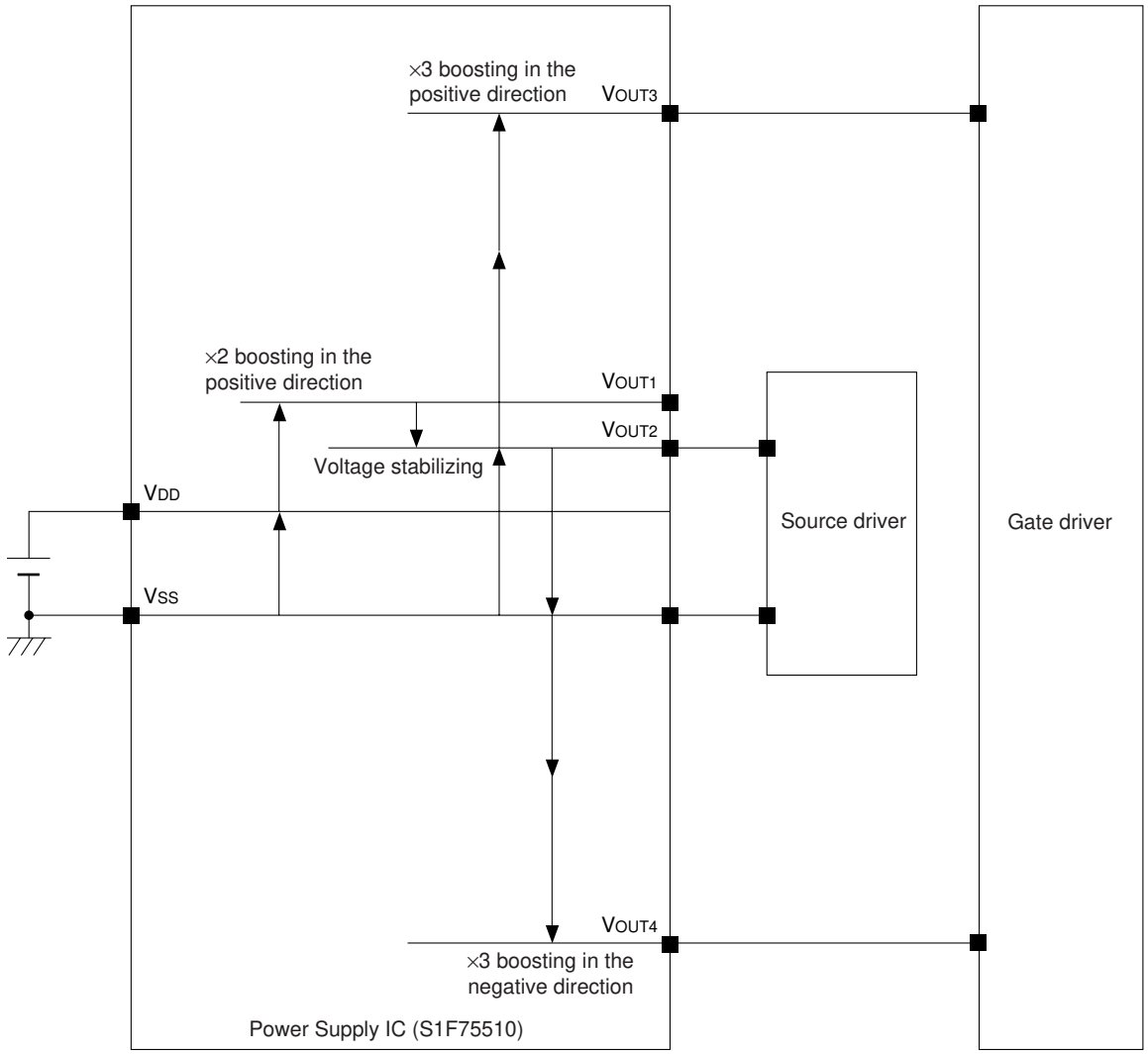


Fig. 3 Potential correlation diagram inside the system

● CR oscillation circuit

The S1F75510 incorporates a CR oscillation circuit as the oscillation circuit for the boosting clock signals. This circuit is to be used connecting the external oscillation resistor ROSC between the OSC1 pin and the OSC2 pin. The CR oscillation circuit will stop operation under the blank mode and when using the external clock (MODE = VSS level and OSCSEL = VSS level) or under the shut down state (POFFX = VSS level). Also, the oscillation will be interrupted by setting the OSC1 pin to the VSS level and, at the same time, setting the OSC2 pin into open state.

As the external oscillation resistance, we recommend use of ROSC = 1 MΩ.

● Mode changeover circuit

By external settings of the mode changeover signal MODE and the internal/external clock selection signal OSCSEL, the charge pump boosting can be driven under optimum frequencies. Since the current consumption of the IC can be suppressed drastically under the blank mode, it is possible to achieve high power conversion efficiency even under light load operations.

MODE pin	OSCSEL pin	Mode name	Max. output current	Built-in CR oscillation circuit	Built in voltage stabilizing circuit
HIGH(V_{DD})	HIGH(V_{DD}) LOW(V_{SS})	Normal mode	V_{OUT2}:(10mA) (TBD) V_{OUT3}:(100µA) (TBD) V_{OUT4}:(100µA) (TBD)	In operation	In normal operation
LOW(V_{SS})	HIGH(V_{DD})	Blank mode	V_{OUT2}:(200µA) (TBD) V_{OUT3}:(10µA) (TBD) V_{OUT4}:(10µA) (TBD)	In operation	In low current consumption operation
	LOW(V_{SS})	Blank mode	V_{OUT2}:(200µA) (TBD) V_{OUT3}:(10µA) (TBD) V_{OUT4}:(10µA) (TBD)	In standstill	In low current consumption operation

● Timing signal forming circuit

This circuit generates the clock signals necessary for charge pump boosting using the internal oscillation or using external clock signals.

Two different types of capacitors are being used as the charge pump capacitors, one being the flying capacitor which shifts between the charging state and the discharging state and the other being the smoothing capacitor which preserves the electric charge. The operating frequency of the flying capacitor should equal to the frequency of the charge pump clock being generated by this timing signal forming circuit.

Under the shut down state (POFFX = V_{SS} level), the charge pump clock stops operation and all the boosting operations of this IC will be interrupted. The operating frequencies of the flying capacitor are as follows.

MODE pin	OSCSEL pin	Mode name	Operating frequencies of the flying capacitor		
			×2 boosting in the positive direction	×3 boosting in the positive direction	×3 boosting in the negative direction
HIGH(V_{DD})	HIGH(V_{DD}) LOW(V_{SS})	Normal mode	(TBD) kHz (Typ.10 kHz)	(TBD) kHz (Typ.10 kHz)	(TBD) kHz (Typ.10 kHz)
LOW(V_{SS})	HIGH(V_{DD})	Blank mode	(TBD) kHz (Typ.625 Hz)	(TBD) kHz (Typ.625 Hz)	(TBD) kHz (Typ.625 Hz)
	LOW(V_{SS})	Blank mode CL=(TBD) Hz (Min.300 Hz)	(TBD) Hz (Min.150 Hz)	(TBD) Hz (Min.150 Hz)	(TBD) Hz (Min.150 Hz)

●×2 boosting circuit in the positive direction

The ×2 boosting circuit in the positive direction generates the voltages necessary to input into the voltage stabilizing circuit. It makes ×2 boosting in the positive direction of the potential difference occurring between the V_{DD} – V_{SS} using the V_{SS} potential as the reference voltage to output through the V_{OUT1} pin.

Under the blank mode, since the boosting operation is being carried out with the flying capacitor C2 stopping its operation, the current consumption can be suppressed accordingly.

The theoretical equation (output voltage value under the idealistic non-load state) for the V_{OUT1} becomes as follows:

$$V_{OUT1} = (V_{DD} - V_{SS}) \times 2$$

Actually, when a load is connected to the V_{OUT1}, the output voltage will drop to the value represented by the equation indicated below.

$$V_{OUT1} = (V_{DD} - V_{SS}) \times 2 - RV_{OUT1} \times IV_{OUT1}$$

RV_{OUT1} : Output impedance of the x2 boosting circuit in the positive direction

IV_{OUT1} : Load current

●Voltage stabilizing circuit

The voltage stabilizing circuit stabilizes the voltage being output through the V_{OUT1} pin by the series regulator to output the positive supply voltage for the source driver through the V_{OUT2} pin.

The output voltage setting for the V_{OUT2} pin should be Typ. +5.0V (TBD).

Since it is necessary to let the V_{OUT1} satisfy the correlation of "$V_{OUT1} > V_{OUT2} + 0.1V$" in order to obtain normal output voltage value through the V_{OUT2} pin, use the IC within the range of the max. load current (7.3).

The circuit configuration · connection diagram for the voltage stabilizing circuit is as follows:

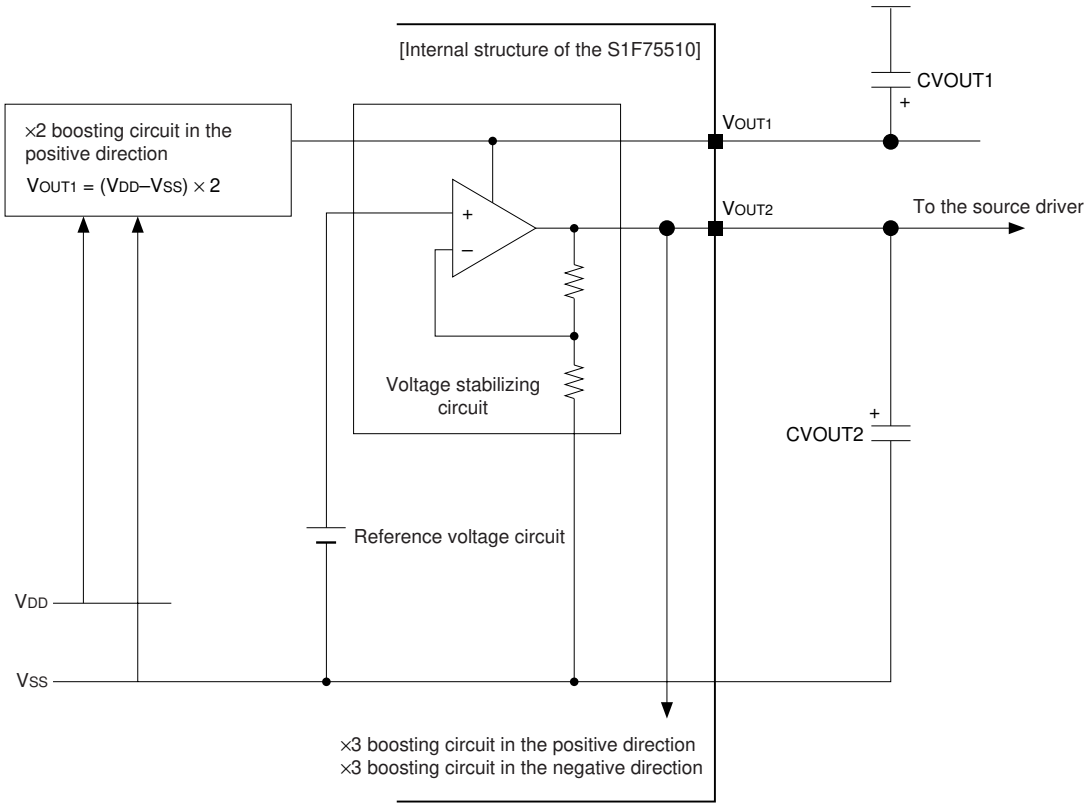


Fig. 4 Configuration diagram of the voltage stabilizing circuit

●×3 boosting circuit in the positive direction

The ×3 boosting circuit in the positive direction generates the V_{OUT3} output voltage, means the positive supply voltage for the gate driver. It makes ×3 boosting in the positive direction of the potential difference occurring between the $V_{OUT2} – V_{SS}$ using the V_{SS} potential as the reference voltage, by charge pump boosting, to output through the V_{OUT3} pin.

The theoretical equation (output voltage value under the idealistic non-load state) for the V_{OUT3} becomes as follows:

$V_{OUT3} = (V_{OUT2} – V_{SS}) \times 3$

Actually, when a load is connected to the V_{OUT3}, the output voltage will drop to the value represented by the equation indicated below.

$V_{OUT3} = (V_{OUT2} – V_{SS}) \times 3 – (RV_{OUT3} \times IV_{OUT3})$

RV_{OUT3} : Output impedance of the ×3 boosting circuit in the positive direction

IV_{OUT3} : Load current

It means that the V_{OUT3} voltage will drop by the load.
To acquire desired output voltage, use the IC within the range of the specified load (7.3).

●×3 boosting circuit in the negative direction

The ×3 boosting circuit in the negative direction generates the V_{OUT3} output voltage, means the negative supply voltage for the gate driver. It makes ×3 boosting in the negative direction of the potential difference occurring between the $V_{OUT2} – V_{SS}$ using the V_{OUT2} potential as the reference voltage, by charge pump boosting, to output through the V_{OUT4} pin.

The theoretical equation (output voltage value under the idealistic non-load state) for the V_{OUT4} becomes as follows:

$V_{OUT4} = (V_{OUT2} – V_{SS}) \times (–2)$ (The voltage value using the V_{SS} potential as the reference voltage)

Actually, when a load is connected to the V_{OUT4}, the output voltage will drop to the value represented by the equation indicated below.

$V_{OUT4} = (V_{OUT2} – V_{SS}) \times (–2) – (RV_{OUT4} \times IV_{OUT4})$

RV_{OUT4} : Output impedance of the ×3 boosting circuit in the negative direction

IV_{OUT4} : Load current

It means that the V_{OUT4} voltage will drop by the load.
To acquire desired output voltage, use the IC within the range of the specified load (7.3).

●Electric charge discharging circuit

The electric charge discharging circuit discharges the electric charge remaining in the V_{OUT3} pin and V_{OUT4} pin to the V_{SS} level.
This circuit starts operation when the POFFX pin is set to the V_{SS} level.

The discharging sequence and the discharging impedance are according to the (TBD).

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating		Unit	Applicable pin	Remarks
		Min.	Max.			
Input supply voltage	V_{DD}	– 0.3	4.0	V	V_{DD}	—
Output voltage 1	V_{OUT1}	– 0.3	7.5	V	V_{OUT1}	—
Output voltage 2	V_{OUT2}	– 0.3	7.5	V	V_{OUT2}	—
Output voltage 3	V_{OUT3}	– 0.3	22.5	V	V_{OUT3}	—
Output voltage 4	V_{OUT4}	– 15.0	0.3	V	V_{OUT4}	—
Input pin voltage 1	V_{IN}	– 0.3	V_{DD} + 0.3	V	<Note 1>	—
Input current	IV_{DD}	—	(TBD)	mA	V_{DD}	
Output current 1	IV_{OUT1}	—	(TBD)	mA	V_{OUT1}	—
Output current 2	IV_{OUT2}	—	(TBD)	mA	V_{OUT2}	—
Output current 3	IV_{OUT3}	—	(TBD)	mA	V_{OUT3}	—
Output current 4	IV_{OUT4}	—	(TBD)	mA	V_{OUT4}	—
Allowable dissipation	P_D	—	(TBD)	mW	—	Ta ≤ 55˚C
Operating temperature	Topr	– 30	85	˚C	—	—
Storage temperature	Tstg	– 55	150	˚C	—	—
Soldering temperature and time	Tsol	—	260·10	˚C·s	—	At leads

<Note 1> The applicable pins are POFFX, OSC1, CL, MODE and OSCSEL.

<Note 2> Do not apply external voltage to the output pins and the pin connecting to the capacitor.

<Note 3> Use of the IC under any conditions exceeding the above absolute maximum ratings may cause malfunctioning or permanent breakdown. Or, even if the IC may operate normally temporarily, the reliability may greatly drop.

■ ELECTRICAL CHARACTERISTICS

● DC characteristics

In case particular designations are not made (Note 1): Ta = –10 to +70˚C

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
Input supply voltage	V_{DD}	Applicable pin: VDD	(TBD)	3.0	3.6	V	—
High level input voltage	V_{IH}	—	0.8V_{DD}	—	V_{DD}	V	2
Low level input voltage	V_{IL}	—	0	—	0.2V_{DD}	V	2
Input leak current 1	I_{LKI1}	$V_{SS} \leq V_I \leq V_{DD}$, V_{DD} = (TBD) to 3.6V	– 0.5	—	0.5	µA	2
Current consumption 1	I_{OPR1}	V_{DD} = 3.0V, no load Under the normal mode	—	(TBD) (300)	(TBD)	µA	—
Current consumption 2	I_{OPR2}	V_{DD} = 3.0V, no load Under the blank mode CL = (TBD) kHz	—	(TBD) (30)	(TBD)	µA	—
Power conversion efficiency 1 (Overall efficiency including the stabilized outputs)	Peff1	V_{DD} = 3.0V Under the normal mode	(TBD)	(TBD)	(TBD)	%	3
Power conversion efficiency 2 (Overall efficiency including the stabilized outputs)	Peff2	V_{DD} = 3.0V Under the blank mode CL = (TBD) kHz	(TBD)	(TBD)	(TBD)	%	4
Resting current	IQ	V_{DD} = 3.6V POFFX = LOW	—	—	(TBD) (1.0)	µA	—

<Note 1> Conditions on the operation mode, external parts constant, pins, etc. in case particular designations are not made are as follows.
Connection and parts constant : Standard connection 1, 10.1
MODE pin : MODE = HIGH (Normal mode)
CL pin : CL = LOW (Fixed voltage)

<Note 2> The applicable pins are XDIS, SSLP, PCK1 and CNT

<Note 3> Load conditions: IV_{OUT2} = (TBD)mA, IV_{OUT3} = (TBD)µA, IV_{OUT4} = (TBD)µA
Conversion efficiency = $[(V_{OUT2} \times IV_{OUT2}) + (V_{OUT3} \times IV_{OUT3}) + (V_{OUT4} \times IV_{OUT4})] / (V_{DD}* \times IV_{DD}*) \times 100$

<Note 4> Load conditions: IV_{OUT2} = (TBD)µA, IV_{OUT3} = (TBD)µA, IV_{OUT4} = (TBD)µA
Conversion efficiency = $[(V_{OUT2} \times IV_{OUT2}) + (V_{OUT3} \times IV_{OUT3}) + (V_{OUT4} \times IV_{OUT4})] / (V_{DD}* \times IV_{DD}*) \times 100$

● Characteristics of ×2 boosting in the positive direction + stabilized output

Ta = –10 to +70˚C

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
V_{OUT1} output impedance (Normal mode)	RV_{OUT1-1}	Applicable pin: V_{OUT1}	—	(TBD)	(TBD)	Ω	5
V_{OUT1} output impedance (Blank mode)	RV_{OUT1-2}	Applicable pin: V_{OUT1}	—	(TBD)	(TBD)	Ω	6
V_{OUT2} Stabilized output voltage	V_{OUT2}	Applicable pin: V_{OUT2}	(TBD) (4.90)	(TBD) (5.00)	(TBD) (5.20)	V	7
V_{OUT2} Stabilized output saturated resistance	RV_{OUT2}	Applicable pin: V_{OUT2}	—	—	10	Ω	8

<Note 5> V_{DD} = (TBD)V to 3.6V, Load condition: IV_{OUT1} = (TBD)mA
<Note 6> V_{DD} = (TBD)V to 3.6V, Load condition: IV_{OUT1} = (TBD)mA
<Note 7> V_{DD} = (TBD)V to 3.6V, Load condition: IV_{OUT2} = (TBD)mA
<Note 8> V_{DD} = (TBD)V to 3.6V, Load condition: IV_{OUT2} = (TBD)mA

● Characteristics of ×3 boosting in the positive direction and ×3 boosting in he negativet direction

Ta = –10 to +70˚C

Item	Symbol	Conditions	Rating			Unit	Remarks
			Min.	Typ.	Max.		
V_{OUT3} output impedance (Normal mode)	RV_{OUT3-1}	Applicable pin: V_{OUT3}	—	(TBD)	(TBD)	Ω	9
V_{OUT3} output impedance (Blank mode)	RV_{OUT3-2}	Applicable pin: V_{OUT3}	—	(TBD)	(TBD)	Ω	10
V_{OUT4} output impedance (Normal mode)	RV_{OUT4-1}	Applicable pin: V_{OUT4}	—	(TBD)	(TBD)	Ω	11
V_{OUT4} output impedance (Blank mode)	RV_{OUT4-2}	Applicable pin: V_{OUT4}	—	(TBD)	(TBD)	Ω	12

<Note 9> V_{DD} = (TBD)V to 3.6V, Load condition: IV_{OUT3} = (TBD)μA
<Note 10> V_{DD} = (TBD)V to 3.6V, Load condition: IV_{OUT3} = (TBD)μA
<Note 11> V_{DD} = (TBD)V to 3.6V, Load condition: IV_{OUT4} = (TBD)μA
<Note 12> V_{DD} = (TBD)V to 3.6V, Load condition: IV_{OUT4} = (TBD)μA

● AC characteristics

Measurement conditions for the AC characteristics

· Input signal level V_{IH} = 0.8 V_{DD} (V)
V_{IL} = 0.2 V_{DD} (V)

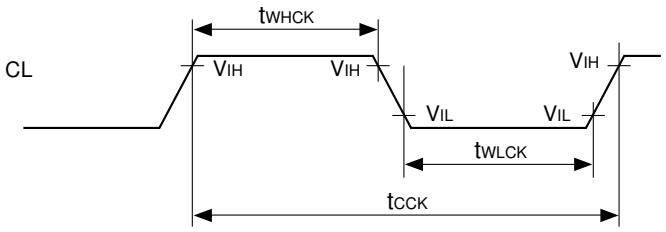
· Input signal rise time Tr = Max. 100ns

· Input signal fall time Tf = Max. 100ns

V_{DD} = (TBD) to 3.6V, V_{SS} = 0V

Ta = –10 to +70˚C

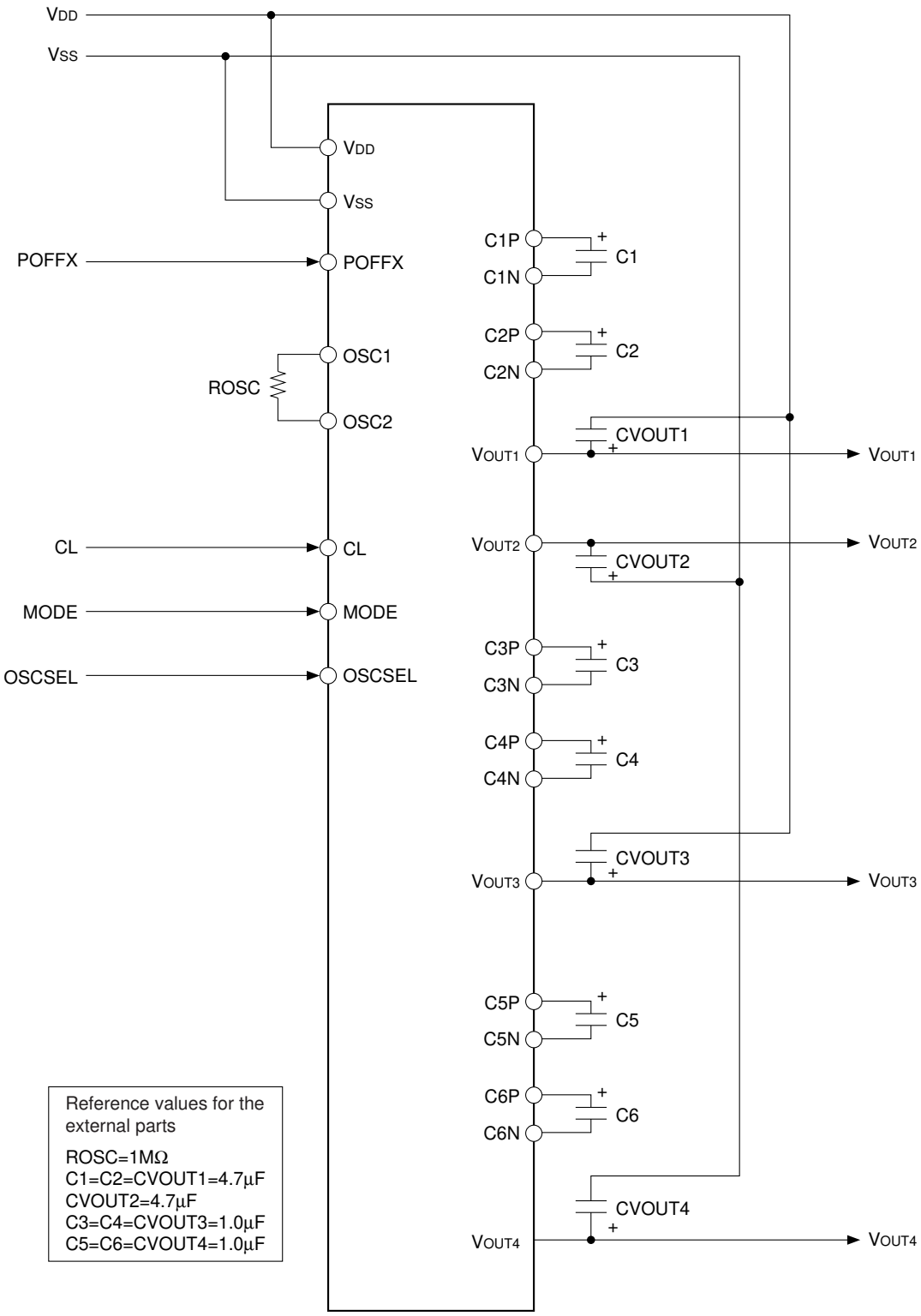
CL inputting timing



Item	Symbol	Rating			Unit	Applicable pin	Remarks
		Min.	Typ.	Max.			
CL cycle	t_{CCK}	(TBD)	(TBD)	(TBD)	µs	CL	—
CL High pulse duration	t_{WHCK}	(TBD)	—	—	ns		
CL Low pulse duration	t_{WICK}	(TBD)	—	—	ns		

■ REFERENCE EXTERNAL CONNECTION (AN EXAMPLE)

● Standard connection 1

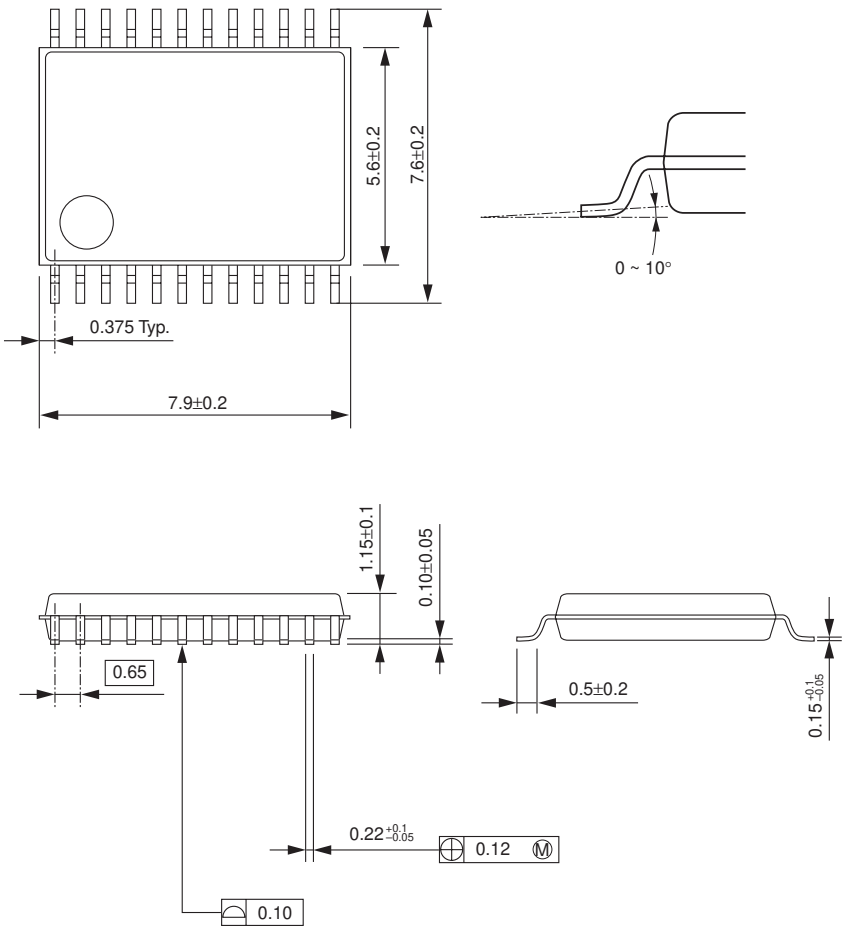


Reference values for the external parts

ROSC=1MΩ
C1=C2=CVOUT1=4.7µF
CVOUT2=4.7µF
C3=C4=CVOUT3=1.0µF
C5=C6=CVOUT4=1.0µF

■ DIMENSIONAL OUTLINE DRAWING

SSOP3–24pin



Unit : mm

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