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### ■ DESCRIPTION

The S1F81150 is a System Power Supply IC. From the Li-Ion/Li-polymer battery, 6 channels of output voltage are generated via external devices. The 6 channels are independent of each other.

On this series, an I<sup>2</sup>C controller (for the slave function), input and output voltage detecting functions and many kinds of operation modes (Normal, Sleep, Deep Sleep, Ultra-Energy-Saving) are provided as well as three PWM controller channels and three series regulator channel.

Table.1 Product list

Model	Package	Mask Option		
		[No.1] CH-2	[No.2] CH-3	[others]
S1F81150F0A2000	QFP12-48	2.9V	1.8V	—
S1F81150F5A2000	QFN7-48	2.9V	1.8V	(Under Development)

### ■ FEATURES

The features of the S1F81150 include the following:

Input voltage: V<sub>IN</sub> 2.9V to 4.5V

Regulator: 6 channels

#### **CH-1 (Vcc1): PWM controller**

Fast synchronized rectification type PWM controller

(Connected to an external component to configure a switching regulator.)

Features include a fast response circuit using a current/voltage returning system, a short-circuit-proof circuit, a soft-start system, more compact external components by a fast clock, and dynamic voltage management system.

Output voltage: 1.5/1.4/1.3/1.2/1.1/1.0/0.9/0.85/0.8V

One of these values is to be selected via the I<sup>2</sup>C controller.

Accuracy: within ±5%

Output current: In the sleep status: OFF.

In the normal operation: Max.: 500mA

#### **CH-2 (Vcc2): PWM controller**

Fast synchronized rectification type PWM controller

(Connected to an external component to configure a switching regulator.)

Features include a fast response circuit using a current/voltage returning system, a short-circuit-proof circuit, a soft-start system and more compact external components by a fast clock.

Output voltage: 2.9V (\*) (\*) Output voltage can be selected by metal option

Accuracy: within ±5%

Output current: In the deep sleep status: OFF.

In the backup operation: Max.: 10mA

In the normal operation: Max.: 1A

#### **CH-3 (Vcc3): PWM controller**

Fast synchronized rectification type PWM controller

(Connected to an external component to configure a switching regulator.)

Features include a fast response circuit using a current/voltage returning system, a short-circuit-proof circuit, a soft-start system and more compact external components by a fast clock.

Output voltage: 1.8V (\*) (\*) Output voltage can be selected by metal option

Accuracy: within ±5%

Output current: In the deep sleep status: OFF.

In the backup operation: Max.: 10mA

In the normal operation: Max.: 1A

# S1F81150 Series

## **CH-4 (Vcc4): Series regulator**

A low power consumption type Series Regulator.

Output voltage: 1.3V

Output current: In the sleep status: OFF.  
In the normal operation: Max: 30mA

## **CH-5 (Vcc5): Series regulator**

A low power consumption type Series Regulator.

Output voltage: 1.1V

Output current: In the sleep status: OFF.  
In the normal operation: Max: 30mA

## **CH-B (VccB): Series regulator**

A low power consumption type Series Regulator.

Output voltage: 3.0V ( $\pm 25\%$ )

Output current: In the CH-2:OFF status: Max.: 5mA  
In the normal operation: OFF.

Conversion Efficiency:	Switching regulator (CH-1):	Max. 85% or more
	Switching regulator (CH-2/CH-3):	Max. 90% or more
Current consumption:	Ultra-Energy-Saving mode:	0.6 $\mu$ A (Typ. @VIN=3.6V)
	Deep Sleep mode	40 $\mu$ A (Typ. @VIN=3.6V)
	Sleep mode	85 $\mu$ A (Typ. @VIN=3.6V)
	Normal mode	1.2mA (Typ. @VIN=3.6V)
External interface:	Built-in interfaces in the I <sup>2</sup> C controller (SDA and SCL, for the slave function only).	
Output voltage detecting function:	1 channel	(nVCC_FLT)
Input voltage detecting function:	1 channel	(nBAT_FLT)
Resetting function:	1 channel	(XRST(I), nRESET(O))
Sleep function:	2 channel	(PWR_EN, SYS_EN)
DVM function:	CH-1 voltage shifting slew rate setting via I <sup>2</sup> C controller. $\Delta V / \Delta t$ in Fig.1 can be set by register.	

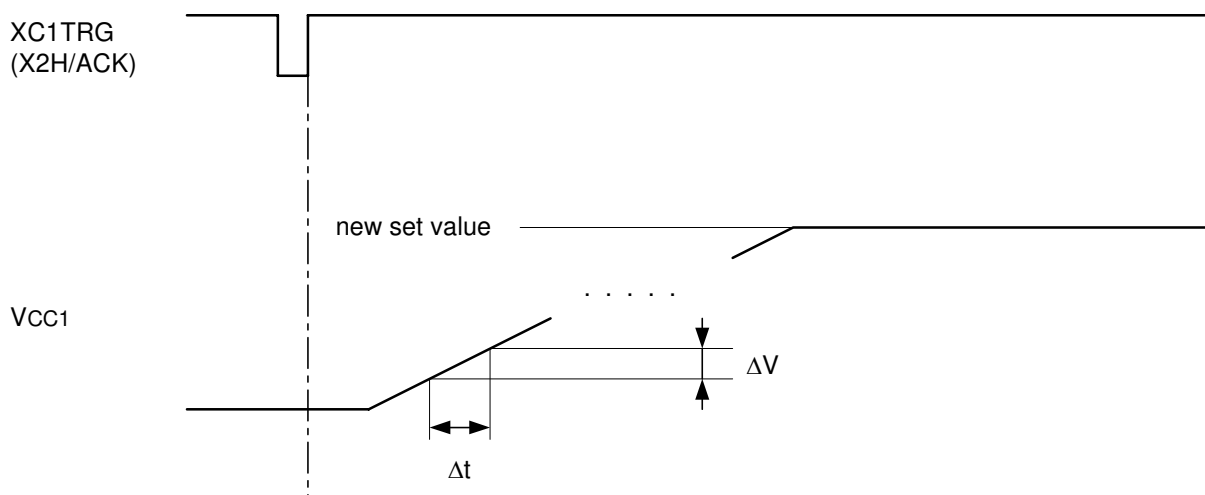


Fig.1 DVM function

# S1F81150 Series

## ■ BLOCK DIAGRAM

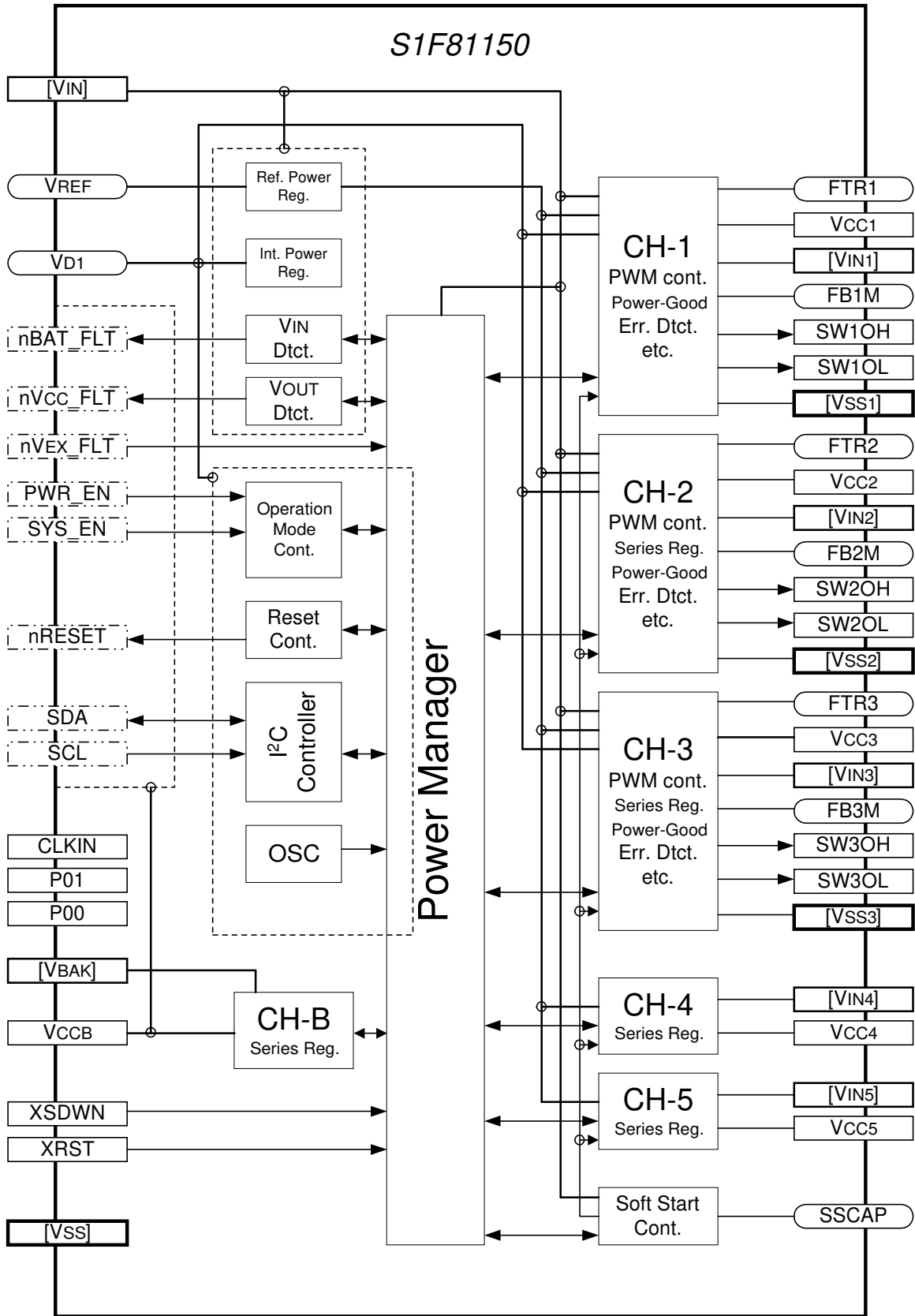


Fig.2 S1F81150 Block diagram

# S1F81150 Series

## ■ PIN ASSIGNMENT

[QFP12-48]

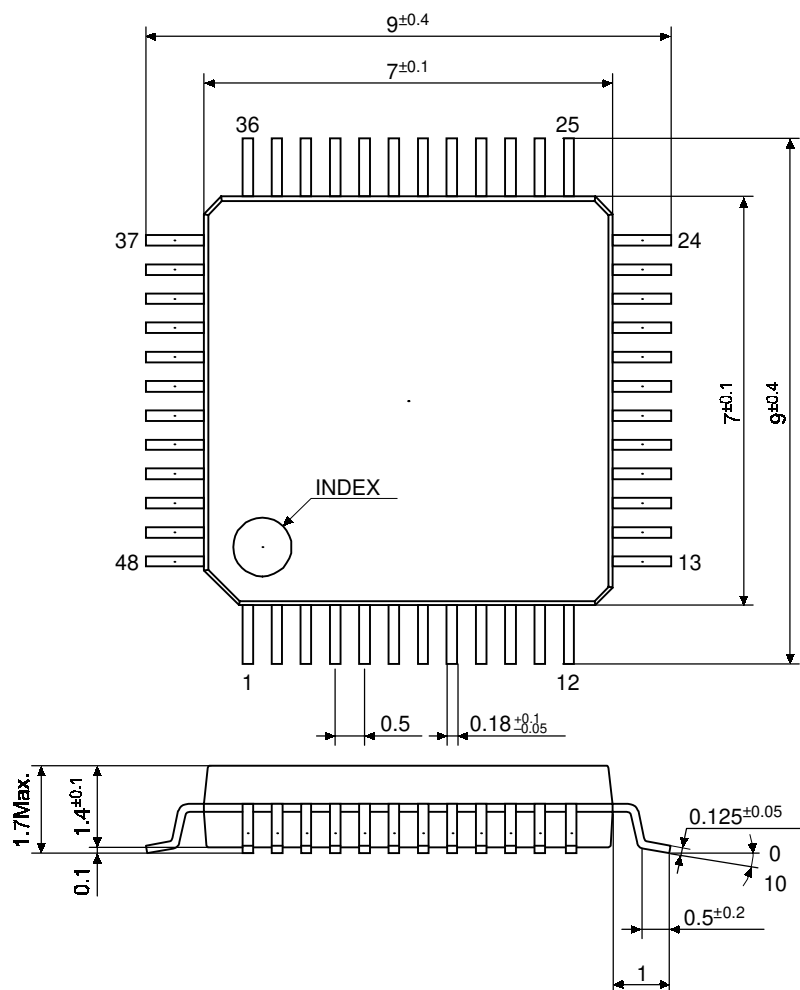


Fig.3 QFP12-48 package gram

Table 2 QFP12-48 pin assignment

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	SW3OH	13	VCC5	25	VBAK	37	P01
2	FB3M	14	VCC4	26	VCCB	38	P02
3	SW3OL	15	VIN4	27	PWR_EN	39	FTR2
4	VSS3	16	VIN5	28	WUP	40	VCC2
5	FTR1	17	XRST	29	nRESET	41	VIN2
6	VCC1	18	VIN	30	nBAT_FLT	42	SW2OH
7	VIN1	19	VREF	31	nVcc_FLT	43	FB2M
8	SW1OH	20	VD1	32	nVEX_FLT	44	SW2OL
9	FB1M	21	VSS	33	SYS_EN	45	VSS2
10	SW1OL	22	XSDWN	34	SCL	46	FTR3
11	VSS1	23	XTEST0	35	SDA	47	VCC3
12	SSCAP	24	CLKIN	36	P00	48	VIN3

# S1F81150 Series

[QFP7-48]

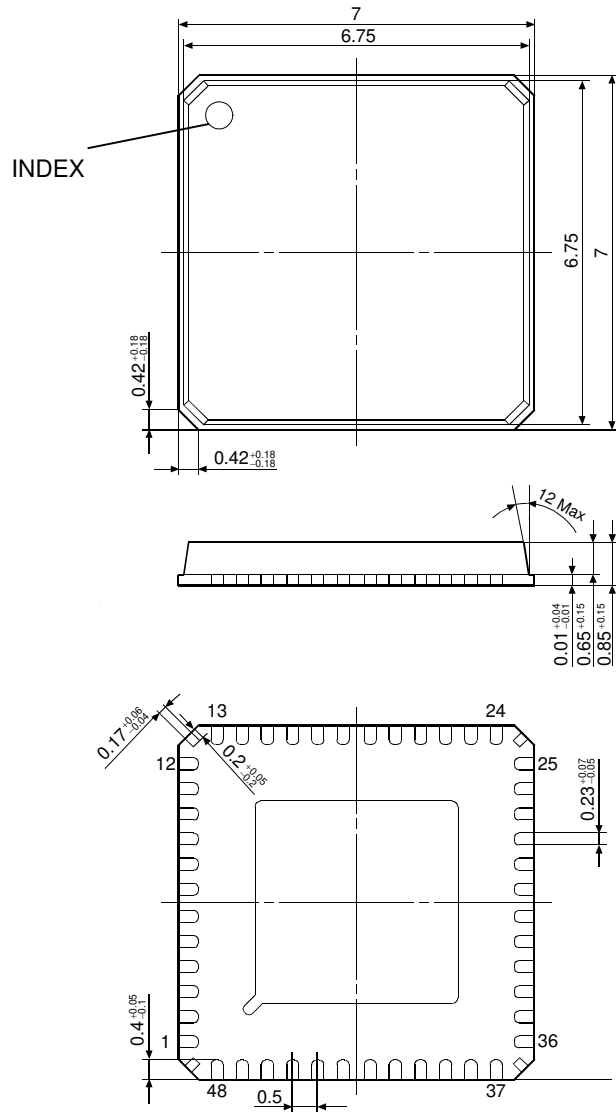


Fig.4 QFP7-48 package gram

Table.3 QFP7-48 pin assignment

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
1	SW3OH	13	VCC5	25	VBAK	37	P01
2	FB3M	14	VCC4	26	VCCB	38	P02
3	SW3OL	15	VIN4	27	PWR_EN	39	FTR2
4	VSS3	16	VIN5	28	WUP	40	VCC2
5	FTR1	17	XRST	29	nRESET	41	VIN2
6	VCC1	18	VIN	30	nBAT_FLT	42	SW2OH
7	VIN1	19	VREF	31	nVCC_FLT	43	FB2M
8	SW1OH	20	VD1	32	nVEX_FLT	44	SW2OL
9	FB1M	21	VSS	33	SYS_EN	45	VSS2
10	SW1OL	22	XSDWN	34	SCL	46	FTR3
11	VSS1	23	XTEST0	35	SDA	47	VCC3
12	SSCAP	24	CLKIN	36	P00	48	VIN3

# S1F81150 Series

## ■ PIN DESCRIPTION

Table.3 S1F81150 Pin description

No.	Name	I/O	Function	Level	Pin No.
<b>[Power terminal/control terminal]</b>					
1	VIN	Power	Main power (+) input terminal	—	
2	VSS	Power	Main power (-) input terminal	—	
3	VD1	Analog	Internal constant power output terminal	—	
4	VREF	Analog	Reference power output terminal	—	
5	nVCC_FLT	O	Output detection result output terminal	VCCB	
6	nBAT_FLT	O	Input detection result output terminal	VCCB	
7	nRESET	O	System reset output terminal	VCCB	
8	PWR_EN	I	Mode setting input terminal	VCCB	
9	SYS_EN	I	Mode setting input terminal	VCCB	
10	WUP	O	Vcc1 power change indication output terminal	VCCB	
11	nVEX_FLT	I	External power detection result input terminal	VCCB	
12	CLKIN	I	External clock input terminal	VCC2	
13	XRST	I	Reset input terminal	VIN	
14	XTEST0	I	Test terminal	VIN	
15	XSDWN	I	Ultra-energy-saving mode setting terminal	VIN	
16	P00	I/O	General purpose I/O terminal	VCC2	
17	P01	I/O	General purpose I/O terminal	VCC2	
18	P02	I/O	Test terminal	VCC2	
19	SCL	I	I <sup>2</sup> C clock input terminal	VCCB	
20	SDA	I/O	I <sup>2</sup> C data input/output terminal	VCCB	
21	SSCAP	Analog	Soft start setting terminal	—	
<b>[CH-1 related terminal]</b>					
22	VIN1	Power	Main power (+) input terminal	—	
23	SW1OH	O	P-ch power MOS drive output terminal	VIN1	
24	SW1OL	O	N-ch power MOS drive output terminal	VIN1	
25	FB1M	Analog	Output current feed back input terminal	—	
26	VCC1	Analog	Output power feed back input terminal	—	
27	FTR1	Analog	N.C.	—	
28	VSS1	Power	Main power (-) input terminal	—	
<b>[CH-2 related terminal]</b>					
29	VIN2	Power	Main power (+) input terminal	—	
30	SW2OH	O	P-ch power MOS drive output terminal	VIN2	
31	SW2OL	O	N-ch power MOS drive output terminal	VIN2	
32	FB2M	Analog	Output current feed back input terminal	—	
33	VCC2	Analog	Output power feed back input terminal	—	
34	FTR2	Analog	Analog filter terminal	—	
35	VSS2	Power	Main power (-) input terminal	—	
<b>[CH-3 related terminal]</b>					
36	VIN3	Power	Main power (+) input terminal	—	
37	SW3OH	O	P-ch power MOS drive output terminal	VIN3	
38	SW3OL	O	N-ch power MOS drive output terminal	VIN3	
39	FB3M	Analog	Output current feed back input terminal	—	
40	VCC3	Analog	Output power feed back input terminal	—	
41	FTR3	Analog	Analog filter terminal	—	
42	VSS3	Power	Main power (-) input terminal	—	
<b>[CH-4 related terminal]</b>					
43	VIN4	Power	CH-4 regulator power (+) input terminal	—	
44	VCC4	Analog	VCC4 power output terminal	—	
<b>[CH-5 related terminal]</b>					
45	VIN5	Power	CH-5 regulator power (+) input terminal	—	
46	VCC5	Analog	VCC5 power output terminal	—	
<b>[CH-B related terminal]</b>					
47	VBAK	Power	CH-B regulator power (+) input terminal	—	
48	VCCB	Analog	VCCB power output terminal	—	

# S1F81150 Series

## EXTERNAL CONNECTION DIAGRAM

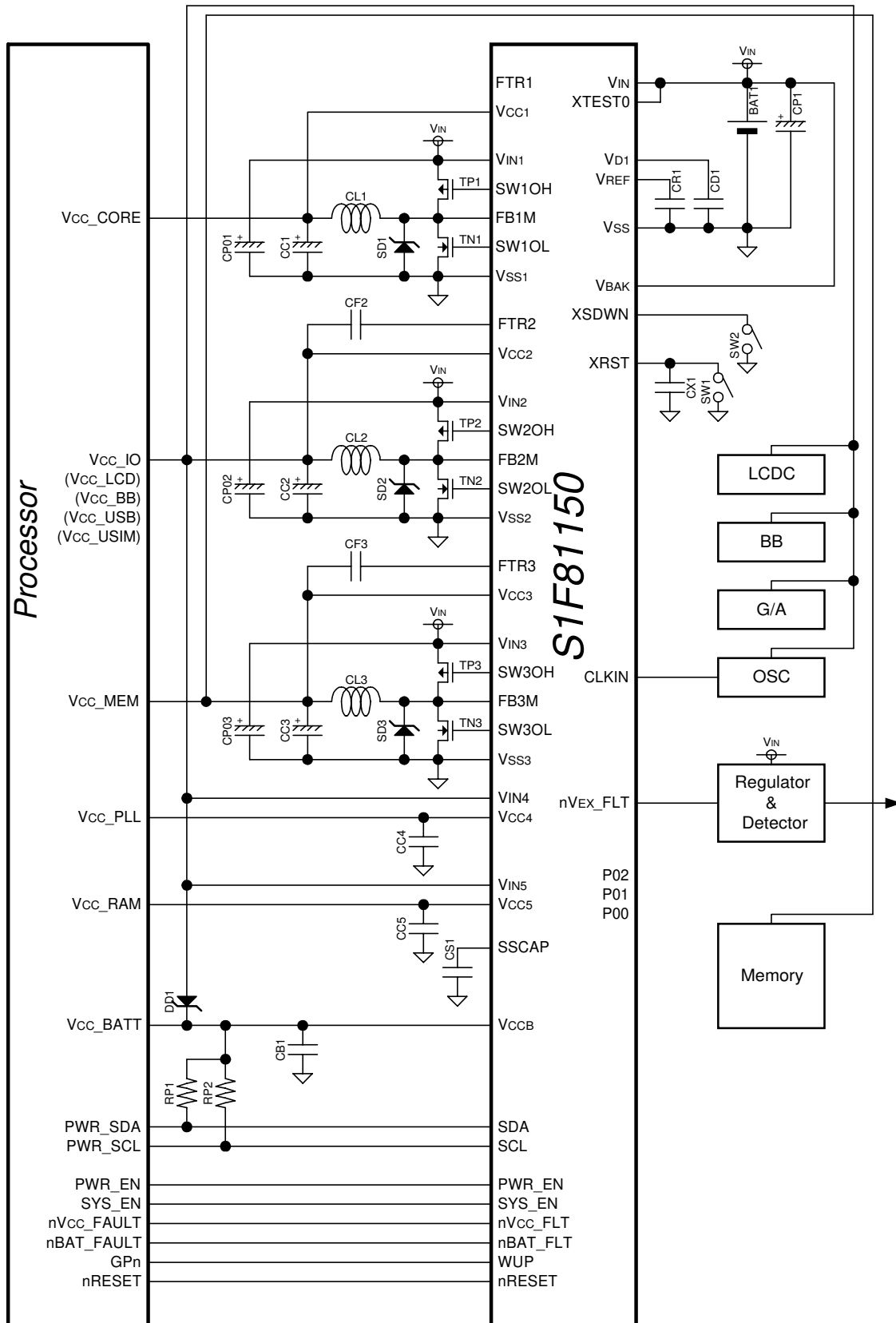


Fig.5 S1F81150 external connection diagram



# S1F81150 Series

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