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EPSON
EXCEED YOUR VISION

S1R72V17***
Technical Manual

SEIKO EPSON CORPORATION

Rev.1.6

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General Rules

Scope of Application

This specification applies to the USB2.0 Controller "S1R72V17B00A***/S1R72V17B00B***/S1R72V17F00C***" manufactured by the Semiconductor Operations Division of Seiko Epson Corporation.

Table of Contents

1. Overview

The S1R72V17 is a USB host/device controller LSI that supports USB2.0-compliant high-speed mode. The host ports and device ports of this LSI are shared, allowing it to operate as a USB host or as a USB device when control is switched over.

This LSI also has characteristics suitable for portable equipment incorporating a DMA interface.

2. Features

<< USB2.0 device functions >>

- Supports HS <480 Mbps) and FS (12 Mbps) transfers.
- Includes FS/HS termination (external circuit unnecessary).
- Includes VBUS 5V interface (external circuit unnecessary).
- Supports control, bulk, interrupt, and isochronous transfers.
- Supports five general-purpose (Bulk, Interrupt, and Isochronous transfer) endpoints and Endpoint 0.

<< USB2.0 host functions >>

- Supports HS (480 Mbps), FS (12 Mbps), and LS (1.5 Mbps) transfers.
- Includes pull-down resistors for downstream ports (external circuit unnecessary).
- Includes HS termination (external circuit unnecessary).
- Supports control, bulk, and interrupt transfers.
  Channel structure
  One (1) channel used exclusively for Control transfer
  Includes five general-purpose (Bulk, and Interrupt transfer) channels.
- USB power switch interface.

<< CPU interface >>

- Accepts 16-bit or 8-bit wide general-purpose CPU interfaces.
- Incorporates one DMA channel (Multiword transfer).
- Big Endian (incorporating a bus swap function for Little Endian CPUs).
- Changeable interface voltages (3.3 V to 1.8 VTyp).
- Supports CPU_Cut mode for reducing current consumption when the CPU is inactive.

<< Other >>

- Accepts a 12 MHz/24 MHz crystal resonator for clock input. (built-in Oscillator circuit and 1M Ωfeedback resistor)
- Dedicated pin for 12 MHz, 24 MHz, or 48 MHz clock input.
- Triple-power supply system: 3.3 V, 1.8 V and variable CPU interface power
- Package type: PFBGA5UX60 (S1R72V17B00A***)
  PFBGA8UX81 (S1R72V17B00B***)
  QFP14-80 (S1R72V17F00C***)
- Guaranteed operation temperature range: –40°C to 85°C

* This LSI is not designed to resist radiation.

3. Block Diagram

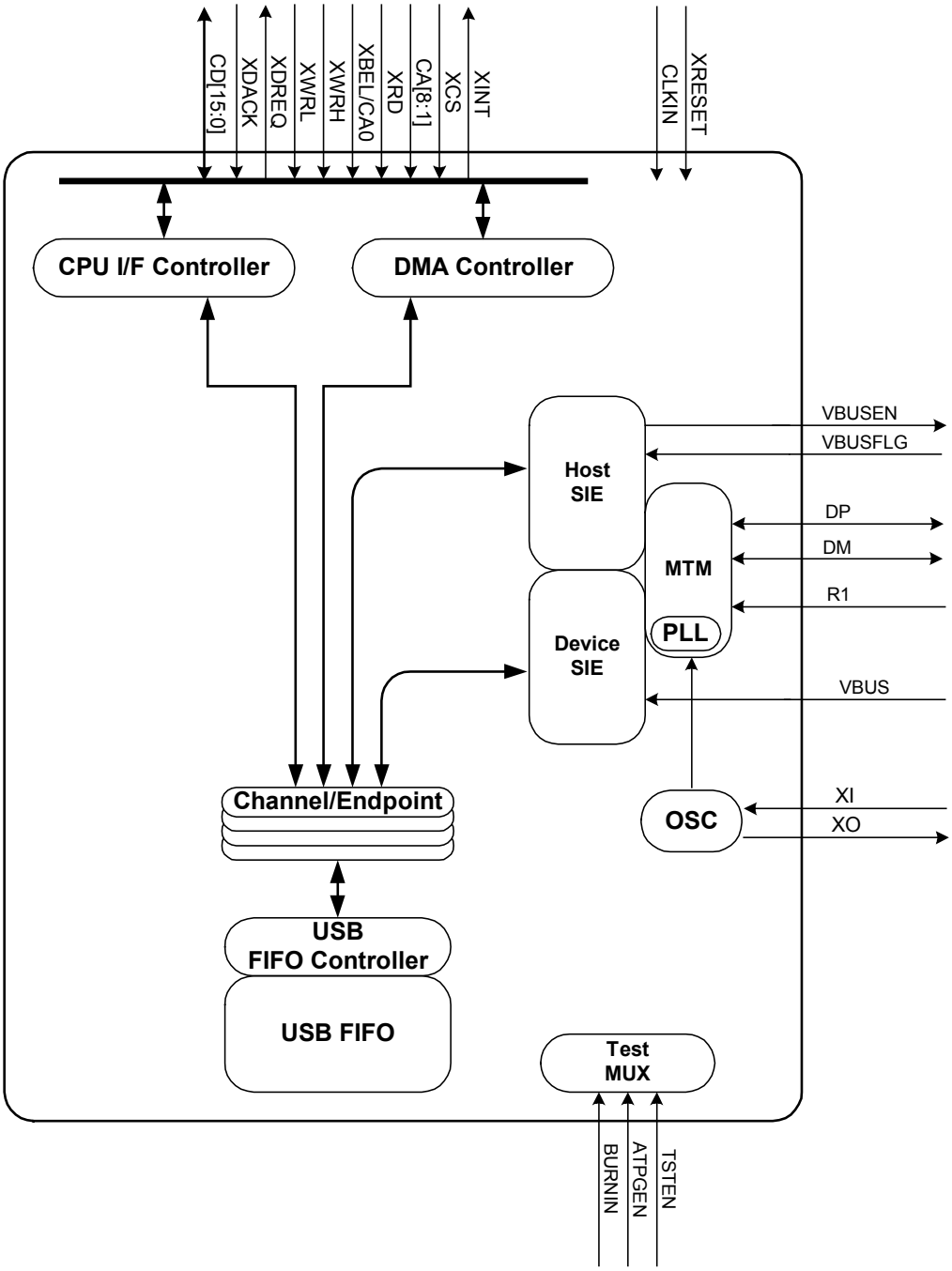

Fig. 3.1 General block diagram

3.1 Multi Transceiver Macro (MTM)

This USB 2.0 transceiver macro is shared by the USB host and USB device. Incorporating an analog circuit and high-speed logic circuit, it supports HS mode (480 Mbps) and FS mode (12 Mbps). LS mode (1.5 Mbps) is supported only for USB hosts.

Incorporates a transmitter, receiver, termination, etc. that together comprise a USB host/device interface.

Furthermore, it has a built-in PLL that generates a 480 MHz clock needed for HS transfer. Internal oscillator or incoming clock through CLKIN pin can be the clock source of the PLL.

3.2 Oscillator

The input clock accepts a 12 MHz or 24 MHz crystal resonator. A 1 MΩ feedback resistor is built-in.

3.3 Device Serial Interface Engine (Device SIE)

This block manages transactions and generates packets.

Furthermore, it controls bus events such as suspend, resume, and reset.

3.4 Host Serial Interface Engine (Host SIE)

This block schedules transactions, manages transactions, and generates packets.

Furthermore, it controls bus events such as suspend, resume, and reset.

It also detects connect/disconnect status and controls the VBUS (in cooperation with an external USB power switch).

3.5 FIFO and FIFO Controller

These blocks comprise a channel/endpoint buffer.

3.6 CPU I/F Controller

Controls the CPU interface timing, allowing registers to be accessed properly.

3.7 DMA Controller

Controls the DMA timing of the CPU interface, allowing access to FIFO. It incorporates one DMA channel.

3.8 Test MUX

This is a test circuit.

4. Pin Layout Diagram

S1R72V17B00A/PFBGA5UX60
TOP View

	1	2	3	4	5	6	7	8
A	NC	LVDD	DP	DM	HVDD	R1	LVDD	BURNIN
B	VBUSFLG	VSS	HVDD	VSS	VSS	VSS	VSS	XI
C	VBUSEN	HVDD	VBUS	CA1	CA3	CD15	LVDD	XO
D	XRESET	XBEL	CA5			CD13	CVDD	CLKIN
E	CA2	CA4	XINT			CD4	CD11	CD14
F	CA7	CA8	XWRH	XDACK	CD3	CD7	CD10	CD12
G	CA6	LVDD	XRD	XDREQ	CD1	CD6	VSS	CD9
H	TESTEN	XCS	XWRL	CD0	CD2	CD5	CD8	ATPGEN

Fig. 4.1 Pin Layout Diagram of the PFBGA5UX60 package

S1R72V17B00B/PFBGA8UX81
TOP View

	1	2	3	4	5	6	7	8	9
A	NC	LVDD	HVDD	DP	DM	HVDD	R1	LVDD	NC
B	VSS	VSS	VBUS	VSS	VSS	VSS	VSS	VSS	XI
C	VBUSFLG	HVDD	LVDD	XBEL	CA1	CVDD	BURNIN	LVDD	XO
D	XRESET	VBUSEN	CA3	NC	NC	NC	CD12	CD15	CLKIN
E	CA2	VSS	CA4	NC	NC	NC	VSS	CD13	CD14
F	CVDD	CA5	CA8	NC	NC	NC	CD7	CD9	CD11
G	CA7	CA6	TESTEN	XCS	XDACK	CD0	CD4	CD8	CD10
H	LVDD	XINT	XWRL	XRD	CD1	CVDD	CD6	ATPGEN	LVDD
J	NC	VSS	XWRH	XDREQ	CD2	CD3	CD5	VSS	NC

Fig. 4.2 Pin Layout Diagram of the PFBGA8UX81 package

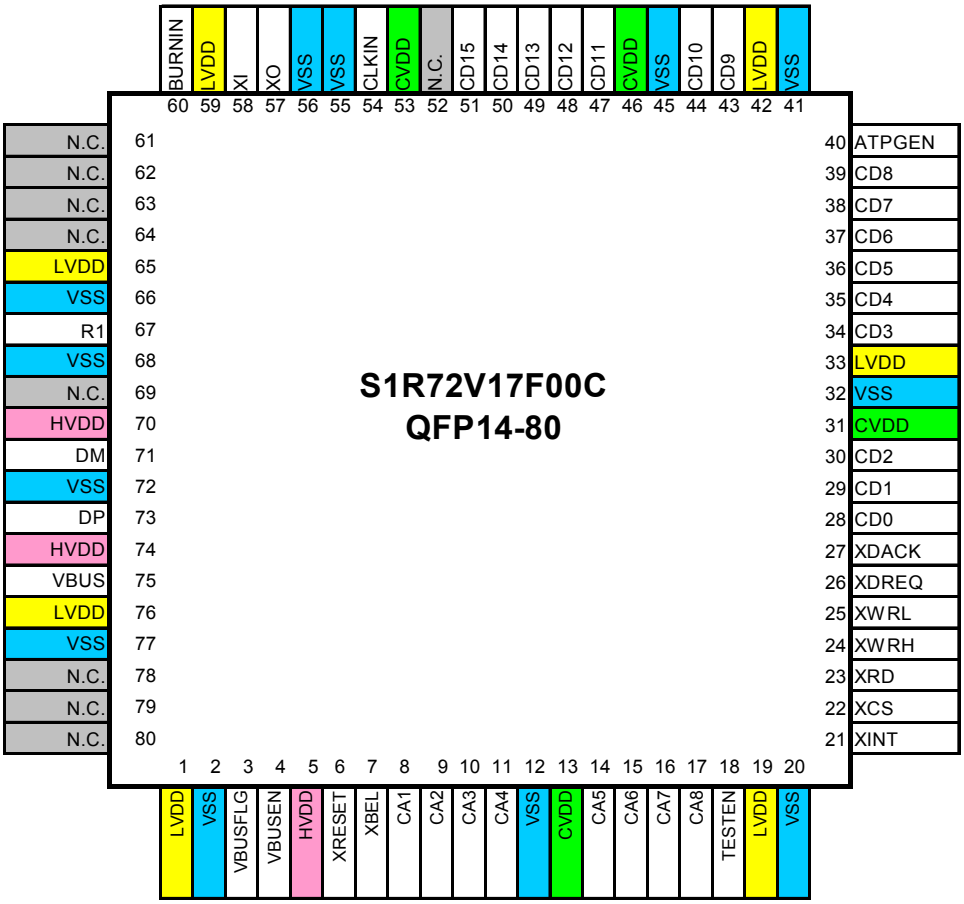

Fig. 4.3 Pin Layout Diagram of the QFP14.80 package

5. Pin Description

OSC

QFP14	PFBGA8	PFBGA5	Name	I/O	RESET	Pin Type	Pin Description
58	B9	B8	XI	IN	-	Analog	Input for the internal oscillator circuit 12 MHz/24 MHz
57	C9	C8	XO	OUT	-	Analog	Output for the internal oscillator circuit

To use the internal oscillator of the LSI, connect a crystal resonator and oscillator circuit to the XI and XO pins and attach the CLKIN pin to the GND potential. To use an external clock by feeding it from the CLKIN pin, attach the XI pin to the GND potential and leave the XO pin open.

TEST

QFP14	PFBGA8	PFBGA5	Name	I/O	RESET	Pin Type	Pin Description
18	G3	H1	TESTEN	IN	(PD)	PD	Test pin (fixed low)
40	H8	H8	ATPGEN	IN	(PD)	PD	Test pin (fixed low)
60	C7	A8	BURNIN	IN	(PD)	PD	Test pin (fixed low)

PD: Pull Down

PU: Pull Up

USB

QFP14	PFBGA8	PFBGA5	Name	I/O	RESET	Pin Type	Pin Description
67	A7	A6	R1	IN	-	Analog	Internal operation setup pin 6.2 kΩ±1% resistor connected between this pin and VSS
73	A4	A3	DP	BI	Hi-Z	Analog	USB data line, Data+
71	A5	A4	DM	BI	Hi-Z	Analog	USB data line, Data–
3	C1	B1	VBUSFLG	IN	(PU)	Schmitt PU	USB power switch fault detection signal 1: Normal; 0: Erratic
4	D2	C1	VBUSEN	OUT	Lo	2mA	USB power switch control signal
75	B3	C3	VBUS	IN	(PD)	PD	USB device bus detection signal

PD: Pull Down

PU: Pull Up