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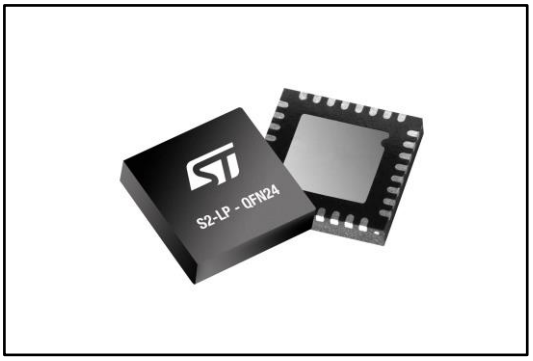
S2-LP

Ultra-low power, high performance, sub-1GHz transceiver

Datasheet - production data



Features

- Frequency bands:
  - 430-470 MHz
  - 860-940 MHz
- Modulation schemes:
  - 2(G)FSK, 4(G)FSK
  - OOK, ASK
- Air data rate from 0.3 to 500 kbps
- Ultra-low power consumption:
  - 7 mA RX
  - 10 mA TX @ +10 dBm
- Excellent performance of receiver sensitivity: down to -130 dBm
- Excellent receiver selectivity and blocking
- Programmable RF output power up to +16 dBm
- Bit rate from 0.3 to 500 kbps
- Programmable RX digital filter
- Programmable channel spacing
- Fast startup and frequency synthesizer settling time
- Automatic frequency offset compensation, AGC and symbol timing recovery
- More than 140 dB RF link budget
- Battery indicator and low battery detector
- RX and TX FIFO buffers
- 4 wires SPI interface
- Automatic packet acknowledgment and retransmission
- Embedded timeout protocol engine
- Antenna diversity algorithm
- Fully integrated ultra-low power RC oscillator
- Wake-up driven by internal timer or external event
- Digital real time RSSI
- Flexible packet length with dynamic payload length
- Programmable preamble and SYNC word quality filtering and detection
- Embedded CSMA/CA engine based on listen-before-talk systems
- IEEE 802.15.4g hardware packet support with whitening, FEC, CRC and dual SYNC word detection
- Wireless M-BUS supported
- Enables operations in the SIGFOX™ networks
- Suitable to build systems targeting:
  - **Europe**: ETSI EN 300 220, ETSI EN 303 131
  - **US**: FCC part 15 and part 90
  - **Japan**: ARIB STD T67, T108
  - **China**: SRRC
- Operating temperature range:
  - -40 °C to +85 °C

Applications

- Sensors to Cloud
- Smart metering
- Home energy management systems
- Wireless alarm systems
- Smart home
- Building automation
- Industrial monitoring and control
- Smart lighting systems

Table 1: Device summary

Order code	Package	Packing
S2-LPQTR	QFN24 4x4x1	Tape and reel

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1 Description

The S2-LP is a high performance ultra-low power RF transceiver, intended for RF wireless applications in the sub-1 GHz band. It is designed to operate in both the license-free ISM and SRD frequency bands at 433, 868 and 920 MHz, but can also be programmed to operate at other additional frequencies in the 430-470 MHz, 860-940 MHz bands.

The S2-LP supports different modulation schemes: 2(G)FSK, 4(G)FSK, OOK and ASK. The air data rate is programmable from 0.3 to 500 kbps.

The S2-LP can be used in systems with channel spacing of 12.5/25 kHz enabling the narrow band operations.

The S2-LP shows an RF link budget higher than 140 dB for long communication ranges and meets the regulatory requirements applicable in territories worldwide, including Europe, Japan, China and the USA.

2 Detailed functional description

The S2-LP integrates a configurable baseband modem with proprietary fully programmable packet format allowing also:

- IEEE 802.15.4g applications
  - The hardware packet supports whitening, CRC, FEC and dual SYNC word detection.
- Wireless M-Bus applications

In order to reduce the overall system power consumption and increase the communication reliability, the S2-LP provides an embedded programmable automatic packet acknowledgment, automatic packet retransmission, CSMA/CA engine, low duty cycle protocol, RX sniff mode and timeout protocol.

The S2-LP fully supports antenna diversity with an integrated antenna switching control algorithm.

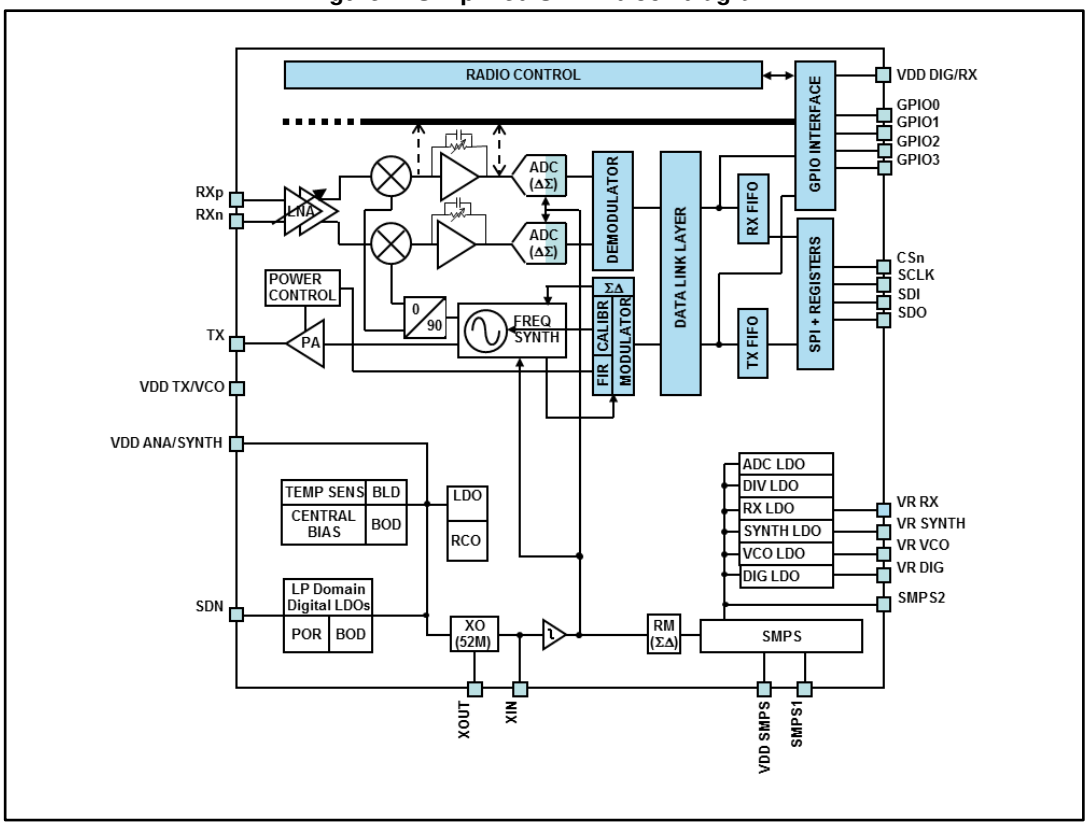
Transmitted/received data bytes are buffered in two different 128 bytes FIFOs (TX FIFO and RX FIFO), accessible via SPI interface for host processing.

In addition, the reduced number of external components enables a cost effective solution permitting a compact PCB footprint.

The S2-LP targets volume applications like:

- sensors to Cloud
- smart metering
- home energy management systems
- wireless alarm systems
- smart home
- building automation
- industrial monitoring and control

Figure 1: Simplified S2-LP block diagram



The receiver architecture is low-IF conversion, the received RF signal is amplified by a two-stage low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). LNA and IF amplifiers make up the RX front-end (RXFE) and have programmable gain. At IF, the ADCs digitalize the I/Q signals. The demodulated data go to an external MCU either through the 128-byte RX FIFO, readable via SPI, or directly using a programmable GPIO pin.

The transmitter part of the S2-LP is based on direct synthesis of the RF frequency. The power amplifier (PA) input is the LO generated by the RF synthesizer, while the output level can be configured between -30 dBm and +14 dBm (+16 dBm in boost mode), at pin level with 0.5 dB steps.

The data to be transmitted can be provided by an external MCU either through the 128-byte TX FIFO writable via SPI, or directly using a programmable GPIO pin. The S2-LP supports frequency hopping, TX/RX and antenna diversity switch control, extending the link range and improving performance.

The S2-LP has a very efficient power management (PM) system. An integrated switched mode power supply (SMPS) regulator allows operation from a battery voltage ranging from +1.8 V to +3.6 V, and with power conversion efficiency of 90%.

A crystal must be connected between XIN and XOUT. It is digitally configurable to operate with different crystals. As an alternative, an external clock signal can be used to feed XIN for proper operation. The S2-LP also has an integrated low-power RC oscillator, generating the 34.7 kHz signal used as a clock for the slowest timeouts.

A standard 4-pin SPI bus is used to communicate with the external MCU. Four configurable general purpose I/Os are available.

3 Typical application diagram and pin description

This section describes two different application diagrams for the S2-LP. *Figure 2: "Suggested application diagram (embedded SMPS used)"* shows the suggested configuration with SMPS-ON.

Figure 2: Suggested application diagram (embedded SMPS used)

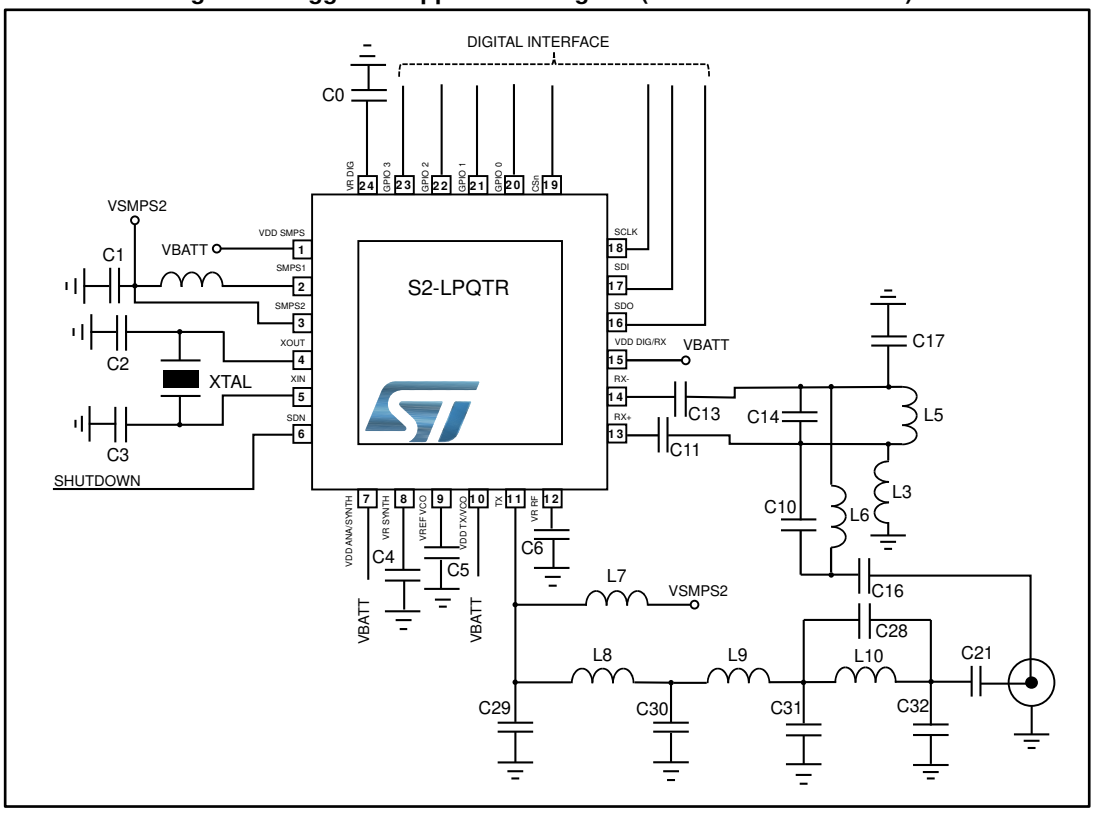


Figure 3: "Suggested application diagram (embedded SMPS not used)" shows the SMPS-OFF mode application diagram, it allows to improve the sensitivity paying that with an increasing of the power consumption.

Figure 3: Suggested application diagram (embedded SMPS not used)

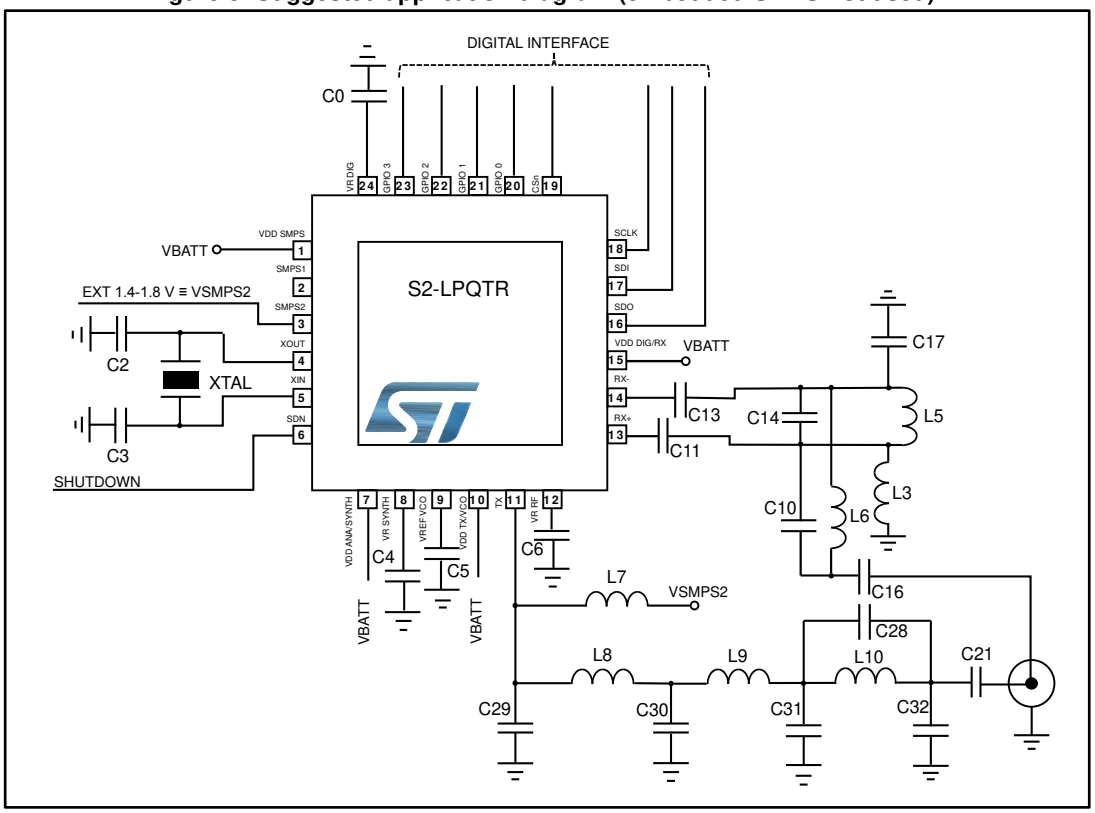


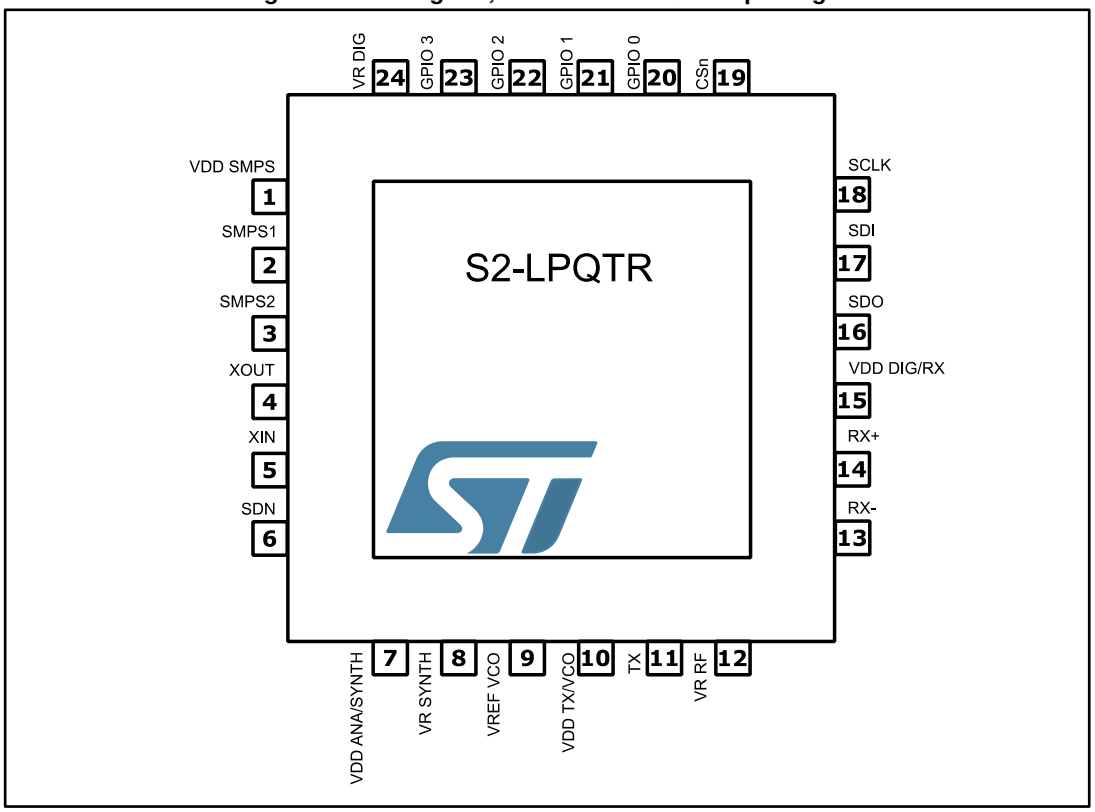
Table 2: Description of the external components of the typical application diagrams

Components	SMPS ON	SMPS OFF	Description
C0	X	X	Decoupling capacitor for on-chip voltage regulator to digital part
C1	X	-	SMPS LC filter capacitors
C2, C3	X	X	Crystal loading capacitors
C4	X	X	Decoupling capacitor for on-chip voltage regulator to synthesizer (LF part)
C5	X	X	Decoupling capacitor for band-gap voltage reference of VCO regulator
C6	X	X	Decoupling capacitor for on-chip voltage regulator to LNA-MIXER
C29, C30, C31, C32	X	X	TX LC filter/matching capacitors
C11, C13, C16, C21	X	X	DC blocking capacitors
C10, C14, C17	X	X	RF balun/matching capacitors
L0	X	-	SMPS LC filter inductor
L7	X	X	RF choke inductor or resonating inductor (upon RF network topology)
L8, L9, L10	X	X	TX LC filter/matching inductors

Components	SMPS ON	SMPS OFF	Description
L3, L5, L6	X	X	RX balun/matching inductors
XTAL	X	X	Crystal

3.1 Pin diagram

Figure 4: Pin diagram, 4 mm x 4 mm QFN24 package



3.2 Pin description

Table 3: Pinout

N.	Pin name	Pin type	Description
1	VDD SMPS	Power	1.8 V to 3.6 V analog power supply for SMPS only.
2	SMPS1	Analog out	1.1 V to 1.8 V SMPS regulator output to be externally filtered.
3	SMPS2	Analog in	1.1 V to 1.8 V SMPS voltage input after LC filtering applied to SMPS1 output.
4	XOUT	Analog out	Crystal oscillator output. Connect to an external crystal or leave floating if driving the XIN pin with an external clock source.
5	XIN	Analog in	Crystal oscillator input. Connect to an external crystal or to an external clock source. If using an external clock source, DC coupling with a minimum 0.2 VDC level is recommended and minimum AC amplitude of 400 mVpp (however, the instantaneous level at input cannot exceed the 0 – 1.4 V range).

N.	Pin name	Pin type	Description
6	SDN	Digital in	Shutdown input pin. SDN should be = '0' in all modes, but SHUTDOWN mode
7	VDD ANA/ SYNTH	Power	1.8 V to 3.6 V power
8	VR SYNTH	Analog in/out	1.2 V SYNTH-LDO output for decoupling
9	VREF VCO	Analog out	1.2 V VCO-LDO for decoupling
10	VDD VCO/TX	Power	1.8 V to 3.6 V power supply
11	TX	RF output	RF output signal
12	VR RF	Analog in/out	1.2 V RX-LDO output for decoupling
13	RXn	RF in	Differential RF input signals for the LNA
14	RXp	RF in	
15	VDD RX/DIG	Power	1.8 V to 3.6 V power supply
16	SDO	Digital out	SPI slave data output
17	SDI	Digital in	SPI slave data input
18	SCLK	Digital in	SPI slave clock input
19	CSn	Digital in	SPI chip select
20	GPIO0	Digital I/O	General purpose I/O that may be configured through the SPI registers to perform various functions
21	GPIO1	Digital I/O	
22	GPIO2	Digital I/O	
23	GPIO3	Digital I/O	
24	VR DIG	Analog in/out	1.2 V digital power supply output for decoupling

4 Specifications

4.1 Absolute maximum ratings

Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages refer to GND.

Table 4: Absolute maximum ratings

Parameter	Min.	Typ.	Max.	Unit
Supply and SMPS pins	-0.3		+3.9	V
DC voltage on VREG pins	-0.3		+3.9	
DC voltage on digital input pins	-0.3		+3.9	
DC voltage on digital output pins	-0.3		+3.9	
DC voltage on ground pins	-0.3		+3.9	
DC voltage on analog pins	-0.3		+1.8	
DC voltage on TX pin	-0.3		+3.9	
Storage temperature range	-40		+105	°C
VESD-HBM	-500		+500	V

4.2 Operating range

Table 5: Operating range

Parameter	Min.	Typ.	Max.	Unit
Operating battery supply voltage (V_{BAT})	1.8	3.0	3.6	V
Operating ambient temperature range	-40	25	85	°C

4.3 Thermal properties

Table 6: Thermal data

Parameter	QFN24	Unit
Thermal resistance junction-ambient	66	°C/W

4.4 Power consumption

Characteristics measured over recommended operating conditions unless otherwise specified. Typical values are referred to 25 °C temperature, V_{BAT} = 3.0 V. All performance is referred to a 50 Ω antenna connector.

Table 7: Low-power states power consumption

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current	Shutdown	-	2.5	-	nA
	Standby		350		
	Sleep		600		
	Sleep (FIFOs retained)		0.9		µA
	Ready		350		

Table 8: Power consumption in reception TA = 25°C, VDD = 3.0 V, fc = 868 MHz

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current	RX @ sensitivity level		8		mA
	RX in sniff mode @ 1.2 kbps(1)		0.9		
	RX in sniff mode @ 38.4 kbps(2)		0.8		
	RX in LDC mode @ 1.2 kbps(3)	-	21	-	µA
	RX in LDC mode @ 38.4 kbps(4)		3		

Notes:

(1)Using 2-FSK 2.4 kHz DEV, DR=1.2 kbps, 4 bytes preamble and 8kHz ch. filter. Where the receiver wakes up at regular intervals to look for an incoming packet.

(2)Using 2-FSK 20 kHz DEV, DR=38.4 kbps, 24 bytes preamble and 100kHz ch. filter. Where the receiver wakes up at regular intervals to look for an incoming packet.

(3)Check for data packet every 1 second in LDC mode. 2-FSK 1.2 kHz DEV and 8kHz ch. filter, DR=1.2 kbps, internal RC oscillator used as sleep timer. Sniff timer enabled.

(4)Check for data packet every 1 second in LDC mode. 2-FSK 20 kHz DEV, DR=38.4 kbps and 100 kHz ch. filter, internal 34.6 kHz RC oscillator used as sleep timer. Sniff timer enabled.

Table 9: Power consumption in transmission fc= 920 MHz

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current	TX CW @ 14 dBm		20.6		mA
	TX CW @ 10 dBm		11.7		
	TX CW @ 16 dBm in Boost(1)		27		

Notes:

(1)SMPS output voltage 1.8 V

Table 10: Power consumption in transmission fc= 868 MHz

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current	TX CW @ 14 dBm		19		mA
	TX CW @ 10 dBm		10.7		
	TX CW @ 16 dBm in Boost(1)		25		

Notes:

(1)SMPS output voltage 1.8 V

Table 11: Power consumption in transmission fc= 434 MHz

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Supply current	TX CW @ 14 dBm		19		mA
	TX CW @ 10 dBm		10.2		

4.5 General characterization

Table 12: General characteristics

Parameter		Typ.	Unit
Frequency range		430 - 470	MHz
		860 - 940	
Data rate DR	2-(G)FSK	0.3 - 250	kbps
	4-(G)FSK	0.6 - 500	
	OOK/ASK	0.3 -125	
Data rate accuracy		±100	ppm
Frequency deviation FDEV		0.15 - 500	kHz

If "Manchester" or "3-out-of-6" or FEC coding options are enabled the actual bit rate is affected as follows

Table 13: Data rate with different coding options

Coding option	4(G)FSK Data rate [kbps]
NRZ	500
FEC	250
Manchester	250
3-out-of-6	333.3

4.6 Frequency synthesizer

Table 14: Frequency synthesizer parameters

Parameter	Test conditions	50 MHz	Unit
Frequency step size	Out-Loop Divider Ratio = 4	25	Hz
RF carrier phase noise 433 MHz	10 kHz	-111.5	dBc/Hz
	100 kHz	-111.8	
	1 MHz	-124.4	
RF carrier phase noise 868 MHz	10 kHz	-104	
	100 kHz	-104.5	
	1 MHz	-119.5	
RF carrier phase noise 915 MHz	10 kHz	-104	
	100 kHz	-104	
	1 MHz	-119	
PLL tuning voltage settling time @ 1% (RX/TX transitions: Δf = IF)	Typical intermediate frequency (IF): 300 kHz	55	µs
PLL calibration time		12	µs

4.7 Crystal oscillator

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to 25 °C temperature, V_{BAT} = 3.0 V.

The device supports crystals in the range [24-26] MHz and [48-52] MHz.

If the crystal is in the [24–26] MHz range, both the analog and the digital parts must work at this frequency. Otherwise, if a crystal in the [48-52] MHz range is used, the analog part must work at this frequency and the digital part at this frequency divided by 2. From now on in this document the XTAL oscillator will be indicated with f_{XO} and the digital clock with f_{dig}.

The divider for the digital part can be set by the PD_CLKDIV bit of the XO_RCO_CONFIG1 in the following way:

- if a [48 – 52] MHz crystal is used, this bit must be 0 (digital divider enabled: $f_{dig} = \frac{f_{xo}}{2}$)
- if a [24 – 26] MHz crystal is used, this bit must be 1 (digital divider disabled: $f_{dig} = f_{xo}$).

The safest procedure to disable the divider without any risk of glitches in the digital clock is to switch into STANDBY mode, hence, disable the divider through register setting, and then come back to the READY state.

In order to avoid potential RF performance degradations, the crystal frequency should be chosen to satisfy the following equation:

$$nF_{CH} - \mathrm{ROUND}\left(n\frac{F_{CH}}{f_{XO}}\right)f_{XO} \geq 1\mathrm{MHz}$$

where n is an integer in the set [1-7, B] (B is the synthesizer's divider ratio).

Table 15: Crystal oscillator characteristics

Parameter	Test conditions	Min.	Typ.	Max.	Unit
Crystal frequency		24		26	MHz
		48		52	
Frequency tolerance(1)			± 40		ppm
Minimum requirement on external reference phase noise mask ($f_{XO} = 26\mathrm{MHz}$), to avoid degradation on synthesizer phase/noise	10 kHz			-135	dBc/Hz
	100 kHz			-140	
	1 MHz			-140	
	10 MHz			-140	
Programmable trans-conductance of the oscillator at start-up			13 -43		mS
Startup time(2)	VBAT=1.8 V, < $f_{XO} = 26\mathrm{MHz}$		200		µs

Notes:

(1)Including initial tolerance, crystal loading, aging, and temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing/bandwidth.

(2)Startup times are crystal dependent. The crystal oscillator trans-conductance can be tuned to compensate the variation of crystal oscillator series resistance

Table 16: Ultra-low power RC oscillator

Parameter	Test conditions	Typ.	Unit
Calibrated frequency	Calibrated RC oscillator frequency is derived from crystal oscillator frequency.	33.3(1)	kHz
Frequency accuracy after calibration		±1	%

Notes:

(1)Depending on the crystal frequency, the reported value is referring to 50MHz.

4.8 RF receiver

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to 25 °C temperature, V_{BAT} = 3.0 V, no frequency offset in the RX signal. All performance is referred to a 50 Ω antenna connector, via the reference design.

Table 17: RF receiver characteristics

Parameter	Test condition		SMPS on	Unit
Receiver channel bandwidth CHF			1-800	kHz
RX input return loss	Max RX gain, tied (RX + TX) matching networks	433 MHz	-15	dB
		868 MHz	-15	
Saturation 1% BER	2-FSK 1.2 kHz FDEV, DR = 1.2 kbps, CHF = 4 kHz	433 MHz	10	dBm
		868 MHz	10	
Input third order intercept point	Interferers are continuous wave @ 6 MHz and 12 MHz offset from carrier.	433 MHz	-23	
		868 MHz	-20	
RX noise figure	Max RX gain, tied (RX + TX) matching networks	433 MHz	8.5	dB
		868 MHz	8.5	
Differential input impedance at LNA	Max RX gain R // C	433 MHz	200 // 1.5	Ω//pF
		868 MHz	200 // 1.5	

4.8.1 Blocking and selectivity at 433 MHz

Table 18: Blocking and selectivity at 433 MHz

Parameter	Test condition	SMPS on	Unit
Selectivity and blocking 1% BER @ 2-GFSK BT=0.5 1.2 kHz FDEV, DR = 1.2 kbps, CHF = 4 kHz	+12.5 kHz (adjacent channel)	68	dB
	-12.5 kHz (adjacent channel)	68	
	+25 kHz (alternate channel)	67	
	-25 kHz (alternate channel)	67	
	Image rejection	67	
	±2 MHz	80	
	±10 MHz	83	
Selectivity and blocking 1% BER @ 2-GFSK BT=0.5 20 kHz FDEV, DR = 38.4 kbps, CHF = 100 kHz	+100 kHz (adjacent channel)	51	dB
	-100 kHz (adjacent channel)	51	
	+200 kHz (alternate channel)	51	
	-200 kHz (alternate channel)	51	
	Image rejection	56	
	±2 MHz	68	
	±10 MHz	69	

4.8.2 Sensitivity at 433 MHz

Table 19: Sensitivity at 433 MHz

Parameter	Test conditions	SMPS on	Unit
Sensitivity 1% BER @ 2-GFSK BT = 0.5	DR = 0.3 kbps, FDEV = 0.25 kHz, CHF = 1 kHz	-131	dBm
	DR = 1.2 kbps, FDEV = 1.2 kHz, CHF = 4 kHz	-125	
	DR = 38.4 kbps, FDEV = 20 kHz, CHF = 100 kHz	-111	
	DR = 100 kbps, FDEV = 50 kHz, CHF = 200 kHz	-106	
Sensitivity 1% BER @ 4-GFSK BT = 0.5	DR = 4.8 kbps, DEV = 2.4 kHz, CHF = 10 kHz	-117	dBm
	DR = 9.6 kbps, DEV = 4.8 kHz, CHF = 20 kHz	-113	
	DR = 19.2 kbps, DEV = 9.6 kHz, CHF = 40 kHz	-110	
Sensitivity 1% BER @ OOK	DR = 0.3 kbps, CHF = 1 kHz	-122	dBm
	DR = 1.2 kbps, CHF = 4 kHz	-120	
	DR = 38.4 kbps, CHF = 100 kHz	-107	
	DR = 125 kbps, CHF = 250 kHz	-100	

4.8.3 Blocking and selectivity at 868 MHz

Table 20: Blocking and selectivity at 868 MHz

Parameter	Test condition	SMPS on	Unit
Selectivity and blocking 1% BER @ 2-GFSK BT=0.5 1.2 kHz FDEV, DR = 1.2 kbps, CHF = 4 kHz	+12.5 kHz (adjacent channel)	60	dB
	-12.5 kHz (adjacent channel)	60	
	+25 kHz (alternate channel)	61	
	-25 kHz (alternate channel)	61	
	Image rejection	59	
	± 2MHz	82	
	± 10MHz	83	
Selectivity and blocking 1% BER @ 2-GFSK BT=0.5 20 kHz FDEV, DR = 38.4 kbps, CHF = 100 kHz	+100 kHz (adjacent channel)	45	dB
	-100 kHz (adjacent channel)	45	
	+200 kHz (alternate channel)	47	
	-200 kHz (alternate channel)	47	
	Image rejection	49	
	±2 MHz	68	
	±10 MHz	69	

4.8.4 Sensitivity at 868 MHz

Table 21: Sensitivity at 868 MHz

Parameter	Test conditions	SMPS on	Unit
Sensitivity 1% BER @ 2-GFSK BT = 0.5	DR = 0.3 kbps, FDEV = 0.25 kHz, CHF = 1 kHz	-129	dBm
	DR = 1.2 kbps, FDEV = 1.2 kHz, CHF = 4 kHz	-123	
	DR = 38.4 kbps, FDEV = 20 kHz, CHF = 100 kHz	-110	
	DR = 100 kbps, FDEV = 50 kHz, CHF = 200 kHz	-107	
Sensitivity 1% BER @ 4-GFSK BT = 0.5	DR = 4.8 kbps, DEV = 2.4 kHz, CHF = 10 kHz	-115	dBm
	DR = 9.6 kbps, DEV = 4.8 kHz, CHF = 20 kHz	-112	
	DR = 19.2 kbps, DEV = 9.6 kHz, CHF = 40 kHz	-110	
Sensitivity 1% BER @ OOK	DR = 0.3 kbps, CHF = 1 kHz	-121	dBm
	DR = 1.2 kbps, CHF = 4 kHz	-120	
	DR = 38.4 kbps, CHF = 100 kHz	-106	
	DR = 125 kbps, CHF = 250 kHz	-101	

4.8.5 Blocking and selectivity at 920 MHz

Table 22: Blocking and selectivity at 920 MHz

Parameter	Test condition	SMPS on	Unit
Selectivity and blocking 1% BER @ 2-GFSK BT=0.5 1.2 kHz FDEV, DR = 1.2 kbps, CHF = 4 kHz	+12.5 kHz (adjacent channel)	58	dB
	-12.5 kHz (adjacent channel)	58	
	+25 kHz (alternate channel)	59	
	-25 kHz (alternate channel)	59	
	Image rejection	59	
	±2 MHz	83	
	±10 MHz	84	
Selectivity and blocking 1% BER @ 2-GFSK BT=0.5 20 kHz FDEV, DR = 38.4 kbps, CHF = 100 kHz	+100 kHz (adjacent channel)	43	dB
	-100 kHz (adjacent channel)	43	
	+200 kHz (alternate channel)	45	
	-200 kHz (alternate channel)	45	
	Image rejection	48	
	±2 MHz	69	
	±10 MHz	71	

4.8.6 Sensitivity at 920 MHz

Table 23: Sensitivity at 920 MHz

Parameter	Test conditions	SMPS ON	Unit
Sensitivity 1% BER @ 2-GFSK BT = 0.5	DR = 0.3 kbps, FDEV = 0.25 kHz, CHF = 1 kHz	-128	dBm
	DR = 1.2 kbps, FDEV = 1.2 kHz, CHF = 4 kHz	-122	
	DR = 38.4 kbps, FDEV = 20 kHz, CHF = 100 kHz	-109	
	DR = 100 kbps, FDEV = 50 kHz, CHF = 200 kHz	-105	
Sensitivity 1% BER @ 4-GFSK BT = 0.5	DR = 4.8 kbps, DEV = 2.4 kHz, CHF = 10 kHz	-114	dBm
	DR = 9.6 kbps, DEV = 4.8 kHz, CHF = 20 kHz	-112	
	DR = 19.2 kbps, DEV = 9.6 kHz, CHF = 40 kHz	-108	
Sensitivity 1% BER @ OOK	DR = 0.3 kbps, CHF = 1 kHz	-121	dBm
	DR = 1.2 kbps, CHF = 4 kHz	-118	
	DR = 38.4 kbps, CHF = 100 kHz	-105	
	DR = 125 kbps, CHF = 250 kHz	-100	

4.9 RF transmitter

Characteristics measured over recommended operating conditions unless otherwise specified. All typical values are referred to 25 °C temperature, V_{BAT} = 3.0 V. All performance is referred to a 50 Ω antenna connector, via the reference design.

Table 24: RF transmitter characteristics

Parameter	Test conditions	Typ.	Unit
Maximum output power	CW @ antenna level	14	dBm
Maximum output power in boost mode	CW @ antenna level	16	
Minimum output power	CW @ antenna level	-30	
Output power step		0.5	dB

Table 25: PA impedance

Parameter	Test conditions	Typ.	Unit
Optimum load impedance	433 MHz	56+25j	Ω
	868 MHz	30+24j	
	920 MHz	29+23j	

Table 26: Regulatory standards

Frequency band	Suitable for compliance with:
430 - 470 MHz	ETSI EN300 220 category 2
	FCC part 15, FCC part 90
	ARIB STD-T67
	Chinese SRRC
860 - 940 MHz	ETSI EN300 220-2
	FCC part 15
	ARIB STD-T108
	Chinese SRRC

4.9.1 Harmonic emission at 433 MHz

Table 27: Harmonic emission at 433 MHz

Parameter	Test conditions	SMPS on	Unit
H1	CW	14	dBm
H2	CW	-51	
H3	CW	-56	
H4	CW	-39	
H5	CW	-34	
H6	CW	-46	
H7	CW	-44	

4.9.2 Harmonic emission at 868 MHz

Table 28: Harmonic emission at 868 MHz

Parameter	Test conditions	SMPS on	Unit
H1	CW	14	dBm
H2	CW	-38	
H3	CW	-54	
H4	CW	-52	
H5	CW	-52	
H6	CW	-43	
H7	CW	-51	

4.9.3 Harmonic emission at 915 MHz

Table 29: Harmonic emission at 915 MHz

Parameter	Test conditions	SMPS on	Unit
H1	CW	14	dBm
H2	CW	-46	
H3	CW	-55	
H4	CW	-46	
H5	CW	-49	
H6	CW	-48	
H7	CW	-51	

4.10 Digital interface specification

Table 30: Digital SPI input, output and GPIO specification

Parameter	Test condition	Min.	Typ.	Max.	Unit
SPI clock frequency			8	10	MHz
Port I/O capacitance			1.4		pF
Rise time	From 0.1*VDD to 0.9*VDD, CL=20 pF (low output current programming)		6.0		ns
	From 0.1*VDD to 0.9*VDD, CL=20 pF (high output current programming)		2.5		
Fall time	From 0.1*VDD to 0.9*VDD, CL=20 pF (low output current programming)		7.0		ns
	From 0.1*VDD to 0.9*VDD, CL=20 pF (high output current programming)		2.5		
Logic high level input voltage		VDD/2 +0.3			V
Logic low level input voltage				VDD/8 +0.3	V
High level output voltage	IOH = -2.4 mA (-4.2 mA into high output current mode).	(5/8)* VDD+ 0.1			V
Low level output voltage	IOL = +2.0 mA (+4.0 mA into high output current mode).			0.5	V
CSn low to positive edge on SCLK in ready state			40		µs