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S25FL064P

64-Mbit 3.0 V SPI Flash Memory

Distinctive Characteristics

Architectural Advantages

- Single power supply operation
  - Full voltage range: 2.7 to 3.6V read and write operations
- Memory architecture
  - Uniform 64-kB sectors
    - Top or bottom parameter block (Two 64-kB sectors (top or bottom) broken down into sixteen 4-kB sub-sectors each)
  - 256-byte page size
  - Backward compatible with the S25FL064A device
- Program
  - Page Program (up to 256 bytes) in 1.5 ms (typical)
  - Program operations are on a page by page basis
  - Accelerated programming mode via 9V W#/ACC pin
  - Quad Page Programming
- Erase
  - Bulk erase function
  - Sector erase (SE) command (D8h) for 64-kB sectors
  - Sub-sector erase (P4E) command (20h) for 4-kB sectors
  - Sub-sector erase (P8E) command (40h) for 8-kB sectors
- Cycling endurance
  - 100,000 cycles per sector typical
- Data retention
  - 20 years typical
- Device ID
  - JEDEC standard two-byte electronic signature
  - RES command one-byte electronic signature for backward compatibility
- One time programmable (OTP) area for permanent, secure identification; can be programmed and locked at the factory or by the customer
- CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
- Process technology
  - Manufactured on 90-nm MirrorBit® process technology
- Package option
  - Industry Standard Pinouts
  - 16-pin SO package (300 mils)
  - 8-contact WSON package (6 × 8 mm)
  - 24-ball BGA package (6 × 8 mm), 5 × 5 pin configuration
  - 24-ball BGA package (6 × 8 mm), 6 × 4 pin configuration

Performance Characteristics

- Speed
  - Normal READ (Serial): 40 MHz clock rate
  - FAST_READ (Serial): 104 MHz clock rate (maximum)
  - DUAL I/O FAST_READ: 80 MHz clock rate or 20 MB/s effective data rate
  - QUAD I/O FAST_READ: 80 MHz clock rate or 40 MB/s effective data rate
- Power saving standby mode
  - Standby Mode 80 µA (typical)
  - Deep Power-Down Mode 3 µA (typical)

Memory Protection Features

- Memory protection
  - W#/ACC pin works in conjunction with Status Register Bits to protect specified memory areas
  - Status Register Block Protection bits (BP2, BP1, BP0) in status register configure parts of memory as read-only

Software Features

- SPI Bus Compatible Serial Interface

General Description

The S25FL064P is a 3.0 Volt (2.7V to 3.6V), single-power-supply flash memory device. The device consists of 128 uniform 64 kB sectors with the two (Top or Bottom) 64 kB sectors further split up into thirty-two 4 kB sub sectors. The S25FL064P device is fully backward compatible with the S25FL064A device.

The device accepts data written to SI (Serial Input) and outputs data on SO (Serial Output). The devices are designed to be programmed in-system with the standard system 3.0-volt V_{CC} supply.

The S25FL064P device adds the following high-performance features using 5 new instructions:

- Dual Output Read using both SI and SO pins as output pins at a clock rate of up to 80 MHz
- Quad Output Read using SI, SO, W#/ACC and HOLD# pins as output pins at a clock rate of up to 80 MHz
- Dual I/O High Performance Read using both SI and SO pins as input and output pins at a clock rate of up to 80 MHz
- Quad I/O High Performance Read using SI, SO, W#/ACC and HOLD# pins as input and output pins at a clock rate of up to 80 MHz
- Quad Page Programming using SI, SO, W#/ACC and HOLD# pins as input pins to program data at a clock rate of up to 80 MHz

The memory can be programmed 1 to 256 bytes at a time, using the Page Program command. The device supports Sector Erase and Bulk Erase commands.

Each device requires only a 3.0-volt power supply (2.7V to 3.6V) for both read and write functions. Internally generated and regulated voltages are provided for the program operations. This device requires a high voltage supply to the W#/ACC pin to enable the Accelerated Programming mode.

The S25FL064P device also offers a One-Time Programmable area (OTP) of up to 128-bits (16 bytes) for permanent secure identification and an additional 490 bytes of OTP space for other use. This OTP area can be programmed or read using the OTPP or OTPR instructions.

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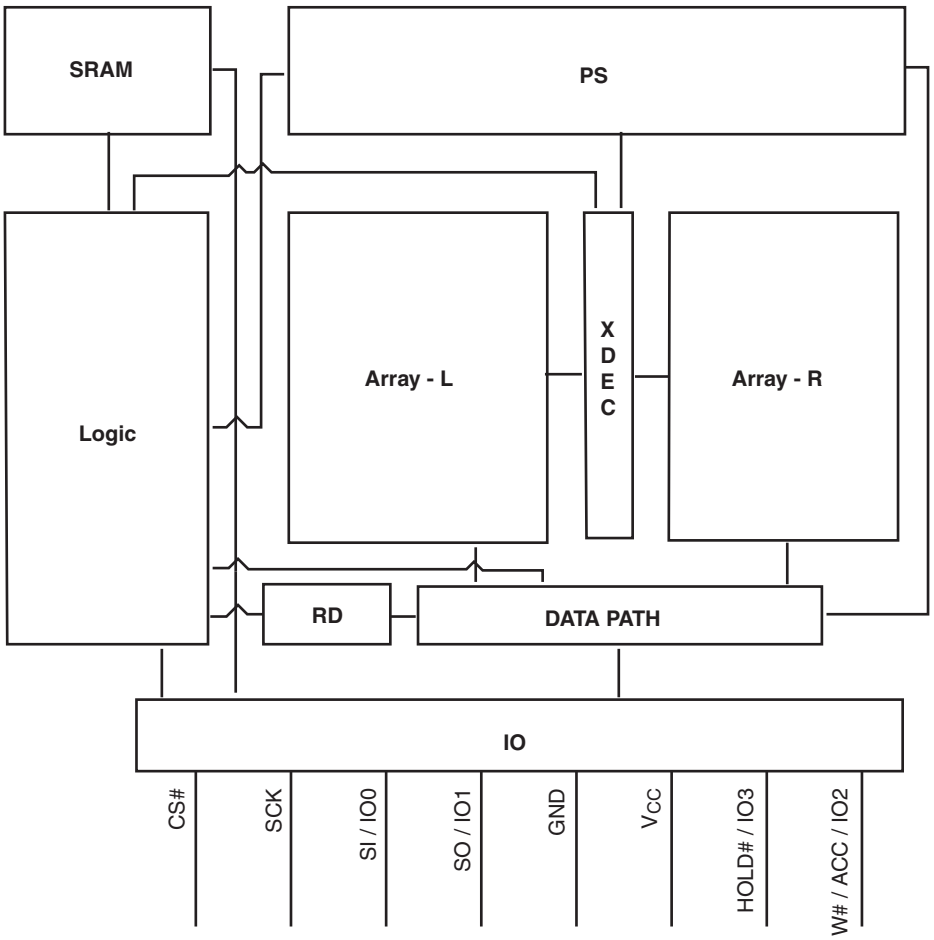
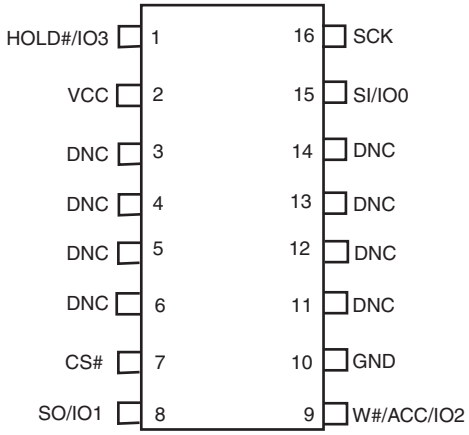
1. Block Diagram



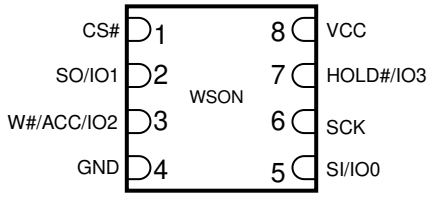
2. Connection Diagrams

Figure 2.1 16-pin Plastic Small Outline Package (SO)



Note
DNC = Do Not Connect (Reserved for future use)

Figure 2.2 8-contact WSON Package (6 x 8 mm)



Note
There is an exposed central pad on the underside of the USON package. This should not be connected to any voltage or signal line on the PCB. Connecting the central pad to GND (V_{SS}) is possible, provided PCB routing ensures 0 mV difference between voltage at the USON GND (V_{SS}) lead and the central exposed pad.

Figure 2.3 6 x 8 mm 24-ball BGA Package, 5 x 5 Pin Configuration

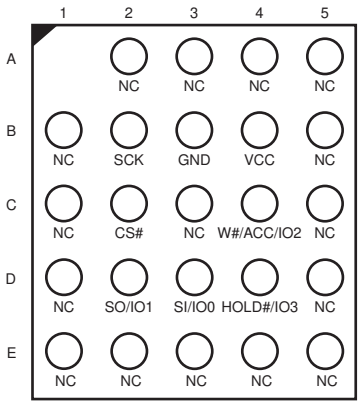
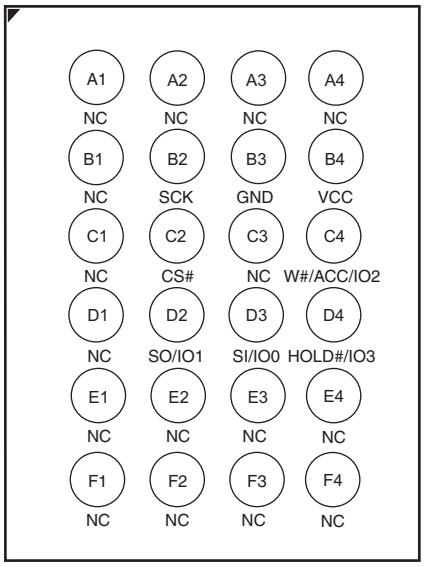


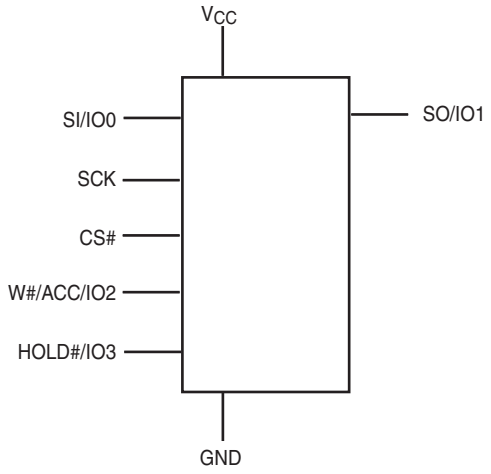
Figure 2.4 6x8 mm 24-ball BGA Package, 6x4 Pin Configuration



3. Input/Output Descriptions

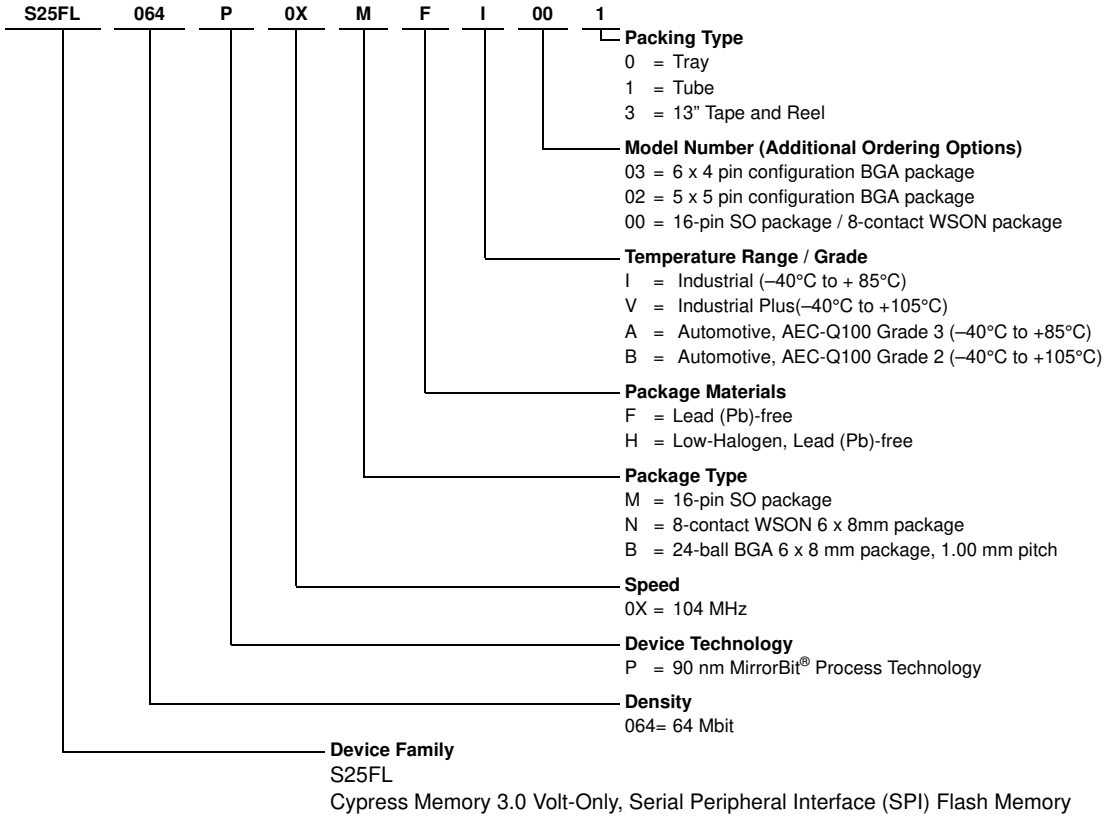
Signal	I/O	Description
SO/IO1	I/O	**Serial Data Output**: Transfers data serially out of the device on the falling edge of SCK. Functions as an input pin in Dual and Quad I/O, and Quad Page Program modes.
SI/IO0	I/O	**Serial Data Input**: Transfers data serially into the device. Device latches commands, addresses, and program data on SI on the rising edge of SCK. Functions as an output pin in Dual and Quad I/O mode.
SCK	Input	**Serial Clock**: Provides serial interface timing. Latches commands, addresses, and data on SI on rising edge of SCK. Triggers output on SO after the falling edge of SCK.
CS#	Input	**Chip Select**: Places device in active power mode when driven low. Deselects device and places SO at high impedance when high. After power-up, device requires a falling edge on CS# before any command is written. Device is in standby mode when a program, erase, or Write Status Register operation is not in progress.
HOLD#/IO3	I/O	**Hold**: Pauses any serial communication with the device without deselecting it. When driven low, SO is at high impedance, and all input at SI and SCK are ignored. Requires that CS# also be driven low. Functions as an output pin in Quad I/O mode.
W#/ACC/IO2	I/O	**Write Protect**: Protects the memory area specified by Status Register bits BP2:BP0. When driven low, prevents any program or erase command from altering the data in the protected memory area. Functions as an output pin in Quad I/O mode.
V_{CC}	Input	**Supply Voltage**
GND	Input	**Ground**

4. Logic Symbol



5. Ordering Information

The ordering part number is formed by a valid combination of the following:



5.1 Valid Combinations

Valid Combinations — Standard

Table 5.1 lists the standard valid combinations configurations planned to be supported in volume for this device.

Table 5.1 S25FL064P Valid Combinations — Standard

S25FL064P Valid Combinations					
Base Ordering Part Number	**Speed Option**	**Package & Temperature**	**Model Number**	**Packing Type**	**Package Marking**
S25FL064P	0X	MFI,NFI	00	0, 1, 3	FL064P + (Temp) + F
		MFV, NFV			
		BHI, BHV	02, 03	0, 3	

Valid Combinations — Automotive Grade / AEC-Q100

Table 5.2 lists configurations that are Automotive Grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Consult your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 5.2 S25FL064P Valid Combinations — Automotive Grade / AEC-Q100

S25FL064P Valid Combinations					
Base Ordering Part Number	**Speed Option**	**Package & Temperature**	**Model Number**	**Packing Type**	**Package Marking**
S25FL064P	0X	MFA,NFA	00	0, 1, 3	FL064P + (Temp) + F
		MFB, NFB			
		BHA, BHB	02, 03	0, 3	

6. SPI Modes

A microcontroller can use either of its two SPI modes to control SPI flash memory devices:

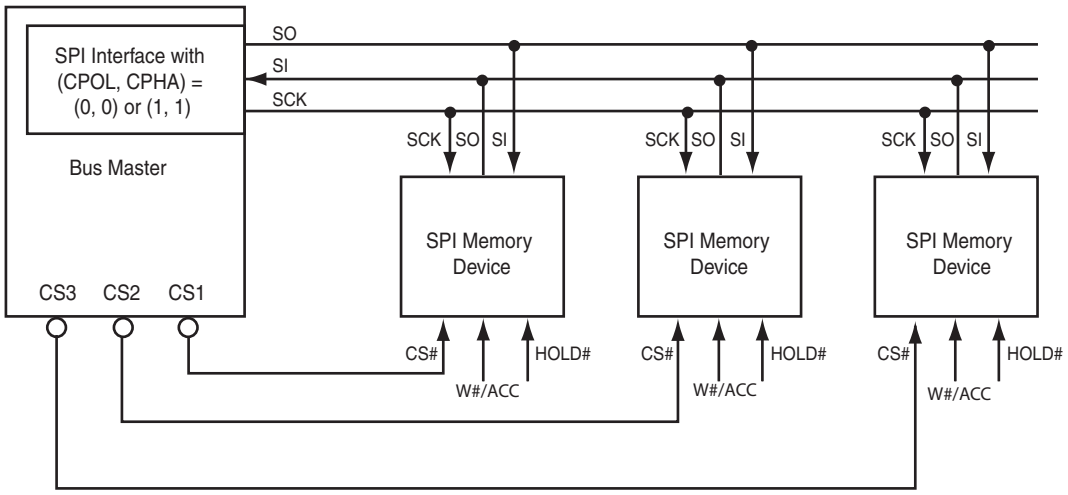
- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

When the bus master is in standby mode, SCK is as shown in Figure 6.2 for each of the two modes:

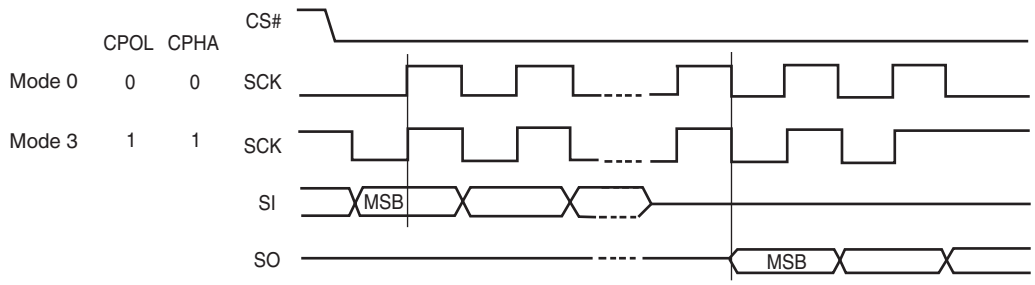
- SCK remains at 0 for (CPOL = 0, CPHA = 0 Mode 0)
- SCK remains at 1 for (CPOL = 1, CPHA = 1 Mode 3)

Figure 6.1 Bus Master and Memory Devices on the SPI Bus



Note
The Write Protect/Accelerated Programming (W#/ACC) and Hold (HOLD#) signals should be driven high (logic level 1) or low (logic level 0) as appropriate.

Figure 6.2 SPI Modes Supported



7. Device Operations

All Cypress SPI devices accept and output data in bytes (8 bits at a time). The SPI device is a slave device that supports an inactive clock while CS# is held low.

7.1 Byte or Page Programming

Programming data requires two commands: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. The Page Program sequence accepts from 1 byte up to 256 consecutive bytes of data (which is the size of one page) to be programmed in one operation. Programming means that bits can either be left at 0, or programmed from 1 to 0. Changing bits from 0 to 1 requires an erase operation.

7.2 Quad Page Programming

The Quad Page Program (QPP) instruction allows up to 256 bytes of data to be programmed using 4 pins as inputs at the same time, thus effectively quadrupling the data transfer rate, compared to the Page Program (PP) instruction. The Write Enable Latch (WEL) bit must be set to a 1 using the Write Enable (WREN) command prior to issuing the QPP command.

7.3 Dual and Quad I/O Mode

The S25FL064P device supports Dual and Quad I/O operation when using the Dual/Quad Output Read Mode and the Dual/Quad I/O High Performance Mode instructions. Using the Dual or Quad I/O instructions allows data to be transferred to or from the device at two to four times the rate of standard SPI devices. When operating in the Dual or Quad I/O High Performance Mode (BBh or EBh instructions), data can be read at fast speed using two or four data bits at a time, and the 3-byte address can be input two or four address bits at a time.

7.4 Sector Erase / Bulk Erase

The Sector Erase (SE) and Bulk Erase (BE) commands set all the bits in a sector or the entire memory array to 1. While bits can be individually programmed from 1 to 0, erasing bits from 0 to 1 must be done on a sector-wide (SE) or array-wide (BE) level. In addition to the 64-kB Sector Erase (SE), the S25FL064P device also offers 4-kB Parameter Sector Erase (P4E) and 8-kB Parameter Sector Erase (P8E).

7.5 Monitoring Write Operations Using the Status Register

The host system can determine when a Write Register, program, or erase operation is complete by monitoring the Write in Progress (WIP) bit in the Status Register. The Read from Status Register command provides the state of the WIP bit. In addition, the S25FL064P device offers two additional bits in the Status Register (P_ERR, E_ERR) to indicate whether a Program or Erase operation was a success or failure.

7.6 Active Power and Standby Power Modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is Low. When CS# is high, the device is disabled, but may still be in the Active Power mode until all program, erase, and Write Registers operations have completed. The device then goes into the Standby Power mode, and power consumption drops to I_{SB}. The Deep Power-Down (DP) command provides additional data protection against inadvertent signals. After writing the DP command, the device ignores any further program or erase commands, and reduces its power consumption to I_{DP}.

7.7 Status Register

The Status Register contains the status and control bits that can be read or set by specific commands (see Table 9.1 on page 18). These bits configure different protection configurations and supply information of operation of the device. (for details see Table 9.8, *S25FL064P Status Register* on page 32):

- **Write In Progress (WIP):** Indicates whether the device is performing a Write Registers, program or erase operation.
- **Write Enable Latch (WEL):** Indicates the status of the internal Write Enable Latch.
- **Block Protect (BP2, BP1, BP0):** Non-volatile bits that define memory area to be software-protected against program and erase commands.
- **Erase Error (E_ERR):** The Erase Error Bit is used as an Erase operation success and failure check.
- **Program Error (P_ERR):** The Program Error Bit is used as an program operation success and failure check.
- **Status Register Write Disable (SRWD):** Places the device in the Hardware Protected mode when this bit is set to 1 and the W#/ACC input is driven low. In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits.

7.8 Configuration Register

The Configuration Register contains the control bits that can be read or set by specific commands. These bits configure different configurations and security features of the device.

- The FREEZE bit locks the BP2-0 bits in Status Register and the TBPROT and TBPARM bits in the Configuration Register. Note that once the FREEZE bit has been set to 1, then it cannot be cleared to 0 until a power-on-reset is executed. As long as the FREEZE bit is set to 0, then the other bits of the Configuration Register, including FREEZE bit, can be written to.
- The QUAD bit is non-volatile and sets the pin out of the device to Quad mode; that is, W#/ACC becomes IO2 and HOLD# becomes IO3. The instructions for Serial, Dual Output, and Dual I/O reads function as normal. The W#/ACC and HOLD# functionality does not work when the device is set in Quad mode.
- The TBPARM bit defines the logical location of the 4 kB parameter sectors. The parameter sectors consist of thirty two 4 kB sectors. All sectors other than the parameter sectors are defined to be 64-kB uniform in size. When TBPARM is set to a 1, the 4 kB parameter sectors starts at the top of the array. When TBPARM is set to a 0, the 4 kB parameter sectors starts at the bottom of the array. Note that once this bit is set to a 1, it cannot be changed back to 0. The desired state of TBPARM must be selected during the initial configuration of the device during system manufacture; before the first program or erase operation on the main flash array. TBPARM must not be programmed after programming or erasing is done in the main flash array.
- The BPNV bit defines whether or not the BP2-0 bits in the Status Register are volatile or non-volatile. When BPNV is set to a 1, the BP2-0 bits in the Status Register are volatile and will be reset to binary 111 after power on reset. When BPNV is set to a 0, the BP2-0 bits in the Status Register are non-volatile. Note that once this bit is set to a 1, it cannot be changed back to 0.
- The TBPROT bit defines the operation of the block protection bits BP2, BP1, and BP0 in the Status Register. When TBPROT is set to a 0, then the block protection is defined to start from the top of the array. When TBPROT is set to a 1, then the block protection is defined to start from the bottom of the array. Note that once this bit is set to a 1, it cannot be changed back to 0. The desired state of TBPROT must be selected during the initial configuration of the device during system manufacture; before the first program or erase operation on the main flash array. TBPROT must not be programmed after programming or erasing is done in the main flash array.

Note: It is suggested that the Block Protection & Parameter sectors not be set to the same area of the array; otherwise, the user cannot utilize the Parameter sectors if they are protected. The following matrix shows the recommended settings.

Table 7.1 Suggested Cross Settings

TBPARM	TBPROT	Array Overview
0	0	Parameter Sectors - Bottom BP Protection - Top (Default)
0	1	Not recommended (Parameters & BP Protection are both Bottom)

Table 7.1 Suggested Cross Settings

TBPARM	TBPROT	Array Overview
1	0	Not recommended (parameters & BP Protection are both Top)
1	1	Parameter Sectors - Top of Array (high address) BP Protection - Bottom of Array (low address

Table 7.2 Configuration Register Table

Bit	Bit Name	Bit Function	Description
7	NA	-	Not Used
6	NA	-	Not Used
5	TBPROT	Configures start of block protection	1 = Bottom Array (low address) 0 = Top Array (high address) (Default)
4	NA	-	Do Not Use
3	BPNV	Configures BP2-0 bits in the Status Register	1 = Volatile 0 = Non-volatile (Default)
2	TBPARM	Configures Parameter sector location	1 = Top Array (high address) 0 = Bottom Array (low address) (Default)
1	QUAD	Puts the device into Quad I/O mode	1 = Quad I/O 0 = Dual or Serial I/O (Default)
0	FREEZE	Locks BP2-0 bits in the Status Register	1 = Enabled 0 = Disabled (Default)

Note
(Default) indicates the value of each Configuration Register bit set upon initial factory shipment.

7.9 Data Protection Modes

Cypress SPI flash memory devices provide the following data protection methods:

- **The Write Enable (WREN) command:** Must be written prior to any command that modifies data. The WREN command sets the Write Enable Latch (WEL) bit. The WEL bit resets (disables writes) on power-up or after the device completes the following commands:
  - Page Program (PP)
  - Sector Erase (SE)
  - Bulk Erase (BE)
  - Write Disable (WRDI)
  - Write Register (WRR)
  - Parameter 4 kB Sector Erase (P4E)
  - Parameter 8 kB Sector Erase (P8E)
  - Quad Page Programming (QPP)
  - OTP Byte Programming (OTPP)
- **Software Protected Mode (SPM):** The Block Protect (BP2, BP1, BP0) bits define the section of the memory array that can be read but not programmed or erased. Table 7.3 and Table 7.4 shows the sizes and address ranges of protected areas that are defined by Status Register bits BP2:BP0.
- **Hardware Protected Mode (HPM):** The Write Protect (W#/ACC) input and the Status Register Write Disable (SRWD) bit together provide write protection.
- **Clock Pulse Count:** The device verifies that all program, erase, and Write Register commands consist of a clock pulse count that is a multiple of eight before executing them.

Table 7.3 TBPROT = 0 (Starts Protection from TOP of Array)

Status Register Block			Memory Array				Protected Portion of Total Memory Area
BP2	BP1	BP0	Protected Address Range	Protected Sectors	Unprotected Address Range	Unprotected Sectors	
0	0	0	None	0	000000h-7FFFFFh	SA127:SA0	0
0	0	1	7E0000h-7FFFFFh	(2) SA127:SA126	000000h-7DFFFFh	SA125:SA0	1/64
0	1	0	7C0000h-7FFFFFh	(4) SA127:SA124	000000h-7BFFFFh	SA123:SA0	1/32
0	1	1	780000h-7FFFFFh	(8) SA127:SA120	000000h-77FFFFh	SA119:SA0	1/16
1	0	0	700000h-7FFFFFh	(16) SA127:SA112	000000h-6FFFFFh	SA111:SA0	1/8
1	0	1	600000h-7FFFFFh	(32) SA127:SA96	000000h-5FFFFFh	SA95:SA0	1/4
1	1	0	400000h-7FFFFFh	(64) SA127:SA64	000000h-3FFFFFh	SA63:SA0	1/2
1	1	1	000000h-7FFFFFh	(128) SA127:SA0	None	None	All

Table 7.4 TBPROT=1 (Starts Protection from BOTTOM of Array)

Status Register Block			Memory Array				Protected Portion of Total Memory Area
BP2	BP1	BP0	Protected Address Range	Protected Sectors	Unprotected Address Range	Unprotected Sectors	
0	0	0	None	0	000000h-7FFFFFh	SA0:SA127	0
0	0	1	000000h-01FFFFh	(2) SA0:SA1	020000h-7FFFFFh	SA2:SA127	1/64
0	1	0	000000h-03FFFFh	(4) SA0:SA3	040000h-7FFFFFh	SA4:SA127	1/32
0	1	1	000000h-07FFFFh	(8) SA0:SA7	080000h-7FFFFFh	SA8:SA127	1/16
1	0	0	000000h-0FFFFFh	(16) SA0:SA15	100000h-7FFFFFh	SA16:SA127	1/8
1	0	1	000000h-1FFFFFh	(32) SA0:SA31	200000h-7FFFFFh	SA32:SA127	1/4
1	1	0	000000h-3FFFFFh	(64) SA0:SA63	400000h-7FFFFFh	SA64:SA127	1/2
1	1	1	000000h-7FFFFFh	(128) SA0:SA127	None	None	All

7.10 Hold Mode (HOLD#)

The Hold input (HOLD#) stops any serial communication with the device, but does not terminate any Write Registers, program or erase operation that is currently in progress.

The Hold mode starts on the falling edge of HOLD# if SCK is also low (see Figure 7.1, standard use). If the falling edge of HOLD# does not occur while SCK is low, the Hold mode begins after the next falling edge of SCK (non-standard use).

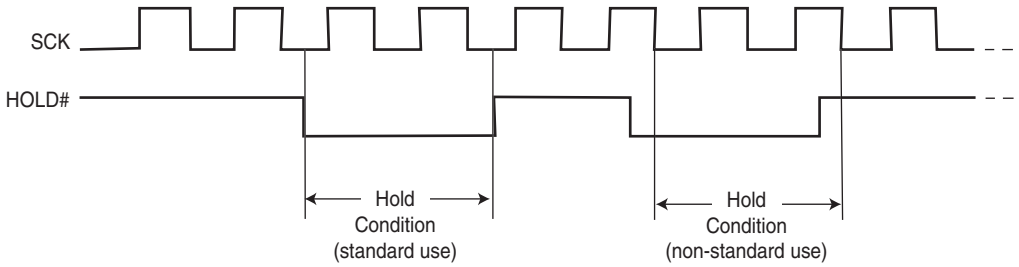
The Hold mode ends on the rising edge of HOLD# signal (standard use) if SCK is also low. If the rising edge of HOLD# does not occur while SCK is low, the Hold mode ends on the next falling edge of CLK (non-standard use) See Figure 7.1.

The SO output is high impedance, and the SI and SCK inputs are ignored (don't care) for the duration of the Hold mode.

CS# must remain low for the entire duration of the Hold mode to ensure that the device internal logic remains unchanged. If CS# goes high while the device is in the Hold mode, the internal logic is reset. To prevent the device from reverting to the Hold mode when device communication is resumed, HOLD# must be held high, followed by driving CS# low.

Note: The HOLD Mode feature is disabled when Quad mode is enabled, i.e., Quad bit in the Configuration register is set to 1.

Figure 7.1 Hold Mode Operation



7.11 Accelerated Programming Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory. If the system asserts V_{HH} on this pin, the device uses the higher voltage on the pin to reduce the time required for program operations. Removing V_{HH} from the W#/ACC pin returns the device to normal operation. Note that the W#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the W#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Note: The ACC function is disabled during Quad I/O Mode.

8. Sector Address Table

The Sector Address tables show the size of the memory array, sectors, and pages. The device uses pages to cache the program data before the data is programmed into the memory array. Each page or byte can be individually programmed (bits are changed from 1 to 0). The data is erased (bits are changed from 0 to 1) on a sub-sector, sector- or device-wide basis using the P4E/P8E, SE or BE commands. Table 8.1 and Table 8.2 show the starting and ending address for each sector. The complete set of sectors comprises the memory array of the flash device.

Table 8.1 S25FL064P Sector Address Table TBPARM=0

Sector	Address range		Sector	Address range		Sector	Address range		Sector	Address range	
	Start address	End Address		Start address	End Address		Start address	End Address		Start address	End Address
SA127	7F0000h	7FFFFFh	SA84	540000h	54FFFFh	SA41	290000h	29FFFFh			
SA126	7E0000h	7EFFFFh	SA83	530000h	53FFFFh	SA40	280000h	28FFFFh			
SA125	7D0000h	7DFFFFh	SA82	520000h	52FFFFh	SA39	270000h	27FFFFh			
SA124	7C0000h	7CFFFFh	SA81	510000h	51FFFFh	SA38	260000h	26FFFFh			
SA123	7B0000h	7BFFFFh	SA80	500000h	50FFFFh	SA37	250000h	25FFFFh			
SA122	7A0000h	7AFFFFh	SA79	4F0000h	4FFFFFh	SA36	240000h	24FFFFh			
SA121	790000h	79FFFFh	SA78	4E0000h	4EFFFFh	SA35	230000h	23FFFFh			
SA120	780000h	78FFFFh	SA77	4D0000h	4DFFFFh	SA34	220000h	22FFFFh			
SA119	770000h	77FFFFh	SA76	4C0000h	4CFFFFh	SA33	210000h	21FFFFh			
SA118	760000h	76FFFFh	SA75	4B0000h	4BFFFFh	SA32	200000h	20FFFFh			
SA117	750000h	75FFFFh	SA74	4A0000h	4AFFFFh	SA31	1F0000h	1FFFFFh	SS31	01F000h	01FFFFh
SA116	740000h	74FFFFh	SA73	490000h	49FFFFh	SA30	1E0000h	1EFFFFh	SS30	01E000h	01EFFFh
SA115	730000h	73FFFFh	SA72	480000h	48FFFFh	SA29	1D0000h	1DFFFFh	SS29	01D000h	01DFFFh
SA114	720000h	72FFFFh	SA71	470000h	47FFFFh	SA28	1C0000h	1CFFFFh	SS28	01C000h	01CFFFh
SA113	710000h	71FFFFh	SA70	460000h	46FFFFh	SA27	1B0000h	1BFFFFh	SS27	01B000h	01BFFFh
SA112	700000h	70FFFFh	SA69	450000h	45FFFFh	SA26	1A0000h	1AFFFFh	SS26	01A000h	01AFFFh
SA111	6F0000h	6FFFFFh	SA68	440000h	44FFFFh	SA25	190000h	19FFFFh	SS25	019000h	019FFFh
SA110	6E0000h	6EFFFFh	SA67	430000h	43FFFFh	SA24	180000h	18FFFFh	SS24	018000h	018FFFh
SA109	6D0000h	6DFFFFh	SA66	420000h	42FFFFh	SA23	170000h	17FFFFh	SS23	017000h	017FFFh
SA108	6C0000h	6CFFFFh	SA65	410000h	41FFFFh	SA22	160000h	16FFFFh	SS22	016000h	016FFFh
SA107	6B0000h	6BFFFFh	SA64	400000h	40FFFFh	SA21	150000h	15FFFFh	SS21	015000h	015FFFh
SA106	6A0000h	6AFFFFh	SA63	3F0000h	3FFFFFh	SA20	140000h	14FFFFh	SS20	014000h	014FFFh
SA105	690000h	69FFFFh	SA62	3E0000h	3EFFFFh	SA19	130000h	13FFFFh	SS19	013000h	013FFFh
SA104	680000h	68FFFFh	SA61	3D0000h	3DFFFFh	SA18	120000h	12FFFFh	SS18	012000h	012FFFh
SA103	670000h	67FFFFh	SA60	3C0000h	3CFFFFh	SA17	110000h	11FFFFh	SS17	011000h	011FFFh
SA102	660000h	66FFFFh	SA59	3B0000h	3BFFFFh	SA16	100000h	10FFFFh	SS16	010000h	010FFFh
SA101	650000h	65FFFFh	SA58	3A0000h	3AFFFFh	SA15	0F0000h	0FFFFFh	SS15	00F000h	00FFFFh
SA100	640000h	64FFFFh	SA57	390000h	39FFFFh	SA14	0E0000h	0EFFFFh	SS14	00E000h	00EFFFh
SA99	630000h	63FFFFh	SA56	380000h	38FFFFh	SA13	0D0000h	0DFFFFh	SS13	00D000h	00DFFFh
SA98	620000h	62FFFFh	SA55	370000h	37FFFFh	SA12	0C0000h	0CFFFFh	SS12	00C000h	00CFFFh
SA97	610000h	61FFFFh	SA54	360000h	36FFFFh	SA11	0B0000h	0BFFFFh	SS11	00B000h	00BFFFh
SA96	600000h	60FFFFh	SA53	350000h	35FFFFh	SA10	0A0000h	0AFFFFh	SS10	00A000h	00AFFFh
SA95	5F0000h	5FFFFFh	SA52	340000h	34FFFFh	SA9	090000h	09FFFFh	SS9	009000h	009FFFh
SA94	5E0000h	5EFFFFh	SA51	330000h	33FFFFh	SA8	080000h	08FFFFh	SS8	008000h	008FFFh
SA93	5D0000h	5DFFFFh	SA50	320000h	32FFFFh	SA7	070000h	07FFFFh	SS7	007000h	007FFFh
SA92	5C0000h	5CFFFFh	SA49	310000h	31FFFFh	SA6	060000h	06FFFFh	SS6	006000h	006FFFh
SA91	5B0000h	5BFFFFh	SA48	300000h	30FFFFh	SA5	050000h	05FFFFh	SS5	005000h	005FFFh
SA90	5A0000h	5AFFFFh	SA47	2F0000h	2FFFFFh	SA4	040000h	04FFFFh	SS4	004000h	004FFFh
SA89	590000h	59FFFFh	SA46	2E0000h	2EFFFFh	SA3	030000h	03FFFFh	SS3	003000h	003FFFh
SA88	580000h	58FFFFh	SA45	2D0000h	2DFFFFh	SA2	020000h	02FFFFh	SS2	002000h	002FFFh
SA87	570000h	57FFFFh	SA44	2C0000h	2CFFFFh	SA1	010000h	01FFFFh	SS1	001000h	001FFFh
SA86	560000h	56FFFFh	SA43	2B0000h	2BFFFFh	SA0	000000h	00FFFFh	SS0	000000h	000FFFh
SA85	550000h	55FFFFh	SA42	2A0000h	2AFFFFh						

Note

Sector SA0 is split up into sub-sectors SS0 - SS15 (dark gray shading)

Sector SA1 is split up into sub-sectors SS16 - SS31(light gray shading)

Table 8.2 S25FL064P Sector Address Table TBPARM=1

Sector	Address range		Sector	Address range		Sector	Address range		Sector	Address range	
	Start address	End Address		Start address	End Address		Start address	End Address		Start address	End Address
SS31	7FF000h	7FFFFFh	SA127	7F0000h	7FFFFFh	SA85	550000h	55FFFFh	SA42	2A0000h	2AFFFFh
SS30	7FE000h	7FEFFFh	SA126	7E0000h	7EFFFFh	SA84	540000h	54FFFFh	SA41	290000h	29FFFFh
SS29	7FD000h	7FDFFFh	SA125	7D0000h	7DFFFFh	SA83	530000h	53FFFFh	SA40	280000h	28FFFFh
SS28	7FC000h	7FCFFFh	SA124	7C0000h	7CFFFFh	SA82	520000h	52FFFFh	SA39	270000h	27FFFFh
SS27	7FB000h	7FBFFFh	SA123	7B0000h	7BFFFFh	SA81	510000h	51FFFFh	SA38	260000h	26FFFFh
SS26	7FA000h	7FAFFFh	SA122	7A0000h	7AFFFFh	SA80	500000h	50FFFFh	SA37	250000h	25FFFFh
SS25	7F9000h	7F9FFFh	SA121	790000h	79FFFFh	SA79	4F0000h	4FFFFFh	SA36	240000h	24FFFFh
SS24	7F8000h	7F8FFFh	SA120	780000h	78FFFFh	SA78	4E0000h	4EFFFFh	SA35	230000h	23FFFFh
SS23	7F7000h	7F7FFFh	SA119	770000h	77FFFFh	SA77	4D0000h	4DFFFFh	SA34	220000h	22FFFFh
SS22	7F6000h	7F6FFFh	SA118	760000h	76FFFFh	SA76	4C0000h	4CFFFFh	SA33	210000h	21FFFFh
SS21	7F5000h	7F5FFFh	SA117	750000h	75FFFFh	SA75	4B0000h	4BFFFFh	SA32	200000h	20FFFFh
SS20	7F4000h	7F4FFFh	SA116	740000h	74FFFFh	SA74	4A0000h	4AFFFFh	SA31	1F0000h	1FFFFFh
SS19	7F3000h	7F3FFFh	SA115	730000h	73FFFFh	SA73	490000h	49FFFFh	SA30	1E0000h	1EFFFFh
SS18	7F2000h	7F2FFFh	SA114	720000h	72FFFFh	SA72	480000h	48FFFFh	SA29	1D0000h	1DFFFFh
SS17	7F1000h	7F1FFFh	SA113	710000h	71FFFFh	SA71	470000h	47FFFFh	SA28	1C0000h	1CFFFFh
SS16	7F0000h	7F0FFFh	SA112	700000h	70FFFFh	SA70	460000h	46FFFFh	SA27	1B0000h	1BFFFFh
SS15	7EF000h	7EFFFFh	SA111	6F0000h	6FFFFFh	SA69	450000h	45FFFFh	SA26	1A0000h	1AFFFFh
SS14	7EE000h	7EEFFFh	SA110	6E0000h	6EFFFFh	SA68	440000h	44FFFFh	SA25	190000h	19FFFFh
SS13	7ED000h	7EDFFFh	SA109	6D0000h	6DFFFFh	SA67	430000h	43FFFFh	SA24	180000h	18FFFFh
SS12	7EC000h	7ECFFFh	SA108	6C0000h	6CFFFFh	SA66	420000h	42FFFFh	SA23	170000h	17FFFFh
SS11	7EB000h	7EBFFFh	SA107	6B0000h	6BFFFFh	SA65	410000h	41FFFFh	SA22	160000h	16FFFFh
SS10	7EA000h	7EAFFFh	SA106	6A0000h	6AFFFFh	SA64	400000h	40FFFFh	SA21	150000h	15FFFFh
SS9	7E9000h	7E9FFFh	SA105	690000h	69FFFFh	SA63	3F0000h	3FFFFFh	SA20	140000h	14FFFFh
SS8	7E8000h	7E8FFFh	SA104	680000h	68FFFFh	SA62	3E0000h	3EFFFFh	SA19	130000h	13FFFFh
SS7	7E7000h	7E7FFFh	SA103	670000h	67FFFFh	SA61	3D0000h	3DFFFFh	SA18	120000h	12FFFFh
SS6	7E6000h	7E6FFFh	SA102	660000h	66FFFFh	SA60	3C0000h	3CFFFFh	SA17	110000h	11FFFFh
SS5	7E5000h	7E5FFFh	SA101	650000h	65FFFFh	SA59	3B0000h	3BFFFFh	SA16	100000h	10FFFFh
SS4	7E4000h	7E4FFFh	SA100	640000h	64FFFFh	SA58	3A0000h	3AFFFFh	SA15	0F0000h	0FFFFFh
SS3	7E3000h	7E3FFFh	SA99	630000h	63FFFFh	SA57	390000h	39FFFFh	SA14	0E0000h	0EFFFFh
SS2	7E2000h	7E2FFFh	SA98	620000h	62FFFFh	SA56	380000h	38FFFFh	SA13	0D0000h	0DFFFFh
SS1	7E1000h	7E1FFFh	SA97	610000h	61FFFFh	SA55	370000h	37FFFFh	SA12	0C0000h	0CFFFFh
SS0	7E0000h	7E0FFFh	SA96	600000h	60FFFFh	SA54	360000h	36FFFFh	SA11	0B0000h	0BFFFFh
			SA95	5F0000h	5FFFFFh	SA53	350000h	35FFFFh	SA10	0A0000h	0AFFFFh
			SA94	5E0000h	5EFFFFh	SA52	340000h	34FFFFh	SA9	090000h	09FFFFh
			SA93	5D0000h	5DFFFFh	SA51	330000h	33FFFFh	SA8	080000h	08FFFFh
			SA92	5C0000h	5CFFFFh	SA50	320000h	32FFFFh	SA7	070000h	07FFFFh
			SA91	5B0000h	5BFFFFh	SA49	310000h	31FFFFh	SA6	060000h	06FFFFh
			SA90	5A0000h	5AFFFFh	SA48	300000h	30FFFFh	SA5	050000h	05FFFFh
			SA89	590000h	59FFFFh	SA47	2F0000h	2FFFFFh	SA4	040000h	04FFFFh
			SA88	580000h	58FFFFh	SA46	2E0000h	2EFFFFh	SA3	030000h	03FFFFh
			SA87	570000h	57FFFFh	SA45	2D0000h	2DFFFFh	SA2	020000h	02FFFFh
			SA86	560000h	56FFFFh	SA44	2C0000h	2CFFFFh	SA1	010000h	01FFFFh
						SA43	2B0000h	2BFFFFh	SA0	000000h	00FFFFh

Note

Sector SA126 is split up into sub-sectors SS0 - SS15 (dark gray shading)

Sector SA127 is split up into sub-sectors SS16 - SS31 (light gray shading)

9. Command Definitions

The host system must shift all commands, addresses, and data in and out of the device, beginning with the most significant bit. On the first rising edge of SCK after CS# is driven low, the device accepts the one-byte command on SI (all commands are one byte long), most significant bit first. Each successive bit is latched on the rising edge of SCK. Table 9.1 lists the complete set of commands.

Every command sequence begins with a one-byte command code. The command may be followed by address, data, both, or nothing, depending on the command. CS# must be driven high after the last bit of the command sequence has been written.

The Read Data Bytes (READ), Read Data Bytes at Higher Speed (FAST_READ), Dual Output Read (DOR), Quad Output Read (QOR), Dual I/O High Performance Read (DIOR), Quad I/O High Performance Read (QIOR), Read Status Register (RDSR), Read Configuration Register (RCR), Read OTP Data (OTPR), Read Manufacturer and Device ID (READ_ID), Read Identification (RDID) and Release from Deep Power-Down and Read Electronic Signature (RES) command sequences are followed by a data output sequence on SO. CS# can be driven high after any bit of the sequence is output to terminate the operation.

The Page Program (PP), Quad Page Program (QPP), 64 kB Sector Erase (SE), 4 kB Parameter Sector Erase (P4E), 8 kB Parameter Sector Erase (P8E), Bulk Erase (BE), Write Status and Configuration Registers (WRR), Program OTP space (OTPP), Write Enable (WREN), or Write Disable (WRDI) commands require that CS# be driven high at a byte boundary, otherwise the command is not executed. Since a byte is composed of eight bits, CS# must therefore be driven high when the number of clock pulses after CS# is driven low is an exact multiple of eight.

The device ignores any attempt to access the memory array during a Write Registers, program, or erase operation, and continues the operation uninterrupted.

The instruction set is listed in Table 9.1.

Table 9.1 Instruction Set

Operation	Command	One Byte Command Code	Description	Address Bytes	Mode Bit Cycle	Dummy Bytes	Data Bytes
Read	READ	**(03h)** 0000 0011	Read Data bytes	3	0	0	1 to ∞
	FAST_READ	**(0Bh)** 0000 1011	Read Data bytes at Fast Speed	3	0	1	1 to ∞
	DOR	**(3Bh)** 0011 1011	Dual Output Read	3	0	1	1 to ∞
	QOR	**(6Bh)** 0110 1011	Quad Output Read	3	0	1	1 to ∞
	DIOR	**(BBh)** 1011 1011	Dual I/O High Performance Read	3	1	0	1 to ∞
	QIOR	**(EBh)** 1110 1011	Quad I/O High Performance Read	3	1	2	1 to ∞
	RDID	**(9Fh)** 1001 1111	Read Identification	0	0	0	1 to 81
	READ_ID	**(90h)** 1001 0000	Read Manufacturer and Device Identification	3	0	0	1 to ∞
Write Control	WREN	**(06h)** 0000 0110	Write Enable	0	0	0	0
	WRDI	**(04h)** 0000 0100	Write Disable	0	0	0	0
Erase	P4E	**(20h)** 0010 0000	4 kB Parameter Sector Erase	3	0	0	0
	P8E	(**40h)** 0100 0000	8 kB (two 4 kB) Parameter Sector Erase	3	0	0	0
	SE	**(D8h)** 1101 1000	64 kB Sector Erase	3	0	0	0
	BE	**(60h)** 0110 0000 or **(C7h)** 1100 0111	Bulk Erase	0	0	0	0
					0	0	
Program	PP	**(02h)** 0000 0010	Page Programming	3	0	0	1 to 256
	QPP	**(32h)** 0011 0010	Quad Page Programming	3	0	0	1 to 256
Status & Configuration Register	RDSR	**(05h)** 0000 0101	Read Status Register	0	0	0	1 to ∞
	WRR	**(01h)** 0000 0001	Write (Status & Configuration) Registers	0	0	0	1 to 2
	RCR	**(35h)** 0011 0101	Read Configuration Register (CFG)	0	0	0	1 to ∞
	CLSR	**(30h)** 0011 0000	Reset the Erase and Program Fail Flag (SR5 and SR6) and restore normal operation)	0	0	0	0
Power Saving	DP	**(B9h)** 1011 1001	Deep Power-Down	0	0	0	0
	RES	**(ABh)** 1010 1011	Release from Deep Power-Down Mode	0	0	0	0
		(ABh) 1010 1011	Release from Deep Power-Down and Read Electronic Signature	0	0	3	1 to ∞
OTP	OTPP	**(42h)** 0100 0010	Programs one byte of data in OTP memory space	3	0	0	1
	OTPR	**(4Bh)** 0100 1011	Read data in the OTP memory space	3	0	1	1 to ∞

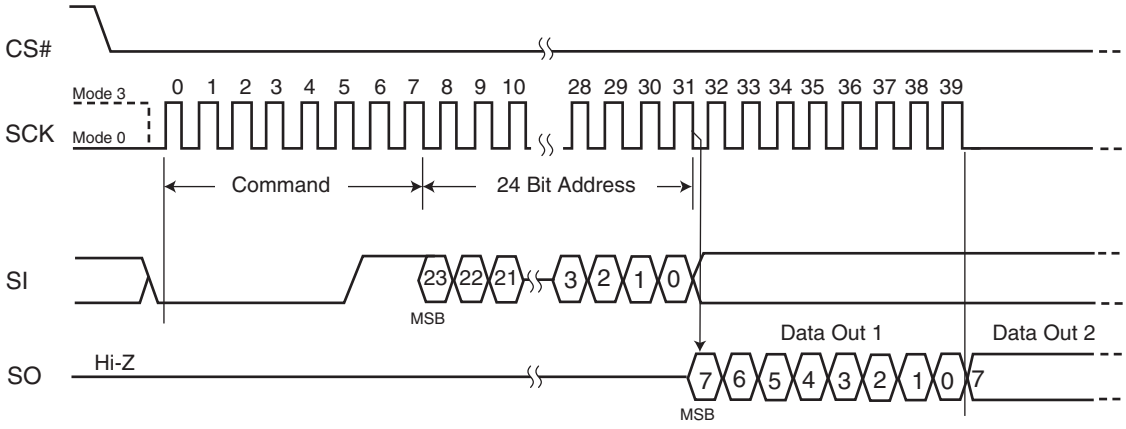
9.1 Read Data Bytes (READ)

The Read Data Bytes (READ) command reads data from the memory array at the frequency (f_R) presented at the SCK input, with a maximum speed of 40 MHz. The host system must first select the device by driving CS# low. The READ command is then written to SI, followed by a 3 byte address (A23-A0). Each bit is latched on the rising edge of SCK. The memory array data, at that address, are output serially on SO at a frequency f_R, on the falling edge of SCK.

Figure 9.1 and Table 9.1 on page 18 detail the READ command sequence. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single READ command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

The READ command is terminated by driving CS# high at any time during data output. The device rejects any READ command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

Figure 9.1 Read Data Bytes (READ) Command Sequence



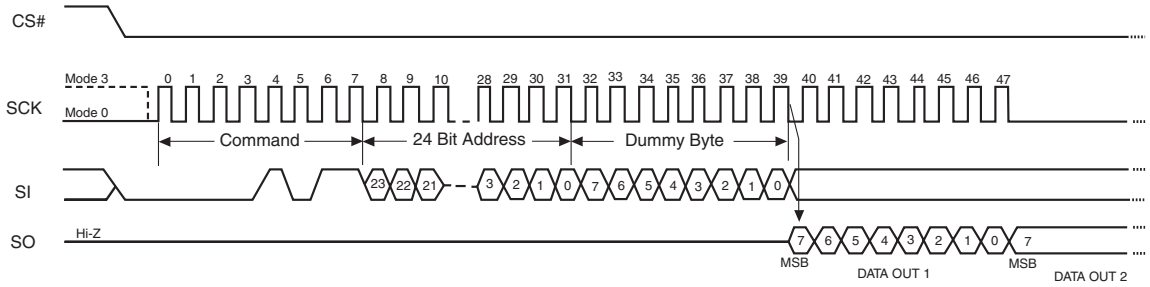
9.2 Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ command reads data from the memory array at the frequency (f_C) presented at the SCK input, with a maximum speed of 104 MHz. The host system must first select the device by driving CS# low. The FAST_READ command is then written to SI, followed by a 3 byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. The memory array data, at that address, are output serially on SO at a frequency f_C, on the falling edge of SCK.

The FAST_READ command sequence is shown in Figure 9.2 and Table 9.1 on page 18. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single FAST_READ command. When the highest address is reached, the address counter reverts to 000000h, allowing the read sequence to continue indefinitely.

The FAST_READ command is terminated by driving CS# high at any time during data output. The device rejects any FAST_READ command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

Figure 9.2 Read Data Bytes at Higher Speed (FAST_READ) Command Sequence



9.3 Dual Output Read Mode (DOR)

The Dual Output Read instruction is similar to the FAST_READ instruction, except that the data is shifted out 2 bits at a time using 2 pins (SI/IO0 and SO/IO1) instead of 1 bit, at a maximum frequency of 80 MHz. The Dual Output Read mode effectively doubles the data transfer rate compared to the FAST_READ instruction.

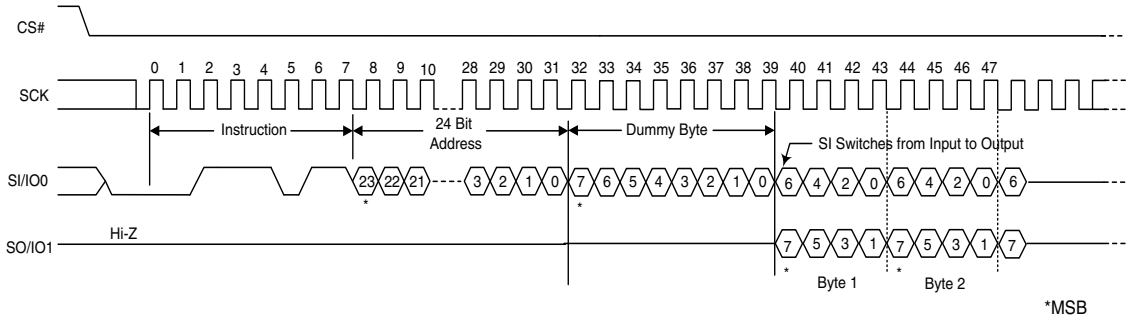
The host system must first select the device by driving CS# low. The Dual Output Read command is then written to SI, followed by a 3-byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. Then the memory contents, at the address that is given, are shifted out two bits at a time through the IO0 (SI) & IO1 (SO) pins at a frequency f_C on the falling edge of SCK.

The Dual Output Read command sequence is shown in Figure 9.3 and Table 9.1 on page 18. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single Dual Output Read command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

It is important that the I/O pins be set to high-impedance prior to the falling edge of the first data out clock.

The Dual Output Read command is terminated by driving CS# high at any time during data output. The device rejects any Dual Output Read command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

Figure 9.3 Dual Output Read Instruction Sequence



9.4 Quad Output Read Mode (QOR)

The Quad Output Read instruction is similar to the FAST_READ instruction, except that the data is shifted out 4 bits at a time using 4 pins (SI/IO0, SO/IO1, W#/ACC/IO2 and HOLD#/IO3) instead of 1 bit, at a maximum frequency of 80 MHz. The Quad Output Read mode effectively doubles the data transfer rate compared to the Dual Output Read instruction, and is four times the data transfer rate of the FAST_READ instruction.

The host system must first select the device by driving CS# low. The Quad Output Read command is then written to SI, followed by a 3-byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. Then the memory contents, at the address that are given, are shifted out four bits at a time through IO0 (SI), IO1 (SO), IO2 (W#/ACC), and IO3 (HOLD#) pins at a frequency f_C on the falling edge of SCK.

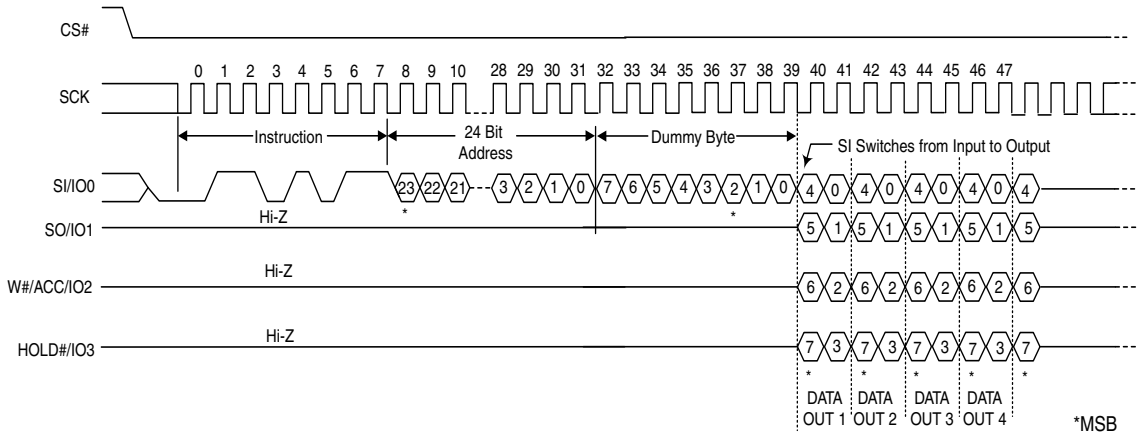
The Quad Output Read command sequence is shown in Figure 9.4 and Table 9.1 on page 18. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single Quad Output Read command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

It is important that the I/O pins be set to high-impedance prior to the falling edge of the first data out clock.

The Quad Output Read command is terminated by driving CS# high at any time during data output. The device rejects any Quad Output Read command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

The Quad bit of Configuration Register must be set (CR Bit1 = 1) to enable the Quad mode capability of the S25FL device.

Figure 9.4 Quad Output Read Instruction Sequence



9.5 DUAL I/O High Performance Read Mode (DIOR)

The Dual I/O High Performance Read instruction is similar to the Dual Output Read instruction, except that it improves throughput by allowing input of the address bits (A23-A0) using 2 bits per SCK via two input pins (SI/IO2 and SO/IO1), at a maximum frequency of 80 MHz.

The host system must first select the device by driving CS# low. The Dual I/O High Performance Read command is then written to SI, followed by a 3-byte address (A23-A0) and a 1-byte Mode instruction, with two bits latched on the rising edge of SCK. Then the memory contents, at the address that is given, are shifted out two bits at a time through IO0 (SI) and IO1 (SO).

The DUAL I/O High Performance Read command sequence is shown in Figure 9.5 and Table 9.1 on page 18. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single DUAL I/O High Performance Read command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

In addition, address jumps can be done without exiting the Dual I/O High Performance Mode through the setting of the Mode bits (after the Address (A23-0) sequence, as shown in Figure 9.5). This added feature removes the need for the instruction sequence and greatly improves code execution (XIP). The upper nibble (bits 7-4) of the Mode bits control the length of the next Dual I/O High Performance instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble (bits 3-0) of the Mode bits are DON'T CARE ("x"). If the Mode bits equal Axh, then the device remains in Dual I/O High Performance Read Mode and the next address can be entered (after CS# is raised high and then asserted low) without requiring the BBh instruction opcode, as shown in Figure 9.6, thus eliminating eight cycles for the instruction sequence. However, if the Mode bits are any value other than Axh, then the next instruction (after CS# is raised high and then asserted low) requires the instruction sequence, which is normal operation. The following sequences will release the device from Dual I/O High Performance Read mode; after which, the device can accept standard SPI instructions:

1. During the Dual I/O High Performance Instruction Sequence, if the Mode bits are any value other than Axh, then the next time CS# is raised high and then asserted low, the device will be released from Dual I/O High Performance Read mode.
2. Furthermore, during any operation, if CS# toggles high to low to high for eight cycles (or less) **and** data input (IO0 & IO1) are not set for a valid instruction sequence, then the device will be released from Dual I/O High Performance Read mode.

It is important that the I/O pins be set to high-impedance prior to the falling edge of the first data out clock.

The read instruction can be terminated by driving the CS# pin to the logic high state. The CS# pin can be driven high at any time during data output to terminate a read operation.

Figure 9.5 DUAL I/O High Performance Read Instruction Sequence

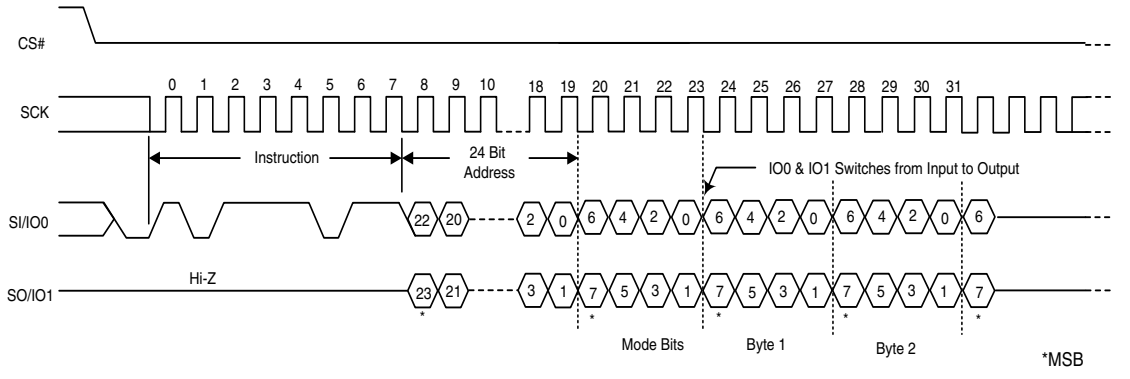
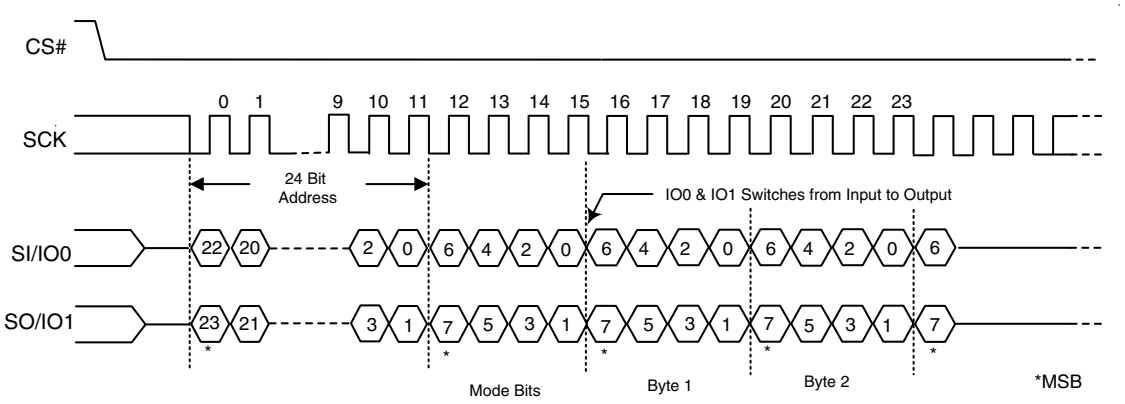


Figure 9.6 Continuous Dual I/O High Performance Read Instruction Sequence



9.6 Quad I/O High Performance Read Mode (QIOR)

The Quad I/O High Performance Read instruction is similar to the Quad Output Read instruction, except that it further improves throughput by allowing input of the address bits (A23-A0) using 4 bits per SCK via four input pins (SI/IO0, SO/IO1, W#/ACC/IO2 and HOLD#/IO3), at a maximum frequency of 80 MHz.

The host system must first select the device by driving CS# low. The Quad I/O High Performance Read command is then written to SI, followed by a 3-byte address (A23-A0) and a 1-byte Mode instruction, with four bits latched on the rising edge of SCK. Note that four dummy clocks are required prior to the data input. Then the memory contents, at the address that is given, are shifted out four bits at a time through IO0 (SI), IO1 (SO), IO2 (W#/ACC), and IO3 (HOLD#).

The Quad I/O High Performance Read command sequence is shown in Figure 9.7 and Table 9.1 on page 18. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single Quad I/O High Performance Read command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

In addition, address jumps can be done without exiting the Quad I/O High Performance Mode through the setting of the Mode bits (after the Address (A23-0) sequence, as shown in Figure 9.7). This added feature the removes the need for the instruction sequence and greatly improves code execution (XIP). The upper nibble (bits 7-4) of the Mode bits control the length of the next Quad I/O High Performance instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble (bits 3-0) of the Mode bits are DON'T CARE (“x”). If the Mode bits equal Axh, then the device remains in Quad I/O High Performance Read Mode and the next address can be entered (after CS# is raised high and then asserted low) without requiring the EBh instruction opcode, as shown in Figure 9.8, thus eliminating eight cycles for the instruction sequence. The following sequences will release the device from Quad I/O High Performance Read mode; after which, the device can accept standard SPI instructions:

1. During the Quad I/O High Performance Instruction Sequence, if the Mode bits are any value other than Axh, then the next time CS# is raised high and then asserted low the device will be released from Quad I/O High Performance Read mode.
2. Furthermore, during any operation, if CS# toggles high to low to high for eight cycles (or less) **and** data input (IO0, IO1, IO2, & IO3) are not set for a valid instruction sequence, then the device will be released from Quad I/O High Performance Read mode.

It is important that the I/O pins be set to high-impedance prior to the falling edge of the first data out clock.

The read instruction can be terminated by driving the CS# pin to the logic high state. The CS# pin can be driven high at any time during data output to terminate a read operation.

Figure 9.7 QUAD I/O High Performance Instruction Sequence

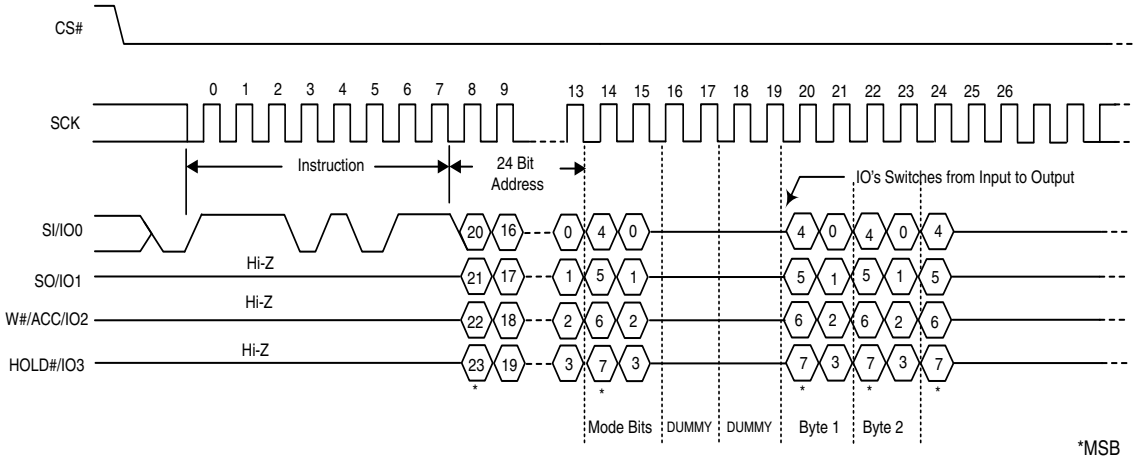


Figure 9.8 Continuous QUAD I/O High Performance Instruction Sequence