Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

S25FL256L/S25FL128L

256 Mbit (32 Mbyte)/128 Mbit (16 Mbyte), 3.0 V FL-L Flash Memory

General Description

The Cypress FL-L Family devices are Flash non-volatile memory products using:

- Floating Gate technology
- 65 nm process lithography

The FL-L family connects to a host system via a Serial Peripheral Interface (SPI). Traditional SPI single bit serial input and output (Single I/O or SIO) is supported as well as optional two bit (Dual I/O or DIO) and four bit wide Quad I/O (QIO) and Quad Peripheral Interface (QPI) commands. In addition, there are Double Data Rate (DDR) read commands for QIO and QPI that transfer address and read data on both edges of the clock.

The architecture features a Page Programming Buffer that allows up to 256-bytes to be programmed in one operation and provides individual 4KB sector, 32KB half block, 64KB block, or entire chip erase.

By using FL-L family devices at the higher clock rates supported, with Quad commands, the instruction read transfer rate can match or exceed traditional parallel interface, asynchronous, NOR Flash memories, while reducing signal count dramatically.

The FL-L family products offer high densities coupled with the flexibility and fast performance required by a variety of mobile or embedded applications. Provides an ideal storage solution for systems with limited space, signal connections, and power. These memories offer flexibility and performance well beyond ordinary serial flash devices. They are ideal for code shadowing to RAM, executing code directly (XIP), and storing re-programmable data.

Features

- **Serial Peripheral Interface (SPI) with Multi-I/O**
  - Clock polarity and phase modes 0 and 3
  - Double Data Rate (DDR) option
  - Quad peripheral Interface (QPI) option
  - Extended Addressing: 24- or 32-bit address options
  - Serial Command subset and footprint compatible with S25FL-A, S25FL1-K, S25FL-P, S25FL-S and S25FS-S SPI families
  - Multi I/O Command subset and footprint compatible with S25FL-P, S25FL-S and S25FS-S SPI families
- **Read**
  - Commands: Normal, Fast, Dual I/O, Quad I/O, DualO, QuadO, DDR Quad I/O.
  - Modes: Burst Wrap, Continuous (XIP), QPI
  - Serial Flash Discoverable Parameters (SFDP) for configuration information.
- **Program Architecture**
  - 256 Bytes Page Programming buffer3.0 V FL-L Flash Memory
  - Program suspend and resume
- **Erase Architecture**
  - Uniform 4KB Sector Erase
  - Uniform 32KB Half Block Erase
  - Uniform 64KB Block Erase
  - Chip erase
  - Erase suspend and resume
- **100,000 Program/Erase Cycles**
- **20 Year Data Retention**
- **Security features**
  - Status and Configuration Register Protection
  - Four Security Regions of 256 bytes each outside the main Flash array
  - Legacy Block Protection: Block range
  - Individual and Region Protection
    - Individual Block Lock: Volatile individual Sector/Block
    - Pointer Region: Non-Volatile Sector/Block range
    - Power Supply Lock-down, Password, or Permanent protection of Security Regions 2 and 3 and Pointer Region
- **Technology**
  - 65 nm Floating Gate Technology
- **Single Supply Voltage with CMOS I/O**
  - 2.7 V to 3.6 V
- **Temperature Range / Grade**
  - Industrial (–40°C to +85°C)
  - Industrial Plus (–40°C to +105°C)
  - Extended (–40°C to +125°C)
  - Automotive, AEC-Q100 Grade 3 (–40°C to +85°C)
  - Automotive, AEC-Q100 Grade 2 (–40°C to +105°C)
  - Automotive, AEC-Q100 Grade 1 (–40°C to +125°C)
- **Packages (all Pb-free)**
  - 8-pin SOIC 208 mil (SOC008) — S25FL128L only
  - WSON 5 × 6 mm (WND008) — S25FL128L only
  - WSON 6 × 8 mm (WNG008) — S25FL256L only
  - 16-pin SOIC 300 mil (SO3016) — S25FL256L only
  - BGA-24 6 × 8 mm
    - 5 × 5 ball (FAB024) footprint
    - 4 × 6 ball (FAC024) footprint

Performance Summary

Maximum Read Rates SDR

Command	Clock Rate (MHz)	MBps
Read	50	6.25
Fast Read	133	16.5
Dual Read	133	33
Quad Read	133	66

Maximum Read Rates DDR

Command	Clock Rate (MHz)	MBps
DDR Quad Read	66	66

Typical Program and Erase Rates

Operation	KBytes/s
Page Programming	854
4 KBytes Sector Erase	80
32 KBytes Half Block Erase	168
64 KBytes Block Erase	237

Typical Current Consumption, –40°C to +85°C

Operation	Typical Current	Unit
Fast Read 5MHz	10	mA
Fast Read 10 MHz	10	mA
Fast Read 20 MHz	10	mA
Fast Read 50 MHz	15	mA
Fast Read 108 MHz	25	mA
Fast Read 133 MHz	30	mA
Quad I/O / QPI Read 108 MHz	25	mA
Quad I/O / QPI Read 133 MHz	30	mA
Quad I/O / QPI DDR Read 33MHz	15	mA
Quad I/O / QPI DDR Read 66MHz	30	mA
Program	40	mA
Erase	40	mA
Standby SPI	20	µA
Standby QPI	60	µA
Deep Power Down	2	µA

Contents

1. Product Overview

1.1 Migration Notes

1.1.1 Features Comparison

The FL-L family is command subset and footprint compatible with prior generation FL-S, FL1-K and FL-P families.

Table 1.1 Cypress SPI Families Comparison

Parameter	FL-L	FL-S	FL1-K	FL-P
Technology Node	65nm	65nm	90nm	90nm
Architecture	Floating Gate	MirrorBit® Eclipse™	Floating Gate	MirrorBit®
Release Date		In Production	In Production	In Production
Density	256Mb	128Mb - 1Gb	4Mb - 64Mb	32Mb - 256Mb
Bus Width	x1, x2, x4	x1, x2, x4	x1, x2, x4	x1, x2, x4
Supply Voltage	2.7 V - 3.6 V	2.7 V - 3.6 V / 1.65 V - 3.6 V V_{IO}	2.7 V - 3.6 V	2.7 V - 3.6 V
Normal Read Speed	6MB/s (50MHz)	6MB/s (50MHz)	6MB/s (50MHz)	5MB/s (40MHz)
Fast Read Speed	16.5MB/s (133MHz)	17MB/s (133MHz)	13MB/s (108MHz)	13MB/s (104MHz)
Dual Read Speed	33MB/s (133MHz)	26MB/s (104MHz)	26MB/s (108MHz)	20MB/s (80MHz)
Quad Read Speed	66MB/s (133MHz)	52MB/s (104MHz)	52MB/s (108MHz)	40MB/s (80MHz)
Quad Read Speed (DDR)	66MB/s (66MHz)	80MB/s (80MHz)	–	–
Program Buffer Size	256B	256B / 512B	256B	256B
Erase Sector/Block Size	4KB / 32KB / 64KB	64KB / 256KB	4KB / 64KB	64KB / 256KB
Parameter Sector Size	-	4KB (option)	–	4KB
Sector / Block Erase Rate (typ.)	80 KB/s (4KB) 168 KB/s (32KB 237KB/s (64KB)	500 KB/s	136 KB/s (4KB) 437 KB/s (64KB)	130 KB/s
Page Programming Rate (typ.)	854KB/s (256B)	1.2 MB/s (256B) 1.5 MB/s (512B)	365 KB/s	170 KB/s
Security Region / OTP	1024B	1024B	768B (3 × 256B)	506B
Individual and Region Protection or Advanced Sector Protection	Yes	Yes	No	No
Erase Suspend/Resume	Yes	Yes	Yes	No
Program Suspend/Resume	Yes	Yes	Yes	No
Operating Temperature	–40°C to +85°C –40°C to +105°C –40°C to +125°C	–40°C to +85°C –40°C to +105°C	–40°C to +85°C	–40°C to +85°C –40°C to +105°C

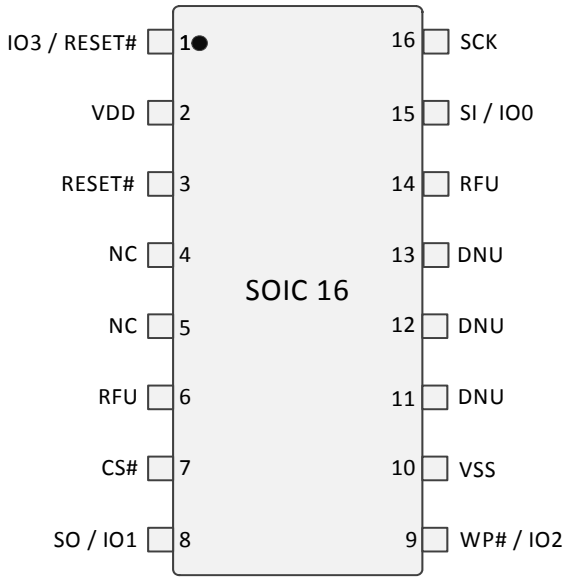
Note:

1. Refer to individual data sheets for further details

2. Connection Diagrams

2.1 SOIC 16-Lead

Figure 2.1 16-Lead SOIC Package (SO3016), Top View



Note:

1. *The RESET# and IO3 / RESET# inputs have an internal pull-up and may be left unconnected in the system if quad mode, mode and hardware reset are not in use.*

2.2 8 Connector Packages

Figure 2.2 8-Pin Plastic Small Outline Package (SOIC8)

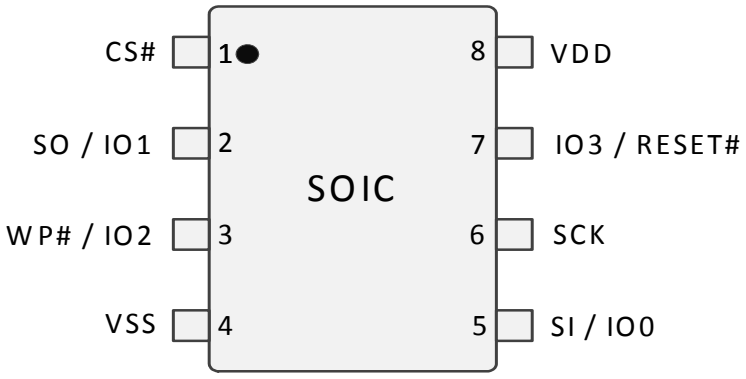
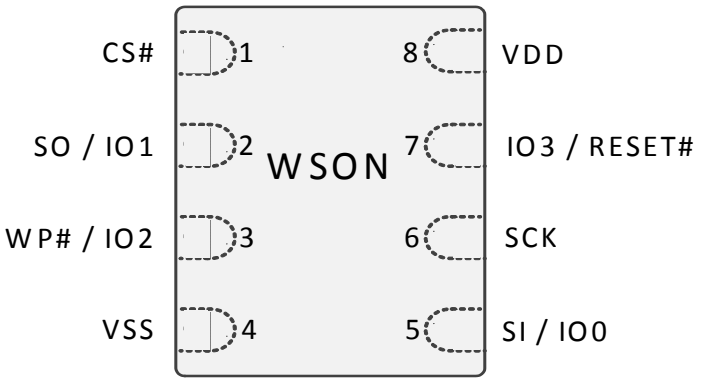


Figure 2.3 8-Connector Package (WSON 6x8) (WSON 5x6), Top View

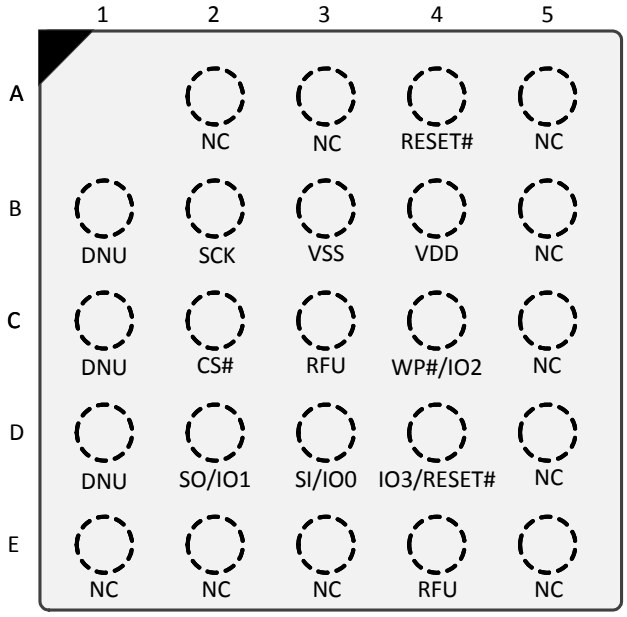


Note:

1. The RESET# input has an internal pull-up and may be left unconnected in the system if quad mode and hardware reset are not in use.

2.3 BGA Ball Footprint

Figure 2.4 24-Ball BGA, 5x5 Ball Footprint (FAB024), Top View

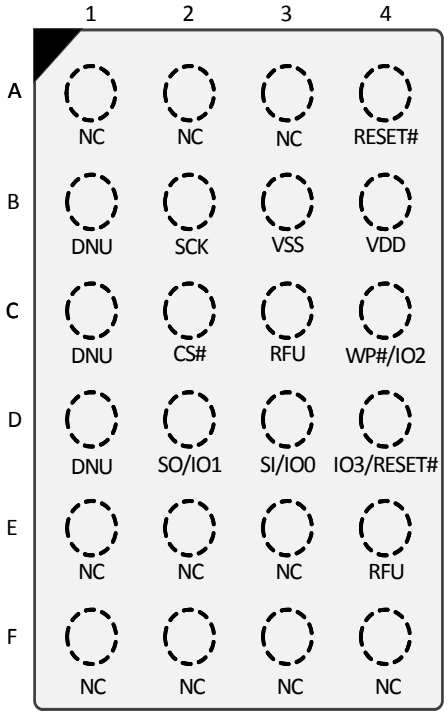


Notes:

1. Signal connections are in the same relative positions as FAC024 BGA, allowing a single PCB footprint to use either package.

2. The RESET# input has an internal pull-up and may be left unconnected in the system if quad mode and hardware reset are not in use.

Figure 2.5 24-Ball BGA, 4x6 Ball Footprint (FAC024), Top View



Note:
1. The RESET# input has an internal pull-up and may be left unconnected in the system if quad mode and hardware reset are not in use.

2.4 Special Handling Instructions for FBGA Packages

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

3. Signal Descriptions

Serial Peripheral Interface with Multiple Input / Output (SPI-MIO)

Many memory devices connect to their host system with separate parallel control, address, and data signals that require a large number of signal connections and larger package size. The large number of connections increase power consumption due to so many signals switching and the larger package increases cost.

The FL-L family reduces the number of signals for connection to the host system by serially transferring all control, address, and data information over 6 signals. This reduces the cost of the memory package, reduces signal switching power, and either reduces the host connection count or frees host connectors for use in providing other features.

The FL-L family uses the industry standard single bit SPI and also supports optional extension commands for two bit (Dual) and four bit (Quad) wide serial transfers. This multiple width interface is called SPI Multi-I/O or SPI-MIO.

3.1 Input/Output Summary

Table 3.1 Signal List

Signal Name	Type	Description
RESET#	Input	**Hardware Reset:** Low = device resets and returns to standby state, ready to receive a command. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used.
SCK	Input	**Serial Clock**
CS#	Input	**Chip Select**
SI / IO0	I/O	**Serial Input** for single bit data commands or IO0 for Dual or Quad commands.
SO / IO1	I/O	**Serial Output** for single bit data commands. IO1 for Dual or Quad commands.
WP# / IO2	I/O	**Write Protect** when not in Quad mode (CR1V[1] = 0 and SR1NV[7] = 1). **IO2** when in Quad mode (CR1V[1] = 1). The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands or write protection. If write protection is enabled by SR1NV[7] = 1 and CR1V[1] = 0, the host system is required to drive WP# high or low during a WRR or WRAR command.
IO3 / RESET#	I/O	**IO3** in Quad-I/O mode, when Configuration Register 1 QUAD bit, CR1V[1] =1, or in QPI mode, when Configuration Register 2 QPI bit, CR2V[3] =1 and CS# is low. **RESET#** when enabled by CR2V[7]=1 and not in Quad-I/O mode, CR1V[1] = 0, or when enabled in quad mode, CR1V[1] = 1 and CS# is high. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands or RESET#.
V_{DD}	Supply	**Power Supply.**
V_{SS}	Supply	**Ground.**
NC	Unused	**Not Connected.** No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). However, any signal connected to an NC must not have voltage levels higher than V_{DD}.
RFU	Reserved	**Reserved for Future Use.** No device internal signal is currently connected to the package connector but there is potential future use of the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU	Reserved	**Do Not Use.** A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

Notes

1. *Inputs with internal pull-ups or pull-downs drive less than 2 µA. Only during power-up is the current larger at 150 µA for 4 µS. Resistance of pull-ups or pull-down resistors with the typical process at Vcc = 3.3 V at –40°C is ~4.5 MΩ and at 90°C is ~6.6 MΩ.*

3.2 Multiple Input / Output (MIO)

Traditional SPI single bit wide commands (Single or SIO) send information from the host to the memory only on the Serial Input (SI) signal. Data may be sent back to the host serially on the Serial Output (SO) signal.

Dual or Quad Input / Output (I/O) commands send instructions to the memory only on the SI/IO0 signal. Address or data is sent from the host to the memory as bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

QPI mode transfers all instructions, addresses, and data from the host to the memory as four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as four bit (nibble) groups on IO0, IO1, IO2, and IO3.

3.3 Serial Clock (SCK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCK signal. Data output changes after the falling edge of SCK, in SDR commands.

3.4 Chip Select (CS#)

The chip select signal indicates when a command is transferring information to or from the device and the other signals are relevant for the memory device.

When the CS# signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. The device will be in the Standby Power mode, unless an internal embedded operation is in progress. An embedded operation is indicated by the Status Register 1 Write-In-Progress bit (SR1V[0]) set to 1, until the operation is completed. Some example embedded operations are: Program, Erase, or Write Registers (WRR) operations.

Driving the CS# input to the logic low state enables the device, placing it in the Active Power mode. After Power-up, a falling edge on CS# is required prior to the start of any command.

3.5 Serial Input (SI) / IO0

This input signals used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal. SI becomes IO0 - an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

3.6 Serial Output (SO) / IO1

This output signals used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal. SO becomes IO1 - an input and output during Dual and Quad commands for receiving addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK in SDR commands, and on every edge of SCK, in DDR commands).

3.7 Write Protect (WP#) / IO2

When WP# is driven Low (V_{IL}), when the Status Register Protect 0 (SRP0_NV) or (SRP0) bit of Status Register 1 (SR1NV[7]) or (SR1V[7]) is set to a 1, it is not possible to write to Status Registers, Configuration Registers or DLR registers. In this situation, the command selecting SR1NV, SR1V, CR1NV,CR1V, CR2NV, CR2V, CR3NV, DLRNV and DLRV is ignored, and no error is set.

This prevents any alteration of the Legacy Block Protection settings. As a consequence, all the data bytes in the memory area that are protected by the Legacy Block Protection feature are also hardware protected against data modification if WP# is Low during commands changing Status Registers, Configuration Registers or DLR registers, with SRP0_NV set to 1. Similarly, the Security Region Lock Bits (LB3-LB0) are protected against programming.

The WP# function is not available when the Quad mode is enabled (CR1V[1]=1) or QPI mode is enabled (CR2V[3]=1). The WP# function is replaced by IO2 for input and output during Quad mode or QPI mode is enabled (CR2V[3]=1) for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

WP# has an internal pull-up resistance; when unconnected, WP# is at V_{IH} and may be left unconnected in the host system if not used for Quad mode or QPI mode or protection.

3.8 IO3 / RESET#

IO3 is used for input and output during Quad mode (CR1V[1]=1) or QPI mode is enabled (CR2V[3]=1) for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

The IO3 / RESET# input may also be used to initiate the hardware reset function when the IO3 / RESET# feature is enabled by writing Configuration Register 2 non-volatile bit 7 (CR2NV[7]=1). The input is only treated as RESET# when the device is not in Quad modes (114,144,444), CR1V[1] = 0, or when CS# is high. When Quad modes are in use, CR1V[1]=1or QPI mode is enabled (CR2V[3]=1), and the device is selected with CS# low, the IO3 / RESET# is used only as IO3 for information transfer. When CS# is high, the IO3 / RESET# is not in use for information transfer and is used as the reset input. By conditioning the reset operation on CS# high during Quad modes (114,144,444), the reset function remains available during Quad modes (114,144,444).

When the system enters a reset condition, the CS# signal must be driven high as part of the reset process and the IO3 / RESET# signal is driven low. When CS# goes high the IO3 / RESET# input transitions from being IO3 to being the reset input. The reset condition is then detected when CS# remains high and the IO3 / RESET# signal remains low for t_{RP}. If a reset is not intended, the system is required to actively drive IO3 / RESET# to high along with CS# being driven high at the end of a transfer of data to the memory. Following transfers of data to the host system, the memory will drive IO3 high during t_{CS}. This will ensure that IO3 / RESET# is not left floating or being pulled slowly to high by the internal or an external passive pull-up. Thus, an unintended reset is not triggered by the IO3 / RESET# not being recognized as high before the end of t_{RP}.

The IO3 / RESET# input reset feature is disabled when (CR2V[7]=0).

The IO3 / RESET# input has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad mode or the reset function. The internal pull-up will hold IO3 / RESET# high after the host system has actively driven the signal high and then stops driving the signal.

Note that IO3 / RESET# input cannot be shared by more than one SPI-MIO memory if any of them are operating in Quad I/O mode as IO3 being driven to or from one selected memory may look like a reset signal to a second non-selected memory sharing the same IO3 / RESET# signal.

3.9 RESET#

The RESET# input provides a hardware method of resetting the device to standby state, ready for receiving a command. When RESET# is driven to logic low (V_{IL}) for at least a period of t_{RP}, the device starts the hardware reset process.

RESET# causes the same initialization process as is performed when power comes up and requires t_{PU} time.

RESET# may be asserted low at any time. To ensure data integrity any operation that was interrupted by a hardware reset should be reinitiated once the device is ready to accept a command sequence.

RESET# has an internal pull-up resistor and may be left unconnected in the host system if not used. The internal pull-up will hold Reset high after the host system has actively driven the signal high and then stops driving the signal.

The RESET# input is not available on all packages options. When not available the RESET# input of the device is tied to the inactive state.

3.10 Voltage Supply (V_{DD})

V_{DD} is the voltage source for all device internal logic. It is the single voltage used for all device internal functions including read, program, and erase.

3.11 Supply and Signal Ground (V_{SS})

V_{SS} is the common voltage drain and ground reference for the device core, input signal receivers, and output drivers.

3.12 Not Connected (NC)

No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).

3.13 Reserved for Future Use (RFU)

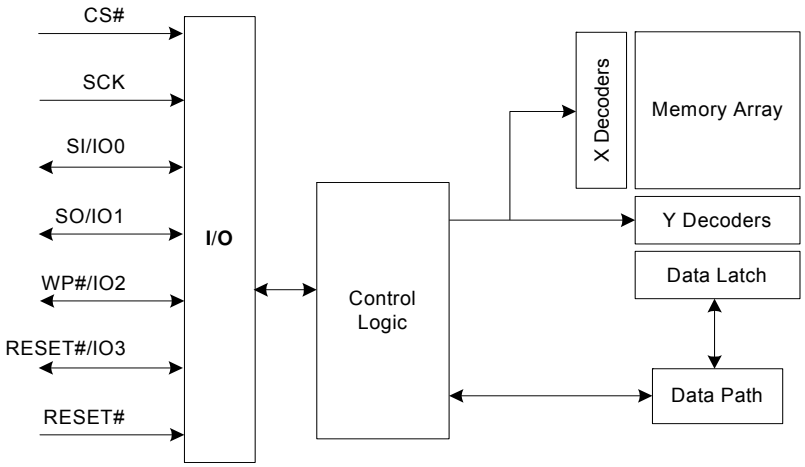
No device internal signal is currently connected to the package connector but there is potential future use of the connector. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.

3.14 Do Not Use (DNU)

A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.

4. Block Diagrams

Figure 4.1 Logic Block Diagram



4.1 System Block Diagrams

Figure 4.2 Bus Master and Memory Devices on the SPI Bus — Single Bit Data Path

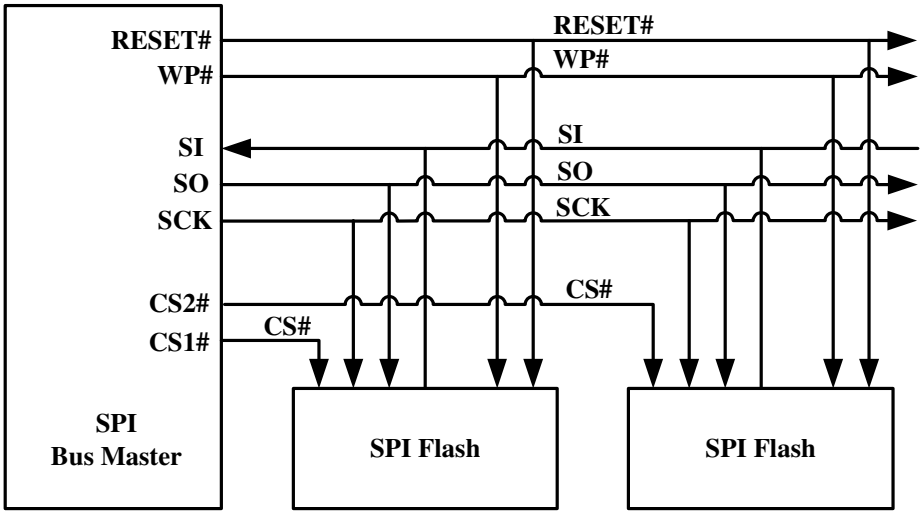


Figure 4.3 Bus Master and Memory Devices on the SPI Bus — Dual Bit Data Path

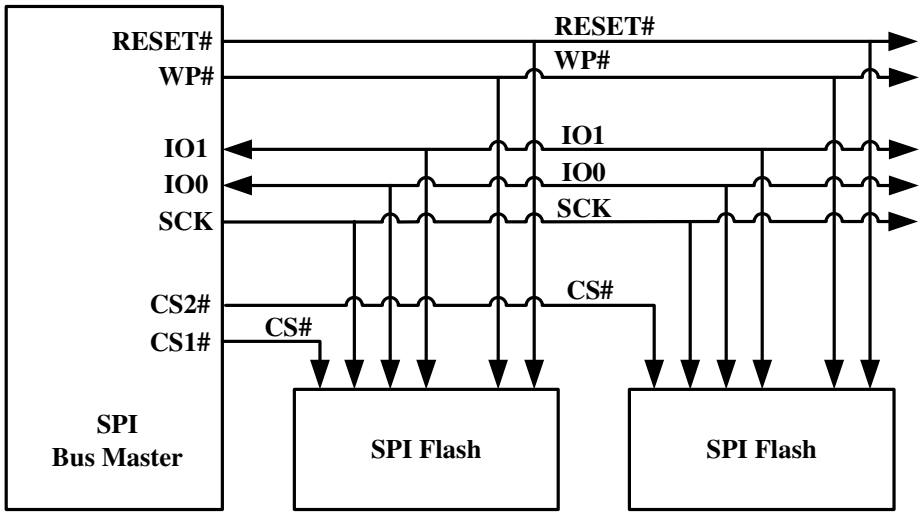


Figure 4.4 Bus Master and Memory Devices on the SPI Bus — Quad Bit Data Path — Separate RESET#

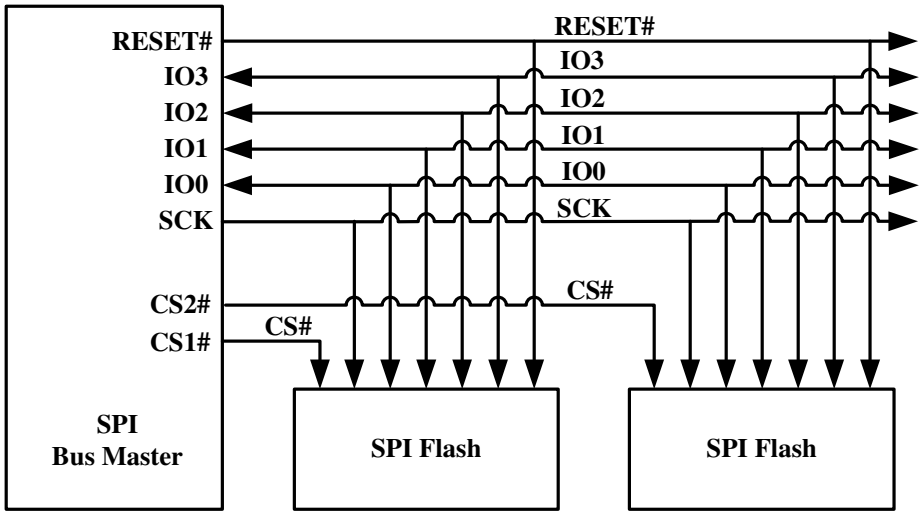
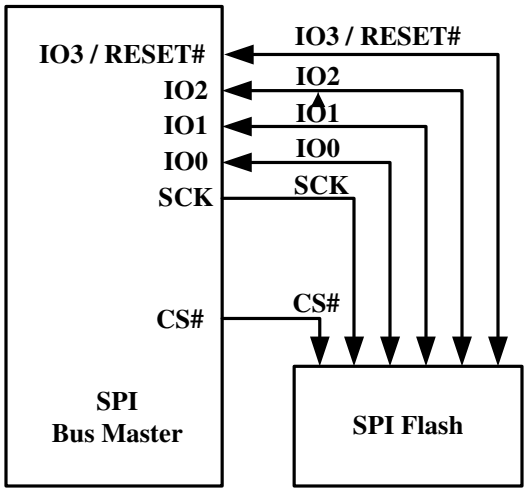


Figure 4.5 Bus Master and Memory Devices on the SPI Bus — Quad Bit Data Path — I/O3 / RESET#



5. Signal Protocols

5.1 SPI Clock Modes

5.1.1 Single Data Rate (SDR)

The FL-L family can be driven by an embedded micro-controller (bus master) in either of the two following clocking modes.

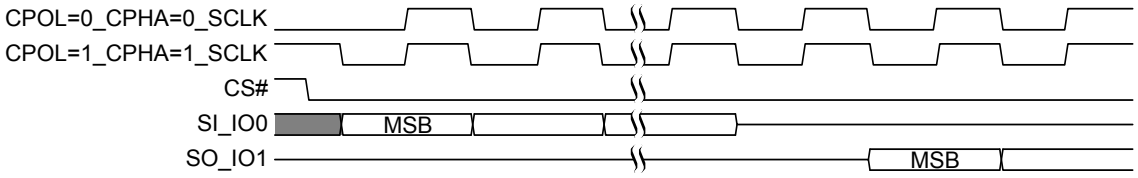
- **Mode 0** with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0
- **Mode 3** with CPOL = 1 and, CPHA = 1

For these two modes, input data into the device is always latched in on the rising edge of the SCK signal and the output data is always available from the falling edge of the SCK clock signal.

The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

- SCK will stay at logic low state with CPOL = 0, CPHA = 0
- SCK will stay at logic high state with CPOL = 1, CPHA = 1

Figure 5.1 SPI SDR Modes Supported



Timing diagrams throughout the remainder of the document are generally shown as both mode 0 and 3 by showing SCK as both high and low at the fall of CS#. In some cases a timing diagram may show only mode 0 with SCK low at the fall of CS#. In such a case, mode 3 timing simply means clock is high at the fall of CS# so no SCK rising edge set up or hold time to the falling edge of CS# is needed for mode 3.

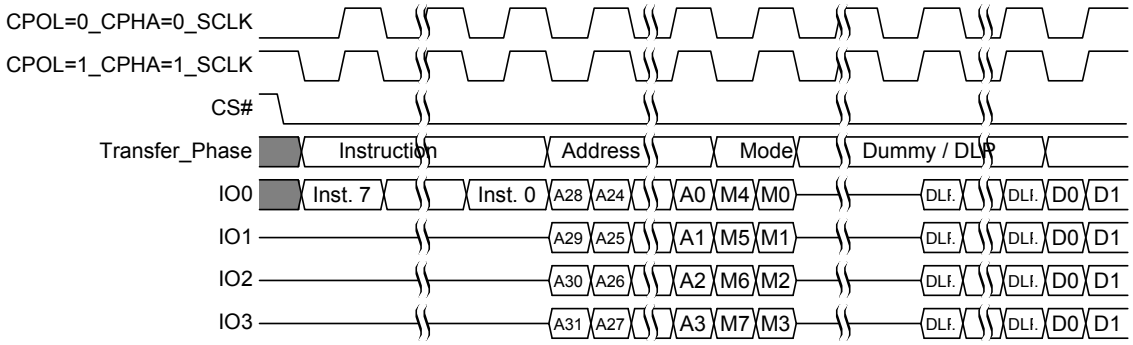
SCK cycles are measured (counted) from one falling edge of SCK to the next falling edge of SCK. In mode 0 the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already low at the beginning of a command.

5.1.2 Double Data Rate (DDR)

Mode 0 and Mode 3 are also supported for DDR commands. In DDR commands, the instruction bits are always latched on the rising edge of clock, the same as in SDR commands. However, the address and input data that follow the instruction are latched on both the rising and falling edges of SCK. The first address bit is latched on the first rising edge of SCK following the falling edge at the end of the last instruction bit. The first bit of output data is driven on the falling edge at the end of the last access latency (dummy) cycle.

SCK cycles are measured (counted) in the same way as in SDR commands, from one falling edge of SCK to the next falling edge of SCK. In mode 0 the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already low at the beginning of a command.

Figure 5.2 SPI DDR Modes Supported



5.2 Command Protocol

All communication between the host system and FL-L family memory devices is in the form of units called commands. See Section 8., *Commands* on page 59 for definition and details for all commands.

All commands begin with an 8-bit instruction that selects the type of information transfer or device operation to be performed. Commands may also have an address, instruction modifier, latency period, data transfer to the memory, or data transfer from the memory. All instruction, address, and data information is transferred sequentially between the host system and memory device.

Command protocols are also classified by a numerical nomenclature using three numbers to reference the transfer width of three command phases:

- instruction;
- address and instruction modifier (continuous read mode bits);
- data.

Single bit wide commands start with an instruction and may provide an address or data, all sent only on the SI signal. Data may be sent back to the host serially on the SO signal. This is referenced as a 1-1-1 command protocol for single bit width instruction, single bit width address and modifier, single bit data.

Dual-O or Quad-O commands provide an address sent from the host as serial on SI (IO0) then followed by dummy cycles. Data is returned to the host as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3. This is referenced as 1-1-2 for Dual-O and 1-1-4 for Quad-O command protocols.

Dual or Quad Input / Output (I/O) commands provide an address sent from the host as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3 then followed by dummy cycles. Data is returned to the host similarly as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3. This is referenced as 1-2-2 for Dual I/O and 1-4-4 for Quad I/O command protocols.

The FL-L family also supports a QPI mode in which all information is transferred in 4-bit width, including the instruction, address, modifier, and data. This is referenced as a 4-4-4 command protocol.

Commands are structured as follows:

- Each command begins with CS# going low and ends with CS# returning high. The memory device is selected by the host driving the Chip Select (CS#) signal low throughout a command.
- The serial clock (SCK) marks the transfer of each bit or group of bits between the host and memory.
- Each command begins with an eight bit (byte) instruction. The instruction selects the type of information transfer or device operation to be performed. The instruction transfers occur on SCK rising edges. However, some read commands are modified by a prior read command, such that the instruction is implied from the earlier command. This is called Continuous Read Mode. When the device is in continuous read mode, the instruction bits are not transmitted at the beginning of the command because the instruction is the same as the read command that initiated the Continuous Read Mode. In Continuous Read mode the command will begin with the read address. Thus, Continuous Read Mode removes eight instruction bits from each read command in a series of same type read commands.

- The instruction may be stand alone or may be followed by address bits to select a location within one of several address spaces in the device. The instruction determines the address space used. The address may be either a 24 bit or a 32 bit, byte boundary, address. The address transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- In legacy SPI mode, the width of all transfers following the instruction are determined by the instruction sent. Following transfers may continue to be single bit serial on only the SI or Serial Output (SO) signals, they may be done in two bit groups per (dual) transfer on the IO0 and IO1 signals, or they may be done in 4 bit groups per (quad) transfer on the IO0-IO3 signals. Within the dual or quad groups the least significant bit is on IO0. More significant bits are placed in significance order on each higher numbered IO signal. Single bits or parallel bit groups are transferred in most to least significant bit order.
- In QPI mode, the width of all transfers is a 4-bit wide (quad) transfer on the IO0-IO3 signals.
- Dual and Quad I/O read instructions send an instruction modifier called Continuous Read mode bits, following the address, to indicate whether the next command will be of the same type with an implied, rather than an explicit, instruction. These mode bits initiate or end the continuous read mode. In continuous read mode, the next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands. The mode bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- The address or mode bits may be followed by write data to be stored in the memory device or by a read latency period before read data is returned to the host.
- Write data bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- SCK continues to toggle during any read access latency period. The latency may be zero to several SCK cycles (also referred to as dummy cycles). At the end of the read latency cycles, the first read data bits are driven from the outputs on SCK falling edge at the end of the last read latency cycle. The first read data bits are considered transferred to the host on the following SCK rising edge. Each following transfer occurs on the next SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- If the command returns read data to the host, the device continues sending data transfers until the host takes the CS# signal high. The CS# signal can be driven high after any transfer in the read data sequence. This will terminate the command.
- At the end of a command that does not return data, the host drives the CS# input high. The CS# signal must go high after the eighth bit, of a stand alone instruction or, of the last write data byte that is transferred. That is, the CS# signal must be driven high when the number of bits after the CS# signal was driven low is an exact multiple of eight bits. If the CS# signal does not go high exactly at the eight bit boundary of the instruction or write data, the command is rejected and not executed.
- All instruction, address, and mode bits are shifted into the device with the Most Significant Bits (MSB) first. The data bits are shifted in and out of the device MSB first. All data is transferred in byte units with the lowest address byte sent first. Following bytes of data are sent in lowest to highest byte address order i.e. the byte address increments.
- All attempts to read the flash memory array during a program, erase, or a write cycle (embedded operations) are ignored. The embedded operation will continue to execute without any affect. A very limited set of commands are accepted during an embedded operation. These are discussed in the individual command descriptions.
- Depending on the command, the time for execution varies. A command to read status information from an executing command is available to determine when the command completes execution and whether the command was successful.

5.2.1 Command Sequence Examples

Figure 5.3 Stand Alone Instruction Command

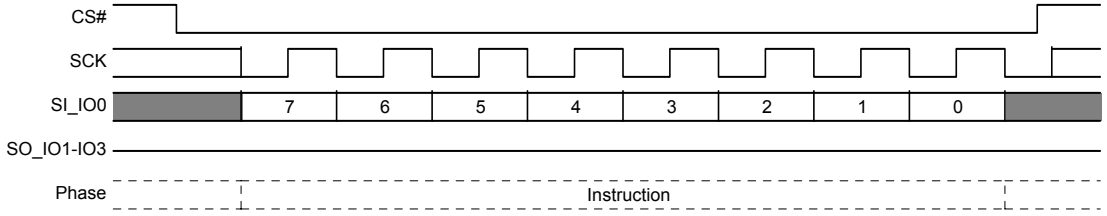


Figure 5.4 Single Bit Wide Input Command

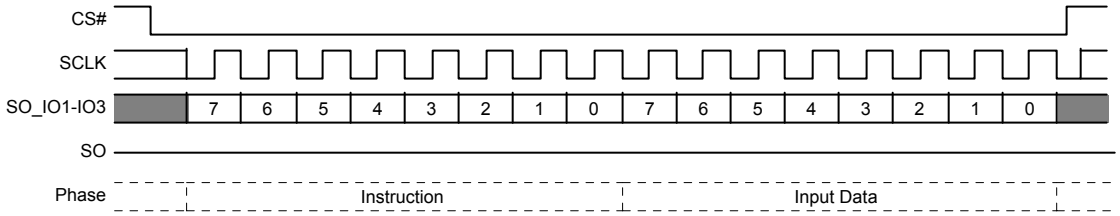


Figure 5.5 Single Bit Wide Output Command without Latency

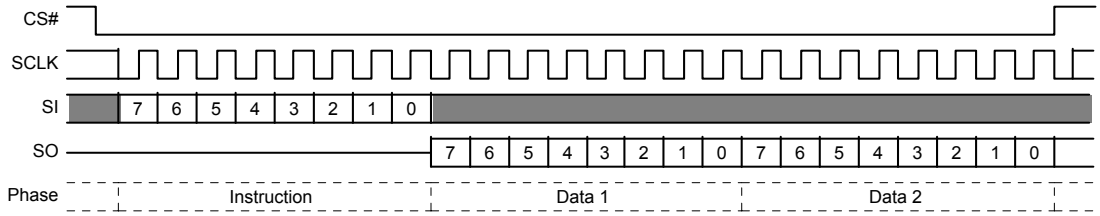


Figure 5.6 Single Bit Wide I/O Command with Latency

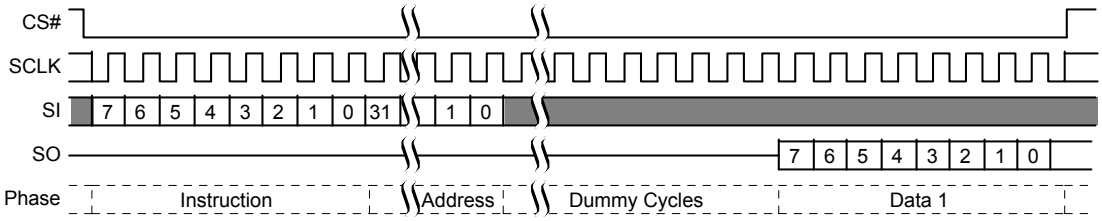


Figure 5.7 Dual Output Read Command

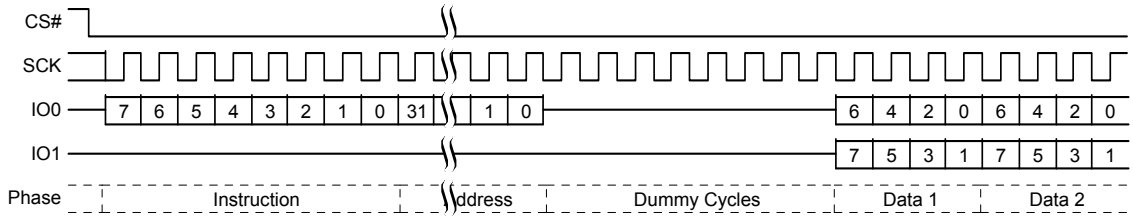


Figure 5.8 Quad Output Read Command

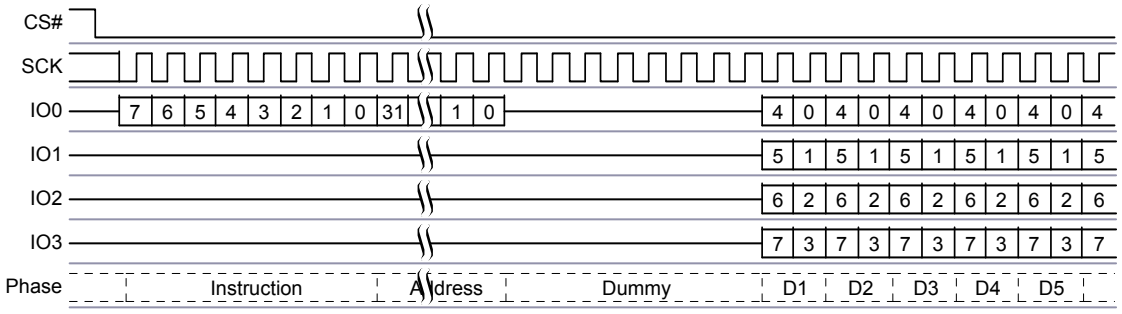


Figure 5.9 Dual I/O Command

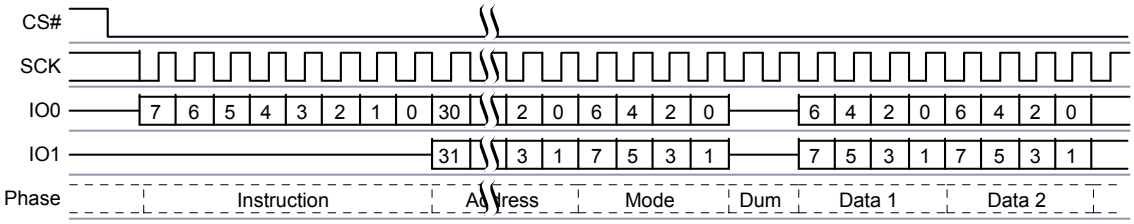
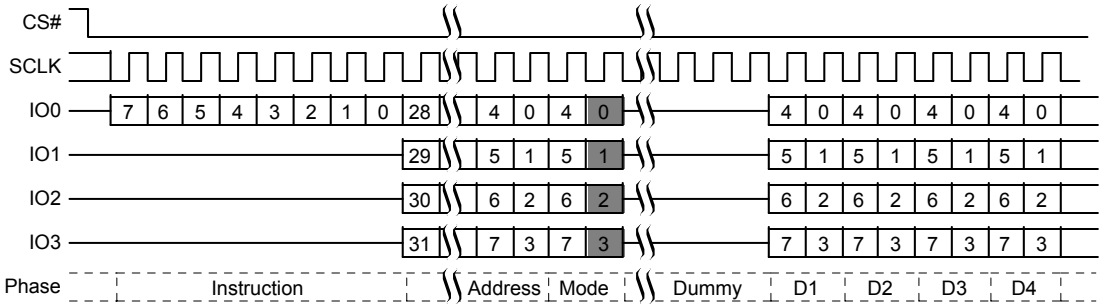
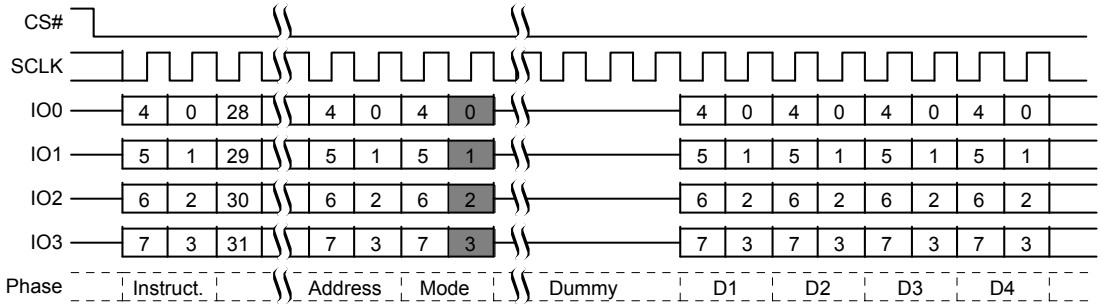


Figure 5.10 Quad I/O Command



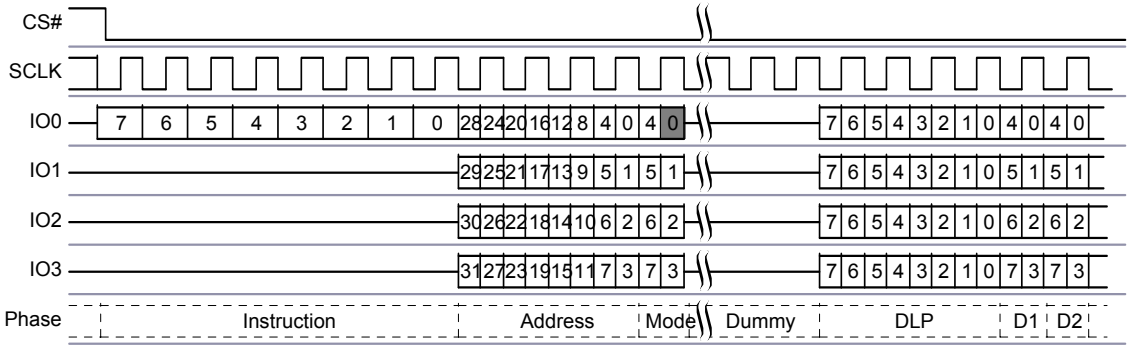
Note: The gray bits are optional, the host does not have to drive bits during that cycle.

Figure 5.11 Quad I/O Read Command in QPI Mode



Note: The gray bits are optional, the host does not have to drive bits during that cycle.

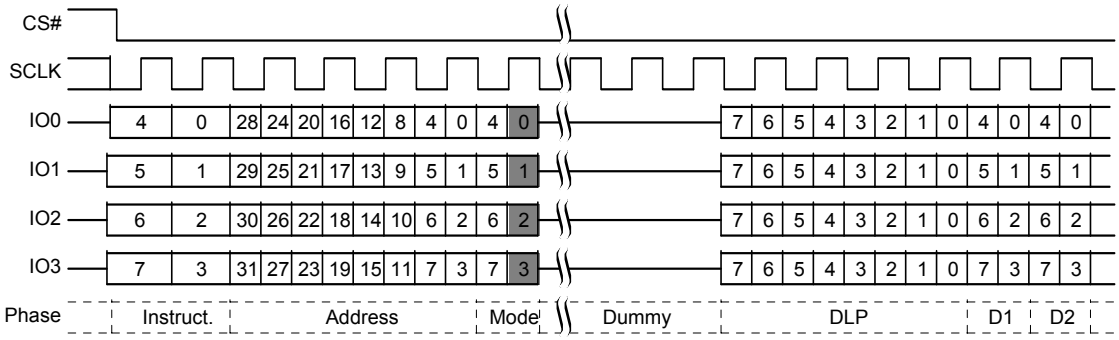
Figure 5.12 DDR Quad I/O Read Command



Note:

1. *The gray bits are optional, the host does not have to drive bits during that cycle.*

Figure 5.13 DDR Quad I/O Read Command QPI Mode



Note:

1. *The gray bits are optional, the host does not have to drive bits during that cycle.*

Additional sequence diagrams, specific to each command, are provided in section 8., *Commands* on page 59.

5.3 Interface States

This section describes the input and output signal levels as related to the SPI interface behavior.

Table 5.1 Interface States Summary

Interface State	V_{DD}	SCK	CS#	RESET#	IO3 / RESET#	WP# / IO2	SO / IO1	SI / IO0
Power-Off	<V_{DD} (low)	X	X	X	X	X	Z	X
Low Power Hardware Data Protection	<V_{DD} (cut-off)	X	X	X	X	X	Z	X
Power-On (Cold) Reset	≥V_{DD} (min)	X	HH	X	X	X	Z	X
Hardware (Warm) Reset Non-Quad Mode	≥V_{DD} (min)	X	X	HL	HL	X	Z	X
Hardware (Warm) Reset Quad Mode	≥V_{DD} (min)	X	HH	HL	HL	X	Z	X
Interface Standby	≥V_{DD} (min)	X	HH	HH	HH	X	Z	X
Instruction Cycle (Legacy SPI)	≥V_{DD} (min)	HT	HL	HH	HH	HV	Z	HV
Single Input Cycle Host to Memory Transfer	≥V_{DD} (min)	HT	HL	HH	HH	X	Z	HV
Single Latency (Dummy) Cycle	≥V_{DD} (min)	HT	HL	HH	HH	X	Z	X
Single Output Cycle Memory to Host Transfer	≥V_{DD} (min)	HT	HL	HH	HH	X	MV	X
Dual Input Cycle Host to Memory Transfer	≥V_{DD} (min)	HT	HL	HH	HH	X	HV	HV
Dual Latency (Dummy) Cycle	≥V_{DD} (min)	HT	HL	HH	HH	X	X	X
Dual Output Cycle Memory to Host Transfer	≥V_{DD} (min)	HT	HL	HH	HH	X	MV	MV
Quad Input Cycle Host to Memory Transfer	≥V_{DD} (min)	HT	HL	HH	HV	HV	HV	HV
Quad Latency (Dummy) Cycle	≥V_{DD} (min)	HT	HL	HH	X	X	X	X
Quad Output Cycle Memory to Host Transfer	≥V_{DD} (min)	HT	HL	HH	MV	MV	MV	MV
DDR Quad Input Cycle Host to Memory Transfer	≥V_{DD} (min)	HT	HL	HH	HV	HV	HV	HV
DDR Latency (Dummy) Cycle	≥V_{DD} (min)	HT	HL	HH	X	X	X	X
DDR Quad Output Cycle Memory to Host Transfer	≥V_{DD} (min)	HT	HL	HH	MV	MV	MV	MV

Legend

- Z = no driver - floating signal
- HL = Host driving V_{IL}
- HH = Host driving V_{IH}
- HV = either HL or HH
- X = HL or HH or Z
- HT = toggling between HL and HH
- ML = Memory driving V_{IL}
- MH = Memory driving V_{IH}
- MV = either ML or MH

5.3.1 Power-Off

When the core supply voltage is at or below the $V_{DD\ (Low)}$ voltage, the device is considered to be powered off. The device does not react to external signals, and is prevented from performing any program or erase operation.

5.3.2 Low Power Hardware Data Protection

When V_{DD} is less than $V_{DD\ (Cut\text{-}off)}$ the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range. When the core voltage supply remains at or below the $V_{DD\ (Low)}$ voltage for ≥ t_{PD} time, then rises to ≥ $V_{DD\ (Minimum)}$ the device will begin its Power On Reset (POR) process. POR continues until the end of t_{PU}. During t_{PU} the device does not react to external input signals nor drive any outputs. Following the end of t_{PU} the device transitions to the Interface Standby state and can accept commands. For additional information on POR see Section 12.3.1, *Power On (Cold) Reset* on page 133

5.3.3 Hardware (Warm) Reset

A configuration option is provided to allow IO3 / RESET# to be used as a hardware reset input when the device is not in any Quad or QPI mode or when it is in any Quad mode or QPI mode and CS# is high. In Quad or QPI mode on some packages a separate reset input is provided (RESET #). When IO3 / RESET# or RESET# is driven low for t_{RP} time the device starts the hardware reset process. The process continues for t_{RPH} time. Following the end of both t_{RPH} and the reset hold time following the rise of RESET# (t_{RH}) the device transitions to the Interface Standby state and can accept commands. For additional information on hardware reset see Section 12.3, *Reset* on page 133

5.3.4 Interface Standby

When CS# is high the SPI interface is in standby state. Inputs other than RESET# are ignored. The interface waits for the beginning of a new command. The next interface state is Instruction Cycle when CS# goes low to begin a new command.

While in interface standby state the memory device draws standby current (I_{SB}) if no embedded algorithm is in progress. If an embedded algorithm is in progress, the related current is drawn until the end of the algorithm when the entire device returns to standby current draw.

5.3.5 Instruction Cycle (Legacy SPI Mode)

When the host drives the MSB of an instruction and CS# goes low, on the next rising edge of SCK the device captures the MSB of the instruction that begins the new command. On each following rising edge of SCK the device captures the next lower significance bit of the 8 bit instruction. The host keeps CS# low, and drives the Write Protect (WP#) and IO3 / RESET# signals as needed for the instruction. However, WP# is only relevant during instruction cycles of a WRR or WRAR command or any other commands which affect Status registers, Configuration registers and DLR registers, and is other wise ignored. IO3 / RESET# is driven high when the device is not in Quad Mode (CR1V[1]=0) or QPI Mode (CR2V[3]=0) and hardware reset is not required.

Each instruction selects the address space that is operated on and the transfer format used during the remainder of the command. The transfer format may be Single, Dual O, Quad O, Dual I/O, or Quad I/O, or DDR Quad I/O. The expected next interface state depends on the instruction received.

Some commands are stand alone, needing no address or data transfer to or from the memory. The host returns CS# high after the rising edge of SCK for the eighth bit of the instruction in such commands. The next interface state in this case is Interface Standby.

5.3.6 Instruction Cycle (QPI Mode)

In QPI mode, when CR2V[3]=1, instructions are transferred 4 bits per cycle. In this mode instruction cycles are the same as a Quad Input Cycle. See Section 5.3.13, *QPP or QOR Address Input Cycle* on page 23.

5.3.7 Single Input Cycle — Host to Memory Transfer

Several commands transfer information after the instruction on the single serial input (SI) signal from host to the memory device. The host keeps RESET# high, CS# low, and drives SI as needed for the command. The memory does not drive the Serial Output (SO) signal.

The expected next interface state depends on the instruction. Some instructions continue sending address or data to the memory using additional Single Input Cycles. Others may transition to Single Latency, or directly to Single, Dual, or Quad Output cycle states.

5.3.8 Single Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main Flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR3V[3:0]). During the latency cycles, the host keeps RESET# and IO3 / RESET# high, CS# low and SCK toggles. The Write Protect (WP#) signal is ignored. The host may drive the SI signal during these cycles or the host may leave SI floating. The memory does not use any data driven on SO or other I/O signals during the latency cycles. The memory does not drive the Serial Output (SO) or I/O signals during the latency cycles.

The next interface state depends on the command structure i.e. the number of latency cycles, and whether the read is single, dual, or quad width.

5.3.9 Single Output Cycle — Memory to Host Transfer

Several commands transfer information back to the host on the single Serial Output (SO) signal. The host keeps RESET# and IO3 / RESET# high, CS# low. The Write Protect (WP#) signal is ignored. The memory ignores the Serial Input (SI) signal. The memory drives SO with data.

The next interface state continues to be Single Output Cycle until the host returns CS# to high ending the command.

5.3.10 Dual Input Cycle — Host to Memory Transfer

The Read Dual I/O command transfers two address or mode bits to the memory in each cycle. The host keeps RESET# and IO3 / RESET# high, CS# low. The Write Protect (WP#) signal is ignored. The host drives address on SI / IO0 and SO / IO1.

The next interface state following the delivery of address and mode bits is a Dual Latency Cycle if there are latency cycles needed or Dual Output Cycle if no latency is required.

5.3.11 Dual Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main Flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR3V[3:0]). During the latency cycles, the host keeps RESET# and IO3 / RESET# high, CS# low, and SCK continues to toggle. The Write Protect (WP#) signal is ignored. The host may drive the SI / IO0 and SO / IO1 signals during these cycles or the host may leave SI / IO0 and SO / IO1 floating. The memory does not use any data driven on SI / IO0 and SO / IO1 during the latency cycles. The host must stop driving SI / IO0 and SO / IO1 on the falling edge of SCK at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the SI / IO0 and SO / IO1 signals during the latency cycles.

The next interface state following the last latency cycle is a Dual Output Cycle.

5.3.12 Dual Output Cycle — Memory to Host Transfer

The Read Dual Output and Read Dual I/O return data to the host two bits in each cycle. The host keeps RESET# and IO3 / RESET# high, CS# low. The Write Protect (WP#) signal is ignored. The memory drives data on the SI / IO0 and SO / IO1 signals during the dual output cycles on the falling edge of SCK.

The next interface state continues to be Dual Output Cycle until the host returns CS# to high ending the command.

5.3.13 QPP or QOR Address Input Cycle

The Quad Page Program and Quad Output Read commands send address to the memory only on IO0. The other IO signals are ignored. The host keeps RESET# and IO3 / RESET# high, CS# low, and drives IO0.

For QPP the next interface state following the delivery of address is the Quad Input Cycle. For QOR the next interface state following address is a Quad Latency Cycle if there are latency cycles needed or Quad Output Cycle if no latency is required.

5.3.14 Quad Input Cycle — Host to Memory Transfer

The Quad I/O Read command transfers four address or mode bits to the memory in each cycle. In QPI mode the Quad I/O Read and Page Program commands transfer four data bits to the memory in each cycle, including the instruction cycles. The host keeps CS# low, and drives the IO signals.

For Quad I/O Read the next interface state following the delivery of address and mode bits is a Quad Latency Cycle if there are latency cycles needed or Quad Output Cycle if no latency is required. For QPI mode Page Program, the host returns CS# high following the delivery of data to be programmed and the interface returns to standby state.

5.3.15 Quad Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main Flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR3V[3:0]). During the latency cycles, the host keeps CS# low and continues to toggle SCK. The host may drive the IO signals during these cycles or the host may leave the IO floating. The memory does not use any data driven on IO during the latency cycles. The host must stop driving the IO signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the IO signals during the latency cycles.

The next interface state following the last latency cycle is a Quad Output Cycle.

5.3.16 Quad Output Cycle — Memory to Host Transfer

The Quad-O and Quad I/O Read returns data to the host four bits in each cycle. The host keeps CS# low. The memory drives data on IO0-IO3 signals during the Quad output cycles.

The next interface state continues to be Quad Output Cycle until the host returns CS# to high ending the command.

5.3.17 DDR Quad Input Cycle — Host to Memory Transfer

The DDR Quad I/O Read command sends address, and mode bits to the memory on all the IO signals. Four bits are transferred on the rising edge of SCK and four bits on the falling edge in each cycle. The host keeps CS# low.

The next interface state following the delivery of address and mode bits is a DDR Latency Cycle.

5.3.18 DDR Latency Cycle

DDR Read commands may have one to several latency cycles during which read data is read from the main Flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR3V[3:0]). During the latency cycles, the host keeps CS# low. The host may not drive the IO signals during these cycles. So that there is sufficient time for the host drivers to turn off before the memory begins to drive. This prevents driver conflict between host and memory when the signal direction changes. The memory has an option to drive all the IO signals with a Data Learning Pattern (DLP) during the last 4 latency cycles. The DLP option should not be enabled when there are fewer than five latency cycles so that there is at least one cycle of high impedance for turn around of the IO signals before the memory begins driving the DLP. When there are more than 4 cycles of latency the memory does not drive the IO signals until the last four cycles of latency.

The next interface state following the last latency cycle is a DDR Quad Output Cycle, depending on the instruction.

5.3.19 DDR Quad Output Cycle — Memory to Host Transfer

The DDR Quad I/O Read command returns bits to the host on all the IO signals. Four bits are transferred on the rising edge of SCK and four bits on the falling edge in each cycle. The host keeps CS# low.

The next interface state continues to be DDR Quad Output Cycle until the host returns CS# to high ending the command.

5.4 Data Protection

Some basic protection against unintended changes to stored data are provided and controlled purely by the hardware design. These are described below. Other software managed protection methods are discussed in the software section of this document.

5.4.1 Power-Up

When the core supply voltage is at or below the $V_{DD\ (Low)}$ voltage, the device is considered to be powered off. The device does not react to external signals, and is prevented from performing any program or erase operation. User is not allowed to enter any valid command during tPU

5.4.2 Low Power

When V_{DD} is less than $V_{DD\ (Cut\text{-}off)}$ the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

5.4.3 Clock Pulse Count

The device verifies that all non-volatile memory and register data modifying commands consist of a clock pulse count that is a multiple of eight bit transfers (byte boundary) before executing them. A command not ending on an 8 bit (byte) boundary is ignored and no error status is set for the command.

5.4.4 Deep Power Down (DPD)

In DPD mode the device responds only to the Resume from DPD command (RES ABh). All other commands are ignored during DPD mode, thereby protecting the memory from program and erase operations. If the IO3 / RESET# function has been enabled (CR2V[7]=1) or if RESET# is active, IO3 / RESET# or RESET# going low will start a hardware reset and release the device from DPD mode.