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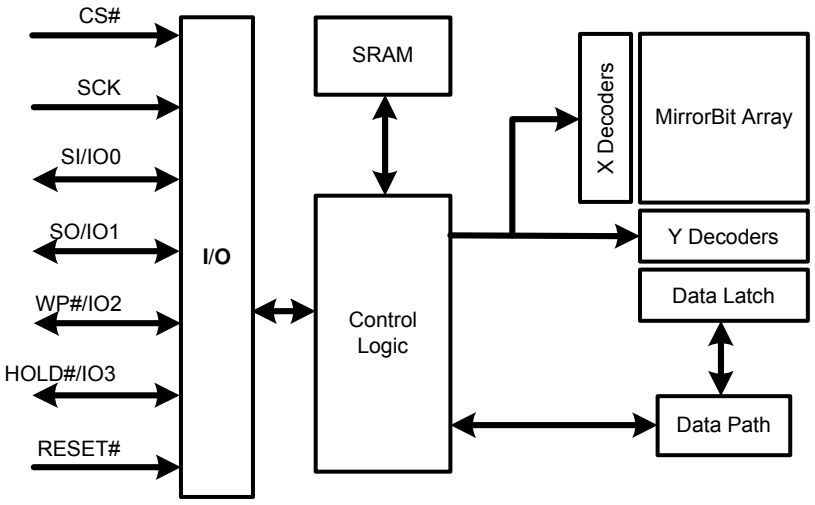
S25FL128S/S25FL256S

128 Mbit (16 Mbyte)/256 Mbit (32 Mbyte) 3.0V SPI Flash Memory

Features

- CMOS 3.0 Volt Core with Versatile I/O
- Serial Peripheral Interface (SPI) with Multi-I/O
  - SPI Clock polarity and phase modes 0 and 3
  - Double Data Rate (DDR) option
  - Extended Addressing: 24- or 32-bit address options
  - Serial Command set and footprint compatible with S25FL-A, S25FL-K, and S25FL-P SPI families
  - Multi I/O Command set and footprint compatible with S25FL-P SPI family
- READ Commands
  - Normal, Fast, Dual, Quad, Fast DDR, Dual DDR, Quad DDR
  - AutoBoot - power up or reset and execute a Normal or Quad read command automatically at a preselected address
  - Common Flash Interface (CFI) data for configuration information.
- Programming (1.5 Mbytes/s)
  - 256 or 512 Byte Page Programming buffer options
  - Quad-Input Page Programming (QPP) for slow clock systems
  - Automatic ECC -internal hardware Error Correction Code generation with single bit error correction
- Erase (0.5 to 0.65 Mbytes/s)
  - Hybrid sector size option - physical set of thirty two 4-kbyte sectors at top or bottom of address space with all remaining sectors of 64 kbytes, for compatibility with prior generation S25FL devices
  - Uniform sector option - always erase 256-kbyte blocks for software compatibility with higher density and future devices.
- Cycling Endurance
  - 100,000 Program-Erase Cycles, minimum
- Data Retention
  - 20 Year Data Retention, minimum
- Security features
  - One Time Program (OTP) array of 1024 bytes
  - Block Protection:
    - Status Register bits to control protection against program or erase of a contiguous range of sectors.
    - Hardware and software control options
  - Advanced Sector Protection (ASP)
    - Individual sector protection controlled by boot code or password
- Cypress® 65 nm MirrorBit® Technology with Eclipse™ Architecture
- Core Supply Voltage: 2.7V to 3.6V
- I/O Supply Voltage: 1.65V to 3.6V
  - SO16 and FBGA packages
- Temperature Range / Grade:
  - Industrial (-40°C to +85°C)
  - Industrial Plus (-40°C to +105°C)
  - Automotive AEC-Q100 Grade 3 (-40°C to +85°C)
  - Automotive AEC-Q100 Grade 2 (-40°C to +105°C)
  - Automotive AEC-Q100 Grade 1 (-40°C to +125°C)
- Packages (all Pb-free)
  - 16-lead SOIC (300 mil)
  - WSON 6 x 8 mm
  - BGA-24 6 x 8 mm
    - 5 x 5 ball (FAB024) and 4 x 6 ball (FAC024) footprint options
  - Known Good Die and Known Tested Die

Logic Block Diagram



Performance Summary

Maximum Read Rates with the Same Core and I/O Voltage (V_{IO} = V_{CC} = 2.7V to 3.6V)

Command	Clock Rate (MHz)	Mbytes/s
Read	50	6.25
Fast Read	133	16.6
Dual Read	104	26
Quad Read	104	52

Maximum Read Rates with Lower I/O Voltage (V_{IO} = 1.65V to 2.7V, V_{CC} = 2.7V to 3.6V)

Command	Clock Rate (MHz)	Mbytes/s
Read	50	6.25
Fast Read	66	8.25
Dual Read	66	16.5
Quad Read	66	33

Maximum Read Rates DDR (V_{IO} = V_{CC} = 3V to 3.6V)

Command	Clock Rate (MHz)	Mbytes/s
Fast Read DDR	80	20
Dual Read DDR	80	40
Quad Read DDR	80	80

Typical Program and Erase Rates

Operation	kbytes/s
Page Programming (256-byte page buffer - Hybrid Sector Option)	1000
Page Programming (512-byte page buffer - Uniform Sector Option)	1500
4-kbyte Physical Sector Erase (Hybrid Sector Option)	30
64-kbyte Physical Sector Erase (Hybrid Sector Option)	500
256-kbyte Logical Sector Erase (Uniform Sector Option)	500

Current Consumption

Operation	Current (mA)
Serial Read 50 MHz	16 (max)
Serial Read 133 MHz	33 (max)
Quad Read 104 MHz	61 (max)
Quad DDR Read 80 MHz	90 (max)
Program	100 (max)
Erase	100 (max)
Standby	0.07 (typ)

Contents

1. Overview

1.1 General Description

The Cypress S25FL128S and S25FL256S devices are flash non-volatile memory products using:

- MirrorBit technology - that stores two data bits in each memory array transistor
- Eclipse architecture - that dramatically improves program and erase performance
- 65 nm process lithography

This family of devices connect to a host system via a Serial Peripheral Interface (SPI). Traditional SPI single bit serial input and output (SIngle I/O or SIO) is supported as well as optional two bit (Dual I/O or DIO) and four bit (Quad I/O or QIO) serial commands. This multiple width interface is called SPI Multi-I/O or MIO. In addition, the FL-S family adds support for Double Data Rate (DDR) read commands for SIO, DIO, and QIO that transfer address and read data on both edges of the clock.

The Eclipse architecture features a Page Programming Buffer that allows up to 128 words (256 bytes) or 256 words (512 bytes) to be programmed in one operation, resulting in faster effective programming and erase than prior generation SPI program or erase algorithms.

Executing code directly from flash memory is often called Execute-In-Place or XIP. By using FL-S devices at the higher clock rates supported, with QIO or DDR-QIO commands, the instruction read transfer rate can match or exceed traditional parallel interface, asynchronous, NOR flash memories while reducing signal count dramatically.

The S25FL128S and S25FL256S products offer high densities coupled with the flexibility and fast performance required by a variety of embedded applications. They are ideal for code shadowing, XIP, and data storage.

1.2 Migration Notes

1.2.1 Features Comparison

The S25FL128S and S25FL256S devices are command set and footprint compatible with prior generation FL-K and FL-P families.

Table 1. FL Generations Comparison

Parameter	FL-K	FL-P	FL-S
Technology Node	90 nm	90 nm	65 nm
Architecture	Floating Gate	MirrorBit	MirrorBit Eclipse
Release Date	In Production	In Production	2H2011
Density	4 Mb - 128 Mb	32 Mb - 256 Mb	128 Mb - 256 Mb
Bus Width	x1, x2, x4	x1, x2, x4	x1, x2, x4
Supply Voltage	2.7V - 3.6V	2.7V - 3.6V	2.7V - 3.6V / 1.65V - 3.6V V_{IO}
Normal Read Speed (SDR)	6 MB/s (50 MHz)	5 MB/s (40 MHz)	6 MB/s (50 MHz)
Fast Read Speed (SDR)	13 MB/s (104 MHz)	13 MB/s (104 MHz)	17 MB/s (133 MHz)
Dual Read Speed (SDR)	26 MB/s (104 MHz)	20 MB/s (80 MHz)	26 MB/s (104 MHz)
Quad Read Speed (SDR)	52 MB/s (104 MHz)	40 MB/s (80 MHz)	52 MB/s (104 MHz)
Fast Read Speed (DDR)	-	-	20 MB/s (80 MHz)
Dual Read Speed (DDR)	-	-	40 MB/s (80 MHz)
Quad Read Speed (DDR)	-	-	80 MB/s (80 MHz)
Program Buffer Size	256B	256B	256B / 512B
Erase Sector Size	4 kB / 32 kB / 64 kB	64 kB / 256 kB	64 kB / 256 kB
Parameter Sector Size	4 kB	4 kB	4 kB (option)
Sector Erase Time (typ.)	30 ms (4 kB), 150 ms (64 kB)	500 ms (64 kB)	130 ms (64 kB), 520 ms (256 kB)
Page Programming Time (typ.)	700 µs (256B)	1500 µs (256B)	250 µs (256B), 340 µs (512B)
OTP	768B (3 x 256B)	506B	1024B
Advanced Sector Protection	No	No	Yes
Auto Boot Mode	No	No	Yes
Erase Suspend/Resume	Yes	No	Yes
Program Suspend/Resume	Yes	No	Yes
Operating Temperature	-40°C to +85°C	-40°C to +85°C / +105°C	-40°C to +85°C / +105°C / +125°C

Notes:

1. *256B program page option only for 128-Mb and 256-Mb density FL-S devices.*
2. *FL-P column indicates FL129P MIO SPI device (for 128-Mb density).*
3. *64-kB sector erase option only for 128-Mb/256-Mb density FL-P and FL-S devices.*
4. *FL-K family devices can erase 4-kB sectors in groups of 32 kB or 64 kB.*
5. *Refer to individual data sheets for further details.*

1.2.2 Known Differences from Prior Generations

1.2.2.1 Error Reporting

Prior generation FL memories either do not have error status bits or do not set them if program or erase is attempted on a protected sector. The FL-S family does have error reporting status bits for program and erase operations. These can be set when there is an internal failure to program or erase or when there is an attempt to program or erase a protected sector. In either case the program or erase operation did not complete as requested by the command.

1.2.2.2 Secure Silicon Region (OTP)

The size and format (address map) of the One Time Program area is different from prior generations. The method for protecting each portion of the OTP area is different. For additional details see Secure Silicon Region (OTP) on page 57.

1.2.2.3 Configuration Register Freeze Bit

The configuration register Freeze bit CR1[0], locks the state of the Block Protection bits as in prior generations. In the FL-S family it also locks the state of the configuration register TBPARM bit CR1[2], TBPROT bit CR1[5], and the Secure Silicon Region (OTP) area.

1.2.2.4 Sector Erase Commands

The command for erasing an 8-kbyte area (two 4-kbyte sectors) is not supported.

The command for erasing a 4-kbyte sector is supported only in the 128-Mbit and 256-Mbit density FL-S devices and only for use on the thirty two 4-kbyte parameter sectors at the top or bottom of the device address space.

The erase command for 64-kbyte sectors are supported for the 128-Mbit and 256-Mbit density FL-S devices when the ordering option for 4-kbyte parameter sectors with 64-kbyte uniform sectors are used. The 64-kbyte erase command may be applied to erase a group of sixteen 4-kbyte sectors.

The erase command for a 256-kbyte sector replaces the 64-kbyte erase command when the ordering option for 256-kbyte uniform sectors is used for the 128-Mbit and 256-Mbit density FL-S devices.

1.2.2.5 Deep Power Down

The Deep Power Down (DPD) function is not supported in FL-S family devices.

The legacy DPD (B9h) command code is instead used to enable legacy SPI memory controllers, that can issue the former DPD command, to access a new bank address register. The bank address register allows SPI memory controllers that do not support more than 24 bits of address, the ability to provide higher order address bits for commands, as needed to access the larger address space of the 256-Mbit density FL-S device. For additional information see Extended Address on page 45.

1.2.2.6 New Features

The FL-S family introduces several new features to SPI category memories:

- Extended address for access to higher memory density.
- AutoBoot for simpler access to boot code following power up.
- Enhanced High Performance read commands using mode bits to eliminate the overhead of SIO instructions when repeating the same type of read command.
- Multiple options for initial read latency (number of dummy cycles) for faster initial access time or higher clock rate read commands.
- DDR read commands for SIO, DIO, and QIO.
- Automatic ECC for enhanced data integrity.
- Advanced Sector Protection for individually controlling the protection of each sector. This is very similar to the Advanced Sector Protection feature found in several other Cypress parallel interface NOR memory families.

1.3 Glossary

Command	All information transferred between the host system and memory during one period while CS# is low. This includes the instruction (sometimes called an operation code or opcode) and any required address, mode bits, latency cycles, or data.
DDP (Dual Die Package)	Two die stacked within the same package to increase the memory capacity of a single package. Often also referred to as a Multi-Chip Package (MCP)
DDR (Double Data Rate)	When input and output are latched on every edge of SCK.
ECC	ECC Unit = 16 byte aligned and length data groups in the main Flash array and OTP array, each of which has its own hidden ECC syndrome to enable error correction on each group.
Flash	The name for a type of Electrical Erase Programmable Read Only Memory (EEPROM) that erases large blocks of memory bits in parallel, making the erase operation much faster than early EEPROM.
High	A signal voltage level ≥ V_{IH} or a logic level representing a binary one (1).
Instruction	The 8 bit code indicating the function to be performed by a command (sometimes called an operation code or opcode). The instruction is always the first 8 bits transferred from host system to the memory in any command.
Low	A signal voltage level ≤ V_{IL} or a logic level representing a binary zero (0).
LSB (Least Significant Bit)	Generally the right most bit, with the lowest order of magnitude value, within a group of bits of a register or data value.
MSB (Most Significant Bit)	Generally the left most bit, with the highest order of magnitude value, within a group of bits of a register or data value.
Non-Volatile	No power is needed to maintain data stored in the memory.
OPN (Ordering Part Number)	The alphanumeric string specifying the memory device type, density, package, factory non-volatile configuration, etc. used to select the desired device.
Page	512 bytes or 256 bytes aligned and length group of data. The size assigned for a page depends on the Ordering Part Number.
PCB	Printed Circuit Board
PPAP	Production Part Approval Process
Register Bit References	Are in the format: Register_name[bit_number] or Register_name[bit_range_MSB: bit_range_LSB]
SDR (Single Data Rate)	When input is latched on the rising edge and output on the falling edge of SCK.
Sector	Erase unit size; depending on device model and sector location this may be 4 kbytes, 64 kbytes or 256 kbytes.
Write	An operation that changes data within volatile or non-volatile registers bits or non-volatile flash memory. When changing non-volatile data, an erase and reprogramming of any unchanged non-volatile data is done, as part of the operation, such that the non-volatile data is modified by the write operation, in the same way that volatile data is modified – as a single operation. The non-volatile data appears to the host system to be updated by the single write command, without the need for separate commands for erase and reprogram of adjacent, but unaffected data.

1.4 Other Resources

1.4.1 Cypress Flash Memory Roadmap

www.cypress.com/product-roadmaps/cypress-flash-memory-roadmap

1.4.2 Links to Software

www.cypress.com/software-and-drivers-cypress-flash-memory

1.4.3 Links to Application Notes

www.cypress.com/appnotes

Hardware Interface

Serial Peripheral Interface with Multiple Input / Output (SPI-MIO)

Many memory devices connect to their host system with separate parallel control, address, and data signals that require a large number of signal connections and larger package size. The large number of connections increase power consumption due to so many signals switching and the larger package increases cost.

The S25FL128S and S25FL256S devices reduce the number of signals for connection to the host system by serially transferring all control, address, and data information over 4 to 6 signals. This reduces the cost of the memory package, reduces signal switching power, and either reduces the host connection count or frees host connectors for use in providing other features.

The S25FL128S and S25FL256S devices use the industry standard single bit Serial Peripheral Interface (SPI) and also supports optional extension commands for two bit (Dual) and four bit (Quad) wide serial transfers. This multiple width interface is called SPI Multi-I/O or SPI-MIO.

2. Signal Descriptions

2.1 Input/Output Summary

Table 2. Signal List

Signal Name	Type	Description
RESET#	Input	**Hardware Reset:** Low = device resets and returns to standby state, ready to receive a command. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used.
SCK	Input	**Serial Clock**
CS#	Input	**Chip Select**
SI / IO0	I/O	**Serial Input** for single bit data commands or IO0 for Dual or Quad commands.
SO / IO1	I/O	**Serial Output** for single bit data commands. IO1 for Dual or Quad commands.
WP# / IO2	I/O	**Write Protect** when not in Quad mode. IO2 in Quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
HOLD# / IO3	I/O	**Hold** (pause) serial transfer in single bit or Dual data commands. IO3 in Quad-I/O mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
V_{CC}	Supply	**Core Power Supply.**
V_{IO}	Supply	**Versatile I/O Power Supply.**
V_{SS}	Supply	**Ground.**
NC	Unused	**Not Connected.** No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). However, any signal connected to an NC must not have voltage levels higher than V_{IO}.
RFU	Reserved	**Reserved for Future Use.** No device internal signal is currently connected to the package connector but there is potential future use of the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU	Reserved	**Do Not Use.** A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

2.2 Address and Data Configuration

Traditional SPI single bit wide commands (Single or SIO) send information from the host to the memory only on the SI signal. Data may be sent back to the host serially on the Serial Output (SO) signal.

Dual or Quad Output commands send information from the host to the memory only on the SI signal. Data will be returned to the host as a sequence of bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Dual or Quad Input/Output (I/O) commands send information from the host to the memory as bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

2.3 RESET#

The RESET# input provides a hardware method of resetting the device to standby state, ready for receiving a command. When RESET# is driven to logic low (V_{IL}) for at least a period of t_{RP}, the device:

- terminates any operation in progress,
- tristates all outputs,
- resets the volatile bits in the Configuration Register,
- resets the volatile bits in the Status Registers,
- resets the Bank Address Register to zero,
- loads the Program Buffer with all ones,
- reloads all internal configuration information necessary to bring the device to standby mode,
- and resets the internal Control Unit to standby state.

RESET# causes the same initialization process as is performed when power comes up and requires t_{PU} time.

RESET# may be asserted low at any time. To ensure data integrity any operation that was interrupted by a hardware reset should be reinitiated once the device is ready to accept a command sequence.

When RESET# is first asserted Low, the device draws I_{CC1} (50 MHz value) during t_{PU}. If RESET# continues to be held at V_{SS} the device draws CMOS standby current (I_{SB}).

RESET# has an internal pull-up resistor and may be left unconnected in the host system if not used.

The RESET# input is not available on all packages options. When not available the RESET# input of the device is tied to the inactive state, inside the package.

2.4 Serial Clock (SCK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCK signal. Data output changes after the falling edge of SCK, in SDR commands, and after every edge in DDR commands.

2.5 Chip Select (CS#)

The chip select signal indicates when a command for the device is in process and the other signals are relevant for the memory device. When the CS# signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. Unless an internal Program, Erase or Write Registers (WRR) embedded operation is in progress, the device will be in the Standby Power mode. Driving the CS# input to logic low state enables the device, placing it in the Active Power mode. After Power-up, a falling edge on CS# is required prior to the start of any command.

2.6 Serial Input (SI) / IO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal.

SI becomes IO0 - an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

2.7 Serial Output (SO) / IO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal.

SO becomes IO1 - an input and output during Dual and Quad commands for receiving addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

2.8 Write Protect (WP#) / IO2

When WP# is driven Low (V_{IL}), during a WRR command and while the Status Register Write Disable (SRWD) bit of the Status Register is set to a 1, it is not possible to write to the Status and Configuration Registers. This prevents any alteration of the Block Protect (BP2, BP1, BP0) and TBPROT bits of the Status Register. As a consequence, all the data bytes in the memory area that are protected by the Block Protect and TBPROT bits, are also hardware protected against data modification if WP# is Low during a WRR command.

The WP# function is not available when the Quad mode is enabled (CR[1]=1). The WP# function is replaced by IO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

WP# has an internal pull-up resistor; when unconnected, WP# is at V_{IH} and may be left unconnected in the host system if not used for Quad mode.

2.9 Hold (HOLD#) / IO3

The Hold (HOLD#) signal is used to pause any serial communications with the device without deselecting the device or stopping the serial clock.

To enter the Hold condition, the device must be selected by driving the CS# input to the logic low state. It is recommended that the user keep the CS# input low state during the entire duration of the Hold condition. This is to ensure that the state of the interface logic remains unchanged from the moment of entering the Hold condition. If the CS# input is driven to the logic high state while the device is in the Hold condition, the interface logic of the device will be reset. To restart communication with the device, it is necessary to drive HOLD# to the logic high state while driving the CS# signal into the logic low state. This prevents the device from going back into the Hold condition.

The Hold condition starts on the falling edge of the Hold (HOLD#) signal, provided that this coincides with SCK being at the logic low state. If the falling edge does not coincide with the SCK signal being at the logic low state, the Hold condition starts whenever the SCK signal reaches the logic low state. Taking the HOLD# signal to the logic low state does not terminate any Write, Program or Erase operation that is currently in progress.

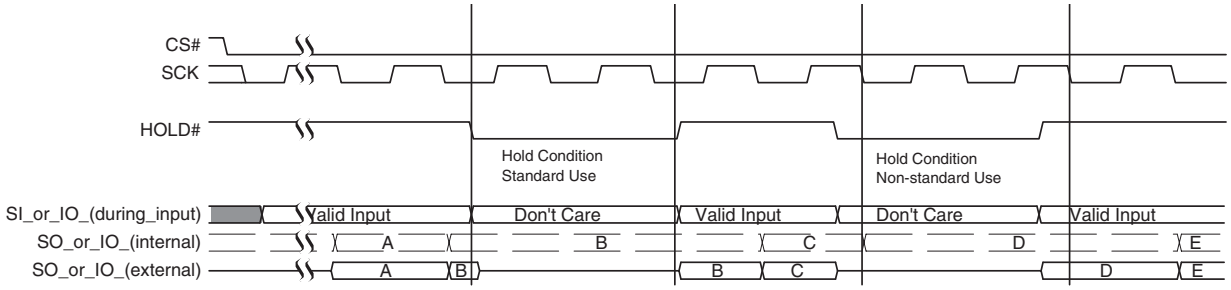
During the Hold condition, SO is in high impedance and both the SI and SCK input are Don't Care.

The Hold condition ends on the rising edge of the Hold (HOLD#) signal, provided that this coincides with the SCK signal being at the logic low state. If the rising edge does not coincide with the SCK signal being at the logic low state, the Hold condition ends whenever the SCK signal reaches the logic low state.

The HOLD# function is not available when the Quad mode is enabled (CR1[1] =1). The Hold function is replaced by IO3 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

The HOLD# signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad mode.

Figure 1. HOLD Mode Operation



2.10 Core Voltage Supply (V_{CC})

V_{CC} is the voltage source for all device internal logic. It is the single voltage used for all device internal functions including read, program, and erase. The voltage may vary from 2.7V to 3.6V.

2.11 Versatile I/O Power Supply (V_{IO})

The Versatile I/O (V_{IO}) supply is the voltage source for all device input receivers and output drivers and allows the host system to set the voltage levels that the device tolerates on all inputs and drives on outputs (address, control, and IO signals). The V_{IO} range is 1.65V to V_{CC}. V_{IO} cannot be greater than V_{CC}.

For example, a V_{IO} of 1.65V - 3.6V allows for I/O at the 1.8V, 2.5V or 3V levels, driving and receiving signals to and from other 1.8V, 2.5V or 3V devices on the same data bus. V_{IO} may be tied to V_{CC} so that interface signals operate at the same voltage as the core of the device. V_{IO} is not available in all package options, when not available the V_{IO} supply is tied to V_{CC} internal to the package.

During the rise of power supplies the V_{IO} supply voltage must remain less than or equal to the V_{CC} supply voltage. This supply is not available in all package options. For a backward compatible SO16 footprint, the V_{IO} supply is tied to V_{CC} inside the package; thus, the IO will function at V_{CC} level.

2.12 Supply and Signal Ground (V_{SS})

V_{SS} is the common voltage drain and ground reference for the device core, input signal receivers, and output drivers.

2.13 Not Connected (NC)

No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). However, any signal connected to an NC must not have voltage levels higher than V_{IO}.

2.14 Reserved for Future Use (RFU)

No device internal signal is currently connected to the package connector but is there potential future use of the connector. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.

2.15 Do Not Use (DNU)

A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.

2.16 Block Diagrams

Figure 2. Bus Master and Memory Devices on the SPI Bus - Single Bit Data Path

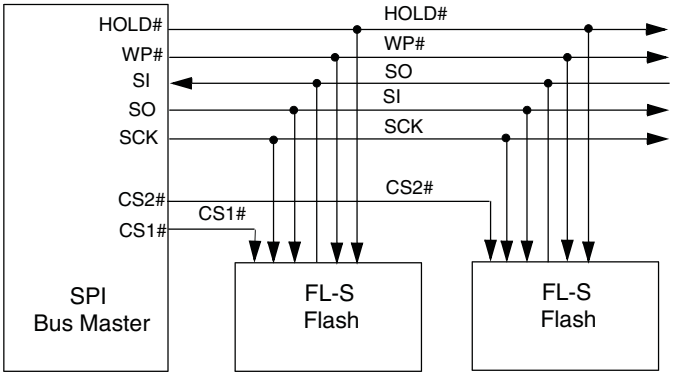


Figure 3. Bus Master and Memory Devices on the SPI Bus - Dual Bit Data Path

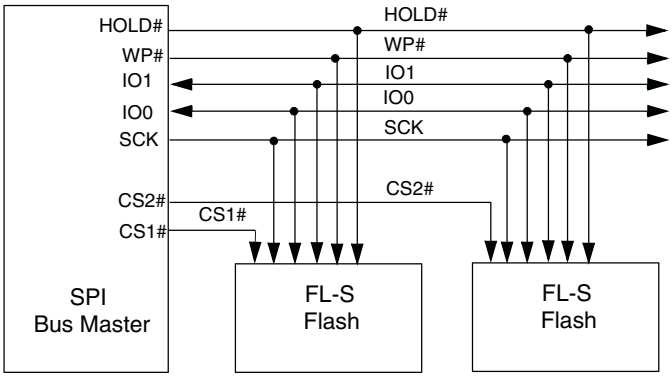
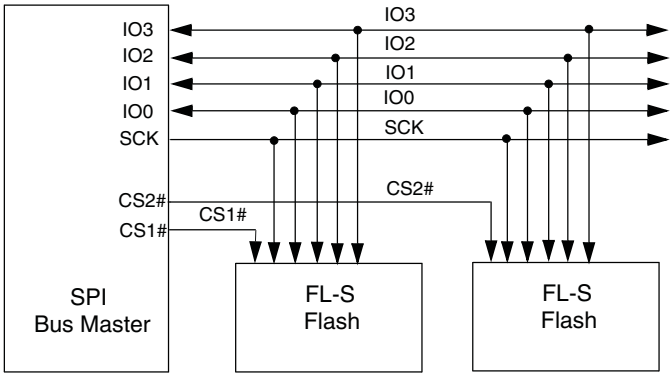


Figure 4. Bus Master and Memory Devices on the SPI Bus - Quad Bit Data Path



3. Signal Protocols

3.1 SPI Clock Modes

3.1.1 Single Data Rate (SDR)

The S25FL128S and S25FL256S devices can be driven by an embedded microcontroller (bus master) in either of the two following clocking modes.

- **Mode 0** with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0
- **Mode 3** with CPOL = 1 and, CPHA = 1

For these two modes, input data into the device is always latched in on the rising edge of the SCK signal and the output data is always available from the falling edge of the SCK clock signal.

The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

- SCK will stay at logic low state with CPOL = 0, CPHA = 0
- SCK will stay at logic high state with CPOL = 1, CPHA = 1

Figure 5. SPI SDR Modes Supported

Timing diagrams throughout the remainder of the document are generally shown as both mode 0 and 3 by showing SCK as both high and low at the fall of CS#. In some cases a timing diagram may show only mode 0 with SCK low at the fall of CS#. In such a case, mode 3 timing simply means clock is high at the fall of CS# so no SCK rising edge set up or hold time to the falling edge of CS# is needed for mode 3.

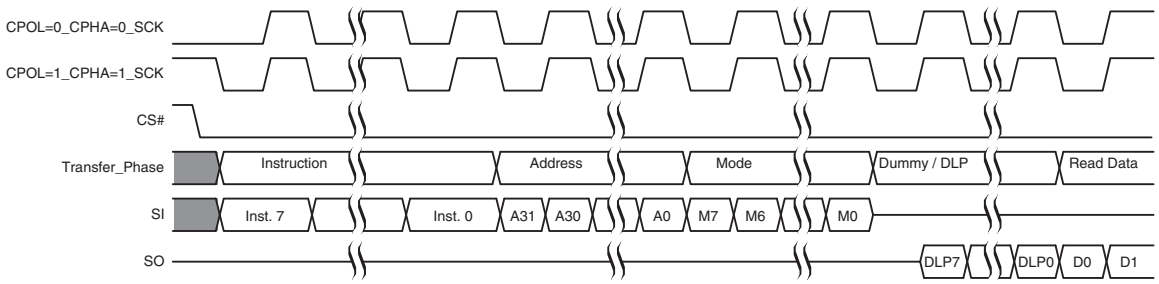
SCK cycles are measured (counted) from one falling edge of SCK to the next falling edge of SCK. In mode 0 the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already low at the beginning of a command.

3.1.2 Double Data Rate (DDR)

Mode 0 and Mode 3 are also supported for DDR commands. In DDR commands, the instruction bits are always latched on the rising edge of clock, the same as in SDR commands. However, the address and input data that follow the instruction are latched on both the rising and falling edges of SCK. The first address bit is latched on the first rising edge of SCK following the falling edge at the end of the last instruction bit. The first bit of output data is driven on the falling edge at the end of the last access latency (dummy) cycle.

SCK cycles are measured (counted) in the same way as in SDR commands, from one falling edge of SCK to the next falling edge of SCK. In mode 0 the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already low at the beginning of a command.

Figure 6. SPI DDR Modes Supported



3.2 Command Protocol

All communication between the host system and S25FL128S and S25FL256S memory devices is in the form of units called commands.

All commands begin with an instruction that selects the type of information transfer or device operation to be performed. Commands may also have an address, instruction modifier, latency period, data transfer to the memory, or data transfer from the memory. All instruction, address, and data information is transferred serially between the host system and memory device.

All instructions are transferred from host to memory as a single bit serial sequence on the SI signal.

Single bit wide commands may provide an address or data sent only on the SI signal. Data may be sent back to the host serially on the SO signal.

Dual or Quad Output commands provide an address sent to the memory only on the SI signal. Data will be returned to the host as a sequence of bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Dual or Quad Input/Output (I/O) commands provide an address sent from the host as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Commands are structured as follows:

- Each command begins with CS# going low and ends with CS# returning high. The memory device is selected by the host driving the Chip Select (CS#) signal low throughout a command.
- The serial clock (SCK) marks the transfer of each bit or group of bits between the host and memory.
- Each command begins with an eight bit (byte) instruction. The instruction is always presented only as a single bit serial sequence on the Serial Input (SI) signal with one bit transferred to the memory device on each SCK rising edge. The instruction selects the type of information transfer or device operation to be performed.
- The instruction may be stand alone or may be followed by address bits to select a location within one of several address spaces in the device. The instruction determines the address space used. The address may be either a 24-bit or a 32-bit byte boundary, address. The address transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- The width of all transfers following the instruction are determined by the instruction sent. Following transfers may continue to be single bit serial on only the SI or Serial Output (SO) signals, they may be done in two bit groups per (dual) transfer on the IO0 and IO1 signals, or they may be done in 4 bit groups per (quad) transfer on the IO0-IO3 signals. Within the dual or quad groups the least significant bit is on IO0. More significant bits are placed in significance order on each higher numbered IO signal. SIngle bits or parallel bit groups are transferred in most to least significant bit order.
- Some instructions send an instruction modifier called mode bits, following the address, to indicate that the next command will be of the same type with an implied, rather than an explicit, instruction. The next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands. The mode bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- The address or mode bits may be followed by write data to be stored in the memory device or by a read latency period before read data is returned to the host.
- Write data bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- SCK continues to toggle during any read access latency period. The latency may be zero to several SCK cycles (also referred to as dummy cycles). At the end of the read latency cycles, the first read data bits are driven from the outputs on SCK falling edge at the end of the last read latency cycle. The first read data bits are considered transferred to the host on the following SCK rising edge. Each following transfer occurs on the next SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- If the command returns read data to the host, the device continues sending data transfers until the host takes the CS# signal high. The CS# signal can be driven high after any transfer in the read data sequence. This will terminate the command.
- At the end of a command that does not return data, the host drives the CS# input high. The CS# signal must go high after the eighth bit, of a stand alone instruction or, of the last write data byte that is transferred. That is, the CS# signal must be driven high when the number of clock cycles after CS# signal was driven low is an exact multiple of eight cycles. If the CS# signal does not go high exactly at the eight SCK cycle boundary of the instruction or write data, the command is rejected and not executed.
- All instruction, address, and mode bits are shifted into the device with the Most Significant Bits (MSB) first. The data bits are shifted in and out of the device MSB first. All data is transferred in byte units with the lowest address byte sent first. Following bytes of data are sent in lowest to highest byte address order i.e. the byte address increments.

- All attempts to read the flash memory array during a program, erase, or a write cycle (embedded operations) are ignored. The embedded operation will continue to execute without any affect. A very limited set of commands are accepted during an embedded operation. These are discussed in the individual command descriptions.
- Depending on the command, the time for execution varies. A command to read status information from an executing command is available to determine when the command completes execution and whether the command was successful.

3.2.1 Command Sequence Examples

Figure 7. Stand Alone Instruction Command

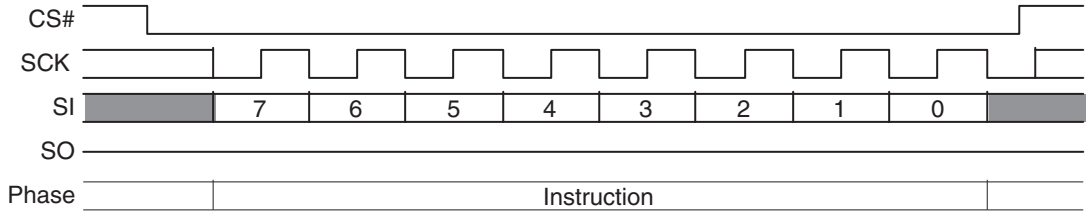


Figure 8. Single Bit Wide Input Command

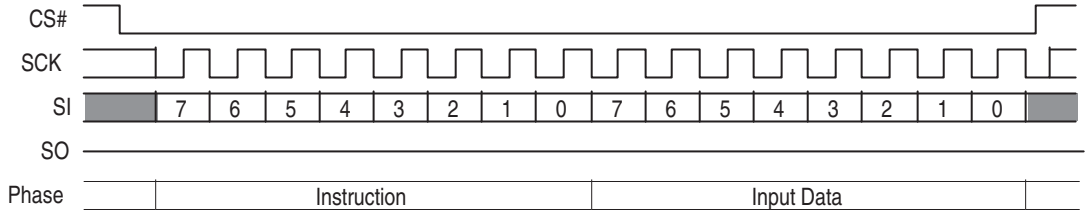


Figure 9. Single Bit Wide Output Command

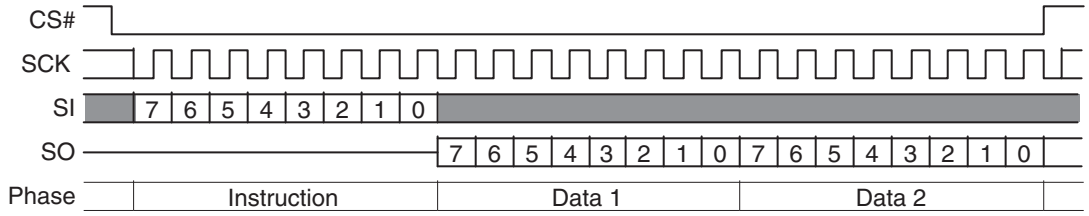


Figure 10. Single Bit Wide I/O Command without Latency

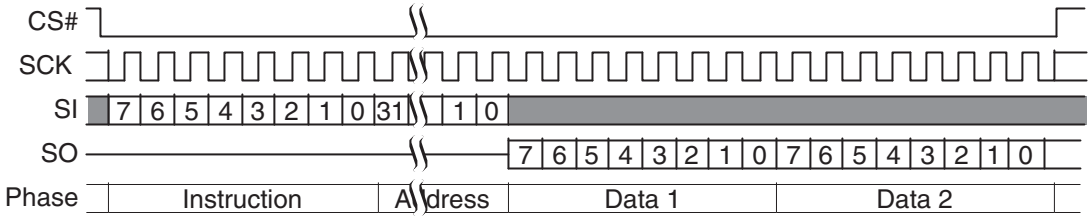


Figure 11. Single Bit Wide I/O Command with Latency

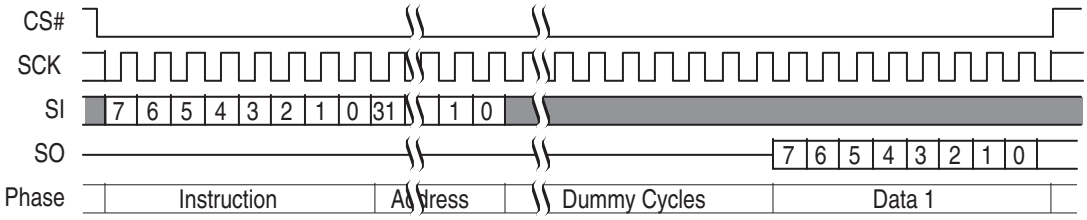


Figure 12. Dual Output Command

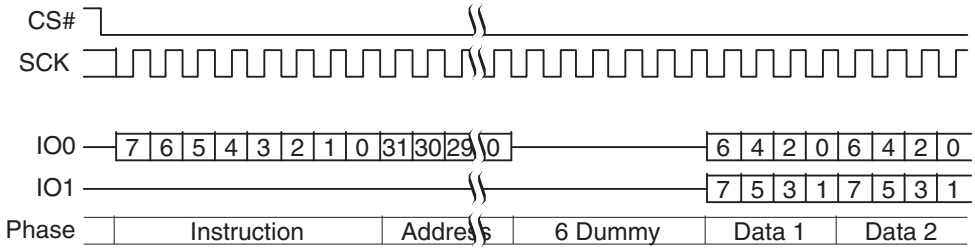


Figure 13. Quad Output Command without Latency

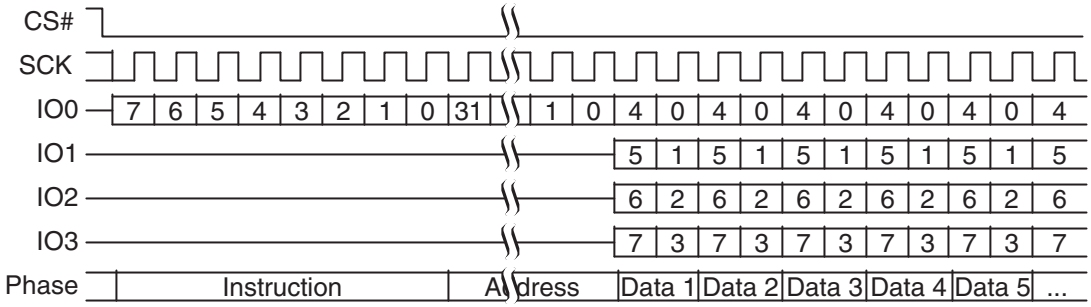


Figure 14. Dual I/O Command

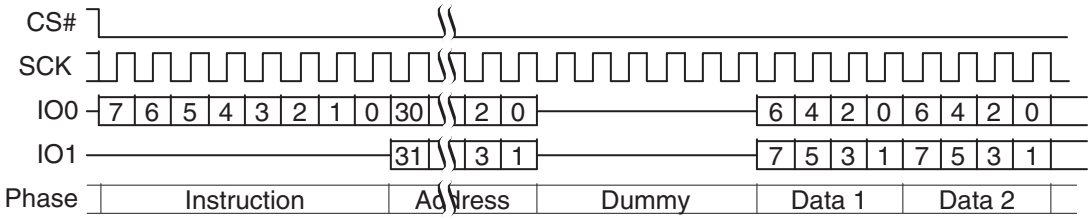


Figure 15. Quad I/O Command

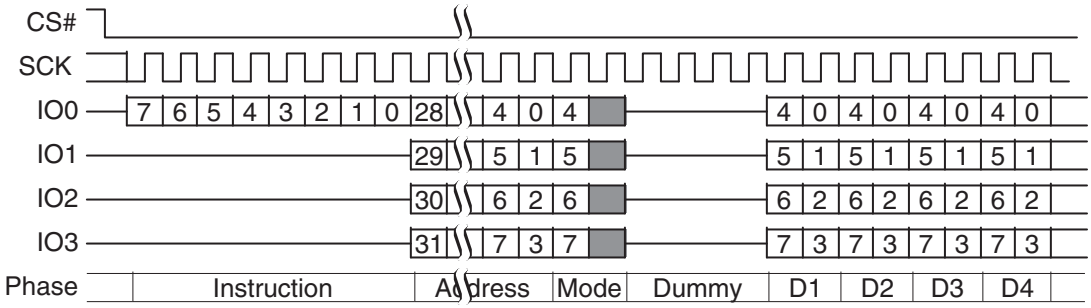


Figure 16. DDR Fast Read with EHPLC = 00b

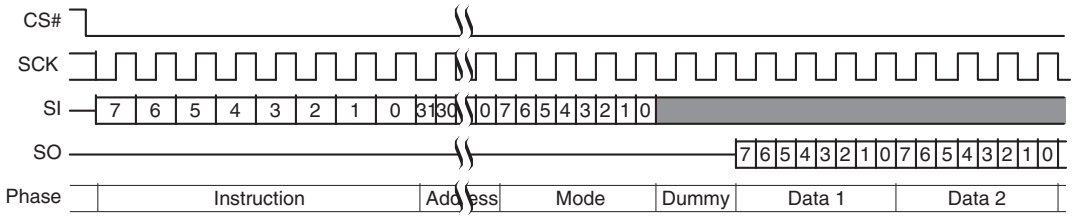


Figure 17. DDR Dual I/O Read with EHPLC = 01b and DLP

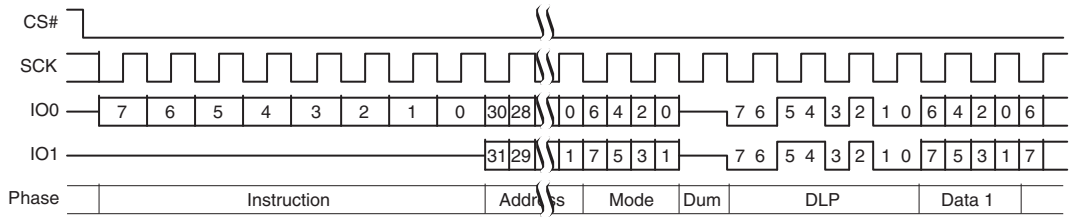
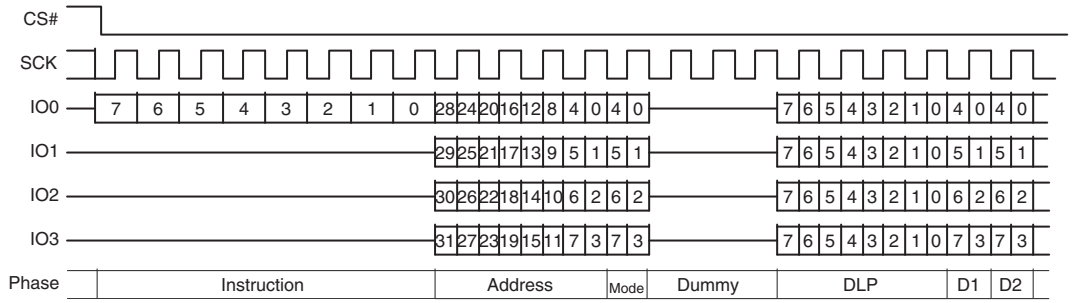


Figure 18. DDR Quad I/O Read



Additional sequence diagrams, specific to each command, are provided in Section 9., Commands on page 63.

3.3 Interface States

This section describes the input and output signal levels as related to the SPI interface behavior.

Table 3. Interface States Summary

Interface State	V_{CC}	V_{IO}	RESET#	SCK	CS#	HOLD# / IO3	WP# / IO2	SO / IO1	SI / IO0
Power-Off	< V_{CC} (low)	≤ V_{CC}	X	X	X	X	X	Z	X
Low Power Hardware Data Protection	< V_{CC} (cut-off)	≤ V_{CC}	X	X	X	X	X	Z	X
Power-On (Cold) Reset	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	X	X	X	X	X	Z	X
Hardware (Warm) Reset	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HL	X	X	X	X	Z	X
Interface Standby	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	X	HH	X	X	Z	X
Instruction Cycle	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HH	HV	Z	HV
Hold Cycle	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HV or HT	HL	HL	X	X	X
Single Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HH	X	Z	HV
Single Latency (Dummy) Cycle	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HH	X	Z	X
Single Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HH	X	MV	X
Dual Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HH	X	HV	HV
Dual Latency (Dummy) Cycle	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HH	X	X	X
Dual Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HH	X	MV	MV
QPP Address Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	X	X	X	HV
Quad Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HV	HV	HV	HV
Quad Latency (Dummy) Cycle	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	X	X	X	X
Quad Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	MV	MV	MV	MV
DDR Single Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	X	X	X	HV
DDR Dual Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	X	X	HV	HV
DDR Quad Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	HV	HV	HV	HV
DDR Latency (Dummy) Cycle	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	MV or Z	MV or Z	MV or Z	MV or Z
DDR Single Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	Z	Z	MV	X
DDR Dual Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	Z	Z	MV	MV
DDR Quad Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	≥ V_{IO} (min) ≤ V_{CC}	HH	HT	HL	MV	MV	MV	MV

Legend
Z = No driver - floating signal
HL = Host driving V_{IL}
HH = Host driving V_{IH}
HV = Either HL or HH
X = HL or HH or Z
HT = Toggling between HL and HH
ML = Memory driving V_{IL}
MH = Memory driving V_{IH}
MV = Either ML or MH

3.3.1 Power-Off

When the core supply voltage is at or below the V_{CC} (low) voltage, the device is considered to be powered off. The device does not react to external signals, and is prevented from performing any program or erase operation.

3.3.2 Low Power Hardware Data Protection

When V_{CC} is less than V_{CC} (cut-off) the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

3.3.3 Power-On (Cold) Reset

When the core voltage supply remains at or below the V_{CC} (low) voltage for ≥ t_{PD} time, then rises to ≥ $V_{CC\ (Minimum)}$ the device will begin its Power-On Reset (POR) process. POR continues until the end of t_{PU}. During t_{PU} the device does not react to external input signals nor drive any outputs. Following the end of t_{PU} the device transitions to the Interface Standby state and can accept commands. For additional information on POR see Power-On (Cold) Reset on page 30.

3.3.4 Hardware (Warm) Reset

Some of the device package options provide a RESET# input. When RESET# is driven low for t_{RP} time the device starts the hardware reset process. The process continues for t_{RPH} time. Following the end of both t_{RPH} and the reset hold time following the rise of RESET# (t_{RH}) the device transitions to the Interface Standby state and can accept commands. For additional information on hardware reset see POR followed by Hardware Reset on page 30.

3.3.5 Interface Standby

When CS# is high the SPI interface is in standby state. Inputs other than RESET# are ignored. The interface waits for the beginning of a new command. The next interface state is Instruction Cycle when CS# goes low to begin a new command.

While in interface standby state the memory device draws standby current (I_{SB}) if no embedded algorithm is in progress. If an embedded algorithm is in progress, the related current is drawn until the end of the algorithm when the entire device returns to standby current draw.

3.3.6 Instruction Cycle

When the host drives the MSB of an instruction and CS# goes low, on the next rising edge of SCK the device captures the MSB of the instruction that begins the new command. On each following rising edge of SCK the device captures the next lower significance bit of the 8-bit instruction. The host keeps RESET# high, CS# low, HOLD# high, and drives Write Protect (WP#) signal as needed for the instruction. However, WP# is only relevant during instruction cycles of a WRR command and is otherwise ignored.

Each instruction selects the address space that is operated on and the transfer format used during the remainder of the command. The transfer format may be Single, Dual output, Quad output, Dual I/O, Quad I/O, DDR Single I/O, DDR Dual I/O, or DDR Quad I/O. The expected next interface state depends on the instruction received.

Some commands are stand alone, needing no address or data transfer to or from the memory. The host returns CS# high after the rising edge of SCK for the eighth bit of the instruction in such commands. The next interface state in this case is Interface Standby.

3.3.7 Hold

When Quad mode is not enabled (CR[1]=0) the HOLD# / IO3 signal is used as the HOLD# input. The host keeps RESET# high, HOLD# low, SCK may be at a valid level or continue toggling, and CS# is low. When HOLD# is low a command is paused, as though SCK were held low. SI / IO0 and SO / IO1 ignore the input level when acting as inputs and are high impedance when acting as outputs during hold state. Whether these signals are input or output depends on the command and the point in the command sequence when HOLD# is asserted low.

When HOLD# returns high the next state is the same state the interface was in just before HOLD# was asserted low.

When Quad mode is enabled the HOLD# / IO3 signal is used as IO3.

During DDR commands the HOLD# and WP# inputs are ignored.

3.3.8 Single Input Cycle - Host to Memory Transfer

Several commands transfer information after the instruction on the single serial input (SI) signal from host to the memory device. The dual output, and quad output commands send address to the memory using only SI but return read data using the I/O signals. The host keeps RESET# high, CS# low, HOLD# high, and drives SI as needed for the command. The memory does not drive the Serial Output (SO) signal.

The expected next interface state depends on the instruction. Some instructions continue sending address or data to the memory using additional Single Input Cycles. Others may transition to Single Latency, or directly to Single, Dual, or Quad Output.

3.3.9 Single Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR[7:6]). During the latency cycles, the host keeps RESET# high, CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The host may drive the SI signal during these cycles or the host may leave SI floating. The memory does not use any data driven on SI / I/O0 or other I/O signals during the latency cycles. In dual or quad read commands, the host must stop driving the I/O signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving I/O signals during latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the Serial Output (SO) or I/O signals during the latency cycles.

The next interface state depends on the command structure i.e. the number of latency cycles, and whether the read is single, dual, or quad width.

3.3.10 Single Output Cycle - Memory to Host Transfer

Several commands transfer information back to the host on the single Serial Output (SO) signal. The host keeps RESET# high, CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The memory ignores the Serial Input (SI) signal. The memory drives SO with data.

The next interface state continues to be Single Output Cycle until the host returns CS# to high ending the command.

3.3.11 Dual Input Cycle - Host to Memory Transfer

The Read Dual I/O command transfers two address or mode bits to the memory in each cycle. The host keeps RESET# high, CS# low, HOLD# high. The Write Protect (WP#) signal is ignored. The host drives address on SI / IO0 and SO / IO1.

The next interface state following the delivery of address and mode bits is a Dual Latency Cycle if there are latency cycles needed or Dual Output Cycle if no latency is required.

3.3.12 Dual Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR[7:6]). During the latency cycles, the host keeps RESET# high, CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The host may drive the SI / IO0 and SO / IO1 signals during these cycles or the host may leave SI / IO0 and SO / IO1 floating. The memory does not use any data driven on SI / IO0 and SO / IO1 during the latency cycles. The host must stop driving SI / IO0 and SO / IO1 on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the SI / IO0 and SO / IO1 signals during the latency cycles.

The next interface state following the last latency cycle is a Dual Output Cycle.

3.3.13 Dual Output Cycle - Memory to Host Transfer

The Read Dual Output and Read Dual I/O return data to the host two bits in each cycle. The host keeps RESET# high, CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The memory drives data on the SI / IO0 and SO / IO1 signals during the dual output cycles.

The next interface state continues to be Dual Output Cycle until the host returns CS# to high ending the command.

3.3.14 QPP or QOR Address Input Cycle

The Quad Page Program and Quad Output Read commands send address to the memory only on IO0. The other IO signals are ignored because the device must be in Quad mode for these commands thus the Hold and Write Protect features are not active. The host keeps RESET# high, CS# low, and drives IO0.

For QPP the next interface state following the delivery of address is the Quad Input Cycle.

For QOR the next interface state following address is a Quad Latency Cycle if there are latency cycles needed or Quad Output Cycle if no latency is required.

3.3.15 Quad Input Cycle - Host to Memory Transfer

The Quad I/O Read command transfers four address or mode bits to the memory in each cycle. The Quad Page Program command transfers four data bits to the memory in each cycle. The host keeps RESET# high, CS# low, and drives the IO signals.

For Quad I/O Read the next interface state following the delivery of address and mode bits is a Quad Latency Cycle if there are latency cycles needed or Quad Output Cycle if no latency is required. For Quad Page Program the host returns CS# high following the delivery of data to be programmed and the interface returns to standby state.

3.3.16 Quad Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR[7:6]). During the latency cycles, the host keeps RESET# high, CS# low. The host may drive the IO signals during these cycles or the host may leave the IO floating. The memory does not use any data driven on IO during the latency cycles. The host must stop driving the IO signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the IO signals during the latency cycles.

The next interface state following the last latency cycle is a Quad Output Cycle.

3.3.17 Quad Output Cycle - Memory to Host Transfer

The Quad Output Read and Quad I/O Read return data to the host four bits in each cycle. The host keeps RESET# high, and CS# low. The memory drives data on IO0-IO3 signals during the Quad output cycles.

The next interface state continues to be Quad Output Cycle until the host returns CS# to high ending the command.

3.3.18 DDR Single Input Cycle - Host to Memory Transfer

The DDR Fast Read command sends address, and mode bits to the memory only on the IO0 signal. One bit is transferred on the rising edge of SCK and one bit on the falling edge in each cycle. The host keeps RESET# high, and CS# low. The other IO signals are ignored by the memory.

The next interface state following the delivery of address and mode bits is a DDR Latency Cycle.

3.3.19 DDR Dual Input Cycle - Host to Memory Transfer

The DDR Dual I/O Read command sends address, and mode bits to the memory only on the IO0 and IO1 signals. Two bits are transferred on the rising edge of SCK and two bits on the falling edge in each cycle. The host keeps RESET# high, and CS# low. The IO2 and IO3 signals are ignored by the memory.

The next interface state following the delivery of address and mode bits is a DDR Latency Cycle.

3.3.20 DDR Quad Input Cycle - Host to Memory Transfer

The DDR Quad I/O Read command sends address, and mode bits to the memory on all the IO signals. Four bits are transferred on the rising edge of SCK and four bits on the falling edge in each cycle. The host keeps RESET# high, and CS# low.

The next interface state following the delivery of address and mode bits is a DDR Latency Cycle.

3.3.21 DDR Latency Cycle

DDR Read commands may have one to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR[7:6]). During the latency cycles, the host keeps RESET# high and CS# low. The host may not drive the IO signals during these cycles. So that there is sufficient time for the host drivers to turn off before the memory begins to drive. This prevents driver conflict between host and memory when the signal direction changes. The memory has an option to drive all the IO signals with a Data Learning Pattern (DLP) during the last 4 latency cycles. The DLP option should not be enabled when there are fewer than five latency cycles so that there is at least one cycle of high impedance for turn around of the IO signals before the memory begins driving the DLP. When there are more than 4 cycles of latency the memory does not drive the IO signals until the last four cycles of latency.

The next interface state following the last latency cycle is a DDR Single, Dual, or Quad Output Cycle, depending on the instruction.

3.3.22 DDR Single Output Cycle - Memory to Host Transfer

The DDR Fast Read command returns bits to the host only on the SO / IO1 signal. One bit is transferred on the rising edge of SCK and one bit on the falling edge in each cycle. The host keeps RESET# high, and CS# low. The other IO signals are not driven by the memory.

The next interface state continues to be DDR Single Output Cycle until the host returns CS# to high ending the command.

3.3.23 DDR Dual Output Cycle - Memory to Host Transfer

The DDR Dual I/O Read command returns bits to the host only on the IO0 and IO1 signals. Two bits are transferred on the rising edge of SCK and two bits on the falling edge in each cycle. The host keeps RESET# high, and CS# low. The IO2 and IO3 signals are not driven by the memory.

The next interface state continues to be DDR Dual Output Cycle until the host returns CS# to high ending the command.

3.3.24 DDR Quad Output Cycle - Memory to Host Transfer

The DDR Quad I/O Read command returns bits to the host on all the IO signals. Four bits are transferred on the rising edge of SCK and four bits on the falling edge in each cycle. The host keeps RESET# high, and CS# low.

The next interface state continues to be DDR Quad Output Cycle until the host returns CS# to high ending the command.

3.4 Configuration Register Effects on the Interface

The configuration register bits 7 and 6 (CR1[7:6]) select the latency code for all read commands. The latency code selects the number of mode bit and latency cycles for each type of instruction.

The configuration register bit 1 (CR1[1]) selects whether Quad mode is enabled to ignore HOLD# and WP# and allow Quad Page Program, Quad Output Read, and Quad I/O Read commands. Quad mode must also be selected to allow Read DDR Quad I/O commands.

3.5 Data Protection

Some basic protection against unintended changes to stored data are provided and controlled purely by the hardware design. These are described below. Other software managed protection methods are discussed in the Software Interface on page 45 section of this document.

3.5.1 Power-Up

When the core supply voltage is at or below the V_{CC} (low) voltage, the device is considered to be powered off. The device does not react to external signals, and is prevented from performing any program or erase operation. Program and erase operations continue to be prevented during the Power-on Reset (POR) because no command is accepted until the exit from POR to the Interface Standby state.

3.5.2 Low Power

When V_{CC} is less than V_{CC} (cut-off) the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

3.5.3 Clock Pulse Count

The device verifies that all program, erase, and Write Registers (WRR) commands consist of a clock pulse count that is a multiple of eight before executing them. A command not having a multiple of 8 clock pulse count is ignored and no error status is set for the command.

4. Electrical Specifications

4.1 Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Storage Temperature Plastic Packages	–65°C to +150°C
Ambient Temperature with Power Applied	–65°C to +125°C
V_{CC}	–0.5V to +4.0V
V_{IO} (Note 1)	–0.5V to +4.0V
Input voltage with respect to Ground (V_{SS}) (Note 2)	–0.5V to +(V_{IO} + 0.5V)
Output Short Circuit Current (Note 3)	100 mA

Notes:
1. *V_{IO} must always be less than or equal V_{CC} + 200 mV.*
2. *See Input Signal Overshoot on page 25 for allowed maximums during signal transition.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

4.2 Thermal Resistance

Table 5. Thermal Resistance

Parameter	Description	WNG008	SO316	FAB024	FAC024	Unit
Theta JA	Thermal resistance (junction to ambient)	28	38	36	36.5	°C/W

4.3 Operating Ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

4.3.1 Power Supply Voltages

Some package options provide access to a separate input and output buffer power supply called V_{IO}. Packages which do not provide the separate V_{IO} connection, internally connect the device V_{IO} to V_{CC}. For these packages the references to V_{IO} are then also references to V_{CC}.

V_{CC}	2.7V to 3.6V
V_{IO}	1.65V to V_{CC} +200 mV

4.3.2 Temperature Ranges

Parameter	Symbol	Device	Spec		Unit
			Min	Max	
Ambient Temperature	T_A	Industrial (I)	–40	+85	°C
		Industrial Plus (V)	–40	+105	
		Extended (N)	–40	+125	
		Automotive, AEC-Q100 Grade 3 (A)	–40	+85	
		Automotive, AEC-Q100 Grade 2 (B)	–40	+105	
		Automotive AEC-Q100 Grade 1 (M)	–40	+125	

Note:
1. *Industrial Plus operating and performance parameters will be determined by device characterization and may vary from standard industrial temperature range devices as currently shown in this specification.*

4.3.3 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{IO}. During voltage transitions, inputs or I/Os may overshoot V_{SS} to –2.0V or overshoot to V_{IO} +2.0V, for periods up to 20 ns.

Figure 19. Maximum Negative Overshoot Waveform

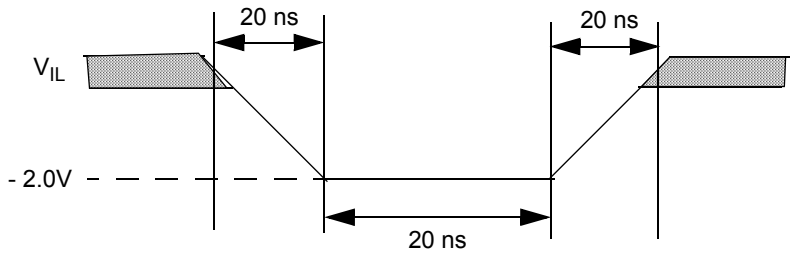
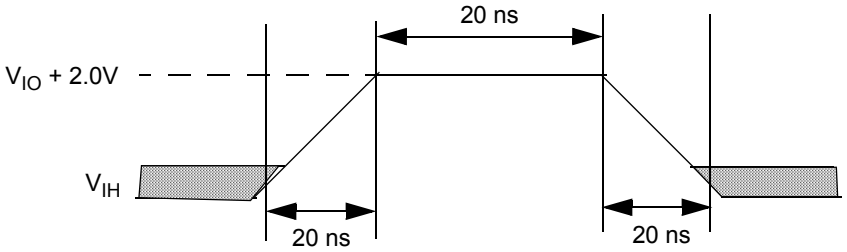


Figure 20. Maximum Positive Overshoot Waveform



4.4 Power-Up and Power-Down

The device must not be selected at power-up or power-down (that is, CS# must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value as follows:

- V_{CC} (min) at power-up, and then for a further delay of t_{PU}
- V_{SS} at power-down

A simple pull-up resistor (generally of the order of 100 kΩ) on Chip Select (CS#) can usually be used to insure safe and proper power-up and power-down.

The device ignores all instructions until a time delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold. See Figure 21. However, correct operation of the device is not guaranteed if V_{CC} returns below V_{CC} (min) during t_{PU}. No command should be sent to the device until the end of t_{PU}.