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Continuity of Ordering Part Numbers

Cypress continues to support existing part numbers. To order these products, please use only the Ordering Part Numbers listed in this document.

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S25FL129P

128-Mbit 3.0 V Flash Memory

This product is not recommended for new and current designs. For new and current designs, S25FL128S supersedes S25FL129P. This is the factory-recommended migration path. Please refer to the S25FL128S data sheet for specifications and ordering information.

Distinctive Characteristics

Architectural Advantages

- Single power supply operation
  - Full voltage range: 2.7 to 3.6V read and write operations
- Memory architecture
  - Uniform 64 KB sectors
    - Top or bottom parameter block (Two 64-KB sectors broken down into sixteen 4-KB sub-sectors each)
  - Uniform 256 KB sectors (no 4-KB sub-sectors)
  - 256-byte page size
  - Backward compatible with the S25FL128P (uniform 256 KB sector) device
- Program
  - Page Program (up to 256 bytes) in 1.5 ms (typical)
  - Program operations are on a page by page basis
  - Accelerated programming mode via 9V W#/ACC pin
  - Quad Page Programming
- Erase
  - Bulk erase function
  - Sector erase (SE) command (D8h) for 64 KB and 256 KB sectors
  - Sub-sector erase (P4E) command (20h) for 4 KB sectors (for uniform 64-KB sector device only)
  - Sub-sector erase (P8E) command (40h) for 8 KB sectors (for uniform 64-KB sector device only)
- Cycling endurance
  - 100,000 cycles per sector typical
- Data retention
  - 20 years typical
- Device ID
  - JEDEC standard two-byte electronic signature
  - RES command one-byte electronic signature for backward compatibility
- One time programmable (OTP) area for permanent, secure identification; can be programmed and locked at the factory or by the customer
- CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
- Process technology
  - Manufactured on 0.09 µm MirrorBit® process technology
- Package option
  - Industry Standard Pinouts
  - 16-pin SO package (300 mils)
  - 8-contact WSON package (6 x 8 mm)
  - 24-ball BGA (6 x 8 mm) package, 5 x 5 pin configuration
  - 24-ball BGA (6 x 8 mm) package, 6 x 4 pin configuration

Performance Characteristics

- Speed
  - Normal READ (Serial): 40 MHz clock rate
  - FAST_READ (Serial): 104 MHz clock rate (maximum)
  - DUAL I/O FAST_READ: 80 MHz clock rate or 20 MB/s effective data rate
  - QUAD I/O FAST_READ: 80 MHz clock rate or 40 MB/s effective data rate
- Power saving standby mode
  - Standby Mode 80 µA (typical)
  - Deep Power-Down Mode 3 µA (typical)

Memory Protection Features

- Memory protection
  - W#/ACC pin works in conjunction with Status Register Bits to protect specified memory areas
  - Status Register Block Protection bits (BP2, BP1, BP0) in status

General Description

The S25FL129P is a 3.0 Volt (2.7V to 3.6V), single-power-supply Flash memory device. The device is offered in two configurations: 256 uniform 64 KB sectors with the two (Top or Bottom) 64 KB sectors further split up into thirty-two 4 KB sub sectors, or 64 uniform 256 KB sectors. The S25FL129P device is backward compatible with the S25FL128P (uniform 256 KB sector) device.

The device accepts data written to SI (Serial Input) and outputs data on SO (Serial Output). The devices are designed to be programmed in-system with the standard system 3.0-volt V_{CC} supply.

The S25FL129P device adds the following high-performance features using 5 new instructions:

- Dual Output Read using both SI and SO pins as output pins at a clock rate of up to 80 MHz
- Quad Output Read using SI, SO, W#/ACC and HOLD# pins as output pins at a clock rate of up to 80 MHz
- Dual I/O High Performance Read using both SI and SO pins as input and output pins at a clock rate of up to 80 MHz
- Quad I/O High Performance Read using SI, SO, W#/ACC and HOLD# pins as input and output pins at a clock rate of up to 80 MHz
- Quad Page Programming using SI, SO, W#/ACC and HOLD# pins as input pins to program data at a clock rate of up to 80 MHz

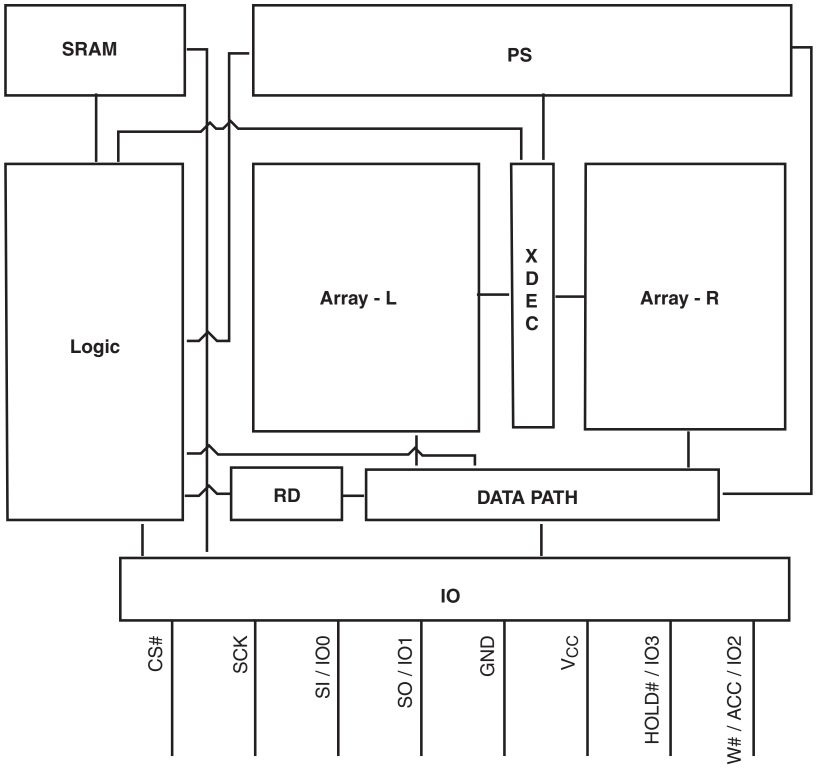
The memory can be programmed 1 to 256 bytes at a time, using the Page Program command. The device supports Sector Erase and Bulk Erase commands.

Each device requires only a 3.0-volt power supply (2.7V to 3.6V) for both read and write functions. Internally generated and regulated voltages are provided for the program operations. This device requires a high voltage supply to the W#/ACC pin to enable the Accelerated Programming mode.

The S25FL129P device also offers a One-Time Programmable area (OTP) of up to 128-bits (16 bytes) for permanent secure identification and an additional 490 bytes of OTP space for other use. This OTP area can be programmed or read using the OTPP or OTPR instructions.

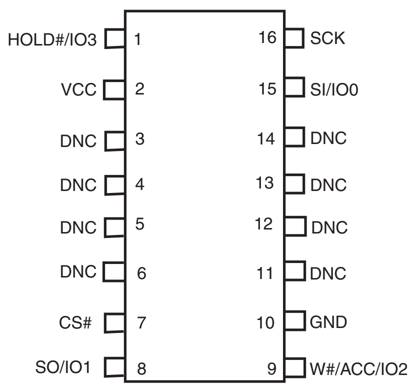
Contents

1. Block Diagram



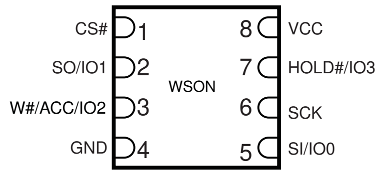
2. Connection Diagrams

Figure 2.1 16-pin Plastic Small Outline Package (SO)



Note
DNC = Do Not Connect (Reserved for future use)

Figure 2.2 8-contact WSON Package (6 x 8 mm)



Note

There is an exposed central pad on the underside of the WSON package. This should not be connected to any voltage or signal line on the PCB. Connecting the central pad to GND (V_{SS}) is possible, provided PCB routing ensures 0mV difference between voltage at the WSON GND (V_{SS}) lead and the central exposed pad.

Figure 2.3 6 x 8 mm 24-ball BGA Package, 5 x 5 Pin Configuration

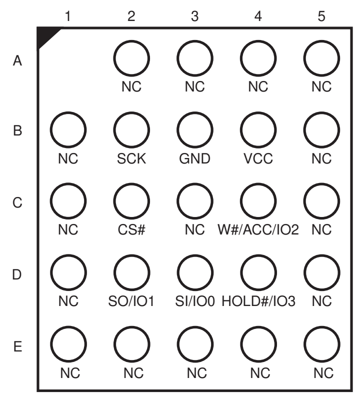
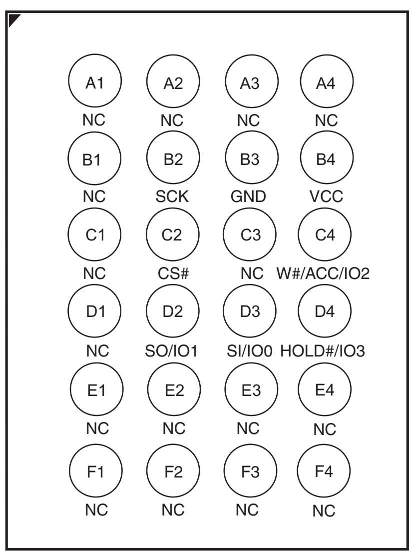


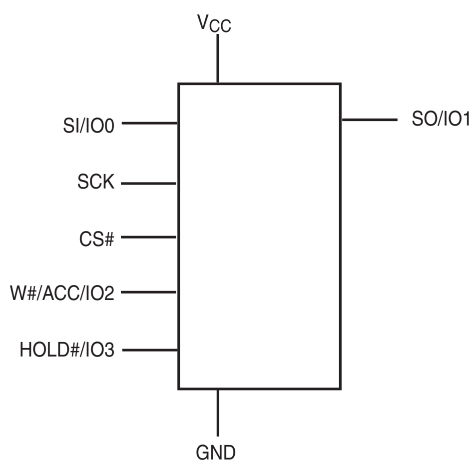
Figure 2.4 6 x 8 mm 24-ball BGA Package, 6 x 4 Pin Configuration



3. Input/Output Descriptions

Signal	I/O	Description
SO/IO1	I/O	**Serial Data Output**: Transfers data serially out of the device on the falling edge of SCK. Functions as an I/O pin in Dual and Quad I/O, and Quad Page Program modes.
SI/IO0	I/O	**Serial Data Input**: Transfers data serially into the device. Device latches commands, addresses, and program data on SI on the rising edge of SCK. Functions as an I/O pin in Dual and Quad I/O mode.
SCK	Input	**Serial Clock**: Provides serial interface timing. Latches commands, addresses, and data on SI on rising edge of SCK. Triggers output on SO after the falling edge of SCK.
CS#	Input	**Chip Select**: Places device in active power mode when driven low. Deselects device and places SO at high impedance when high. After power-up, device requires a falling edge on CS# before any command is written. Device is in standby mode when a program, erase, or Write Status Register operation is not in progress.
HOLD#/IO3	I/O	**Hold**: Pauses any serial communication with the device without deselecting it. When driven low, SO is at high impedance, and all input at SI and SCK are ignored. Requires that CS# also be driven low. Functions as an I/O pin in Quad I/O mode.
W#/ACC/IO2	I/O	**Write Protect**: Protects the memory area specified by Status Register bits BP2:BP0. When driven low, prevents any program or erase command from altering the data in the protected memory area. Functions as an I/O pin in Quad I/O mode.
V_{CC}	Input	**Supply Voltage**
GND	Input	**Ground**

4. Logic Symbol



5. Ordering Information

This product is not recommended for new and current designs. For new and current designs, S25FL128S supersedes S25FL129P. This is the factory-recommended migration path. Please refer to the S25FL128S data sheet for specifications and ordering information.

The ordering part number is formed by a valid combination of the following:

S25FL 129 P 0X M F I 00 1

Packing Type (Note 1)
0 = Tray
1 = Tube
3 = 13” Tape and Reel

Model Number (Additional Ordering Options)
31 = 6x4 pin configuration BGA package, Uniform 256 KB sectors
30 = 6x4 pin configuration BGA package, Uniform 64 KB sectors
21 = 5x5 pin configuration BGA package, Uniform 256 KB sectors
20 = 5x5 pin configuration BGA package, Uniform 64 KB sectors
01 = SO/WSON package, Uniform 256 KB sectors
00 = SO/WSON package, Uniform 64 KB sectors

Temperature Range
I = Industrial (–40°C to + 85°C)
V = Automotive In-Cabin (-40*C to + 105*C)

Package Materials
F = Lead (Pb)-free
H = Low-Halogen, Lead (Pb)-free

Package Type
M = 16-pin SO package
N = 8-contact WSON package
B = 24-ball BGA 6 x 8 mm package, 1.00 mm pitch

Speed
0X = 104 MHz

Device Technology
P = 0.09 µm MirrorBit® Process Technology

Density
129= 128 Mbit

Device Family
S25FL
Cypress Memory 3.0 Volt-only, Serial Peripheral Interface (SPI) Flash Memory

5.1 Valid Combinations

Table 5.1 lists the valid combinations configurations planned to be supported in volume for this device.

Table 5.1 S25FL129P Valid Combinations Table

S25FL129P Valid Combinations					
Base Ordering Part Number	**Speed Option**	**Package and Temperature**	**Model Number**	**Packing Type**	**Package Marking**
S25FL129P	0X	MFI, NFI	00	0, 1, 3	FL129P + (Temp) + F
		MFV , NFV	01		FL129P + (Temp) + FL
		BHI	20, 30	0, 3	FL129P + (Temp) + F
		BHV	21, 31		FL129P + (Temp) + FL

Note

1. Package Marking omits the leading “S25” and speed, package and model number.

6. SPI Modes

A microcontroller can use either of its two SPI modes to control Cypress SPI Flash memory devices:

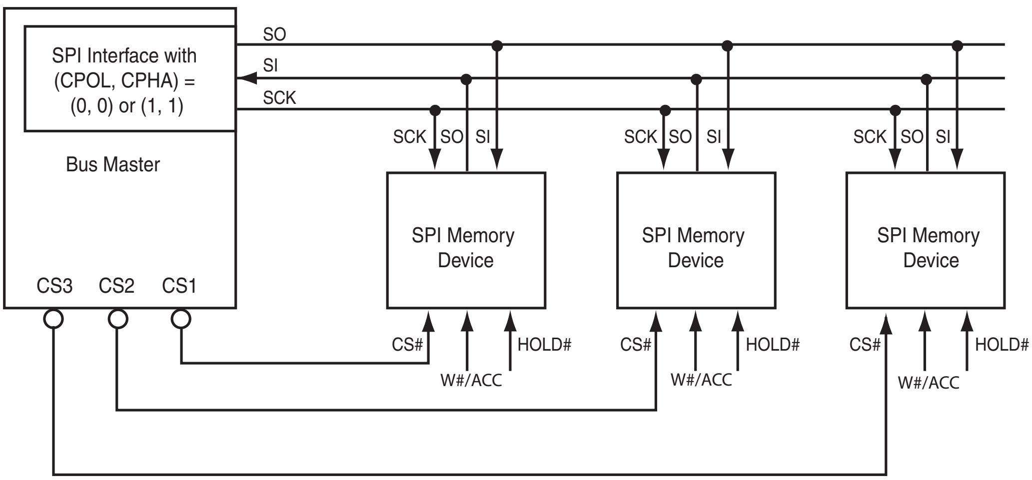
- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

When the bus master is in standby mode, SCK is as shown in Figure 6.2 for each of the two modes:

- SCK remains at 0 for (CPOL = 0, CPHA = 0 Mode 0)
- SCK remains at 1 for (CPOL = 1, CPHA = 1 Mode 3)

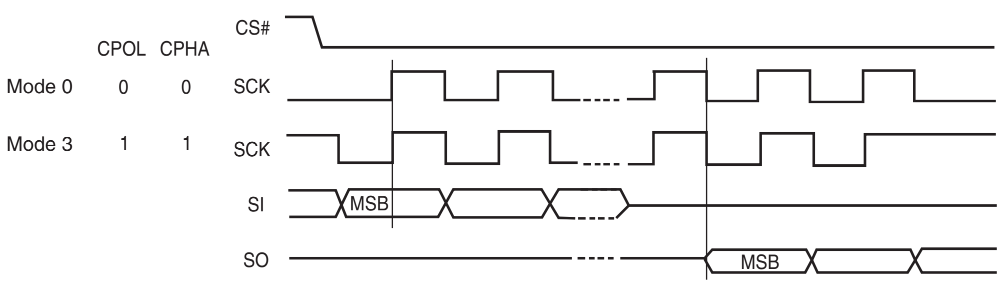
Figure 6.1 Bus Master and Memory Devices on the SPI Bus



Note

The Write Protect/Accelerated Programming (W#/ACC) and Hold (HOLD#) signals should be driven high (logic level 1) or low (logic level 0) as appropriate.

Figure 6.2 SPI Modes Supported



7. Device Operations

All Cypress SPI devices accept and output data in bytes (8 bits at a time). The SPI device is a slave device that supports an inactive clock while CS# is held low.

7.1 Byte or Page Programming

Programming data requires two commands: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. The Page Program sequence accepts from 1 byte up to 256 consecutive bytes of data (which is the size of one page) to be programmed in one operation. Programming means that bits can either be left at 0, or programmed from 1 to 0. Changing bits from 0 to 1 requires an erase operation.

7.2 Quad Page Programming

The Quad Page Program (QPP) instruction allows up to 256 bytes of data to be programmed using 4 pins as inputs at the same time, thus effectively quadrupling the data transfer rate, compared to the Page Program (PP) instruction. The Write Enable Latch (WEL) bit must be set to a 1 using the Write Enable (WREN) command prior to issuing the QPP command.

7.3 Dual and Quad I/O Mode

The S25FL129P device supports Dual and Quad I/O operation when using the Dual/Quad Output Read Mode and the Dual/Quad I/O High Performance Mode instructions. Using the Dual or Quad I/O instructions allows data to be transferred to or from the device at two to four times the rate of standard SPI devices. When operating in the Dual or Quad I/O High Performance Mode (BBh or EBh instructions), data can be read at fast speed using two or four data bits at a time, and the 3-byte address can be input two or four address bits at a time.

7.4 Sector Erase / Bulk Erase

The Sector Erase (SE) and Bulk Erase (BE) commands set all the bits in a sector or the entire memory array to 1. While bits can be individually programmed from 1 to 0, erasing bits from 0 to 1 must be done on a sector-wide (SE) or array-wide (BE) level. In addition to the 64-KB Sector Erase (SE), the S25FL129P device also offers 4-KB Parameter Sector Erase (P4E) and 8-KB Parameter Sector Erase (P8E) (only applicable for the uniform 64 KB sector device).

7.5 Monitoring Write Operations Using the Status Register

The host system can determine when a Write Register, program, or erase operation is complete by monitoring the Write in Progress (WIP) bit in the Status Register. The Read from Status Register command provides the state of the WIP bit. In addition, the S25FL129P device offers two additional bits in the Status Register (P_ERR, E_ERR) to indicate whether a Program or Erase operation was a success or failure.

7.6 Active Power and Standby Power Modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is Low. When CS# is high, the device is disabled, but may still be in the Active Power mode until all program, erase, and Write Registers operations have completed. The device then goes into the Standby Power mode, and power consumption drops to I_{SB}. The Deep Power-Down (DP) command provides additional data protection against inadvertent signals. After writing the DP command, the device ignores any further program or erase commands, and reduces its power consumption to I_{DP}.

7.7 Status Register

The Status Register contains the status and control bits that can be read or set by specific commands (see Table 9.1 on page 21). These bits configure different protection configurations and supply information of operation of the device. (for details see Table 9.8, *S25FL129P Status Register* on page 35):

- **Write In Progress (WIP):** Indicates whether the device is performing a Write Registers, program or erase operation.
- **Write Enable Latch (WEL):** Indicates the status of the internal Write Enable Latch.
- **Block Protect (BP2, BP1, BP0):** Non-volatile bits that define memory area to be software-protected against program and erase commands.
- **Erase Error (E_ERR):** The Erase Error Bit is used as an Erase operation success and failure check.
- **Program Error (P_ERR):** The Program Error Bit is used as an program operation success and failure check.
- **Status Register Write Disable (SRWD):** Places the device in the Hardware Protected mode when this bit is set to 1 and the W#/ACC input is driven low. In this mode, the non-volatile bits of the Status Register (SRWD, BP2, BP1, BP0) become read-only bits.

7.8 Configuration Register

The Configuration Register contains the control bits that can be read or set by specific commands. These bits configure different configurations and security features of the device.

- The FREEZE bit locks the BP2-0 bits in Status Register and the TBPROT and TBPARM bits in the Configuration Register. Note that once the FREEZE bit has been set to ‘1’, then it cannot be cleared to ‘0’ until a power-on-reset is executed. As long as the FREEZE bit is set to ‘0’, then the other bits of the Configuration Register, including FREEZE bit, can be written to.
- The QUAD bit is non-volatile and sets the pin out of the device to Quad mode; that is, W#/ACC becomes IO2 and HOLD# becomes IO3. The instructions for Serial, Dual Output, and Dual I/O reads function as normal. The W#/ACC and HOLD# functionality does not work when the device is set in Quad mode.
- The TBPARM bit defines the logical location of the 4 KB parameter sectors. The parameter sectors consist of thirty two 4 KB sectors. All sectors other than the parameter sectors are defined to be 64-KB uniform in size. When TBPARM is set to a ‘1’, the 4 KB parameter sectors starts at the top of the array. When TBPARM is set to a ‘0’, the 4 KB parameter sectors starts at the bottom of the array. Note that once this bit is set to a '1', it cannot be changed back to '0'. (This function is not applicable to the uniform 256 KB sector product.) The desired state of TBPARM must be selected during the initial configuration of the device during system manufacture; before the first program or erase operation on the main Flash array. TBPARM must not be programmed after programming or erasing is done in the main Flash array.
- The BPNV bit defines whether or not the BP2-0 bits in the Status Register are volatile or non-volatile. When BPNV is set to a ‘1’, the BP2-0 bits in the Status Register are volatile and will be reset to binary 111 after power on reset. When BPNV is set to a ‘0’, the BP2-0 bits in the Status Register are non-volatile. Note that once this bit is set to a '1', it cannot be changed back to '0'.
- The TBPROT bit defines the operation of the block protection bits BP2, BP1, and BP0 in the Status Register. When TBPROT is set to a ‘0’, then the block protection is defined to start from the top of the array. When TBPROT is set to a ‘1’, then the block protection is defined to start from the bottom of the array. Note that once this bit is set to a '1', it cannot be changed back to '0'. The desired state of TBPROT must be selected during the initial configuration of the device during system manufacture; before the first program or erase operation on the main Flash array. TBPROT must not be programmed after programming or erasing is done in the main Flash array.

Note: It is suggested that the Block Protection and Parameter sectors not be set to the same area of the array; otherwise, the user cannot utilize the Parameter sectors if they are protected. The following matrix shows the recommended settings.

TBPARM	TBPROT	Array Overview
0	0	Parameter Sectors - Bottom BP Protection - Top (default)
0	1	Not recommended (Parameters and BP Protection are both Bottom)
1	0	Not recommended (parameters and BP Protection are both Top)
1	1	Parameter Sectors - Top of Array (high address) BP Protection - Bottom of Array (low address)

Table 7.1 Configuration Register Table (Uniform 64 KB sector)

Bit	Bit Name	Bit Function	Description
7	NA	-	Not Used
6	NA	-	Not Used
5	TBPROT	Configures start of block protection	1 = Bottom Array (low address) 0 = Top Array (high address) (Default)
4	NA	-	Do Not Use
3	BPNV	Configures BP2-0 bits in the Status Register	1 = Volatile 0 = Non-volatile (Default)
2	TBPARM	Configures Parameter sector location	1 = Top Array (high address) 0 = Bottom Array (low address) (Default)
1	QUAD	Puts the device into Quad I/O mode	1 = Quad I/O 0 = Dual or Serial I/O (Default)
0	FREEZE	Locks BP2-0 bits in the Status Register	1 = Enabled 0 = Disabled (Default)

Note
(Default) indicates the value of each Configuration Register bit set upon initial factory shipment.

Table 7.2 Configuration Register Table (Uniform 256 KB sector)

Bit	Bit Name	Bit Function	Description
7	N/A	-	Not Used
6	N/A	-	Not Used
5	TBPROT	Configures start of block protection	1 = Bottom Array (low address) 0 = Top Array (high address) (Default)
4	N/A	-	Do Not Use
3	BPNV	Configures BP2-0 bits in the Status Register	1 = Volatile 0 = Non-volatile (Default)
2	N/A	-	Do not Use
1	QUAD	Puts the device into Quad I/O mode	1 = Quad I/O 0 = Dual or Serial I/O (Default)
0	FREEZE	Locks BP2-0 bits in the Status Register	1 = Enabled 0 = Disabled (Default)

Note
1. *(Default) indicates the value of each Configuration Register bit set upon initial factory shipment.*

7.9 Data Protection Modes

Cypress SPI Flash memory devices provide the following data protection methods:

- **The Write Enable (WREN) command:** Must be written prior to any command that modifies data. The WREN command sets the Write Enable Latch (WEL) bit. The WEL bit resets (disables writes) on power-up or after the device completes the following commands:
  - Page Program (PP)
  - Sector Erase (SE)
  - Bulk Erase (BE)
  - Write Disable (WRDI)
  - Write Register (WRR)
  - Parameter 4 KB Sector Erase (P4E)
  - Parameter 8 KB Sector Erase (P8E)
  - Quad Page Programming (QPP)
  - OTP Byte Programming (OTPP)
- **Software Protected Mode (SPM):** The Block Protect BP2, BP1, BP0 bits define the section of the memory array that can be read but not programmed or erased. Table 7.3 and Table 7.4 shows the sizes and address ranges of protected areas that are defined by Status Register bits BP2:BP0.
- **Hardware Protected Mode (HPM):** The Write Protect (W#/ACC) input and the Status Register Write Disable (SRWD) bit together provide write protection.
- **Clock Pulse Count:** The device verifies that all program, erase, and Write Register commands consist of a clock pulse count that is a multiple of eight before executing them.

Table 7.3 TBPROT = 0 (Starts Protection from TOP of Array)

Status Register Block			Memory Array						
				Protected Sectors			Unprotected Sectors		
BP2	BP1	BP0	Protected Address Range	Uniform 64 KB	Uniform 256 KB	Unprotected Address Range	Uniform 64 KB	Uniform 256 KB	Protected Portion of Total Memory Area
0	0	0	None	0	0	000000h - FFFFFFh	SA255:SA0	SA63:SA0	0
0	0	1	FC0000h - FFFFFFh	(4) SA255:SA252	(1) SA63	000000h - FBFFFFh	SA251:SA0	SA62:SA0	1/64
0	1	0	F80000h - FFFFFFh	(8) SA255:SA248	(2)SA63:SA62	000000h - F7FFFFh	SA247:SA0	SA61:SA0	1/32
0	1	1	F00000h - FFFFFFh	(16) SA255:SA240	(4)SA63:SA60	000000h - EFFFFFh	SA239:SA0	SA59:SA0	1/16
1	0	0	E00000h - FFFFFFh	(32) SA255:SA224	(8)SA63:SA56	000000h - DFFFFFh	SA223:SA0	SA55:SA0	1/8
1	0	1	C00000h - FFFFFFh	(64)SA255:SA192	(16)SA63:SA48	000000h - BFFFFFh	SA191:SA0	SA47:SA0	1/4
1	1	0	800000h - FFFFFFh	(128)SA255:SA128	(32)SA63:SA32	000000h - 7FFFFFh	SA127:SA0	SA31:SA0	1/2
1	1	1	000000h - FFFFFFh	(256)SA255:SA0	(64)SA63:SA0	None	None	None	All

Table 7.4 TBPROT = 1 (Starts Protection from BOTTOM of Array)

Status Register Block			Memory Array						
				Protected Sectors			Unprotected Sectors		
BP2	BP1	BP0	Protected Address Range	Uniform 64 KB	Uniform 256 KB	Unprotected Address Range	Uniform 64 KB	Uniform 256 KB	Protected Portion of Total Memory Area
0	0	0	None	0	0	000000h - FFFFFFh	SA0:SA255	SA0:SA63	0
0	0	1	000000h - 03FFFFh	(4) SA0:SA3	(1) SA0	040000h - FFFFFFh	SA4:SA255	SA1:SA63	1/64
0	1	0	000000h - 07FFFFh	(8) SA0:SA7	(2)SA0:SA1	080000h - FFFFFFh	SA8:SA255	SA2:SA63	1/32
0	1	1	000000h - 0FFFFFh	(16)SA0:SA15	(4)SA0:SA3	100000h - FFFFFFh	SA16:SA255	SA4:SA63	1/16
1	0	0	000000h - 1FFFFFh	(32)SA0:SA31	(8)SA0:SA7	200000h - FFFFFFh	SA32:SA255	SA8:SA63	1/8

Table 7.4 TBPROT = 1 (Starts Protection from BOTTOM of Array)

Status Register Block			Memory Array						
				Protected Sectors			Unprotected Sectors		
BP2	BP1	BP0	Protected Address Range	Uniform 64 KB	Uniform 256 KB	Unprotected Address Range	Uniform 64 KB	Uniform 256 KB	Protected Portion of Total Memory Area
1	0	1	000000h - 3FFFFFh	(64)SA0:SA63	(16)SA0:SA15	400000h - FFFFFFh	SA64:SA255	SA16:SA63	1/4
1	1	0	000000h - 7FFFFFh	(128)SA0:SA127	(32)SA0:SA31	800000h - FFFFFFh	SA128:255	SA32:SA63	1/2
1	1	1	000000h - FFFFFFh	(256)SA0:SA255	(64)SA0:SA63	None	None	None	All

7.10 Hold Mode (HOLD#)

The Hold input (HOLD#) stops any serial communication with the device, but does not terminate any Write Registers, program or erase operation that is currently in progress.

The Hold mode starts on the falling edge of HOLD# if SCK is also low (see Figure 7.1, standard use). If the falling edge of HOLD# does not occur while SCK is low, the Hold mode begins after the next falling edge of SCK (non-standard use).

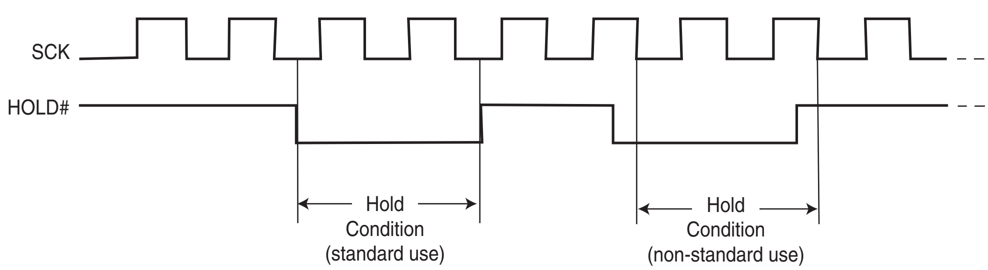
The Hold mode ends on the rising edge of HOLD# signal (standard use) if SCK is also low. If the rising edge of HOLD# does not occur while SCK is low, the Hold mode ends on the next falling edge of CLK (non-standard use) See Figure 7.1.

The SO output is high impedance, and the SI and SCK inputs are ignored (don't care) for the duration of the Hold mode.

CS# must remain low for the entire duration of the Hold mode to ensure that the device internal logic remains unchanged. If CS# goes high while the device is in the Hold mode, the internal logic is reset. To prevent the device from reverting to the Hold mode when device communication is resumed, HOLD# must be held high, followed by driving CS# low.

Note: The HOLD Mode feature is disabled during Quad I/O Mode.

Figure 7.1 Hold Mode Operation



7.11 Accelerated Programming Operation

The device offers accelerated program operations through the ACC function. This function is primarily intended to allow faster manufacturing throughput at the factory. If the system asserts V_{HH} on this pin, the device uses the higher voltage on the pin to reduce the time required for program operations. Removing V_{HH} from the W#/ACC pin returns the device to normal operation. Note that the W#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, the W#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

Note: The ACC function is disabled during Quad I/O Mode.

8. Sector Address Table

The Sector Address tables show the size of the memory array, sectors, and pages. The device uses pages to cache the program data before the data is programmed into the memory array. Each page or byte can be individually programmed (bits are changed from 1 to 0). The data is erased (bits are changed from 0 to 1) on a sub-sector, sector- or device-wide basis using the P4E/P8E (applicable only for the uniform 64 KB sector device), SE or BE commands. Table 8.1 to Table 8.3 show the starting and ending address for each sector. The complete set of sectors comprises the memory array of the Flash device.

Table 8.1 S25FL129P Sector Address Table (Uniform 256 KB sector)

Sector	Address Range		Sector	Address Range	
	Start Address	End Address		Start Address	End Address
63	FC0000h	FFFFFFh	31	7C0000h	7FFFFFh
62	F80000h	FBFFFFh	30	780000h	7BFFFFh
61	F40000h	F7FFFFh	29	740000h	77FFFFh
60	F00000h	F3FFFFh	28	700000h	73FFFFh
59	EC0000h	EFFFFFh	27	6C0000h	6FFFFFh
58	E80000h	EBFFFFh	26	680000h	6BFFFFh
57	E40000h	E7FFFFh	25	640000h	67FFFFh
56	E00000h	E3FFFFh	24	600000h	63FFFFh
55	DC0000h	DFFFFFh	23	5C0000h	5FFFFFh
54	D80000h	DBFFFFh	22	580000h	5BFFFFh
53	D40000h	D7FFFFh	21	540000h	57FFFFh
52	D00000h	D3FFFFh	20	500000h	53FFFFh
51	CC0000h	CFFFFFh	19	4C0000h	4FFFFFh
50	C80000h	CBFFFFh	18	480000h	4BFFFFh
49	C40000h	C7FFFFh	17	440000h	47FFFFh
48	C00000h	C3FFFFh	16	400000h	43FFFFh
47	BC0000h	BFFFFFh	15	3C0000h	3FFFFFh
46	B80000h	BBFFFFh	14	380000h	3BFFFFh
45	B40000h	B7FFFFh	13	340000h	37FFFFh
44	B00000h	B3FFFFh	12	300000h	33FFFFh
43	AC0000h	AFFFFFh	11	2C0000h	2FFFFFh
42	A80000h	ABFFFFh	10	280000h	2BFFFFh
41	A40000h	A7FFFFh	9	240000h	27FFFFh
40	A00000h	A3FFFFh	8	200000h	23FFFFh
39	9C0000h	9FFFFFh	7	1C0000h	1FFFFFh
38	980000h	9BFFFFh	6	180000h	1BFFFFh
37	940000h	97FFFFh	5	140000h	17FFFFh
36	900000h	93FFFFh	4	100000h	13FFFFh
35	8C0000h	8FFFFFh	3	0C0000h	0FFFFFh
34	880000h	8BFFFFh	2	080000h	0BFFFFh
33	840000h	87FFFFh	1	040000h	07FFFFh
32	800000h	83FFFFh	0	000000h	03FFFFh

Table 8.2 S25FL129P Sector Address Table (Uniform 64 KB sector, TBPARM=0) (Sheet 1 of 2)

Sector	Address Range		Sector	Address Range		Sector	Address Range	
	Start Address	End Address		Start Address	End Address		Start Address	End Address
SA108	6C0000h	6CFFFFh	SA61	3D0000h	3DFFFFh	SA14	0E0000h	0EFFFFh
SA107	6B0000h	6BFFFFh	SA60	3C0000h	3CFFFFh	SA13	0D0000h	0DFFFFh
SA106	6A0000h	6AFFFFh	SA59	3B0000h	3BFFFFh	SA12	0C0000h	0CFFFFh
SA105	690000h	69FFFFh	SA58	3A0000h	3AFFFFh	SA11	0B0000h	0BFFFFh
SA104	680000h	68FFFFh	SA57	390000h	39FFFFh	SA10	0A0000h	0AFFFFh
SA103	670000h	67FFFFh	SA56	380000h	38FFFFh	SA9	090000h	09FFFFh
SA102	660000h	66FFFFh	SA55	370000h	37FFFFh	SA8	080000h	08FFFFh
SA101	650000h	65FFFFh	SA54	360000h	36FFFFh	SA7	070000h	07FFFFh
SA100	640000h	64FFFFh	SA53	350000h	35FFFFh	SA6	060000h	06FFFFh
SA99	630000h	63FFFFh	SA52	340000h	34FFFFh	SA5	050000h	05FFFFh
SA98	620000h	62FFFFh	SA51	330000h	33FFFFh	SA4	040000h	04FFFFh
SA97	610000h	61FFFFh	SA50	320000h	32FFFFh	SA3	030000h	03FFFFh
SA96	600000h	60FFFFh	SA49	310000h	31FFFFh	SA2	020000h	02FFFFh
SA95	5F0000h	5FFFFFh	SA48	300000h	30FFFFh	SA1	010000h	01FFFFh
SA94	5E0000h	5EFFFFh	SA47	2F0000h	2FFFFFh	SA0	000000h	00FFFFh
SA93	5D0000h	5DFFFFh	SA46	2E0000h	2EFFFFh	SS31	01F000h	01FFFFh
SA92	5C0000h	5CFFFFh	SA45	2D0000h	2DFFFFh	SS30	01E000h	01EFFFh
SA91	5B0000h	5BFFFFh	SA44	2C0000h	2CFFFFh	SS29	01D000h	01DFFFh
SA90	5A0000h	5AFFFFh	SA43	2B0000h	2BFFFFh	SS28	01C000h	01CFFFh
SA89	590000h	59FFFFh	SA42	2A0000h	2AFFFFh	SS27	01B000h	01BFFFh
SA88	580000h	58FFFFh	SA41	290000h	29FFFFh	SS26	01A000h	01AFFFh
SA87	570000h	57FFFFh	SA40	280000h	28FFFFh	SS25	019000h	019FFFh
SA86	560000h	56FFFFh	SA39	270000h	27FFFFh	SS24	018000h	018FFFh
SA85	550000h	55FFFFh	SA38	260000h	26FFFFh	SS23	017000h	017FFFh
SA84	540000h	54FFFFh	SA37	250000h	25FFFFh	SS22	016000h	016FFFh
SA83	530000h	53FFFFh	SA36	240000h	24FFFFh	SS21	015000h	015FFFh
SA82	520000h	52FFFFh	SA35	230000h	23FFFFh	SS20	014000h	014FFFh
SA81	510000h	51FFFFh	SA34	220000h	22FFFFh	SS19	013000h	013FFFh
SA80	500000h	50FFFFh	SA33	210000h	21FFFFh	SS18	012000h	012FFFh
SA79	4F0000h	4FFFFFh	SA32	200000h	20FFFFh	SS17	011000h	011FFFh
SA78	4E0000h	4EFFFFh	SA31	1F0000h	1FFFFFh	SS16	010000h	010FFFh
SA77	4D0000h	4DFFFFh	SA30	1E0000h	1EFFFFh	SS15	00F000h	00FFFFh
SA76	4C0000h	4CFFFFh	SA29	1D0000h	1DFFFFh	SS14	00E000h	00EFFFh
SA75	4B0000h	4BFFFFh	SA28	1C0000h	1CFFFFh	SS13	00D000h	00DFFFh
SA74	4A0000h	4AFFFFh	SA27	1B0000h	1BFFFFh	SS12	00C000h	00CFFFh
SA73	490000h	49FFFFh	SA26	1A0000h	1AFFFFh	SS11	00B000h	00BFFFh
SA72	480000h	48FFFFh	SA25	190000h	19FFFFh	SS10	00A000h	00AFFFh
SA71	470000h	47FFFFh	SA24	180000h	18FFFFh	SS9	009000h	009FFFh
SA70	460000h	46FFFFh	SA23	170000h	17FFFFh	SS8	008000h	008FFFh
SA69	450000h	45FFFFh	SA22	160000h	16FFFFh	SS7	007000h	007FFFh
SA68	440000h	44FFFFh	SA21	150000h	15FFFFh	SS6	006000h	006FFFh
SA67	430000h	43FFFFh	SA20	140000h	14FFFFh	SS5	005000h	005FFFh
SA66	420000h	42FFFFh	SA19	130000h	13FFFFh	SS4	004000h	004FFFh
SA65	410000h	41FFFFh	SA18	120000h	12FFFFh	SS3	003000h	003FFFh
SA64	400000h	40FFFFh	SA17	110000h	11FFFFh	SS2	002000h	002FFFh
SA63	3F0000h	3FFFFFh	SA16	100000h	10FFFFh	SS1	001000h	001FFFh
SA62	3E0000h	3EFFFFh	SA15	0F0000h	0FFFFFh	SS0	000000h	000FFFh

Table 8.2 S25FL129P Sector Address Table (Uniform 64 KB sector, TBPARM=0) (Sheet 2 of 2)

Sector	Address Range		Sector	Address Range		Sector	Address Range	
	Start Address	End Address		Start Address	End Address		Start Address	End Address
SA255	FF0000h	FFFFFFh	SA206	CE0000h	CEFFFFh	SA157	9D0000h	9DFFFFh
SA254	FE0000h	FEFFFFh	SA205	CD0000h	CDFFFFh	SA156	9C0000h	9CFFFFh
SA253	FD0000h	FDFFFFh	SA204	CC0000h	CCFFFFh	SA155	9B0000h	9BFFFFh
SA252	FC0000h	FCFFFFh	SA203	CB0000h	CBFFFFh	SA154	9A0000h	9AFFFFh
SA251	FB0000h	FBFFFFh	SA202	CA0000h	CAFFFFh	SA153	990000h	99FFFFh
SA250	FA0000h	FAFFFFh	SA201	C90000h	C9FFFFh	SA152	980000h	98FFFFh
SA249	F90000h	F9FFFFh	SA200	C80000h	C8FFFFh	SA151	970000h	97FFFFh
SA248	F80000h	F8FFFFh	SA199	C70000h	C7FFFFh	SA150	960000h	96FFFFh
SA247	F70000h	F7FFFFh	SA198	C60000h	C6FFFFh	SA149	950000h	95FFFFh
SA246	F60000h	F6FFFFh	SA197	C50000h	C5FFFFh	SA148	940000h	94FFFFh
SA245	F50000h	F5FFFFh	SA196	C40000h	C4FFFFh	SA147	930000h	93FFFFh
SA244	F40000h	F4FFFFh	SA195	C30000h	C3FFFFh	SA146	920000h	92FFFFh
SA243	F30000h	F3FFFFh	SA194	C20000h	C2FFFFh	SA145	910000h	91FFFFh
SA242	F20000h	F2FFFFh	SA193	C10000h	C1FFFFh	SA144	900000h	90FFFFh
SA241	F10000h	F1FFFFh	SA192	C00000h	C0FFFFh	SA143	8F0000h	8FFFFFh
SA240	F00000h	F0FFFFh	SA191	BF0000h	BFFFFFh	SA142	8E0000h	8EFFFFh
SA239	EF0000h	EFFFFFh	SA190	BE0000h	BEFFFFh	SA141	8D0000h	8DFFFFh
SA238	EE0000h	EEFFFFh	SA189	BD0000h	BDFFFFh	SA140	8C0000h	8CFFFFh
SA237	ED0000h	EDFFFFh	SA188	BC0000h	BCFFFFh	SA139	8B0000h	8BFFFFh
SA236	EC0000h	ECFFFFh	SA187	BB0000h	BBFFFFh	SA138	8A0000h	8AFFFFh
SA235	EB0000h	EBFFFFh	SA186	BA0000h	BAFFFFh	SA137	890000h	89FFFFh
SA234	EA0000h	EAFFFFh	SA185	B90000h	B9FFFFh	SA136	880000h	88FFFFh
SA233	E90000h	E9FFFFh	SA184	B80000h	B8FFFFh	SA135	870000h	87FFFFh
SA232	E80000h	E8FFFFh	SA183	B70000h	B7FFFFh	SA134	860000h	86FFFFh
SA231	E70000h	E7FFFFh	SA182	B60000h	B6FFFFh	SA133	850000h	85FFFFh
SA230	E60000h	E6FFFFh	SA181	B50000h	B5FFFFh	SA132	840000h	84FFFFh
SA229	E50000h	E5FFFFh	SA180	B40000h	B4FFFFh	SA131	830000h	83FFFFh
SA228	E40000h	E4FFFFh	SA179	B30000h	B3FFFFh	SA130	820000h	82FFFFh
SA227	E30000h	E3FFFFh	SA178	B20000h	B2FFFFh	SA129	810000h	81FFFFh
SA226	E20000h	E2FFFFh	SA177	B10000h	B1FFFFh	SA128	800000h	80FFFFh
SA225	E10000h	E1FFFFh	SA176	B00000h	B0FFFFh	SA127	7F0000h	7FFFFFh
SA224	E00000h	E0FFFFh	SA175	AF0000h	AFFFFFh	SA126	7E0000h	7EFFFFh
SA223	DF0000h	DFFFFFh	SA174	AE0000h	AEFFFFh	SA125	7D0000h	7DFFFFh
SA222	DE0000h	DEFFFFh	SA173	AD0000h	ADFFFFh	SA124	7C0000h	7CFFFFh
SA221	DD0000h	DDFFFFh	SA172	AC0000h	ACFFFFh	SA123	7B0000h	7BFFFFh
SA220	DC0000h	DCFFFFh	SA171	AB0000h	ABFFFFh	SA122	7A0000h	7AFFFFh
SA219	DB0000h	DBFFFFh	SA170	AA0000h	AAFFFFh	SA121	790000h	79FFFFh
SA218	DA0000h	DAFFFFh	SA169	A90000h	A9FFFFh	SA120	780000h	78FFFFh
SA217	D90000h	D9FFFFh	SA168	A80000h	A8FFFFh	SA119	770000h	77FFFFh
SA216	D80000h	D8FFFFh	SA167	A70000h	A7FFFFh	SA118	760000h	76FFFFh
SA215	D70000h	D7FFFFh	SA166	A60000h	A6FFFFh	SA117	750000h	75FFFFh
SA214	D60000h	D6FFFFh	SA165	A50000h	A5FFFFh	SA116	740000h	74FFFFh
SA213	D50000h	D5FFFFh	SA164	A40000h	A4FFFFh	SA115	730000h	73FFFFh
SA212	D40000h	D4FFFFh	SA163	A30000h	A3FFFFh	SA114	720000h	72FFFFh
SA211	D30000h	D3FFFFh	SA162	A20000h	A2FFFFh	SA113	710000h	71FFFFh
SA210	D20000h	D2FFFFh	SA161	A10000h	A1FFFFh	SA112	700000h	70FFFFh
SA209	D10000h	D1FFFFh	SA160	A00000h	A0FFFFh	SA111	6F0000h	6FFFFFh
SA208	D00000h	D0FFFFh	SA159	9F0000h	9FFFFFh	SA110	6E0000h	6EFFFFh
SA207	CF0000h	CFFFFFh	SA158	9E0000h	9EFFFFh	SA109	6D0000h	6DFFFFh

Note
Sector SA0 is split up into sub-sectors SS0 - SS15 (dark gray shading)
Sector SA1 is split up into sub-sectors SS16 - SS31(light gray shading)

Table 8.3 S25FL129P Sector Address Table (Uniform 64 KB sector, TBPARM=1) (Sheet 1 of 2)

Sector	Address Range		Sector	Address Range		Sector	Address Range	
	Start Address	End Address		Start Address	End Address		Start Address	End Address
SS31	FFF000h	FFFFFFh	SA239	EF0000h	EFFFFFh	SA191	BF0000h	BFFFFFh
SS30	FFE000h	FFEFFFh	SA238	EE0000h	EEFFFFh	SA190	BE0000h	BEFFFFh
SS29	FFD000h	FFDFFFh	SA237	ED0000h	EDFFFFh	SA189	BD0000h	BDFFFFh
SS28	FFC000h	FFCFFFh	SA236	EC0000h	ECFFFFh	SA188	BC0000h	BCFFFFh
SS27	FFB000h	FFBFFFh	SA235	EB0000h	EBFFFFh	SA187	BB0000h	BBFFFFh
SS26	FFA000h	FFAFFFh	SA234	EA0000h	EAFFFFh	SA186	BA0000h	BAFFFFh
SS25	FF9000h	FF9FFFh	SA233	E90000h	E9FFFFh	SA185	B90000h	B9FFFFh
SS24	FF8000h	FF8FFFh	SA232	E80000h	E8FFFFh	SA184	B80000h	B8FFFFh
SS23	FF7000h	FF7FFFh	SA231	E70000h	E7FFFFh	SA183	B70000h	B7FFFFh
SS22	FF6000h	FF6FFFh	SA230	E60000h	E6FFFFh	SA182	B60000h	B6FFFFh
SS21	FF5000h	FF5FFFh	SA229	E50000h	E5FFFFh	SA181	B50000h	B5FFFFh
SS20	FF4000h	FF4FFFh	SA228	E40000h	E4FFFFh	SA180	B40000h	B4FFFFh
SS19	FF3000h	FF3FFFh	SA227	E30000h	E3FFFFh	SA179	B30000h	B3FFFFh
SS18	FF2000h	FF2FFFh	SA226	E20000h	E2FFFFh	SA178	B20000h	B2FFFFh
SS17	FF1000h	FF1FFFh	SA225	E10000h	E1FFFFh	SA177	B10000h	B1FFFFh
SS16	FF0000h	FF0FFFh	SA224	E00000h	E0FFFFh	SA176	B00000h	B0FFFFh
SS15	FEF000h	FEFFFFh	SA223	DF0000h	DFFFFFh	SA175	AF0000h	AFFFFFh
SS14	FEE000h	FEEFFFh	SA222	DE0000h	DEFFFFh	SA174	AE0000h	AEFFFFh
SS13	FED000h	FEDFFFh	SA221	DD0000h	DDFFFFh	SA173	AD0000h	ADFFFFh
SS12	FEC000h	FECFFFh	SA220	DC0000h	DCFFFFh	SA172	AC0000h	ACFFFFh
SS11	FEB000h	FEBFFFh	SA219	DB0000h	DBFFFFh	SA171	AB0000h	ABFFFFh
SS10	FEA000h	FEAFFFh	SA218	DA0000h	DAFFFFh	SA170	AA0000h	AAFFFFh
SS9	FE9000h	FE9FFFh	SA217	D90000h	D9FFFFh	SA169	A90000h	A9FFFFh
SS8	FE8000h	FE8FFFh	SA216	D80000h	D8FFFFh	SA168	A80000h	A8FFFFh
SS7	FE7000h	FE7FFFh	SA215	D70000h	D7FFFFh	SA167	A70000h	A7FFFFh
SS6	FE6000h	FE6FFFh	SA214	D60000h	D6FFFFh	SA166	A60000h	A6FFFFh
SS5	FE5000h	FE5FFFh	SA213	D50000h	D5FFFFh	SA165	A50000h	A5FFFFh
SS4	FE4000h	FE4FFFh	SA212	D40000h	D4FFFFh	SA164	A40000h	A4FFFFh
SS3	FE3000h	FE3FFFh	SA211	D30000h	D3FFFFh	SA163	A30000h	A3FFFFh
SS2	FE2000h	FE2FFFh	SA210	D20000h	D2FFFFh	SA162	A20000h	A2FFFFh
SS1	FE1000h	FE1FFFh	SA209	D10000h	D1FFFFh	SA161	A10000h	A1FFFFh
SS0	FE0000h	FE0FFFh	SA208	D00000h	D0FFFFh	SA160	A00000h	A0FFFFh
SA255	FF0000h	FFFFFFh	SA207	CF0000h	CFFFFFh	SA159	9F0000h	9FFFFFh
SA254	FE0000h	FEFFFFh	SA206	CE0000h	CEFFFFh	SA158	9E0000h	9EFFFFh
SA253	FD0000h	FDFFFFh	SA205	CD0000h	CDFFFFh	SA157	9D0000h	9DFFFFh
SA252	FC0000h	FCFFFFh	SA204	CC0000h	CCFFFFh	SA156	9C0000h	9CFFFFh
SA251	FB0000h	FBFFFFh	SA203	CB0000h	CBFFFFh	SA155	9B0000h	9BFFFFh
SA250	FA0000h	FAFFFFh	SA202	CA0000h	CAFFFFh	SA154	9A0000h	9AFFFFh
SA249	F90000h	F9FFFFh	SA201	C90000h	C9FFFFh	SA153	990000h	99FFFFh
SA248	F80000h	F8FFFFh	SA200	C80000h	C8FFFFh	SA152	980000h	98FFFFh
SA247	F70000h	F7FFFFh	SA199	C70000h	C7FFFFh	SA151	970000h	97FFFFh
SA246	F60000h	F6FFFFh	SA198	C60000h	C6FFFFh	SA150	960000h	96FFFFh
SA245	F50000h	F5FFFFh	SA197	C50000h	C5FFFFh	SA149	950000h	95FFFFh
SA244	F40000h	F4FFFFh	SA196	C40000h	C4FFFFh	SA148	940000h	94FFFFh
SA243	F30000h	F3FFFFh	SA195	C30000h	C3FFFFh	SA147	930000h	93FFFFh
SA242	F20000h	F2FFFFh	SA194	C20000h	C2FFFFh	SA146	920000h	92FFFFh
SA241	F10000h	F1FFFFh	SA193	C10000h	C1FFFFh	SA145	910000h	91FFFFh
SA240	F00000h	F0FFFFh	SA192	C00000h	C0FFFFh	SA144	900000h	90FFFFh

Table 8.3 S25FL129P Sector Address Table (Uniform 64 KB sector, TBPARM=1) (Sheet 2 of 2)

Sector	Address Range		Sector	Address Range		Sector	Address Range	
	Start Address	End Address		Start Address	End Address		Start Address	End Address
SA143	8F0000h	8FFFFFh	SA95	5F0000h	5FFFFFh	SA47	2F0000h	2FFFFFh
SA142	8E0000h	8EFFFFh	SA94	5E0000h	5EFFFFh	SA46	2E0000h	2EFFFFh
SA141	8D0000h	8DFFFFh	SA93	5D0000h	5DFFFFh	SA45	2D0000h	2DFFFFh
SA140	8C0000h	8CFFFFh	SA92	5C0000h	5CFFFFh	SA44	2C0000h	2CFFFFh
SA139	8B0000h	8BFFFFh	SA91	5B0000h	5BFFFFh	SA43	2B0000h	2BFFFFh
SA138	8A0000h	8AFFFFh	SA90	5A0000h	5AFFFFh	SA42	2A0000h	2AFFFFh
SA137	890000h	89FFFFh	SA89	590000h	59FFFFh	SA41	290000h	29FFFFh
SA136	880000h	88FFFFh	SA88	580000h	58FFFFh	SA40	280000h	28FFFFh
SA135	870000h	87FFFFh	SA87	570000h	57FFFFh	SA39	270000h	27FFFFh
SA134	860000h	86FFFFh	SA86	560000h	56FFFFh	SA38	260000h	26FFFFh
SA133	850000h	85FFFFh	SA85	550000h	55FFFFh	SA37	250000h	25FFFFh
SA132	840000h	84FFFFh	SA84	540000h	54FFFFh	SA36	240000h	24FFFFh
SA131	830000h	83FFFFh	SA83	530000h	53FFFFh	SA35	230000h	23FFFFh
SA130	820000h	82FFFFh	SA82	520000h	52FFFFh	SA34	220000h	22FFFFh
SA129	810000h	81FFFFh	SA81	510000h	51FFFFh	SA33	210000h	21FFFFh
SA128	800000h	80FFFFh	SA80	500000h	50FFFFh	SA32	200000h	20FFFFh
SA127	7F0000h	7FFFFFh	SA79	4F0000h	4FFFFFh	SA31	1F0000h	1FFFFFh
SA126	7E0000h	7EFFFFh	SA78	4E0000h	4EFFFFh	SA30	1E0000h	1EFFFFh
SA125	7D0000h	7DFFFFh	SA77	4D0000h	4DFFFFh	SA29	1D0000h	1DFFFFh
SA124	7C0000h	7CFFFFh	SA76	4C0000h	4CFFFFh	SA28	1C0000h	1CFFFFh
SA123	7B0000h	7BFFFFh	SA75	4B0000h	4BFFFFh	SA27	1B0000h	1BFFFFh
SA122	7A0000h	7AFFFFh	SA74	4A0000h	4AFFFFh	SA26	1A0000h	1AFFFFh
SA121	790000h	79FFFFh	SA73	490000h	49FFFFh	SA25	190000h	19FFFFh
SA120	780000h	78FFFFh	SA72	480000h	48FFFFh	SA24	180000h	18FFFFh
SA119	770000h	77FFFFh	SA71	470000h	47FFFFh	SA23	170000h	17FFFFh
SA118	760000h	76FFFFh	SA70	460000h	46FFFFh	SA22	160000h	16FFFFh
SA117	750000h	75FFFFh	SA69	450000h	45FFFFh	SA21	150000h	15FFFFh
SA116	740000h	74FFFFh	SA68	440000h	44FFFFh	SA20	140000h	14FFFFh
SA115	730000h	73FFFFh	SA67	430000h	43FFFFh	SA19	130000h	13FFFFh
SA114	720000h	72FFFFh	SA66	420000h	42FFFFh	SA18	120000h	12FFFFh
SA113	710000h	71FFFFh	SA65	410000h	41FFFFh	SA17	110000h	11FFFFh
SA112	700000h	70FFFFh	SA64	400000h	40FFFFh	SA16	100000h	10FFFFh
SA111	6F0000h	6FFFFFh	SA63	3F0000h	3FFFFFh	SA15	0F0000h	0FFFFFh
SA110	6E0000h	6EFFFFh	SA62	3E0000h	3EFFFFh	SA14	0E0000h	0EFFFFh
SA109	6D0000h	6DFFFFh	SA61	3D0000h	3DFFFFh	SA13	0D0000h	0DFFFFh
SA108	6C0000h	6CFFFFh	SA60	3C0000h	3CFFFFh	SA12	0C0000h	0CFFFFh
SA107	6B0000h	6BFFFFh	SA59	3B0000h	3BFFFFh	SA11	0B0000h	0BFFFFh
SA106	6A0000h	6AFFFFh	SA58	3A0000h	3AFFFFh	SA10	0A0000h	0AFFFFh
SA105	690000h	69FFFFh	SA57	390000h	39FFFFh	SA9	090000h	09FFFFh
SA104	680000h	68FFFFh	SA56	380000h	38FFFFh	SA8	080000h	08FFFFh
SA103	670000h	67FFFFh	SA55	370000h	37FFFFh	SA7	070000h	07FFFFh
SA102	660000h	66FFFFh	SA54	360000h	36FFFFh	SA6	060000h	06FFFFh
SA101	650000h	65FFFFh	SA53	350000h	35FFFFh	SA5	050000h	05FFFFh
SA100	640000h	64FFFFh	SA52	340000h	34FFFFh	SA4	040000h	04FFFFh
SA99	630000h	63FFFFh	SA51	330000h	33FFFFh	SA3	030000h	03FFFFh
SA98	620000h	62FFFFh	SA50	320000h	32FFFFh	SA2	020000h	02FFFFh
SA97	610000h	61FFFFh	SA49	310000h	31FFFFh	SA1	010000h	01FFFFh
SA96	600000h	60FFFFh	SA48	300000h	30FFFFh	SA0	000000h	00FFFFh

Note

Sector SA254 is split up into sub-sectors SS0 - SS15 (dark gray shading)
Sector SA255 is split up into sub-sectors SS16 - SS31(light gray shading)

9. Command Definitions

The host system must shift all commands, addresses, and data in and out of the device, beginning with the most significant bit. On the first rising edge of SCK after CS# is driven low, the device accepts the one-byte command on SI (all commands are one byte long), most significant bit first. Each successive bit is latched on the rising edge of SCK. Table 9.1 lists the complete set of commands.

Every command sequence begins with a one-byte command code. The command may be followed by address, data, both, or nothing, depending on the command. CS# must be driven high after the last bit of the command sequence has been written.

The Read Data Bytes (READ), Read Data Bytes at Higher Speed (FAST_READ), Dual Output Read (DOR), Quad Output Read (QOR), Dual I/O High Performance Read (DIOR), Quad I/O High Performance Read (QIOR), Read Status Register (RDSR), Read Configuration Register (RCR), Read OTP Data (OTPR), Read Manufacturer and Device ID (READ_ID), Read Identification (RDID) and Release from Deep Power-Down and Read Electronic Signature (RES) command sequences are followed by a data output sequence on SO. CS# can be driven high after any bit of the sequence is output to terminate the operation.

The Page Program (PP), Quad Page Program (QPP), 64 KB Sector Erase (SE), 4 KB Parameter Sector Erase (P4E), 8 KB Parameter Sector Erase (P8E), Bulk Erase (BE), Write Status and Configuration Registers (WRR), Program OTP space (OTPP), Write Enable (WREN), or Write Disable (WRDI) commands require that CS# be driven high at a byte boundary, otherwise the command is not executed. Since a byte is composed of eight bits, CS# must therefore be driven high when the number of clock pulses after CS# is driven low is an exact multiple of eight.

The device ignores any attempt to access the memory array during a Write Registers, program, or erase operation, and continues the operation uninterrupted.

The instruction set is listed in Table 9.1.

Table 9.1 Instruction Set

Operation	Command	One byte Command Code	Description	Address Byte Cycle	Mode Bit Cycle	Dummy Byte Cycle	Data Byte Cycle
Read	READ	(03h) 0000 0011	Read Data bytes	3	0	0	1 to ∞
	FAST_READ	(0Bh) 0000 1011	Read Data bytes at Fast Speed	3	0	1	1 to ∞
	DOR	(3Bh) 0011 1011	Dual Output Read	3	0	1	1 to ∞
	QOR	(6Bh) 0110 1011	Quad Output Read	3	0	1	1 to ∞
	DIOR	(BBh) 1011 1011	Dual I/O High Performance Read	3	1	0	1 to ∞
	QIOR	(EBh) 1110 1011	Quad I/O High Performance Read	3	1	2	1 to ∞
	RDID	(9Fh) 1001 1111	Read Identification	0	0	0	1 to 81
	READ_ID	(90h) 1001 0000	Read Manufacturer and Device Identification	3	0	0	1 to ∞
Write Control	WREN	(06h) 0000 0110	Write Enable	0	0	0	0
	WRDI	(04h) 0000 0100	Write Disable	0	0	0	0
Erase	P4E (1)	(20h) 0010 0000	4 KB Parameter Sector Erase	3	0	0	0
	P8E (1)	(40h) 0100 0000	8 KB (two 4KB) Parameter Sector Erase	3	0	0	0
	SE	(D8h) 1101 1000	64 KB and 256 KB Sector Erase	3	0	0	0
	BE	(60h) 0110 0000 or (C7h) 1100 0111	Bulk Erase	0	0	0	0
Program	PP	(02h) 0000 0010	Page Programming	3	0	0	1 to 256
	QPP	(32h) 0011 0010	Quad Page Programming	3	0	0	1 to 256
Status and Configuration Register	RDSR	(05h) 0000 0101	Read Status Register	0	0	0	1 to ∞
	WRR	(01h) 0000 0001	Write (Status and Configuration) Register	0	0	0	1 to 2
	RCR	(35h) 0011 0101	Read Configuration Register (CFG)	0	0	0	1 to ∞
	CLSR	(30h) 0011 0000	Reset the Erase and Program Fall Flag (SRS and SR6) and restore normal operation)	0	0	0	0
Power Saving	DP	(B9h) 1011 1001	Deep Power-Down	0	0	0	0
	RES	(ABh) 1010 1011	Release from Deep Power-Down Mode	0	0	0	0
		(ABh) 1010 1011	Release from Deep Power-Down and Read Electronic Signature	0	0	3	1 to ∞
OTP	OTPP	(42h) 0100 0010	Program one byte of data in OTP memory space	3	0	0	1
	OTPR	(4Bh) 0100 1011	Read data in the OTP memory space	3	0	1	1 to ∞

Note
1. *For uniform 64 KB sector device only.*

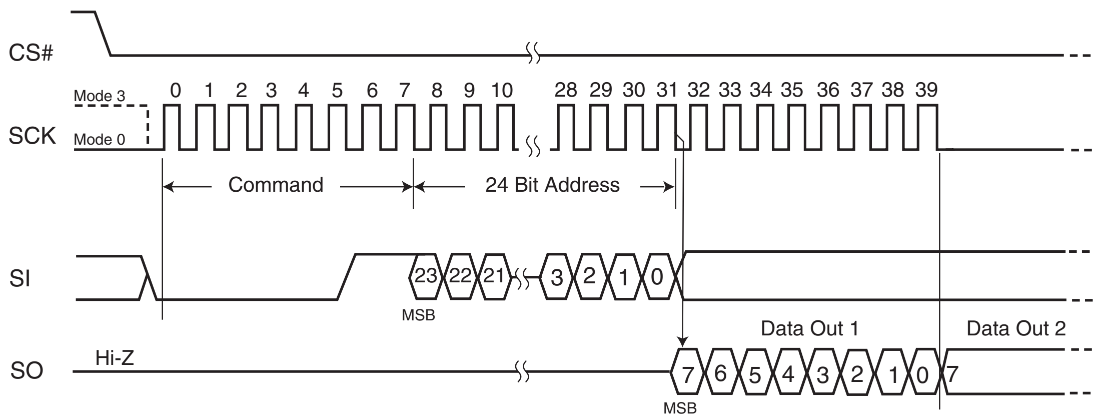
9.1 Read Data Bytes (READ)

The Read Data Bytes (READ) command reads data from the memory array at the frequency (f_R) presented at the SCK input, with a maximum speed of 40 MHz. The host system must first select the device by driving CS# low. The READ command is then written to SI, followed by a 3 byte address (A23-A0). Each bit is latched on the rising edge of SCK. The memory array data, at that address, are output serially on SO at a frequency f_R, on the falling edge of SCK.

Figure 9.1 and Table 9.1 on page 21 detail the READ command sequence. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single READ command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

The READ command is terminated by driving CS# high at any time during data output. The device rejects any READ command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

Figure 9.1 Read Data Bytes (READ) Command Sequence



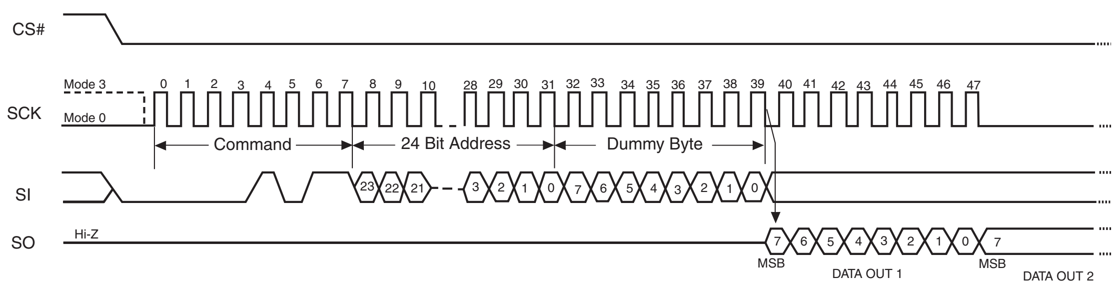
9.2 Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ command reads data from the memory array at the frequency (f_C) presented at the SCK input, with a maximum speed of 104 MHz. The host system must first select the device by driving CS# low. The FAST_READ command is then written to SI, followed by a 3 byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. The memory array data, at that address, are output serially on SO at a frequency f_C, on the falling edge of SCK.

The FAST_READ command sequence is shown in Figure 9.2 and Table 9.1 on page 21. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single FAST_READ command. When the highest address is reached, the address counter reverts to 000000h, allowing the read sequence to continue indefinitely.

The FAST_READ command is terminated by driving CS# high at any time during data output. The device rejects any FAST_READ command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

Figure 9.2 Read Data Bytes at Higher Speed (FAST_READ) Command Sequence



9.3 Dual Output Read Mode (DOR)

The Dual Output Read instruction is similar to the FAST_READ instruction, except that the data is shifted out 2 bits at a time using 2 pins (SI/IO0 and SO/IO1) instead of 1 bit, at a maximum frequency of 80 MHz. The Dual Output Read mode effectively doubles the data transfer rate compared to the FAST_READ instruction.

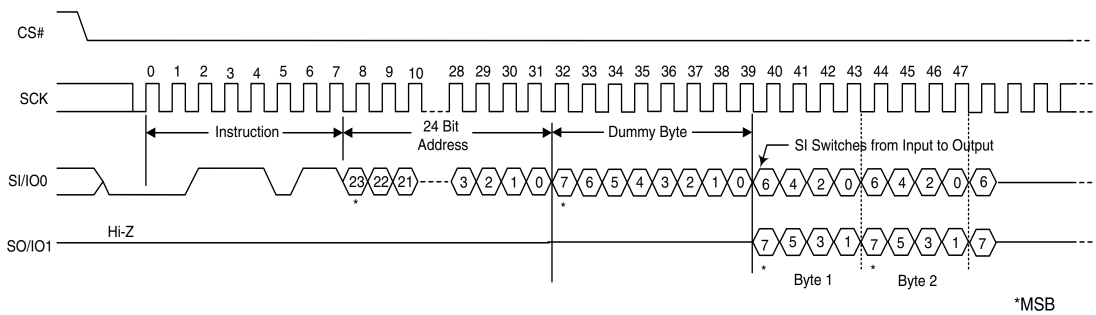
The host system must first select the device by driving CS# low. The Dual Output Read command is then written to SI, followed by a 3-byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. Then the memory contents, at the address that is given, are shifted out two bits at a time through the IO0 (SI) and IO1 (SO) pins at a frequency f_C on the falling edge of SCK.

The Dual Output Read command sequence is shown in Figure 9.3 and Table 9.1 on page 21. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single Dual Output Read command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

It is important that the I/O pins be set to high-impedance prior to the falling edge of the first data out clock.

The Dual Output Read command is terminated by driving CS# high at any time during data output. The device rejects any Dual Output Read command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

Figure 9.3 Dual Output Read Instruction Sequence



9.4 Quad Output Read Mode (QOR)

The Quad Output Read instruction is similar to the FAST_READ instruction, except that the data is shifted out 4 bits at a time using 4 pins (SI/IO0, SO/IO1, W#/ACC/IO2 and HOLD#/IO3) instead of 1 bit, at a maximum frequency of 80 MHz. The Quad Output Read mode effectively doubles the data transfer rate compared to the Dual Output Read instruction, and is four times the data transfer rate of the FAST_READ instruction.

The host system must first select the device by driving CS# low. The Quad Output Read command is then written to SI, followed by a 3-byte address (A23-A0) and a dummy byte. Each bit is latched on the rising edge of SCK. Then the memory contents, at the address that are given, are shifted out four bits at a time through IO0 (SI), IO1 (SO), IO2 (W#/ACC), and IO3 (HOLD#) pins at a frequency f_C on the falling edge of SCK.

The Quad Output Read command sequence is shown in Figure 9.4 and Table 9.1 on page 21. The first address byte specified can start at any location of the memory array. The device automatically increments to the next higher address after each byte of data is output. The entire memory array can therefore be read with a single Quad Output Read command. When the highest address is reached, the address counter reverts to 00000h, allowing the read sequence to continue indefinitely.

It is important that the I/O pins be set to high-impedance prior to the falling edge of the first data out clock.

The Quad Output Read command is terminated by driving CS# high at any time during data output. The device rejects any Quad Output Read command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

The Quad bit of Configuration Register must be set (CR Bit1 = 1) to enable the Quad mode capability of the S25FL device.

Figure 9.4 Quad Output Read Instruction Sequence