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S25FL116K/S25FL132K/S25FL164K

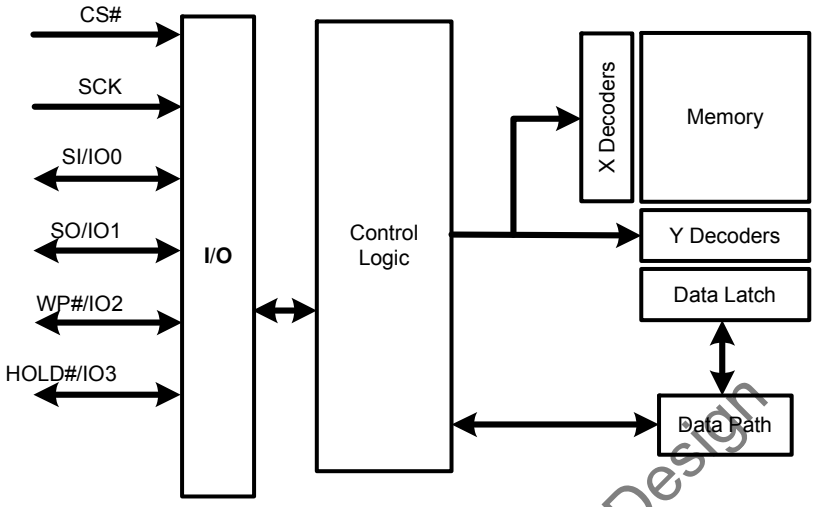
16-Mbit (2 Mbyte)/32-Mbit (4 Mbyte)/ 64-Mbit (8 Mbyte), 3.0 V, SPI Flash Memory

This product family has been retired and is not recommended for designs. For new and current designs, S25FL064L supersede the S25FL1-K family. These are the factory-recommended migration paths. Please refer to the S25FL-L Family datasheets for specifications and ordering information.

Features

- Serial Peripheral Interface (SPI) with Multi-I/O
  - SPI Clock polarity and phase modes 0 and 3
  - Command subset and footprint compatible with S25FL-K
- Read
  - Normal Read (Serial):
    - 50 MHz clock rate (–40 °C to +85 °C/105 °C)
  - Fast Read (Serial):
    - 108 MHz clock rate (–40 °C to +85 °C/105 °C)
  - Dual Read:
    - 108 MHz clock rate (–40 °C to +85 °C/105 °C)
  - Quad Read:
    - 108 MHz clock rate (–40 °C to +85 °C/105 °C)
  - 54 MB/s maximum continuous data transfer rate (–40 °C to +85 °C/105 °C)
  - Efficient Execute-In-Place (XIP)
  - Continuous and wrapped read modes
  - Serial Flash Discoverable Parameters (SFDP)
- Program
  - Serial-input Page Program (up to 256 bytes)
  - Program Suspend and Resume
- Erase
  - Uniform sector erase (4 kB)
  - Uniform block erase (64 kB)
  - Chip erase
  - Erase Suspend and Resume
- Cycling Endurance
  - 100K Program-Erase cycles, minimum
- Data Retention
  - 20-year data retention, minimum
- Security
  - Three 256-byte Security Registers with OTP protection
  - Low supply voltage protection of the entire memory
  - Pointer-based security protection feature (**S25FL132K and S25FL164K**)
  - Top / Bottom relative Block Protection Range, 4 kB to all of memory
  - 8-Byte Unique ID for each device
  - Non-volatile Status Register bits control protection modes
    - Software command protection
    - Hardware input signal protection
    - Lock-Down until power cycle protection
    - OTP protection of security registers
- 90 nm Floating Gate Technology
- Single Supply Voltage
  - 2.7 V to 3.6 V (Industrial, Industrial Plus, and Extended temperature range)
  - 2.6 V to 3.6 V (Extended temperature range)
- Temperature Ranges
  - Industrial (–40 °C to +85 °C)
  - Industrial Plus (–40 °C to +105 °C)
  - Automotive, AEC-Q100 Grade 3 (–40°C to +85°C)
  - Automotive, AEC-Q100 Grade 2 (–40°C to +105°C))
- Package Options
  - **S25FL116K**
    - 8-lead SOIC (150 mil) – SOA008
    - 8-lead SOIC (208 mil) – SOC008
    - 8-contact WSON 5 mm x 6 mm – WND008
    - 24-ball BGA 6 mm × 8 mm – FAB024 and FAC024
    - KGD / KGW
  - **S25FL132K**
    - 8-lead SOIC (150 mil) – SOA008
    - 8-lead SOIC (208 mil) – SOC008
    - 8-contact USON 4 mm × 4 mm – UNF008
    - 8-contact WSON 5 mm × 6 mm – WND008
    - 24-ball BGA 6 mm × 8 mm – FAB024 and FAC024
    - KGD / KGW
  - **S25FL164K**
    - 8-lead SOIC (208 mil) – SOC008
    - 16-lead SOIC (300 mil) – SO3016
    - 8-contact WSON 5 mm × 6 mm – WND008
    - 24-ball BGA 6 mm × 8 mm – FAB024 and FAC024

Logic Block Diagram



Performance Summary

Maximum Read Rates (V_{CC} = 2.7 V to 3.6 V, 85 °C/105 °C)

Command	Clock Rate (MHz)	Mbytes/s
Read	50	6.25
Fast Read	108	13.5
Dual Read	108	27
Quad Read	108	54

Typical Program and Erase Rates (V_{CC} = 2.7 V to 3.6 V, 85 °C/105 °C)

Operation	kbytes/s
Page Programming (256-byte page buffer)	365
4-kbyte Sector Erase	81
64-kbyte Sector Erase	131

Typical Current Consumption (V_{CC} = 2.7 V to 3.6 V, 85 °C/105 °C)

Operation	Current (mA)
Serial Read 50 MHz	7
Serial Read 108 MHz	12
Dual Read 108 MHz	14
Quad Read 108 MHz	16
Program	20
Erase	20
Standby	0.015
Deep-Power Down	0.002

Contents

1. General Description

The S25FL1-K of non-volatile flash memory devices connect to a host system via a Serial Peripheral Interface (SPI). Traditional SPI single bit serial input and output (Single I/O or SIO) is supported as well as optional two bit (Dual I/O or DIO) and four bit (Quad I/O or QIO) serial protocols. This multiple width interface is called SPI Multi-I/O or MIO.

The SPI-MIO protocols use only 4 to 6 signals:

- Chip Select (CS#)
- Serial Clock (SCK)
  - IO0 (SI)
  - IO1 (SO)
  - IO2 (WP#)
  - IO3 (HOLD#)
- Serial Data

The SIO protocol uses Serial Input (SI) and Serial Output (SO) for data transfer. The DIO protocols use IO0 and IO1 to input or output two bits of data in each clock cycle.

The Write Protect (WP#) input signal option allows hardware control over data protection. Software controlled commands can also manage data protection.

The HOLD# input signal option allows commands to be suspended and resumed on any clock cycle.

The QIO protocols use all of the data signals (IO0 to IO3) to transfer 4 bits in each clock cycle. When the QIO protocols are enabled the WP# and HOLD# inputs and features are disabled.

Clock frequency of up to 108 MHz is supported, allowing data transfer rates up to:

- Single bit data path = 13.5 Mbytes/s
- Dual bit data path = 27 Mbytes/s
- Quad bit data path = 54 Mbytes/s

Executing code directly from flash memory is often called execute-In-Place or XIP. By using S25FL1-K devices at the higher clock rates supported, with QIO commands, the command read transfer rate can match or exceed traditional x8 or x16 parallel interface, asynchronous, NOR flash memories, while reducing signal count dramatically. The Continuous Read Mode allows for random memory access with as few as 8-clocks of overhead for each access, providing efficient XIP operation. The Wrapped Read mode provides efficient instruction or data cache refill via a fast read of the critical byte that causes a cache miss, followed by reading all other bytes in the same cache line in a single read command.

The S25FL1-K:

- Support JEDEC standard manufacturer and device type identification.
- Program pages of 256 bytes each. One to 256 bytes can be programmed in each Page Program operation. Pages can be erased in groups of 16 (4-kB aligned sector erase), groups of 256 (64-kB aligned block erase), or the entire chip (chip erase).
- The S25FL1-K devices operate on a single 2.6V/2.7V to 3.6V power supply and all devices are offered in space-saving packages.
- Provides an ideal storage solution for systems with limited space, signal connections, and power. These memories offer flexibility and performance well beyond ordinary serial flash devices. They are ideal for code shadowing to RAM, executing code directly (XIP), and storing reprogrammable data.

1.1 Migration Notes

1.1.1 Features Comparison

The S25FL1-K is command set and footprint compatible with prior generation FL-K and FL-P families.

Table 1. FL Generations Comparison

Parameter	S25FL1-K	S25FL-K	S25FL-P
Technology Node	90 nm	90 nm	90 nm
Architecture	Floating Gate	Floating Gate	MirrorBit®
Release Date	In Production	In Production	In Production
Density	16 Mbit - 64 Mbit	4 Mbit - 128 Mbit	32 Mbit - 256 Mbit
Bus Width	x1, x2, x4	x1, x2, x4	x1, x2, x4
Supply Voltage	2.6V / 2.7V - 3.6V	2.7V - 3.6V	2.7V - 3.6V
Normal Read Speed	6 MB/s (50 MHz)	6 MB/s (50 MHz)	5 MB/s (40 MHz)
Fast Read Speed	13.5 MB/s (108 MHz)	13 MB/s (104 MHz)	13 MB/s (104 MHz)
Dual Read Speed	27 MB/s (108 MHz)	26 MB/s (104 MHz)	20 MB/s (80 MHz)
Quad Read Speed	54 MB/s (108 MHz at 85°C/105°C)	52 MB/s (104 MHz)	40 MB/s (80 MHz)
Program Buffer Size	256B	256B	256B
Page Programming Time (typ.)	700 µs (256B)	700 µs (256B)	1500 µs (256B)
Program Suspend / Resume	Yes	Yes	No
Erase Sector Size	4 kB / 64 kB	4 kB / 32 kB / 64 kB	64 kB / 256 kB
Parameter Sector Size	N/A	N/A	4 kB
Sector Erase Time (typ.)	50 ms (4 kB), 500 ms (64 kB)	30 ms (4 kB), 150 ms (64 kB)	500 ms (64 kB)
Erase Suspend / Resume	Yes	Yes	No
OTP Size	768B (3 x 256B)	768B (3 x 256B)	506B
Operating Temperature	-40°C to +85°C / +105°C	-40°C to +85°C	-40°C to +85°C / +105°C

Notes:

1. *S25FL-K family devices can erase 4-kB sectors in groups of 32 kB or 64 kB.*
2. *S25FL1-K family devices can erase 4-kB sectors in groups of 64 kB.*
3. *S25FL-P has either 64-kB or 256-kB uniform sectors depending on an ordering option.*
4. *Refer to individual data sheets for further details.*

1.1.2 Known Feature Differences from Prior Generations

1.1.2.1 Secure Silicon Region (OTP)

The size and format (address map) of the One Time Program area is the same for the S25FL1-K and the S25FL-K but different for the S25FL-P.

1.1.2.2 Commands Not Supported

The following S25FL-K and S25FL-P commands are not supported:

- Quad Page PGM (32h)
- Half-Block Erase 32K (52h)
- Word read Quad I/O (E7)
- Octal Word Read Quad I/O (E3h)
- MFID dual I/O (92h)
- MFID quad I/O (94h)
- Read Unique ID (4Bh)

1.1.2.3 New Features

The S25FL1-K introduces new features to low density SPI category memories:

- Variable read latency (number of dummy cycles) for faster initial access time or higher clock rate read commands
- Industrial Plus and Extended temperature range
- Volatile configuration option in addition to legacy non-volatile configuration

1.2 Glossary

- **Command.** All information transferred between the host system and memory during one period while CS# is low. This includes the instruction (sometimes called an operation code or opcode) and any required address, mode bits, latency cycles, or data.
- **Flash**. The name for a type of Electrical Erase Programmable Read Only Memory (EEPROM) that erases large blocks of memory bits in parallel, making the erase operation much faster than early EEPROM.
- **High**. A signal voltage level ≥ V_{IH} or a logic level representing a binary one (1).
- **Instruction**. The 8-bit code indicating the function to be performed by a command (sometimes called an operation code or opcode). The instruction is always the first 8 bits transferred from host system to the memory in any command.
- **Low**. A signal voltage level ≤ V_{IL} or a logic level representing a binary zero (0).
- **LSB**. Least Significant Bit. Generally the right most bit, with the lowest order of magnitude value, within a group of bits of a register or data value.
- **MSB**. Most Significant Bit. Generally the left most bit, with the highest order of magnitude value, within a group of bits of a register or data value.
- **Non-Volatile**. No power is needed to maintain data stored in the memory.
- **OPN**. Ordering Part Number. The alphanumeric string specifying the memory device type, density, package, factory non-volatile configuration, etc. used to select the desired device.
- **Page**. 256-byte aligned and length group of data.
- **PCB**. Printed Circuit Board.
- **Register Bit References**. Are in the format: Register_name[bit_number] or Register_name[bit_range_MSB: bit_range_LSB].
- **Sector**. Erase unit size; all sectors are physically 4-kbytes aligned and length. Depending on the erase command used, groups of physical sectors may be erased as a larger logical sector of 64 kbytes.
- **Write**. An operation that changes data within volatile or non-volatile registers bits or non-volatile flash memory. When changing non-volatile data, an erase and reprogramming of any unchanged non-volatile data is done, as part of the operation, such that the non-volatile data is modified by the write operation, in the same way that volatile data is modified – as a single operation. The non-volatile data appears to the host system to be updated by the single write command, without the need for separate commands for erase and reprogram of adjacent, but unaffected data.

1.3 Other Resources

1.3.1 Cypress Flash Memory Roadmap

www.cypress.com/product-roadmaps/cypress-flash-memory-roadmap

1.3.2 Links to Software

www.cypress.com/software-and-drivers-cypress-flash-memory

1.3.3 Links to Application Notes

www.cypress.com/cypressappnotes

Hardware Interface

Serial Peripheral Interface with Multiple Input / Output (SPI-MIO)

Many memory devices connect to their host system with separate parallel control, address, and data signals that require a large number of signal connections and larger package size. The large number of connections increase power consumption due to so many signals switching and the larger package increases cost.

The S25FL1-K reduces the number of signals for connection to the host system by serially transferring all control, address, and data information over 4 to 6 signals. This reduces the cost of the memory package, reduces signal switching power, and either reduces the host connection count or frees host connectors for use in providing other features.

The S25FL1-K uses the industry standard single bit Serial Peripheral Interface (SPI) and also supports commands for two bit (Dual) and four bit (Quad) wide serial transfers. This multiple width interface is called SPI Multi-I/O or SPI-MIO.

2. Signal Descriptions

2.1 Input / Output Summary

Table 2. Signal List

Signal Name	Type	Description
SCK	Input	**Serial Clock.**
CS#	Input	**Chip Select.**
SI (IO0)	I/O	**Serial Input** for single bit data commands. IO0 for Dual or Quad commands.
SO (IO1)	I/O	**Serial Output** for single bit data commands. IO1 for Dual or Quad commands.
WP# (IO2)	I/O	**Write Protect** in single bit or Dual data commands. IO2 in Quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
HOLD# (IO3)	I/O	**Hold** (pause) serial transfer in single bit or Dual data commands. IO3 in Quad-I/O mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands.
V_{CC}	Supply	**Core and I/O Power Supply.**
V_{SS}	Supply	**Ground.**
NC	Unused	**Not Connected.** No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). However, any signal connected to an NC must not have voltage levels higher than V_{CC}.
RFU	Reserved	**Reserved for Future Use.** No device internal signal is currently connected to the package connector but there is potential future use of the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU	Reserved	**Do Not Use.** Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

Note:

1. A signal name ending with the # symbol is active when low.

2.2 Address and Data Configuration

Traditional SPI single bit wide commands (Single or SIO) send information from the host to the memory only on the SI signal. Data may be sent back to the host serially on the Serial Output (SO) signal.

Dual or Quad Output commands send information from the host to the memory only on the SI signal. Data will be returned to the host as a sequence of bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Dual or Quad Input / Output (I/O) commands send information from the host to the memory as bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

2.3 Serial Clock (SCK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCK signal. Data output changes after the falling edge of SCK.

2.4 Chip Select (CS#)

The chip select signal indicates when a command for the device is in process and the other signals are relevant for the memory device. When the CS# signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. Unless an internal Program, Erase or Write Status Registers embedded operation is in progress, the device will be in the Standby Power mode. Driving the CS# input to logic low state enables the device, placing it in the Active Power mode. After Power-Up, a falling edge on CS# is required prior to the start of any command.

2.5 Serial Input (SI) / IO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal.

SI becomes IO0 - an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK).

2.6 Serial Output (SO) / IO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal.

SO becomes IO1, an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK).

2.7 Write Protect (WP#) / IO2

When WP# is driven Low (V_{IL}), while the Status Register Protect bits (SRP1 and SRP0) of the Status Registers (SR2[0] and SR1[7]) are set to 0 and 1 respectively, it is not possible to write to the Status Registers. This prevents any alteration of the Status Registers. As a consequence, all the data bytes in the memory area that are protected by the Block Protect, TB, SEC, and CMP bits in the status registers, are also hardware protected against data modification while WP# remains Low.

The WP# function is not available when the Quad mode is enabled (QE) in Status Register-2 (SR2[1]=1). The WP# function is replaced by IO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK).

WP# has an internal pull-up resistance; when unconnected, WP# is at V_{IH} and may be left unconnected in the host system if not used for Quad mode.

2.8 HOLD# / IO3

The HOLD# signal is used to pause any serial communications with the device without deselecting the device or stopping the serial clock.

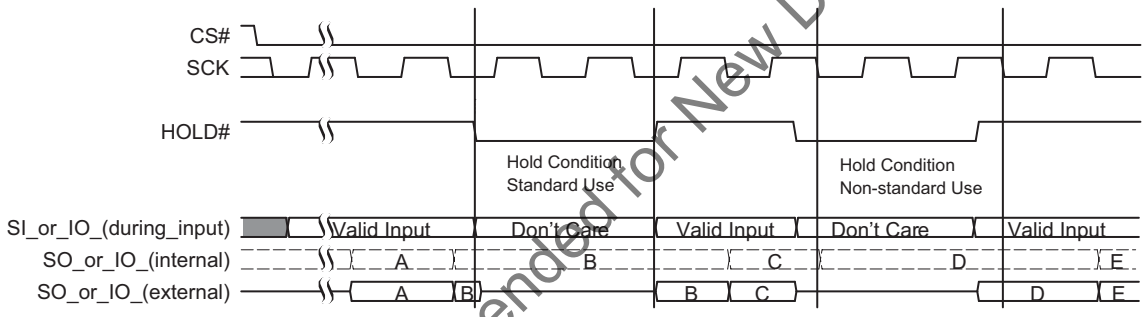
To enter the Hold condition, the device must be selected by driving the CS# input to the logic low state. It is required that the user keep the CS# input low state during the entire duration of the Hold condition. This is to ensure that the state of the interface logic remains unchanged from the moment of entering the Hold condition.

The Hold condition starts on the falling edge of the Hold (HOLD#) signal, provided that this coincides with SCK being at the logic low state. If the falling edge does not coincide with the SCK signal being at the logic low state, the Hold condition starts whenever the SCK signal reaches the logic low state. Taking the HOLD# signal to the logic low state does not terminate any Write, Program or Erase operation that is currently in progress.

During the Hold condition, SO is in high impedance and both the SI and SCK input are Don't Care.

The Hold condition ends on the rising edge of the Hold (HOLD#) signal, provided that this coincides with the SCK signal being at the logic low state. If the rising edge does not coincide with the SCK signal being at the logic low state, the Hold condition ends whenever the SCK signal reaches the logic low state.

Figure 1. Hold Condition



2.9 Core and I/O Signal Voltage Supply (V_{CC})

V_{CC} is the voltage source for all device internal logic and input / output signals. It is the single voltage used for all device functions including read, program, and erase.

2.10 Supply and Signal Ground (V_{SS})

V_{SS} is the common voltage drain and ground reference for the device core, input signal receivers, and output drivers.

2.11 Not Connected (NC)

No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).

2.12 Reserved for Future Use (RFU)

No device internal signal is currently connected to the package connector but is there potential future use for the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.

2.13 Do Not Use (DNU)

A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.

2.14 Block Diagrams

Figure 2. Bus Master and Memory Devices on the SPI Bus – Single Bit Data Path

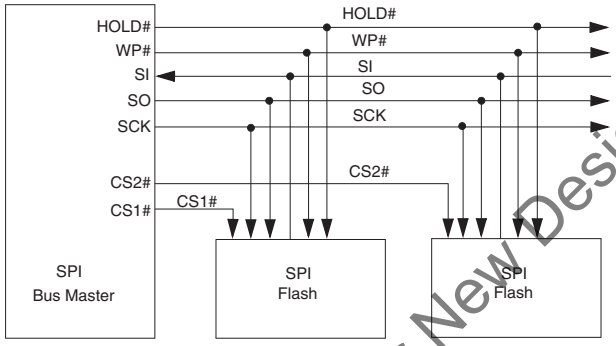


Figure 3. Bus Master and Memory Devices on the SPI Bus – Dual Bit Data Path

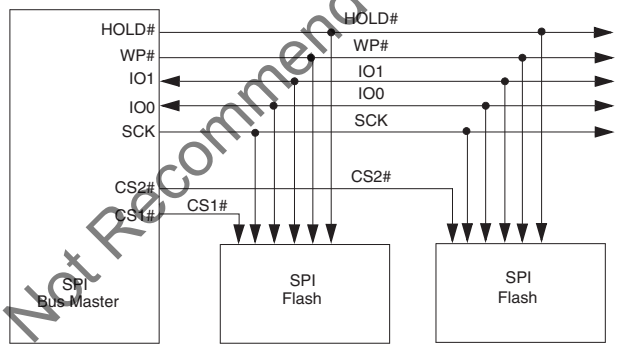
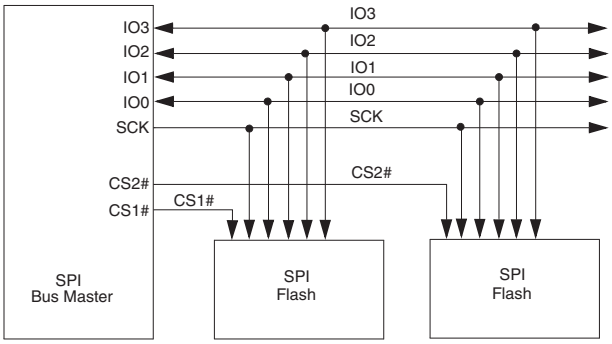


Figure 4. Bus Master and Memory Devices on the SPI Bus – Quad Bit Data Path



3. Signal Protocols

3.1 SPI Clock Modes

The S25FL1-K can be driven by an embedded microcontroller (bus master) in either of the two following clocking modes.

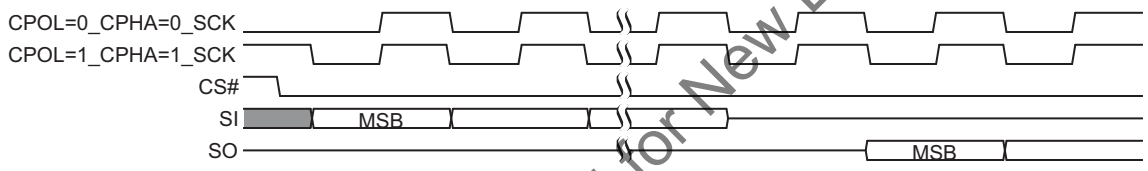
- **Mode 0** with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0
- **Mode 3** with CPOL = 1 and, CPHA = 1

For these two modes, input data into the device is always latched in on the rising edge of the SCK signal and the output data is always available from the falling edge of the SCK clock signal.

The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

- SCK will stay at logic low state with CPOL = 0, CPHA = 0
- SCK will stay at logic high state with CPOL = 1, CPHA = 1

Figure 5. SPI Modes Supported



Timing diagrams throughout the remainder of the document are generally shown as both mode 0 and 3 by showing SCK as both high and low at the fall of CS#. In some cases a timing diagram may show only mode 0 with SCK low at the fall of CS#. In such a case, mode 3 timing simply means clock is high at the fall of CS# so no SCK rising edge set up or hold time to the falling edge of CS# is needed for mode 3.

SCK cycles are measured (counted) from one falling edge of SCK to the next falling edge of SCK. In mode 0 the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already low at the beginning of a command.

3.2 Command Protocol

All communication between the host system and S25FL1-K memory devices is in the form of units called commands.

All commands begin with an instruction that selects the type of information transfer or device operation to be performed. Commands may also have an address, instruction modifier (mode), latency period, data transfer to the memory, or data transfer from the memory. All instruction, address, and data information is transferred serially between the host system and memory device.

All instructions are transferred from host to memory as a single bit serial sequence on the SI signal.

Single bit wide commands may provide an address or data sent only on the SI signal. Data may be sent back to the host serially on the SO signal.

Dual or Quad Output commands provide an address sent to the memory only on the SI signal. Data will be returned to the host as a sequence of bit pairs on IO0 and IO1 or four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Dual or Quad Input / Output (I/O) commands provide an address sent from the host as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or, four bit (nibble) groups on IO0, IO1, IO2, and IO3.

Commands are structured as follows:

- Each command begins with CS# going low and ends with CS# returning high. The memory device is selected by the host driving the Chip Select (CS#) signal low throughout a command.
- The serial clock (SCK) marks the transfer of each bit or group of bits between the host and memory.
- Each command begins with an eight bit (byte) instruction. The instruction is always presented only as a single bit serial sequence on the Serial Input (SI) signal with one bit transferred to the memory device on each SCK rising edge. The instruction selects the type of information transfer or device operation to be performed.
- The instruction may be stand alone or may be followed by address bits to select a location within one of several address spaces in the device. The instruction determines the address space used. The address is a 24-bit, byte boundary, address. The address transfers occur on SCK rising edge.
- The width of all transfers following the instruction are determined by the instruction sent. Following transfers may continue to be single bit serial on only the SI or Serial Output (SO) signals, they may be done in 2-bit groups per (dual) transfer on the IO0 and IO1 signals, or they may be done in 4-bit groups per (quad) transfer on the IO0-IO3 signals. Within the dual or quad groups the least significant bit is on IO0. More significant bits are placed in significance order on each higher numbered IO signal. SIngle bits or parallel bit groups are transferred in most to least significant bit order.
- Some instructions send an instruction modifier called mode bits, following the address, to indicate that the next command will be of the same type with an implied, rather than an explicit, instruction. The next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands. The mode bit transfers occur on SCK rising edge.
- The address or mode bits may be followed by write data to be stored in the memory device or by a read latency period before read data is returned to the host.
- Write data bit transfers occur on SCK rising edge.
- SCK continues to toggle during any read access latency period. The latency may be zero to several SCK cycles (also referred to as dummy cycles). At the end of the read latency cycles, the first read data bits are driven from the outputs on SCK falling edge at the end of the last read latency cycle. The first read data bits are considered transferred to the host on the following SCK rising edge. Each following transfer occurs on the next SCK rising edge.
- If the command returns read data to the host, the device continues sending data transfers until the host takes the CS# signal high. The CS# signal can be driven high after any transfer in the read data sequence. This will terminate the command.
- At the end of a command that does not return data, the host drives the CS# input high. The CS# signal must go high after the eighth bit, of a stand alone instruction or of the last write data byte that is transferred. That is, the CS# signal must be driven high when the number of clock cycles after CS# signal was driven low is an exact multiple of eight cycles. If the CS# signal does not go high exactly at the eight SCK cycle boundary of the instruction or write data, the command is rejected and not executed.
- All instruction, address, and mode bits are shifted into the device with the most significant bits (MSB) first. The data bits are shifted in and out of the device MSB first. All data is transferred in byte units with the lowest address byte sent first. Following bytes of data are sent in lowest to highest byte address order i.e. the byte address increments.
- All attempts to read the flash memory array during a program, erase, or a write cycle (embedded operations) are ignored. The embedded operation will continue to execute without any affect. A very limited set of commands are accepted during an embedded operation. These are discussed in the individual command descriptions.
- Depending on the command, the time for execution varies. A command to read status information from an executing command is available to determine when the command completes execution and whether the command was successful.

3.2.1 Command Sequence Examples

Figure 6. Stand Alone Instruction Command

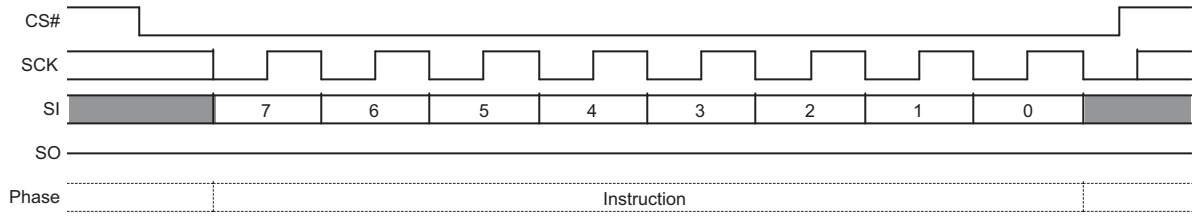


Figure 7. Single Bit Wide Input Command

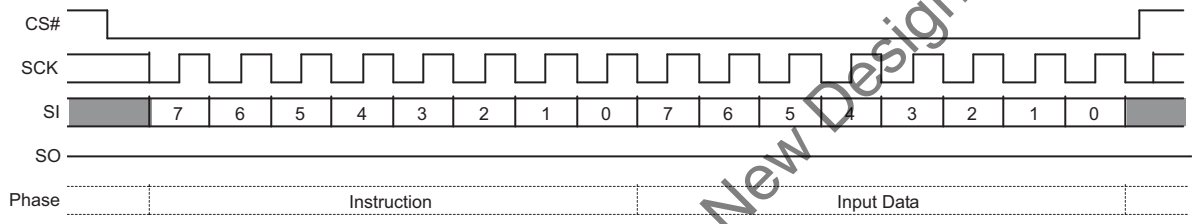


Figure 8. Single Bit Wide Output Command

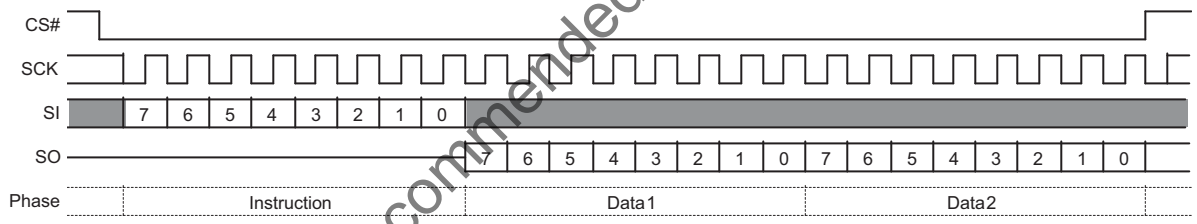


Figure 9. Single Bit Wide I/O Command without Latency

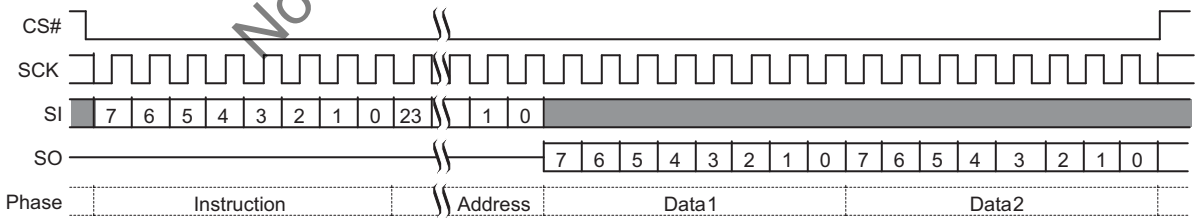


Figure 10. Single Bit Wide I/O Command with Latency

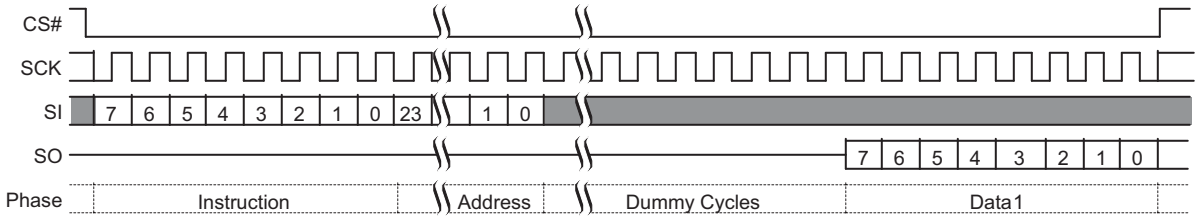


Figure 11. Dual Output Command

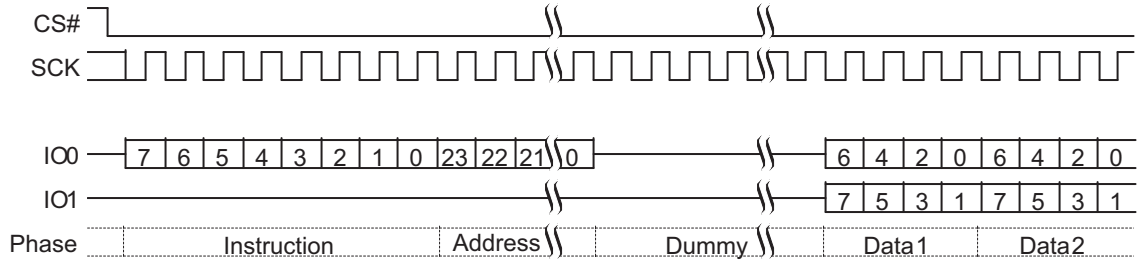


Figure 12. Quad Output Command without Latency

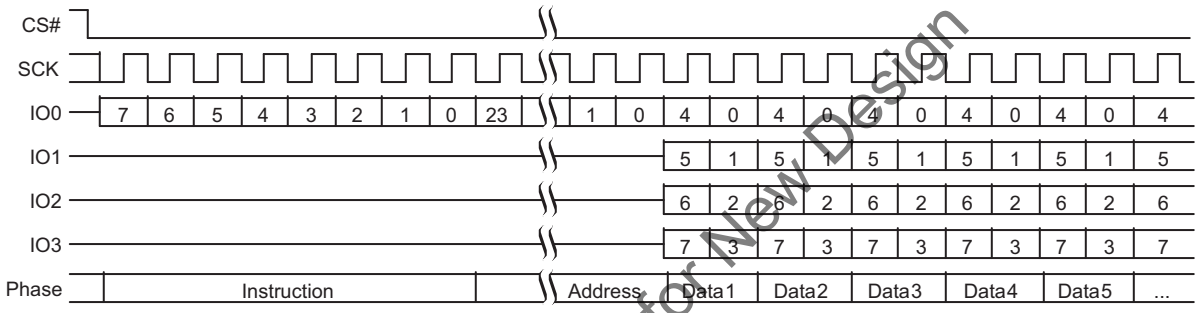


Figure 13. Dual I/O Command

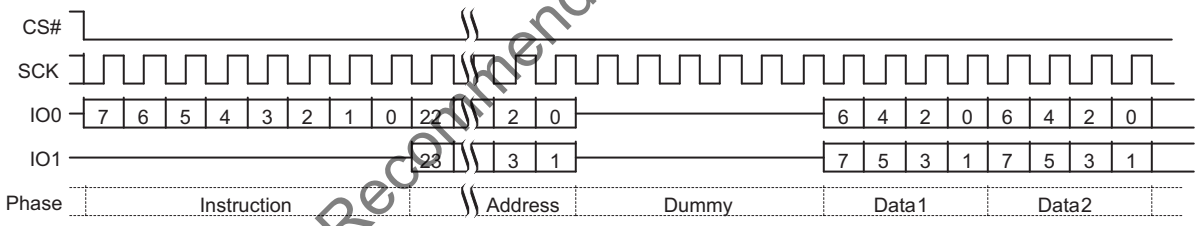
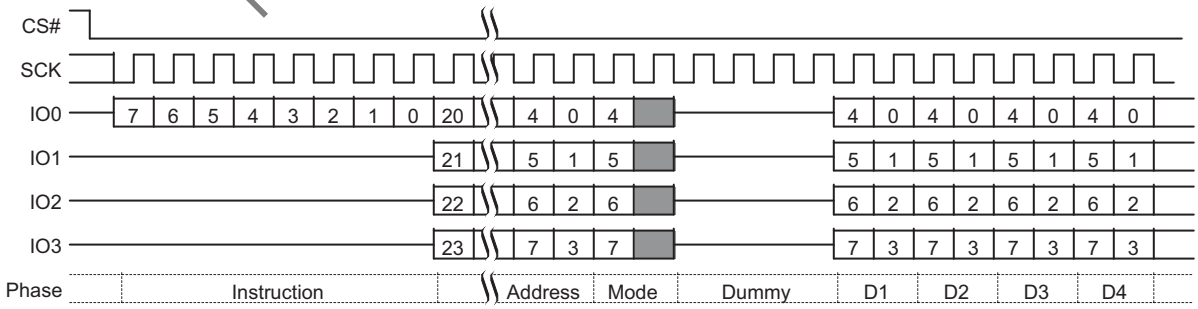


Figure 14. Quad I/O Command



Additional sequence diagrams, specific to each command, are provided in Commands on page 62.

3.3 Interface States

This section describes the input and output signal levels as related to the SPI interface behavior.

Table 3. Interface States Summary

Interface State	V_{CC}	SCK	CS#	HOLD# / IO3	WP# / IO2	SO / IO1	SI / IO0
Low Power Hardware Data Protection	< V_{WI}	X	X	X	X	Z	X
Power-On (Cold) Reset	≥ V_{CC} (min)	X	HH	X	X	Z	X
Interface Standby	≥ V_{CC} (min)	X	X	X	X	Z	X
Instruction Cycle	≥ V_{CC} (min)	HT	HL	HH	HV	Z	HV
Hold Cycle	≥ V_{CC} (min)	HV or HT	HL	HL	X	X	X
Single Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	HT	HL	HH	X	Z	HV
Single Latency (Dummy) Cycle	≥ V_{CC} (min)	HT	HL	HH	X	Z	X
Single Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	HT	HL	HH	X	MV	X
Dual Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	HT	HL	HH	X	HV	HV
Dual Latency (Dummy) Cycle	≥ V_{CC} (min)	HT	HL	HH	X	X	X
Dual Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	HT	HL	HH	X	MV	MV
Quad Input Cycle Host to Memory Transfer	≥ V_{CC} (min)	HT	HL	HV	HV	HV	HV
Quad Latency (Dummy) Cycle	≥ V_{CC} (min)	HT	HL	X	X	X	X
Quad Output Cycle Memory to Host Transfer	≥ V_{CC} (min)	HT	HL	MV	MV	MV	MV

Legend:
Z = no driver - floating signal
HL = Host driving V_{IL}
HH = Host driving V_{IH}
HV = either HL or HH
X = HL or HH or Z
HT = toggling between HL and HH
ML = Memory driving V_{IL}
MH = Memory driving V_{IH}
MV = either ML or MH

3.3.1 Low Power Hardware Data Protection

When V_{CC} is less than V_{WI} the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

3.3.2 Power-On (Cold) Reset

When the core voltage supply remains at or below the $V_{CC\ (Low)}$ voltage for > t_{PD} time, then rises to ≥ V_{WI} the device will begin its Power-On-Reset (POR) process. POR continues until the end of t_{PUW}. During t_{PUW} the device does not react to write commands. Following the end of t_{PUW} the device transitions to the Interface Standby state and can accept write commands. For additional information on POR see Power-On (Cold) Reset on page 25.

3.3.3 Interface Standby

When CS# is high the SPI interface is in standby state. Inputs are ignored. The interface waits for the beginning of a new command. The next interface state is Instruction Cycle when CS# goes low to begin a new command.

While in interface standby state the memory device draws standby current (I_{SB}) if no embedded algorithm is in progress. If an embedded algorithm is in progress, the related current is drawn until the end of the algorithm when the entire device returns to standby current draw.

3.3.4 Instruction Cycle

When the host drives the MSB of an instruction and CS# goes low, on the next rising edge of SCK the device captures the MSB of the instruction that begins the new command. On each following rising edge of SCK the device captures the next lower significance bit of the 8-bit instruction. The host keeps CS# low, HOLD# high, and drives Write Protect (WP#) signal as needed for the instruction. However, WP# is only relevant during instruction cycles of a Write Status Registers command and is otherwise ignored.

Each instruction selects the address space that is operated on and the transfer format used during the remainder of the command. The transfer format may be Single, Dual output, Quad output, Dual I/O, or Quad I/O. The expected next interface state depends on the instruction received.

Some commands are stand alone, needing no address or data transfer to or from the memory. The host returns CS# high after the rising edge of SCK for the eighth bit of the instruction in such commands. The next interface state in this case is Interface Standby.

3.3.5 Hold

When Quad mode is not enabled (SR2[1]=0) the HOLD# / IO3 signal is used as the HOLD# input. The host keeps HOLD# low, SCK may be at a valid level or continue toggling, and CS# is low. When HOLD# is low a command is paused, as though SCK were held low. SI / IO0 and SO / IO1 ignore the input level when acting as inputs and are high impedance when acting as outputs during hold state. Whether these signals are input or output depends on the command and the point in the command sequence when HOLD# is asserted low.

When HOLD# returns high the next state is the same state the interface was in just before HOLD# was asserted low.

3.3.6 Single Input Cycle — Host to Memory Transfer

Several commands transfer information after the instruction on the single serial input (SI) signal from host to the memory device. The dual output, and quad output commands send address to the memory using only SI but return read data using the I/O signals. The host keeps CS# low, HOLD# high, and drives SI as needed for the command. The memory does not drive the Serial Output (SO) signal.

The expected next interface state depends on the instruction. Some instructions continue sending address or data to the memory using additional Single Input Cycles. Others may transition to Single Latency, or directly to Single, Dual, or Quad Output.

3.3.7 Single Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the instruction. During the latency cycles, the host keeps CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The host may drive the SI signal during these cycles or the host may leave SI floating. The memory does not use any data driven on SI / I/O0 or other I/O signals during the latency cycles. In dual or quad read commands, the host must stop driving the I/O signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving I/O signals during latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the Serial Output (SO) or I/O signals during the latency cycles.

The next interface state depends on the command structure i.e. the number of latency cycles, and whether the read is single, dual, or quad width.

3.3.8 Single Output Cycle — Memory to Host Transfer

Several commands transfer information back to the host on the single Serial Output (SO) signal. The host keeps CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The memory ignores the Serial Input (SI) signal. The memory drives SO with data.

The next interface state continues to be Single Output Cycle until the host returns CS# to high ending the command.

3.3.9 Dual Input Cycle — Host to Memory Transfer

The Read Dual I/O command transfers two address or mode bits to the memory in each cycle. The host keeps CS# low, HOLD# high. The Write Protect (WP#) signal is ignored. The host drives address on SI / IO0 and SO / IO1.

The next interface state following the delivery of address and mode bits is a Dual Latency Cycle if there are latency cycles needed or Dual Output Cycle if no latency is required.

3.3.10 Dual Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the instruction. During the latency cycles, the host keeps CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The host may drive the SI / IO0 and SO / IO1 signals during these cycles or the host may leave
SI / IO0 and SO / IO1 floating. The memory does not use any data driven on SI / IO0 and SO / IO1 during the latency cycles. The host must stop driving SI / IO0 and SO / IO1 on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the SI / IO0 and SO / IO1 signals during the latency cycles.

The next interface state following the last latency cycle is a Dual Output Cycle.

3.3.11 Dual Output Cycle — Memory to Host Transfer

The Read Dual Output and Read Dual I/O return data to the host two bits in each cycle. The host keeps CS# low, and HOLD# high. The Write Protect (WP#) signal is ignored. The memory drives data on the SI / IO0 and SO / IO1 signals during the dual output cycles.

The next interface state continues to be Dual Output Cycle until the host returns CS# to high ending the command.

3.3.12 Quad Input Cycle — Host to Memory Transfer

The Read Quad I/O command transfers four address, mode, or data bits to the memory in each cycle. The host keeps CS# low, and drives the IO signals.

For Read Quad I/O the next interface state following the delivery of address and mode bits is a Quad Latency Cycle if there are latency cycles needed or Quad Output Cycle if no latency is required.

3.3.13 Quad Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Control in the Status Register-3 (SR3[3:0]). During the latency cycles, the host keeps CS# low. The host may drive the IO signals during these cycles or the host may leave the IO floating. The memory does not use any data driven on IO during the latency cycles. The host must stop driving the IO signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the IO signals during the latency cycles.

The next interface state following the last latency cycle is a Quad Output Cycle.

3.3.14 Quad Output Cycle — Memory to Host Transfer

The Read Quad Output and Read Quad I/O return data to the host four bits in each cycle. The host keeps CS# low. The memory drives data on IO0-IO3 signals during the Quad output cycles.

The next interface state continues to be Quad Output Cycle until the host returns CS# to high ending the command.

3.4 Status Register Effects on the Interface

The Status Register-2, bit 1 (SR2[1]), selects whether Quad mode is enabled to ignore HOLD# and WP# and allow Read Quad Output, and Read Quad I/O commands.

3.5 Data Protection

Some basic protection against unintended changes to stored data are provided and controlled purely by the hardware design. These are described below. Other software managed protection methods are discussed in the software section of this document.

3.5.1 Low Power

When V_{CC} is less than V_{WI} the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

3.5.2 Power-Up

Program and erase operations continue to be prevented during the Power-Up to Write delay (t_{PUW}) because no write command is accepted until after t_{PUW}.

3.5.3 Deep Power-Down (DPD)

In DPD mode the device responds only to the Resume from DPD command (RES ABh). All other commands are ignored during DPD mode, thereby protecting the memory from program and erase operations.

3.5.4 Clock Pulse Count

The device verifies that all program, erase, and Write Status Registers commands consist of a clock pulse count that is a multiple of eight before executing them. A command not having a multiple of 8 clock pulse count is ignored and no error status is set for the command.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Parameters (1)	Symbol	Conditions	Range	Unit
Supply Voltage	V_{CC}		–0.6 to +4.0	V
Voltage Applied to any Pin	V_{IO}	Relative to Ground	–0.6 to +4.0	V
Transient Voltage on any Pin	V_{IOT}	< 20 ns Transient Relative to Ground	–2.0 to 6.0	V
Storage Temperature	T_{STG}		–65 to +150	°C
Lead Temperature	T_{LEAD}		(2)	°C
Electrostatic Discharge Voltage	V_{ESD}	Human Body Model (3)	–2000 to +2000	V

Notes:

1. *This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.*
2. *Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.*
3. *JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).*

4.1.1 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{CC}. During voltage transitions, inputs or I/Os may overshoot V_{SS} to negative V_{IOT} or overshoot to positive V_{IOT}, for periods up to 20 ns.

Figure 15. Maximum Negative Overshoot Waveform

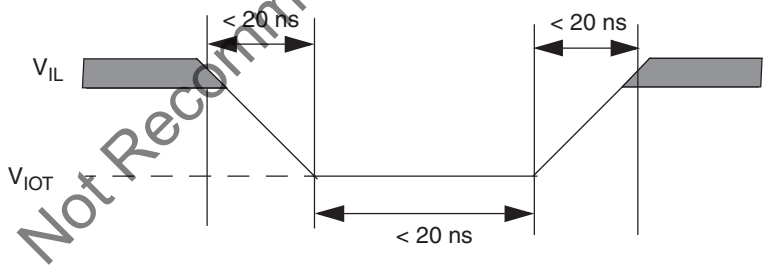
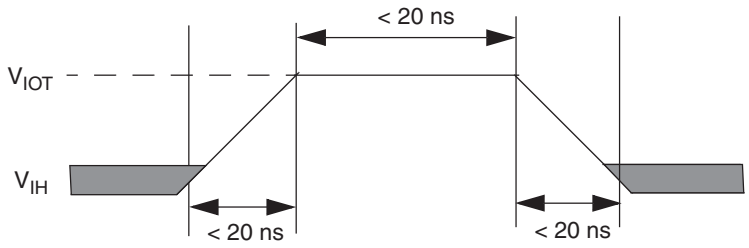


Figure 16. Maximum Positive Overshoot Waveform



4.1.2 Latchup Characteristics

Table 5. Latchup Specification

Description	Min	Max	Unit
Input voltage with respect to V_{SS} on all input only connections	–1.0	V_{CC} + 1.0	V
Input voltage with respect to V_{SS} on all I/O connections	–1.0	V_{CC} + 1.0	V
V_{CC} Current	–100	+100	mA

Note:
1. *Excludes power supply V_{CC}. Test conditions: V_{CC} = 3.0V, one connection at a time tested, connections not being tested are at V_{SS}.*

4.2 Thermal Resistance

Table 6. Thermal Resistance

Parameter	Description	SOA008	SOC008	FAB024	FAC024	WSON	Unit
Theta JA	Thermal resistance (junction to ambient)	75	75	39	39	18	°C/W

4.3 Operating Ranges

Operating ranges define those limits between which functionality of the device is guaranteed.

Table 7. Operating Ranges

Parameter	Symbol	Conditions	Spec		Unit
			Min	Max	
Ambient Temperature	T_A	Industrial	-40	+85	°C
		Industrial Plus	-40	+105	
Supply Voltage	V_{CC}	Industrial and Industrial Plus Temp	2.7	3.6	V

Note:
1. *V_{CC} voltage during read can operate across the min and max range but should not exceed ± 10% of the voltage used during programming or erase of the data being read.*

4.4 DC Electrical Characteristics

Table 8. DC Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max		Unit
					-40 to 85°C	-40 to 105°C	
Input Leakage	I_{LI}				±2		µA
I/O Leakage	I_{LO}				±2		µA
Standby Current	I_{CC1}	CS# = V_{CC}, V_{IN} = GND or V_{CC}		15	25	25	µA
Deep Power-Down Current **(S25FL116K)**	I_{CC2}	CS# = V_{CC}, V_{IN} = GND or V_{CC}		2	5	5	µA
Deep Power-Down Current **(S25FL132K / S25FL164K)**	I_{CC2}	CS# = V_{CC}, V_{IN} = GND or V_{CC}		2	8	10	µA
Current: Read Single / Dual / Quad 1 MHz (4.4.1)	I_{CC3}	SCK = 0.1 V_{CC} / 0.9 V_{CC} SO = Open		4 / 5 / 6	6 / 7.5 / 9	6 / 7.5 / 9	mA
Current: Read Single / Dual / Quad 33 MHz (4.4.1)	I_{CC3}	SCK = 0.1 V_{CC} / 0.9 V_{CC} SO = Open		6 / 7 / 8	9 / 10.5 / 12	9 / 10.5 / 12	mA
Current: Read Single / Dual / Quad 50 MHz (4.4.1)	I_{CC3}	SCK = 0.1 V_{CC} / 0.9 V_{CC} SO = Open		7 / 8 / 9	10 / 12 / 13.5	10 / 12 / 13.5	mA
Current: Read Single / Dual / Quad 108 MHz (4.4.1)	I_{CC3}	SCK = 0.1 V_{CC} / 0.9 V_{CC} SO = Open		12 / 14 / 16	18 / 22 / 25	18 / 22 / 25	mA
Current: Write Status Registers	I_{CC4}	CS# = V_{CC}		8	12	12	mA
Current Page Program	I_{CC5}	CS# = V_{CC}		20	25	25	mA
Current Sector / Block Erase	I_{CC6}	CS# = V_{CC}		20	25	25	mA
Current Chip Erase	I_{CC7}	CS# = V_{CC}		20	25	25	mA
Input Low Voltage **(S25FL116K)**	V_{IL}		-0.5		V_{CC} x 0.2	V_{CC} x 0.2	V
Input Low Voltage **(S25FL132K / S25FL164K)**	V_{IL}		-0.5		V_{CC} x 0.3	V_{CC} x 0.3	V
Input High Voltage	V_{IH}		V_{CC} x 0.7		V_{CC} + 0.4	V_{CC} + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 100 µA	V_{SS}		0.2	0.2	V
		I_{OL} = 1.6 mA	V_{SS}		0.4	0.4	
Output High Voltage	V_{OH}	I_{OH} = –100 µA	V_{CC} – 0.2		V_{CC}	V_{CC}	V

Notes:
1. Tested on sample basis and specified through design and characterization data. T_A = 25°C, V_{CC} = 3V.

4.4.1 Active Power and Standby Power Modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is Low. When CS# is high, the device is disabled, but may still be in an Active Power mode until all program, erase, and write operations have completed. The device then goes into the Standby Power mode, and power consumption drops to I_{SB}.

4.5 AC Measurement Conditions

Figure 17. Test Setup

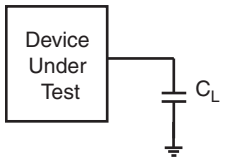
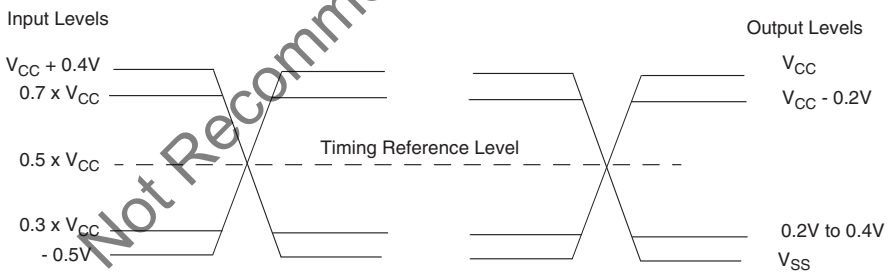


Table 9. AC Measurement Conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance		30	pF
TR, TF	Input Rise and Fall Times		2.4	ns
	Input Pulse Voltage	0.2 x V_{CC} to 0.8 V_{CC}		V
	Input Timing Ref Voltage	0.5 V_{CC}		V
	Output Timing Ref Voltage	0.5 V_{CC}		V

Notes:
1. *Output High-Z is defined as the point where data is no longer driven.*
2. *Input slew rate: 1.5 V/ns.*
3. *AC characteristics tables assume clock and data signals have the same slew rate (slope).*

Figure 18. Input, Output, and Timing Reference Levels



4.5.1 Capacitance Characteristics

Table 10. Capacitance

	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance (applies to SCK, CS#)	1 MHz		8	pF
C_{OUT}	Output Capacitance (applies to All I/O)	1 MHz		8	pF

Notes:
1. *Sampled, not 100% tested.*
2. *Test conditions TA = 25°C, f = 1.0 MHz.*

4.6 Power-Up Timing

Table 11. Power-Up Timing and Voltage Levels

Parameter	Symbol	Spec		Unit
		Min	Max	
V_{CC} (min) to CS# Low	t_{VSL}	10		µs
Power-Up to Write — Time Delay Before Write Command	t_{PUW}	10		ms
Write Inhibit Threshold Voltage	V_{WI}	2.4		V
Power-Down Time	t_{PD}	10.0		µs
V_{CC} Power-Down Reset Threshold Voltage	V_{CC} Low	1.0		V

Note:
1. These parameters are characterized only.

Figure 19. Power-Up Timing and Voltage Levels

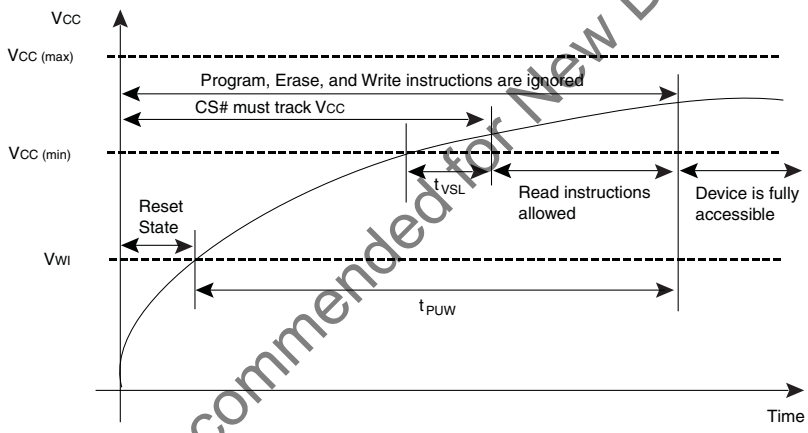
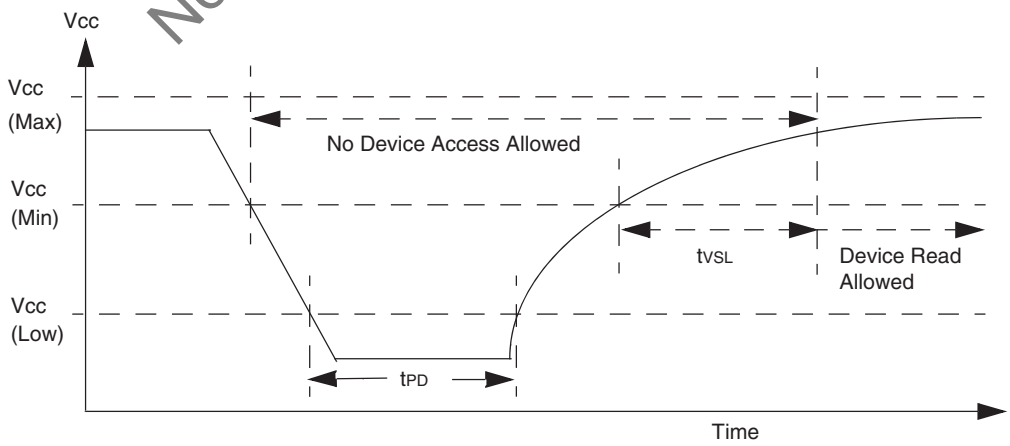


Figure 20. Power-Down and Voltage Drop



4.7 Power-On (Cold) Reset

The device executes a Power-On Reset (POR) process until a time delay of t_{PUW} has elapsed after the moment that V_{CC} rises above the V_{WI} threshold. See Figure 19 on page 24, Figure 20 on page 24, and Table on page 24. The device must not be selected (CS# to go high with V_{CC}) until after (t_{VSL}), i.e. no commands may be sent to the device until the end of t_{VSL}.

4.8 AC Electrical Characteristics

Table 12. AC Electrical Characteristics: –40°C to +85°C/105°C at 2.7V to 3.6V

Description	Symbol	Alt	Spec			Unit
			Min	Typ	Max	
Clock frequency for all SPI commands except for Read Data command (03h) and Fast Read command (0Bh) 2.7 V - 3.6V V_{CC}	F_R	f_C	D.C.		108	MHz
Clock frequency for Read Data command (03h)	f_R		D.C.		50	MHz
Clock frequency for all Fast Read commands SIO and MIO	f_{FR}		D.C.		108	MHz
Clock Period	P_{SCK}		9.25			ns
Clock High, Low Time for f_{FR}	t_{CLH}, t_{CLL} (1)	t_{CH}, t_{CL}	3.3			ns
Clock High, Low Time for F_R	t_{CLH}, t_{CLL} (1)	t_{CH}, t_{CL}	4.3			ns
Clock High, Low Time for f_R	t_{CRLH}, t_{CRLL} (1)	t_{CH}, t_{CL}	6			ns
Clock Rise Time	t_{CLCH} (2)	t_{CRT}	0.1			V/ns
Clock Fall Time	t_{CHCL} (2)	t_{CFT}	0.1			V/ns
CS# Active Setup Time relative to SCK	t_{SLCH}	t_{CSS}	5			ns
CS# Not Active Hold Time relative to SCK	t_{CHSL}	t_{CSH}	5			ns
Data In Setup Time	t_{DVCH}	t_{SU}	2			ns
Data In Hold Time	t_{CHDX}	t_{HD}	5			ns
CS# Active Hold Time relative to SCK	t_{CHSH}	t_{CSS}	5			ns
CS# Not Active Setup Time relative to SCK	t_{SHCH}	t_{CSH}	5			ns
CS# High Time		t_{CS}	10			ns
CS# Deselect Time (for Array Read -> Array Read)	t_{SHSL1}	t_{CS1}	7			ns
CS# Deselect Time (for Erase or Program -> Read Status Registers)	t_{SHSL2}	t_{CS2}	40			ns
Volatile Status Register Write Time			40			
CS# Deselect Time (for Erase or Program -> Suspend command)	t_{SHSL3}	t_{CS3}	130			ns
Output Disable Time	t_{SHQZ} (2)	t_{DIS}			7	ns
Clock Low to Output Valid, 30 pF, 2.7V - 3.6V	t_{CLQV1}	t_{V1}			7	ns
Clock Low to Output Valid, 15 pF, 2.7V - 3.6V	t_{CLQV1}	t_{V1}			6	ns
Clock Low to Output Valid (for Read ID commands) 2.7V - 3.6V	t_{CLQV2}	t_{V2}			8.5	ns
Output Hold Time	t_{CLQX}	t_{HO}	2			ns
HOLD# Active Setup Time relative to SCK	t_{HLCH}		5			ns
HOLD# Active Hold Time relative to SCK	t_{CHHH}		5			ns
HOLD# Not Active Setup Time relative to SCK	t_{HHCH}		5			ns