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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
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S25FL204K

4-Mbit 3.0 V SPI Flash Memory

Distinctive Features

- Single power supply operation
  - Full voltage range: 2.7 to 3.6V
- 4-Mbit Serial Flash
  - 4-Mbit/512 kbyte/2048 pages
  - 256 bytes per programmable page
  - Uniform 4-kbyte Sectors/64-kbyte Blocks
- Standard and Dual
  - Standard SPI: SCK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCK, CS#, SI/IO0, SO, WP#, HOLD#
  - Fast Read Dual Output instruction
  - Auto-increment Read capability
- High Performance
  - FAST READ (Serial): 85 MHz clock rate
  - DUAL OUTPUT READ: 85 MHz clock rate
- Low Power Consumption
  - 12 mA typical active current
  - 15 µA typical standby current
- Flexible Architecture with 4 kB Sectors
  - Sector Erase (4 kB)
  - Block Erase (64 kB)
  - Page Program up to 256 bytes
  - 100k erase/program cycles typical
  - 20-year data retention typical
- Software and Hardware Write Protection
  - Write Protect all or portion of memory via software
  - Enable/Disable protection with WP# pin
- High Performance Program/Erase Speed
  - Page program time: 1.5 ms typical
  - Sector erase time (4 kB): 50 ms typical
  - Block erase time (64 kB): 500 ms typical
  - Chip erase time: 3.5 seconds typical
- Package Options
  - 8-pin SOIC 150/208-mil
  - All Pb-free packages are RoHS compliant

General Description

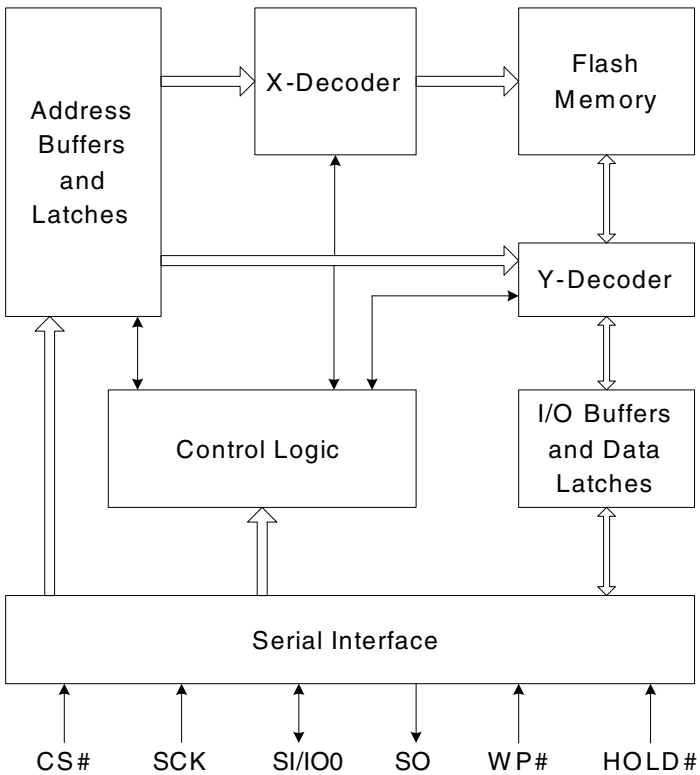
The S25FL204K (4-Mbit, 512-kbyte) Serial Flash memory, with advanced write protection mechanisms. TheS25FL204K supports the standard Serial Peripheral Interface (SPI), and a high performance Dual output using SPI pins: Serial Clock, Chip Select, Serial SI/IO0, SO, WP# and HOLD#. SPI clock frequencies of up to 85 MHz are supported along with a clock rate of 85 MHz for Dual Output Read.

The S25FL204K array is organized into 2048 programmable pages of 256 bytes each. Up to 256 bytes can be programmed at a time. Pages can be erased in groups of 16 (4 kB Sector Erase), groups of 256 (64 kB Block Erase) or the entire chip (Chip Erase). The S25FL204K has128 erasable sectors and 8 erasable blocks. The small 4 kB sectors allow for greater flexibility in applications that require data and parameter storage.

A Hold pin, Write Protect Pin and programmable write protection provide further control flexibility. Additionally, the S25FL204K device supports JEDEC standard manufacturer and device identification.

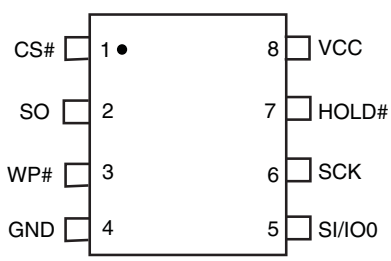
Table of Contents

1. Block Diagram



2. Connection Diagrams

Figure 2.1 8-pin SOIC (150/208 mil)



3. Signal Descriptions

Serial Data Input / Output (SI/IO0)
The SPI Serial Data Input/Output (SI/IO0) pin provides a means for instructions, addresses and data to be serially written to (shifted into) the device. Data is latched on the rising edge of the Serial Clock (SCK) input pin. The SI/IO0 pin is also used as an output pin when the Fast Read Dual Output instruction is executed.

Serial Data Output (SO)
The SPI Serial Data Output (SO) pin provides a means for data and status to be serially read from (shifted out of) the device. Data is shifted out on the falling edge of the Serial Clock (SCK) input pin.

Serial Clock (SCK)
The SPI Serial Clock Input (SCK) pin provides the timing for serial input and output operations. See *SPI Modes* on page 8.

Chip Select (CS#)
The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high the device is deselected and the Serial Data Output pins are at high impedance.

When deselected, the device's power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When CS# is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

HOLD (HOLD#)
The HOLD# pin allows the device to be paused while it is actively selected. When HOLD# is brought low, while CS# is low, the SO pin will be at high impedance and signals on the SI and SCK pins will be ignored (don't care). The HOLD# function can be useful when multiple devices are sharing the same SPI signals.

Write Protect (WP#)
The Write Protect (WP#) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP0, BP1 and BP2, BP3) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected.

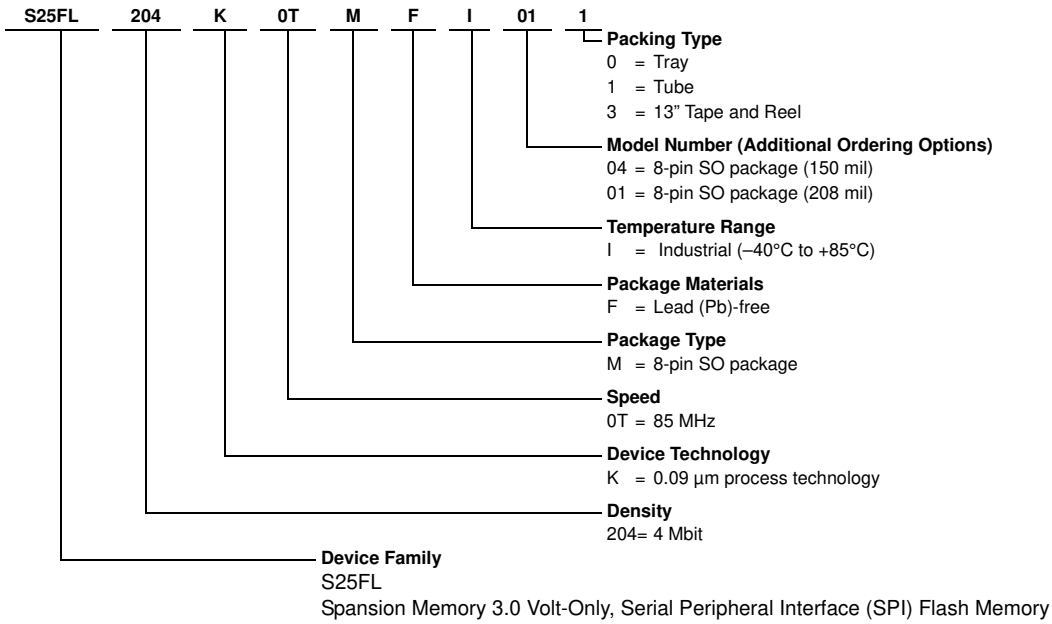
Table 3.1 Pin Descriptions

Symbol	Pin Name
SCK	Serial Clock Input
SI/IO0	Serial Data Input / Output (1)
SO	Serial Data Output
CS#	Chip Enable
WP#	Write Protect
HOLD#	Hold Input
VCC	Supply Voltage (2.7-3.6V)
GND	Ground

Note:
1. SI/IO0 output is used for Dual Output Read instruction.

4. Ordering Information

The ordering part number is formed by a valid combination of the following:



4.1 Valid Combinations

Table 4.1 lists the valid combinations configurations planned to be supported in volume for this device.

Table 4.1 S25FL204K Valid Combinations

S25FL204K Valid Combinations					
Base Ordering Part Number	**Speed Option**	**Package and Temperature**	**Model Number**	**Packing Type**	**Package Marking**
S25FL204K	0T	MFI	01, 04	0, 1, 3	FL204KIF

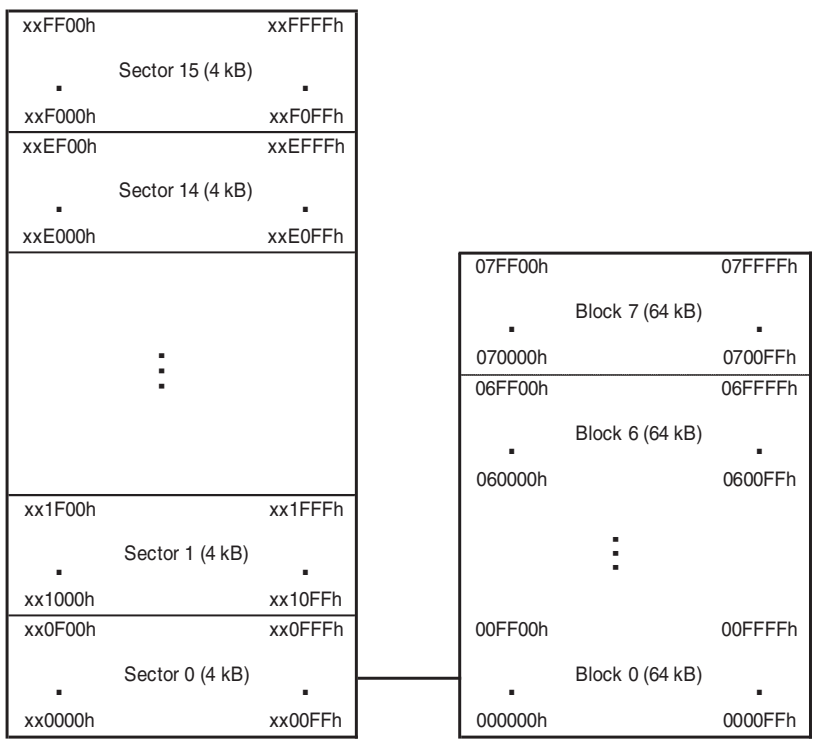
5. Memory Organizations

The memory is organized as:

- 524,288 bytes
- Uniform Sector Architecture
  - 8 blocks of 64 kB
  - 128 sectors of 4 kB
- 2,048 pages (256 bytes each)

Each page can be individually programmed (bits are programmed from 1 to 0). The device is Sector, Block or Chip Erasable but not Page Erasable.

Figure 5.1 Memory Organization



6. Functional Description

6.1 SPI Modes

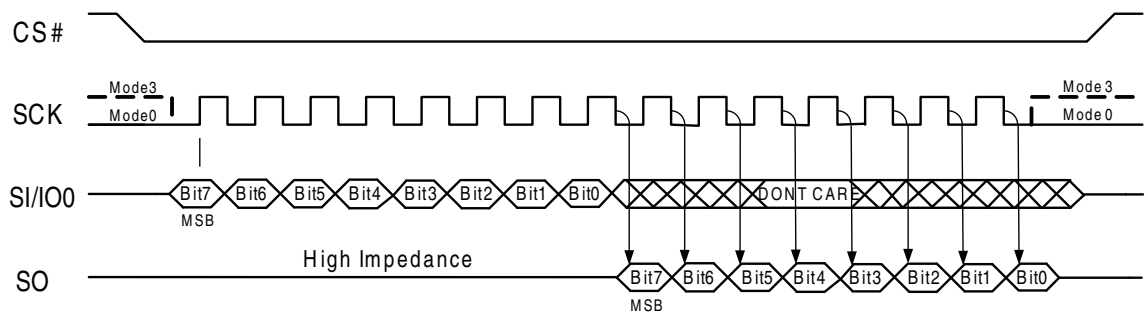
The S25FL204K device can be driven by an embedded microcontroller (bus master) in either of the two following clocking modes.

- Mode 0 with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0
- Mode 3 with CPOL = 1 and, CPHA = 1

For these two modes, input data into the device is always latched in on the rising edge of the SCK signal and the output data is always available from the falling edge of the SCK clock signal. The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

- SCK will stay at logic low state with CPOL = 0, CPHA = 0
- SCK will stay at logic high state with CPOL = 1, CPHA = 1

Figure 6.1 SPI Modes



6.2 Dual Output SPI

The S25FL204K supports Dual Output Operation when using the “Fast Read with Dual Output” (3B hex) command. This feature allows data to be transferred from the Serial Flash at twice the rate possible with the standard SPI. This command can be used to quickly download code from Flash to RAM upon Power-up (Code-shadowing) or for applications that cache code-segments to RAM for execution.

The Dual Output feature simply allows the SPI data input pin (SI) to also serve as an output during this command. All other operations use the standard SPI interface with single signal. The host keeps CS# low and HOLD# high. The Write Protect (WP#) signal is ignored. The memory drives data on the SI/IO0 and SO signals during the dual output cycles. The next interface state continues to be Dual Output Cycle until the host returns CS# to high ending the command.

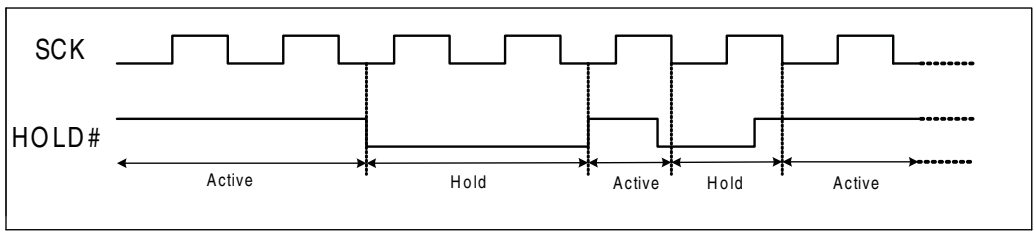
6.3 Hold Function

The Hold (HOLD#) signal is used to pause any serial communications with the S25FL204K device without deselecting the device or stopping the serial clock. To enter the Hold condition, the device must be selected by driving the CS# input to the logic low state. It is recommended that the user keep the CS# input low state during the entire duration of the Hold condition. This is to ensure that the state of the interface logic remains unchanged from the moment of entering the Hold condition. If the CS# input is driven to the logic high state while the device is in the Hold condition, the interface logic of the device will be reset. To restart communication with the device, it is necessary to drive HOLD# to the logic high state while driving the CS# signal into the logic low state. This prevents the device from going back into the Hold condition.

The Hold condition starts on the falling edge of the Hold (HOLD#) signal, provided that this coincides with SCK being at the logic low state. If the falling edge does not coincide with the SCK signal being at the logic low state, the Hold condition starts whenever the SCK signal reaches the logic low state. Taking the HOLD# signal to the logic low state does not terminate any Write, Program or Erase operation that is currently in progress.

During the Hold condition, SO is in high impedance and both the SI and SCK input are Don't Care. The Hold condition ends on the rising edge of the Hold (HOLD#) signal, provided that this coincides with the SCK signal being at the logic low state. If the rising edge does not coincide with the SCK signal being at the logic low state, the Hold condition ends whenever the SCK signal reaches the logic low state.

Figure 6.2 Hold Condition Waveform



6.4 Status Register

The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions

Table 6.1 Status Register Bit Locations

R7	R6	R5	R4	R3	R2	R1	R0
SRP	REV	BP3	BP2	BP1	BP0	WEL	WIP

- **Write in Progress (WIP)** is a read only bit in the status register (R0) which indicates whether the device is performing a program, write, erase operation, or any other operation, during which a new operation command will be ignored. When the WIP bit is set to 1, the device is busy performing an operation. When the bit is cleared to 0, no operation is in progress.
- **Write Enable Latch (WEL)** is a read only bit in the status register (R1) that must be set to 1 to enable program, write, or erase operations as a means to provide protection against inadvertent changes to memory or register values. The Write Enable (WREN) command execution sets the Write Enable Latch to a 1 to allow any program, erase, or write commands to execute afterwards. The Write Disable (WRDI) command can be used to set the Write Enable Latch to a 0 to prevent all program, erase, and write commands from execution. The WEL bit is cleared to 0 at the end of any successful program, write, or erase operation. After a power down/power up sequence, hardware reset, or software reset, the Write Enable Latch is set to a 0.
- **Block Protect Bits (BP3, BP2, BP1, BP0)** are non-volatile read/write bits in the status register (R5, R4, R3, and R2) that define the main flash array area to be software protected against program and erase commands. When one or more of the BP bits is set to 1, the relevant memory area is protected against program and erase. The Chip Erase (CE) command can be executed only when the BP bits are cleared to 0's. See Table 7.1 on page 10 for a description of how the BP bit values select the memory array area protected. The factory default setting for all the BP bits is 0, which implies that none of array is protected.
- **Reserved Bits (REV)**, Status register bit location R6 is reserved for future use. Current devices will read 0 for this bit location. It is recommended to mask out the reserved bit when testing the Status Register. Doing this will ensure compatibility with future devices.
- **The Status Register Protect (SRP)** bit is a non-volatile read/write bit in status register (R7) that can be used in conjunction with the Write Protect (WP#) pin to disable writes to status register. When the SRP bit is set to a 0 state (factory default) the WP# pin has no control over status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the WP# pin is low. When the WP# pin is high the Write Status Register instruction is allowed.

7. Write Protection

Some basic protection against unintended changes to stored data is provided and controlled purely by the hardware design. These protection mechanisms in the S25FL204K device are described below:

- Power-On Reset and an internal timer (t_{PUW}) can provide protection against inadvertent changes while the power supply is outside the operating specification.
- Program, Erase and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:

– Power-up

– Write Disable (WRDI) instruction completion or Write Status Register (WRSR) instruction completion or Page Program (PP) instruction completion or Sector Erase (SE) instruction completion or Block Erase (BE) instruction completion or Chip Erase (CE) instruction completion

- The Block Protect (BP3, BP2, BP1, and BP0) bits allow part of the memory to be configured as read-only. This is the Software Protected Mode (SPM).
- The Write Protect (WP#) signal allows the Block Protect (BP3, BP2, BP1, BP0) bits and Status Register Protect (SRP) bit to be protected. This is the Hardware Protected Mode (HPM).
- In addition to the low power consumption feature, the Deep Power-down mode offers extra software protection from inadvertent Write, Program and Erase instructions, as all instructions are ignored except one particular instruction (the Release from Deep Power-down instruction).

Table 7.1 Protected Area Sizes Block Organization — S25FL204K

Status Bit				Protect Blocks
BP3	BP2	BP1	BP0	
0	0	0	0	0 (None)
0	0	0	1	1 (1 block, block 7th)
0	0	1	0	2 (2 blocks, block 6th~7th)
0	0	1	1	3 (4 blocks, block 4th~7th)
0	1	0	0	4 (8 blocks, all)
0	1	0	1	5 (8 blocks, all)
0	1	1	0	6 (8 blocks, all)
0	1	1	1	7 (8 blocks, all)
1	0	0	0	8 none
1	0	0	1	9 (126 sectors, sector 0th~125th)
1	0	1	0	10 (124 sectors, sector 0th~123rd)
1	0	1	1	11 (120 sectors, sector 0th~119th)
1	1	0	0	12 (112 sectors, sector 0th~111th)
1	1	0	1	13 (96 sectors, sectors 0th~95th)
1	1	1	0	14 (64 sectors, sectors 0th~63rd)
1	1	1	1	15 (128 sectors, all)

7.1 Page Programming

To program one data byte, two instructions are required: Write Enable (WREN), which is one byte, and a Page Program (PP) sequence, which consists of four bytes plus data. This is followed by the internal Program cycle (of duration t_{PP}). To spread this overhead, the Page Program (PP) instruction allows up to 256 bytes to be programmed at a time (changing bits from 1 to 0), provided that they lie in consecutive addresses on the same page of memory.

7.2 Sector Erase, Block Erase, and Chip Erase

The Page Program (PP) instruction allows bits to be reset from 1 to 0. Before this can be applied, the bytes of memory need to have been erased to all 1s (FFh). This can be achieved a sector at a time, using the Sector Erase (SE) instruction, a block at a time using the Block Erase (BE) instruction or throughout the entire memory, using the Chip Erase (CE) instruction. This starts an internal Erase cycle (of duration t_{SE}, t_{BE}, or t_{CE}). The Erase instruction must be preceded by a Write Enable (WREN) instruction.

7.3 Polling During a Write, Program, or Erase Cycle

A further improvement in the time to Write Status Register (WRSR), Program (PP) or Erase (SE, BE, or CE) can be achieved by not waiting for the worst case delay (t_W, t_{PP}, t_{SE}, t_{BE}, or t_{CE}). The Write In Progress (WIP) bit is provided in the Status Register so that the application program can monitor its value, polling it to establish when the previous Write cycle, Program cycle or Erase cycle is complete.

7.4 Active Power, Stand-by Power, and Deep Power-Down Modes

When Chip Select (CS#) is Low, the device is enabled, and in the Active Power mode. When Chip Select (CS#) is High, the device is disabled, but could remain in the Active Power mode until all internal cycles have completed (Program, Erase, Write Status Register). The device then goes into the Standby Power mode. The device consumption drops to I_{CC1}.

The Deep Power-down mode is entered when the specific instruction (the Enter Deep Power-down Mode (DP) instruction) is executed with the device consumption at I_{CC2}. The device remains in this mode until another specific instruction (the Release from Deep Power-down Mode and Read Device ID (RDI) instruction) is executed.

All other instructions are ignored while the device is in the Deep Power-down mode. This can be used as an extra software protection mechanism, when the device is not in active use, to protect the device from inadvertent Write, Program or Erase instructions.

8. Commands

The command set of the S25FL204K consists of fifteen basic instructions that are fully controlled through the SPI bus (see Table 8.1). The host system must shift all commands, addresses, and data in and out of the device, beginning with the most significant bit. On the first rising edge of SCK after CS# is driven low, the device accepts the one-byte command on SI (all commands are one byte long), most significant bit first. Each successive bit is latched on the rising edge of SCK.

Every command sequence begins with a one-byte command code. The command may be followed by address, data, both, or nothing, depending on the command. CS# must be driven high after the last bit of the command sequence has been written. All commands that write, program or erase require that CS# be driven high at a byte boundary, otherwise the command is not executed. Since a byte is composed of eight bits, CS# must therefore be driven high when the number of clock pulses after CS# is driven low is an exact multiple of eight. The device ignores any attempt to access the memory array during a Write Registers, program, or erase operation, and continues the operation uninterrupted.

Table 8.1 Command Set

Command Name	Byte1 Code	Byte2	Byte3	Byte4	Byte5	Byte6	N-bytes
Write Enable	06h						
write Disable	04h						
Read Status Register	05h	(S7-S0) (1)					(Note 2)

Table 8.1 Command Set

Command Name	Byte1 Code	Byte2	Byte3	Byte4	Byte5	Byte6	N-bytes
Write Status Register	01h	S7-S0					
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	continuous
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(Next byte) continuous
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	dummy	I/O= (D6, D4, D2, D0) O= (D7, D5, D3, D1)	(One byte per 4 clocks, continuous)
Page Program	02h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	Up to 256 bytes
Block Erase (64 kB)	D8h	A23-A16	A15-A8	A7-A0			
Sector Erase (4 kB)	20h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/60h						
Power-down	B9h						
Release Power-down / Device ID	ABh	dummy	dummy	dummy	(ID7-ID0) (4)		
Manufacturer / Device ID (3)	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	
JEDEC ID	9Fh	(M7-M0) manufacturer	(ID15-ID8) Memory Type	(ID7-ID0) Capacity			

Notes:

1. *Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data being read from the device on the SO pin.*
2. *The Status Register contents will repeat continuously until CS# terminates the instruction.*
3. *See Table 8.2, Manufacturer and Device Identification on page 12 for Device ID information.*
4. *The Device ID will repeat continuously until CS# terminates the instruction.*

Table 8.2 Manufacturer and Device Identification

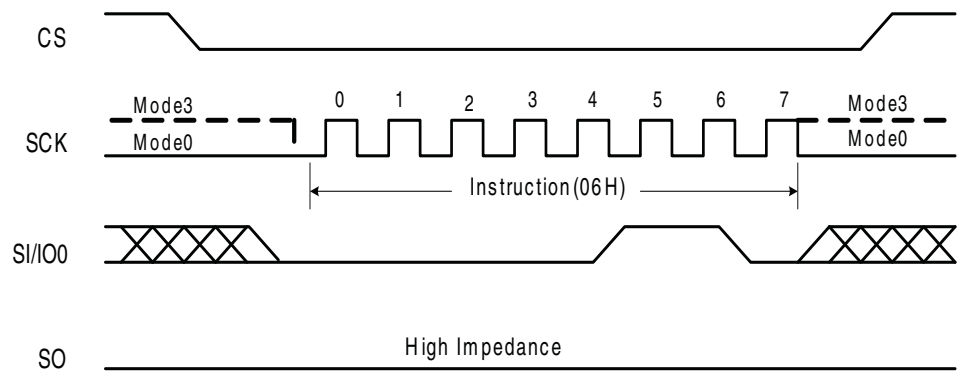
OP Code	(M7-M0)	(ID15-ID0)	(ID7-ID0)
ABh			12h
90h	01h		12h
9Fh	01h	4013h	

8.1 Write Enable (06h)

The Write Enable command (Figure 8.1) sets the Write Enable Latch (WEL) bit in the Status Register to a 1, which enables the device to accept a Write Status Register, program, or erase command.

The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase, and Write Status Register command. The host system must first drive CS# low, write the WREN command, and then drive CS# high.

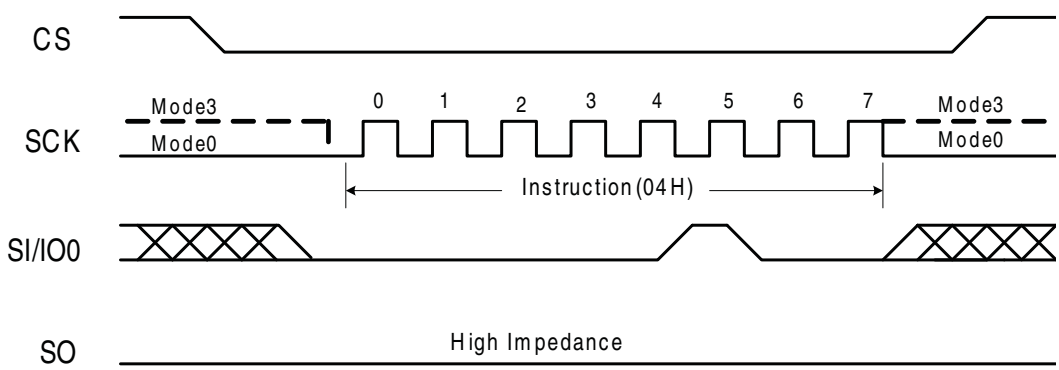
Figure 8.1 Write Enable Command Sequence



8.2 Write Disable (04h)

The Write Disable command (Figure 8.2) resets the Write Enable Latch (WEL) bit to a 0, which disables the device from accepting a write, program or erase command. The host system must first drive CS# low, write the WRDI command, and then drive CS# high. The WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase, and Chip Erase commands.

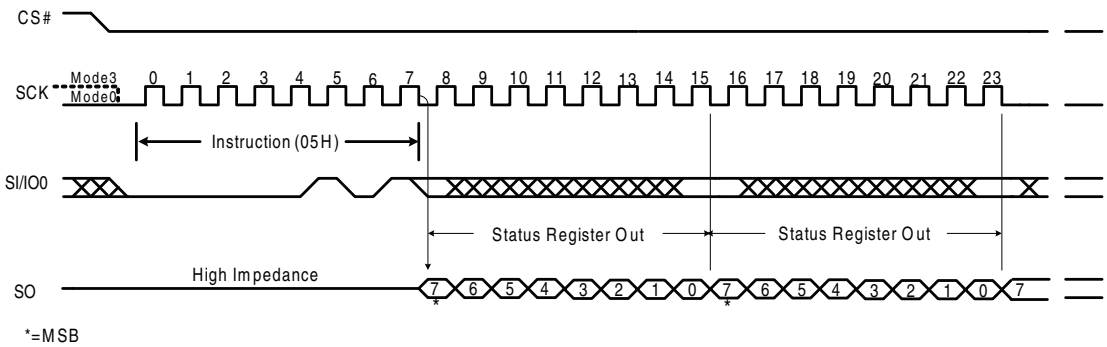
Figure 8.2 Write Disable Command Sequence



8.3 Read Status Register (05h)

The Read Status Register (RDSR) command outputs the state of the Status Register bits. The RDSR command may be written at any time, even while a program, erase, or Write Registers operation is in progress. The host system should check the Write In Progress (WIP) bit before sending a new command to the device if an operation is already in progress. Figure 8.3 shows the RDSR command sequence, which also shows that it is possible to read the Status Register continuously until CS# is driven high. (See Section 6.4, *Status Register* on page 9).

Figure 8.3 Read Status Register Command Sequence



8.4 Write Status Register (01h)

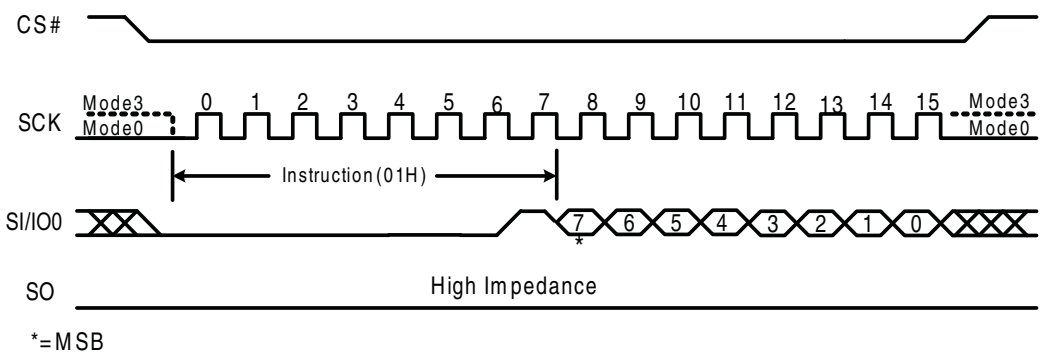
The Write Status Register command allows the Status Register to be written. A Write Enable command must previously have been executed for the device to accept the Write Status Register command (Status Register bit WEL must equal 1). Once write enabled, the command is entered by driving CS# low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in Figure 8.4. The Status Register bits are shown in Table 6.1 on page 9 and described in Section 6.4, *Status Register* on page 9.

Only non-volatile Status Register bits SRP, BP3, BP2, BP1, and BP0 (bits 7, 5, 4, 3, and 2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register command.

The CS# chip select input pin must be driven to the logic high state after the eighth bit of data has been latched in. If not, the Write Status Register command is not executed. As soon as the CS# chip select input pin is driven to the logic high state, the self-timed Write Status Register cycle is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is a 1 during the self-timed Write Status Register cycle, and is a 0 when it is completed. When the Write Status Register cycle is completed, the Write Enable Latch (WEL) is set to a 0.

The Write Status Register command allows the Block Protect bits (BP3, BP2, BP1, and BP0) to be set for protecting all, a portion, or none of the memory from erase and program commands. Protected areas become read-only (see Table 7.1 on page 10). The Write Status Register command also allows the Status Register Protect bit (SRP) to be set. This bit is used in conjunction with the Write Protect (WP#) pin to disable writes to the status register. When the SRP bit is set to a 0 state (factory default) the WP# pin has no control over the status register. When the SRP pin is set to a 1, the Write Status Register command is locked out while the WP# pin is low. When the WP# pin is high the Write Status Register command is allowed.

Figure 8.4 Write Status Register Command Sequence

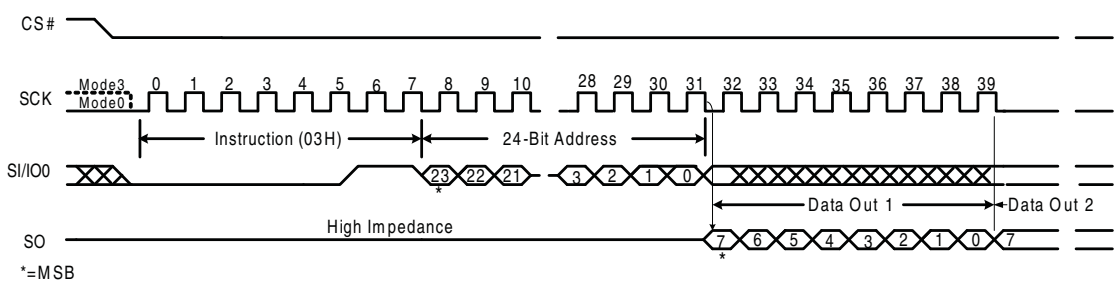


8.5 Read Data (03h)

The Read Data command allows one more data bytes to be sequentially read from the memory. The command is initiated by driving the CS# pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the SI/IO0 pin. The code and address bits are latched on the rising edge of the SCK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of SCK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues. The command is completed by driving CS# high.

The Read Data command sequence is shown in Figure 8.5. If a Read Data command is issued while an Erase, Program or Write cycle is in process (WIP=1) the command is ignored and will not have any effects on the current cycle. The Read Data command allows clock rates from D.C. to a maximum of f_R. See *AC Characteristics* on page 28.

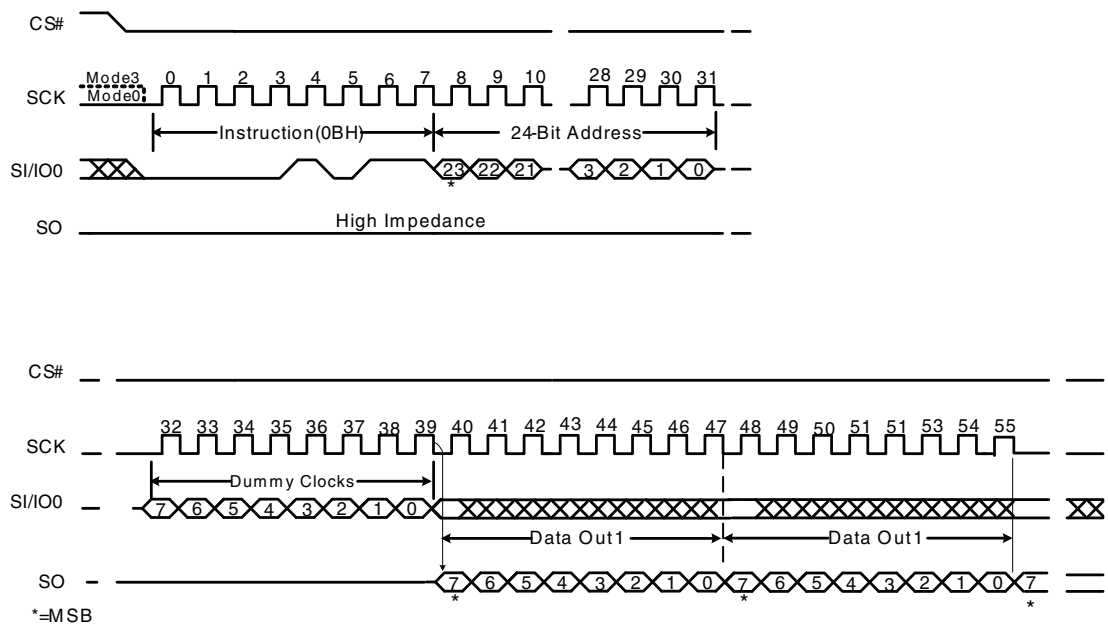
Figure 8.5 Read Data Command Sequence



8.6 Fast Read (0Bh)

The Fast Read command is similar to the Read Data command except that it can operate at higher frequency than the traditional Read Data command. See *AC Characteristics* on page 28. This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 8.6. The dummy clocks allow the device’s internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the SI pin is a “don’t care”.

Figure 8.6 Fast Read Command Sequence

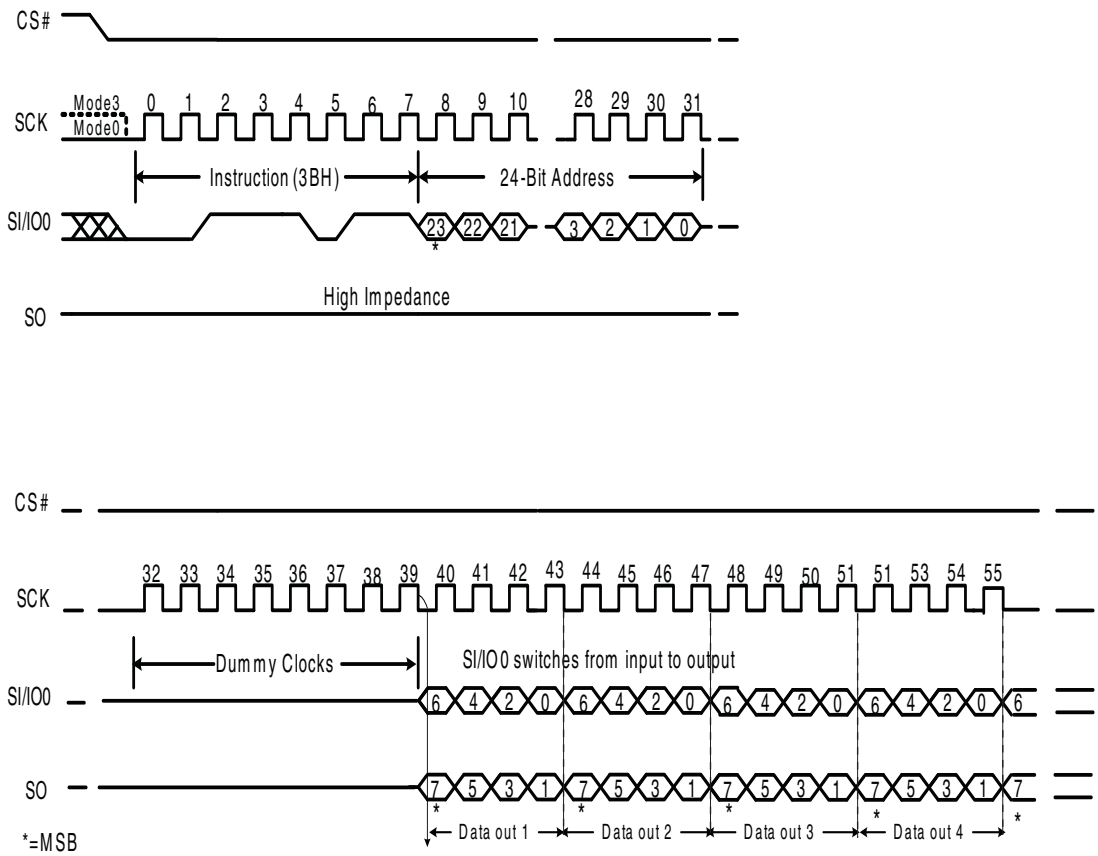


8.7 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) command is similar to the standard Fast Read (0Bh) command except that data is output on two pins, SO and SI/IO0, instead of just SO. This allows data to be transferred from the S25FL204K at twice the rate of standard SPI devices. The Fast Read Dual Output command is ideal for quickly downloading code from the SPI flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read command, the Fast Read Dual Output command can operate at higher frequencies than the traditional Read Data command. See *AC Characteristics* on page 28. This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in Figure 8.7. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the SI/IO0 pin should be high-impedance prior to the falling edge of the first data out clock.

Figure 8.7 Fast Read Dual Output Command Sequence



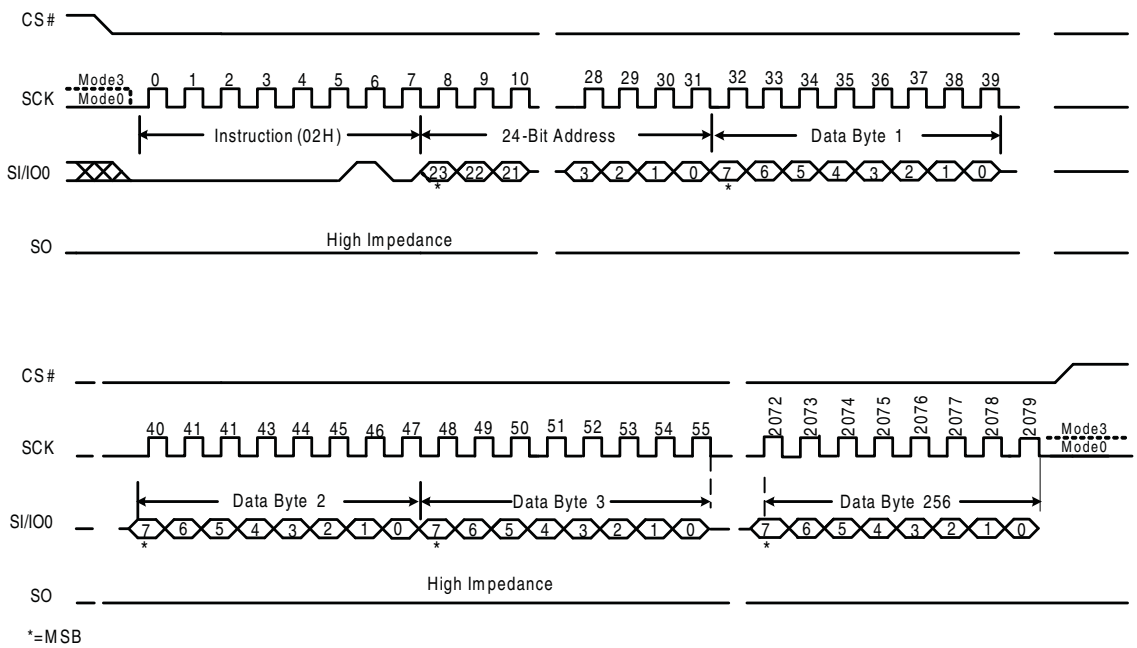
8.8 Page Program (PP) (02h)

The Page Program command allows up to 256 bytes of data to be programmed at previously erased to all 1s (FFh) memory locations. A Write Enable command must be executed before the device will accept the Page Program command (Status Register bit WEL must equal 1). The command is initiated by driving the CS# pin low then shifting the command code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the SI/IO0 pin. The CS# pin must be held low for the entire length of the command while data is being sent to the device. The Page Program command sequence is shown in Figure 8.8.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceed the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase commands, the CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program command will not be executed. After CS# is driven high, the self-timed Page Program command will commence for a time duration of t_{PP}. See *AC Characteristics* on page 28. While the Page Program cycle is in progress, the Read Status Register command may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program command will not be executed if the addressed page is protected by the Block Protect (BP3, BP2, BP1, and BP0) bits (see Table 7.1 on page 10).

Figure 8.8 Page Program Command Sequence

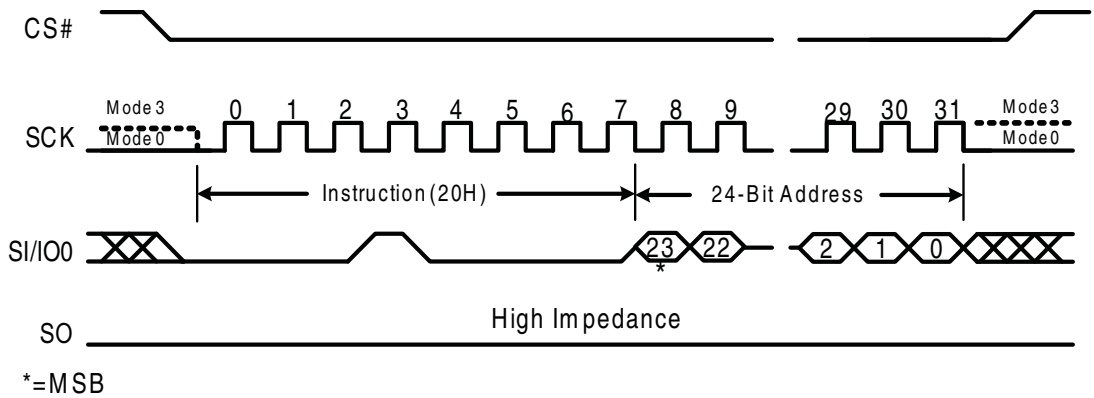


8.9 Sector Erase (SE) (20h)

The Sector Erase command sets all bits in the addressed 4 kB sector to 1 (all bytes are FFh). Before the Sector Erase command can be accepted by the device, a Write Enable command must be issued and decoded by the device, which sets the Write Enable Latch bit in the Status Register to enable any write operations. The command is initiated by driving the CS# pin low and shifting the command code “20h” followed by a 24-bit sector address (A23-A0). The Sector Erase command sequence is shown in Figure 8.9.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase command will not be executed. After CS# is driven high, the self-timed Sector Erase command will commence for a time duration of t_{SE}. See *AC Characteristics* on page 28. While the Sector Erase cycle is in progress, the Read Status Register command may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase command will not be executed if the addressed page is protected by the Block Protect (BP3, BP2, BP1, and BP0) bits (see Table 7.1 on page 10).

Figure 8.9 Sector Erase Command Sequence

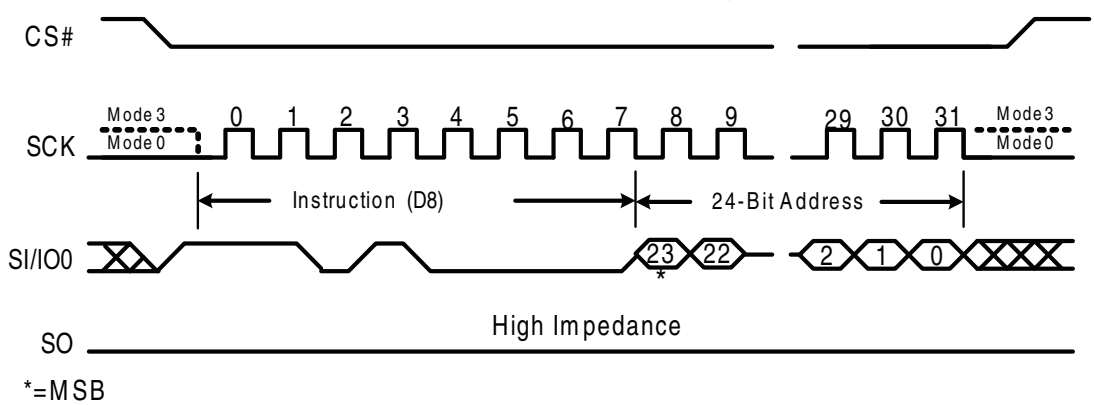


8.10 Block Erase (BE) (D8h)

The Block Erase command sets all bits in the addressed 64 kB block to 1 (all bytes are FFh). Before the BE command can be accepted by the device, a Write Enable command must be issued and decoded by the device, which sets the Write Enable Latch in the Status Register to enable any write operations. The command is initiated by driving the CS# pin low and shifting the command code “D8h” followed a 24-bit block address (A23-A0). The Block Erase command sequence is shown in Figure 8.10.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase command will not be executed. After CS# is driven high, the self-timed Block Erase command will commence for a time duration of t_{BE}. See *AC Characteristics* on page 28. While the Block Erase cycle is in progress, the Read Status Register command may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase command will not be executed if the addressed page is protected by the Block Protect (BP3, BP2, BP1, and BP0) bits (see Table 7.1 on page 10).

Figure 8.10 Block Erase Command Sequence

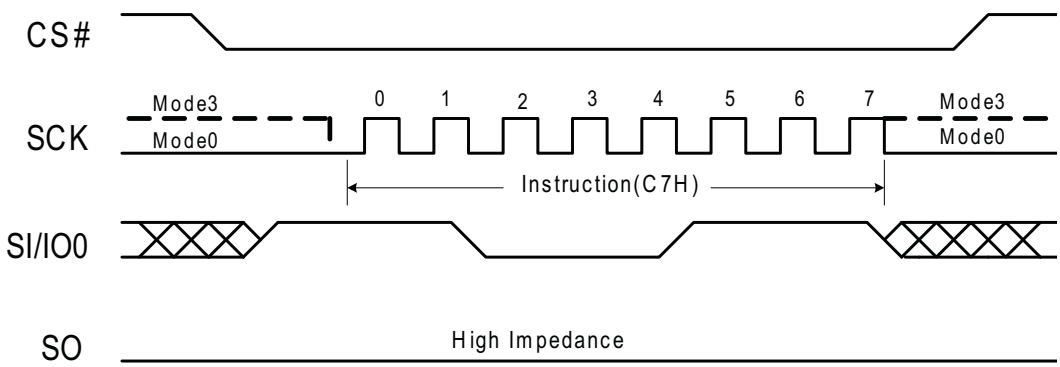


8.11 Chip Erase (CE) (C7h)

The Chip Erase command sets all bits to 1 (all bytes are FFh) inside the entire flash memory array. Before the CE command can be accepted by the device, a Write Enable command must be issued and decoded by the device, which sets the Write Enable Latch in the Status Register to enable any write operations. The command is initiated by driving the CS# pin low and shifting the command code “C7h”. The Chip Erase command sequence is shown in Figure 8.11.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase command will not be executed. After CS# is driven high, the self-timed Chip Erase command will commence for a time duration of t_{CE}. See *AC Characteristics* on page 28. While the Chip Erase cycle is in progress, the Read Status Register command may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other commands again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase command will not be executed if any page is protected by the Block Protect (BP3, BP2, BP1, and BP0) bits (see Table 7.1 on page 10).

Figure 8.11 Chip Erase Command Sequence

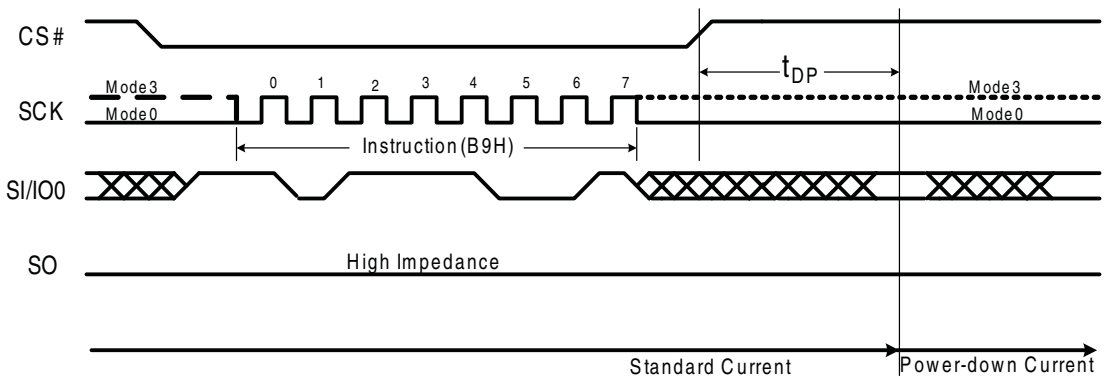


8.12 Deep Power-down (DP) (B9h)

The Deep Power-Down (DP) command provides the lowest power consumption mode of the device. It is intended for periods when the device is not in active use, and ignores all commands except for the Release from Deep Power-Down (RES) command. The lower power consumption makes the Deep Power-down command especially useful for battery powered applications (See I_{CC1} and I_{CC2} in *DC Characteristics* on page 27.) The command is initiated by driving the CS# pin low and shifting the command code “B9h” as shown in Figure 8.12.

The CS# pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power-down command will not be executed. After CS# is driven high, the power-down state will enter within the time duration of t_{DP} (See *AC Characteristics* on page 28.) While in the power-down state only the Release from Power-down / Device ID command, which restores the device to normal operation, will be recognized. All other commands are ignored. This includes the Read Status Register command, which is always available during normal operation. The Deep Power-down mode therefore provides the maximum data protection against unintended write operations. Deep Power-down mode automatically terminates when power is removed, and the device always powers up in the standard standby mode. The device rejects any Deep Power-down command issued while it is executing a program, erase, or Write Registers operation, and continues the operation uninterrupted.

Figure 8.12 Deep Power-down Command Sequence



8.13 Release Deep Power-down / Device ID (ABh)

The Release from Deep Power-down / Device ID command is a multi-purpose command. The device requires the Release from Deep Power-down command to exit the Deep Power-down mode. When the device is in the Deep Power-down mode, all commands except Release from Deep Power-down command are ignored. In addition, the ABh command can also be used to read the device's 8-bit electronic Device ID.

When used only to release the device from the power-down state, the command is issued by driving the CS# pin low, shifting the command code “ABh” and driving CS# high as shown in Figure 8.13. After the time duration of t_{RES1} (See *AC Characteristics* on page 28.) the device will resume normal operation and other commands will be accepted. The CS# pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the Deep power-down state, the command is initiated by driving the CS# pin low and shifting the command code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of SCK with most significant bit (MSB) first as shown in Figure 8.14. The Device ID value for the S25FL204K is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When used to release the device from the Deep power-down state and obtain the Device ID, the command is the same as previously described, and shown in Figure 8.14, except that after CS# is driven high it must remain high for a time duration of t_{RES2} (See *AC Characteristics* on page 28.). After this time duration the device will resume normal operation and other commands will be accepted. If the Release from Deep Power-down / Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equals 1) the command is ignored and will not have any effects on the current cycle.

Figure 8.13 Release Deep Power-down Command

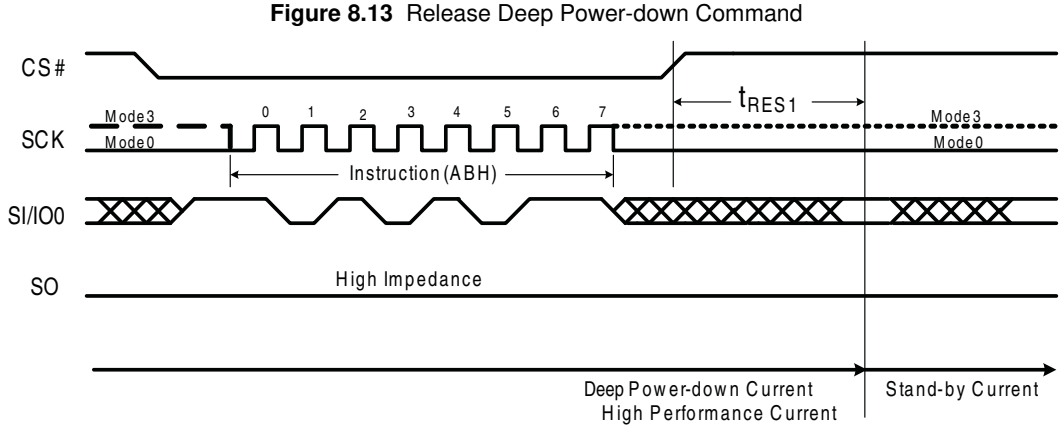
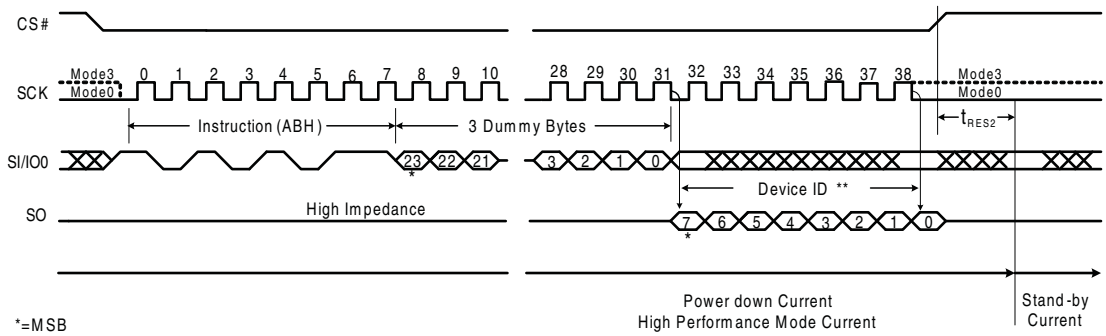


Figure 8.14 Release Deep Power-down / Device ID Command Sequence

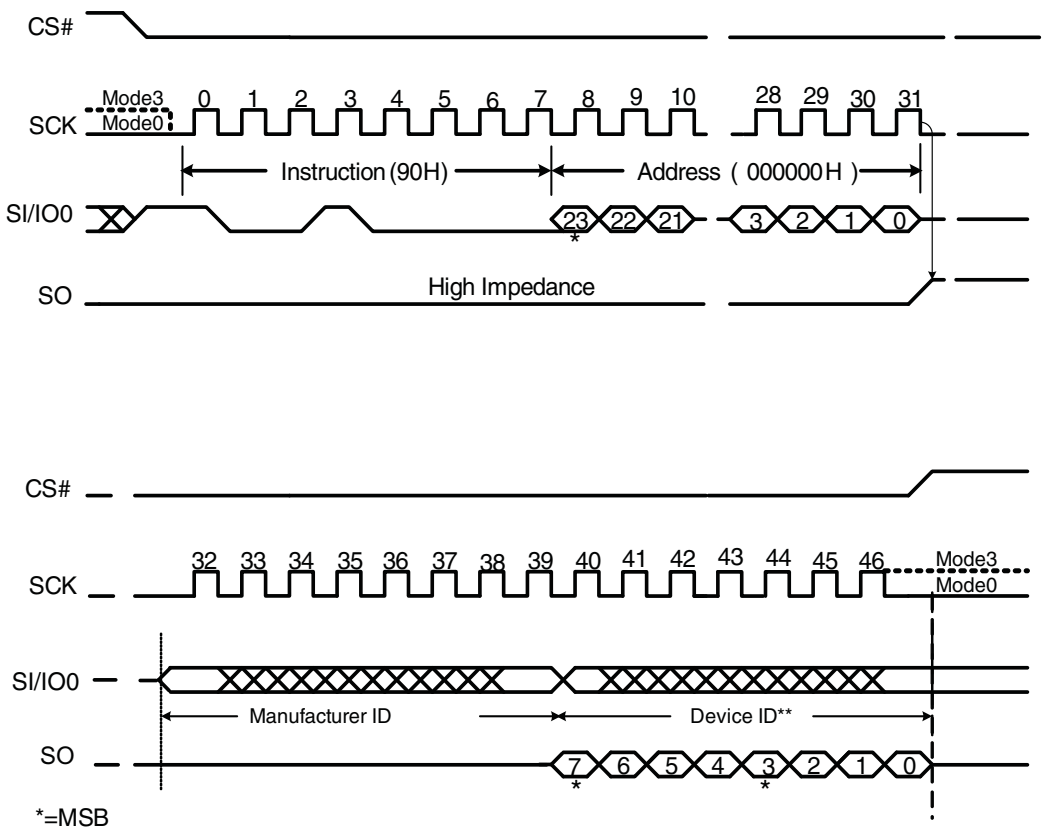


8.14 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID command is an alternative to the Release from Deep Power-down /Device ID command that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID command is very similar to the Release from Deep Power-down / Device ID command. The command is initiated by driving the CS# pin low and shifting the command code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Spansion (01h) and the Device ID are shifted out on the falling edge of SCK with most significant bit (MSB) first as shown in Figure 8.15. The Device ID values for the S25FL204K are listed in Table 8.2 on page 12. If the 24-bit address is initially set to 000001h the Device ID will be read first, followed by the Manufacturer ID.

Figure 8.15 Read Manufacturer / Device ID Command Sequence

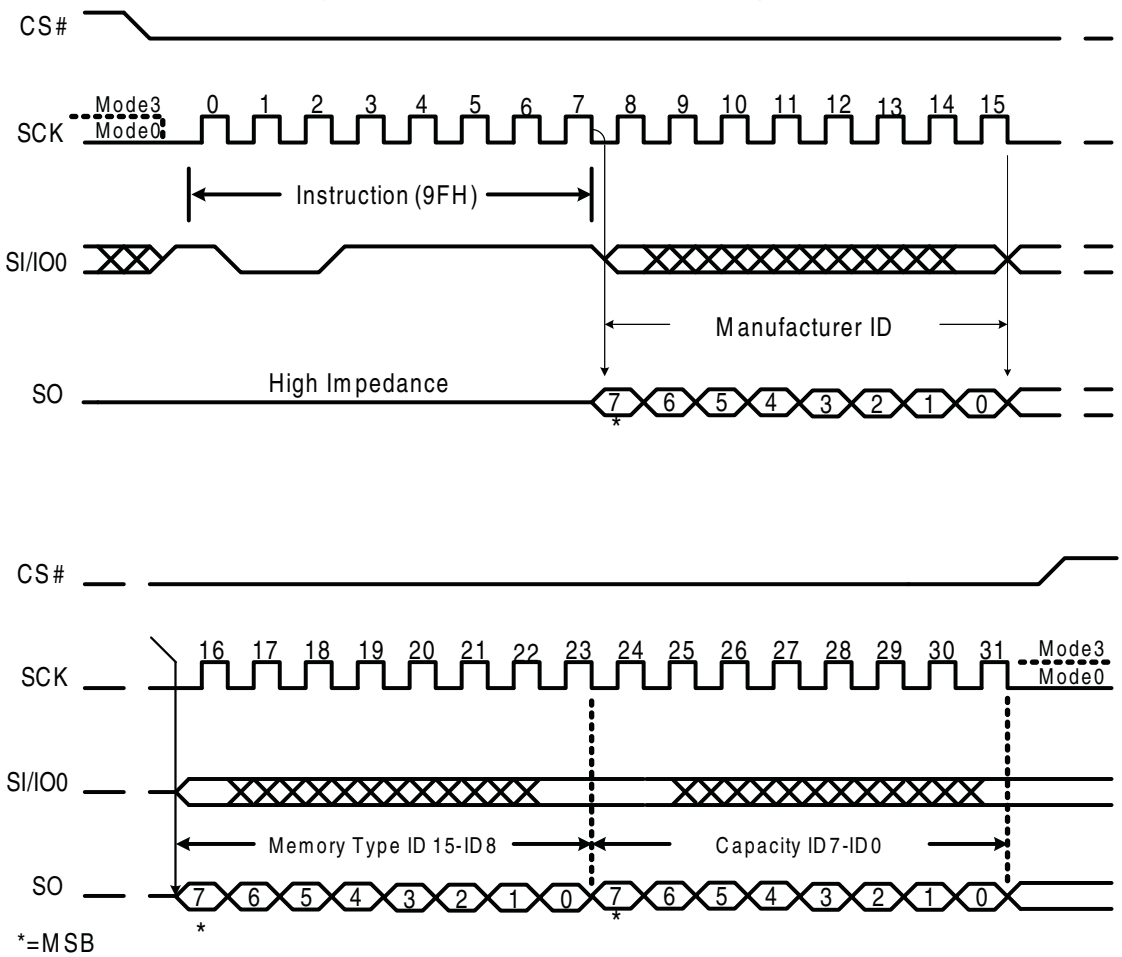


8.15 Read Identification (RDID) (9Fh)

For compatibility reasons, the S25FL204K provides several commands to electronically determine the identity of the device. The Read JEDEC ID command is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003.

The command is initiated by driving the CS# pin low and shifting the command code “9Fh”. The JEDEC assigned Manufacturer ID byte for Spansion (01h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of SCK with most significant bit (MSB) first as shown in Figure 8.16. For memory type and capacity values refer to Table 8.2, *Manufacturer and Device Identification* on page 12.

Figure 8.16 Read JEDEC ID Command Sequence



9. Electrical Specifications

9.1 Power-up Timing

Figure 9.1 Power-up Timing

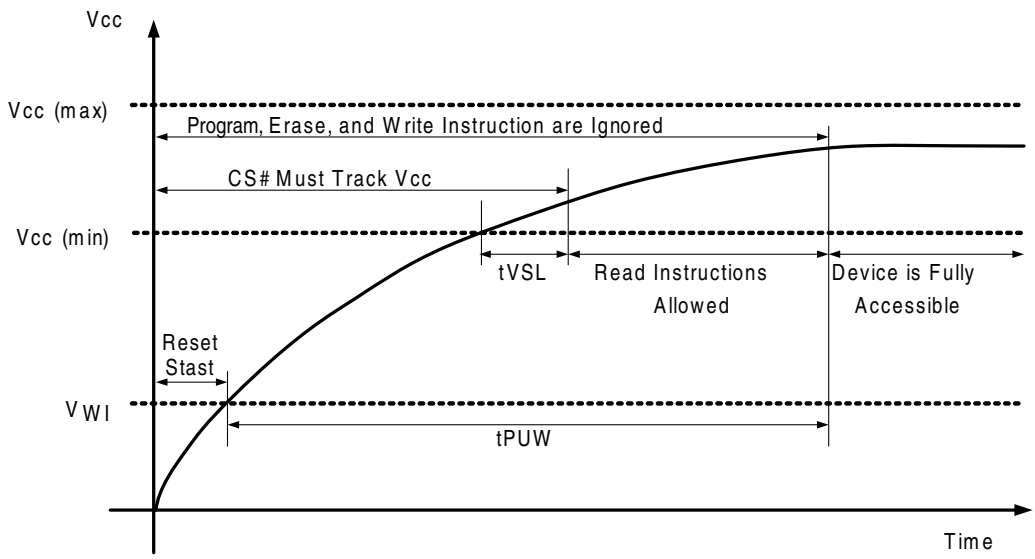


Table 9.1 Power-up Voltage and Timing

Parameter	Symbol	Type		Unit
		Min	Max	
V_{CC} (min) to CS# Low	t_{VSL} (1)	10		µs
Time Delay Before Write Instruction	t_{PUW} (1)	1	10	ms
Write Inhibit Threshold Voltage	V_{WI} (1)	1	2	V

Notes:

1. *The parameters are characterized only.*
2. *V_{CC} (max.) is 3.6V and V_{CC} (min.) is 2.7V.*