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S25FS512S

512 Mbit, 1.8 V Serial Peripheral Interface with Multi-I/O Flash

Features

- Serial Peripheral Interface (SPI) with Multi-I/O
  - SPI Clock polarity and phase modes 0 and 3
  - Double Data Rate (DDR) option
  - Extended Addressing – 24 or 32-bit address options
  - Serial Command subset and footprint compatible with S25FL-A, S25FL-K, S25FL-P, and S25FL-S SPI families
  - Multi I/O Command subset and footprint compatible with S25FL-P, and S25FL-S SPI families
- Read
  - Commands: Normal, Fast, Dual I/O, Quad I/O, DDR Quad I/O
  - Modes: Burst Wrap, Continuous (XIP), QPI
  - Serial Flash Discoverable Parameters (SFDP) and Common Flash Interface (CFI), for configuration information.
- Program
  - 256 or 512 Bytes Page Programming buffer
  - Program suspend and resume
  - Automatic Error Checking and Correction (ECC) – internal hardware ECC with single bit error correction
- Erase
  - Hybrid sector option
    - Physical set of eight 4-kbytes sectors and one 224-kbytes sector at the top or bottom of address space with all remaining sectors of 256 kbytes
  - Uniform sector option
    - Uniform 256 kbyte blocks
  - Erase suspend and resume
  - Erase status evaluation
  - 100,000 Program-Erase Cycles, minimum
  - 20 Year Data Retention, minimum
- Security Features
  - One Time Program (OTP) array of 1024 bytes
  - Block Protection:
    - Status Register bits to control protection against program or erase of a contiguous range of sectors.
    - Hardware and software control options
  - Advanced Sector Protection (ASP)
    - Individual sector protection controlled by boot code or password
    - Option for password control of read access
- Technology
  - Cypress 65-nm MirrorBit® Technology with Eclipse™ Architecture
- Supply Voltage
  - 1.7 V to 2.0 V
- Temperature Range / Grade
  - Industrial (–40 °C to +85 °C)
  - Industrial Plus (–40 °C to +105 °C)
  - Automotive, AEC-Q100 Grade 3 (–40 °C to +85 °C)
  - Automotive, AEC-Q100 Grade 2 (–40 °C to +105 °C)
  - Automotive, AEC-Q100 Grade 1 (–40 °C to +125 °C)
- Packages (all Pb-free)
  - 16-lead SOIC 300 mil (SO3016)
  - WSON 6 × 8 mm (WNH008)
  - BGA-24 6 × 8 mm
    - 5 × 5 ball (FAB024) footprint
  - Known Good Die and Known Tested Die

Performance Summary

Maximum Read Rates

Command	Clock Rate (MHz)	Mbytes/s
Read	50	6.25
Fast Read	133	16.5
Dual Read	133	33
Quad Read	133	66
DDR Quad I/O Read	80	80

Typical Program and Erase Rates

Operation	kbytes/s
Page Programming (256-bytes page buffer)	712
Page Programming (512-bytes page buffer)	1080
4-kbytes Physical Sector Erase (Hybrid Sector Option)	28
256-kbytes Sector Erase (Uniform Logical Sector Option)	250

Typical Current Consumption, –40°C to +85°C

Operation	Current (mA)
Serial Read 50 MHz	10
Serial Read 133 MHz	20
Quad Read 133 MHz	60
Quad DDR Read 80 MHz	70
Program	60
Erase	60
Standby	0.07
Deep Power Down	0.006

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1. Overview

1.1 General Description

The Cypress S25FS512S device is a flash non-volatile memory product using:

- MirrorBit technology — that stores two data bits in each memory array transistor
- Eclipse architecture — that dramatically improves program and erase performance
- 65 nm process lithography

The S25FS512S connects to a host system via a Serial Peripheral Interface (SPI). Traditional SPI single bit serial input and output (Single I/O or SIO) is supported as well as optional two-bit (Dual I/O or DIO) and four-bit wide Quad I/O (QIO) or Quad Peripheral Interface (QPI) serial commands. This multiple-width interface is called SPI Multi-I/O or MIO. In addition, there are Double Data Rate (DDR) read commands for QIO and QPI that transfer address and read data on both edges of the clock.

The FS-S Eclipse architecture features a Page Programming Buffer that allows up to 512 bytes to be programmed in one operation, resulting in faster effective programming and erase than prior generation SPI program or erase algorithms.

Executing code directly from flash memory is often called Execute-In-Place or XIP. By using S25FS512S devices at the higher clock rates supported, with Quad or DDR-Quad commands, the instruction read transfer rate can match or exceed traditional parallel interface, asynchronous, NOR flash memories, while reducing signal count dramatically.

The S25FS512S products offer high densities coupled with the flexibility and fast performance required by a variety of mobile or embedded applications. They are an excellent solution for systems with limited space, signal connections, and power. They are ideal for code shadowing to RAM, executing code directly (XIP), and storing reprogrammable data.

1.2 Migration Notes

1.2.1 Features Comparison

The S25FS512S is command subset and footprint compatible with prior generation FL-S, FL-K, and FL-P families. However, the power supply and interface voltages are nominal 1.8V.

Table 1.1 Cypress SPI Families Comparison

Parameter	FS-S	FL-S	FL-K	FL-P
Technology Node	65 nm	65 nm	90 nm	90 nm
Architecture	MirrorBit® Eclipse™	MirrorBit® Eclipse™	Floating Gate	MirrorBit®
Density	128 Mb - 512 Mb	128 Mb - 1 Gb	4 Mb - 128 Mb	32 Mb - 256 Mb
Bus Width	x1, x2, x4	x1, x2, x4	x1, x2, x4	x1, x2, x4
Supply Voltage	1.7V - 2.0V	2.7V - 3.6V / 1.65V - 3.6V V_{IO}	2.7V - 3.6V	2.7V - 3.6V
Normal Read Speed (SDR)	6 MB/s (50 MHz)	6 MB/s (50 MHz)	6 MB/s (50 MHz)	5 MB/s (40 MHz)
Fast Read Speed (SDR)	16.5 MB/s (133 MHz)	17 MB/s (133 MHz)	13 MB/s (104 MHz)	13 MB/s (104 MHz)
Dual Read Speed (SDR)	33 MB/s (133 MHz)	26 MB/s (104 MHz)	26 MB/s (104 MHz)	20 MB/s (80 MHz)
Quad Read Speed (SDR)	66 MB/s (133 MHz)	52 MB/s (104 MHz)	52 MB/s (104 MHz)	40 MB/s (80 MHz)
Quad Read Speed (DDR)	80 MB/s (80 MHz)	80 MB/s (80 MHz)	—	—
Program Buffer Size	256B / 512B	256B / 512B	256B	256B
Erase Sector Size	64 kB / 256 kB	64 kB / 256 kB	4 kB / 32 kB / 64 kB	64 kB / 256 kB
Parameter Sector Size	4 kB (option)	4 kB (option)	4 kB	4 kB
Sector Erase Rate (typ.)	500 kB/s	500 kB/s	136 kB/s (4 kB) 437 kB/s (64 kB)	130 kB/s

Table 1.1 Cypress SPI Families Comparison (Continued)

Parameter	FS-S	FL-S	FL-K	FL-P
Page Programming Rate (typ.)	0.71 MB/s (256B) 1.08 MB/s (512B)	1.2 MB/s (256B) 1.5 MB/s (512B)	365 kB/s	170 kB/s
OTP	1024B	1024B	768B (3x256B)	506B
Advanced Sector Protection	Yes	Yes	No	No
Auto Boot Mode	No	Yes	No	No
Erase Suspend/Resume	Yes	Yes	Yes	No
Program Suspend/ Resume	Yes	Yes	Yes	No
Deep Power-Down Mode	Yes	No	Yes	Yes
Operating Temperature	-40°C to +85°C / +105°C	-40°C to +85°C / +105°C / +125°C	-40°C to +85°C	-40°C to +85°C / +105°C

Notes:

1. *256B program page option only for 128 Mb and 256 Mb density FL-S devices.*
2. *FL-P column indicates FL129P MIO SPI device (for 128 Mb density), FL128P does not support MIO, OTP, or 4 kB sectors.*
3. *64-kB sector erase option only for 128 Mb / 256 Mb density FL-P, FL-S, and FS-S devices.*
4. *FL-K family devices can erase 4-kB sectors in groups of 32 kB or 64 kB.*
5. *Only 128 Mb/256 Mb density FL-S devices have 4-kB parameter sector option.*
6. *512 Mb / 1 Gb FL-S devices support 256 kB-sector only.*
7. *The FS512 device does not support 64 kB-sectors.*
8. *Refer to individual product data sheets for further details.*

1.2.2 Known Differences from Prior Generations

1.2.2.1 Error Reporting

FL-K and FL-P memories either do not have error status bits or do not set them if program or erase is attempted on a protected sector. The FS-S and FL-S families do have error reporting status bits for program and erase operations. These can be set when there is an internal failure to program or erase, or when there is an attempt to program or erase a protected sector. In these cases the program or erase operation did not complete as requested by the command. The P_ERR or E_ERR bits and the WIP bit will be set to and remain 1 in SR1V. The clear status register command must be sent to clear the errors and return the device to standby state.

1.2.2.2 Secure Silicon Region (OTP)

The FS-S size and format (address map) of the One Time Program area is different from FL-K and FL-P generations. The method for protecting each portion of the OTP area is different. For additional details see *Secure Silicon Region (OTP)* *on page 65*.

1.2.2.3 Configuration Register Freeze Bit

The Configuration Register 1 Freeze Bit CR1V[0], locks the state of the Block Protection bits (SR1NV[4:2] and SR1V[4:2]), TBPARM_O bit (CR1NV[2]), and TBPROT_O bit (CR1NV[5]), as in prior generations. In the FS-S and FL-S families the Freeze Bit also locks the state of the Configuration Register 1 BPNV_O bit (CR1NV[3]), and the Secure Silicon Region (OTP) area.

1.2.2.4 Sector Erase Commands

The command for erasing a 4-kbytes sector is supported only for use on 4-kbytes parameter sectors at the top or bottom of the FS-S device address space.

The command for erasing an 8-kbyte area (two 4-kbytes sectors) is not supported.

The command for erasing a 32-kbyte area (eight 4-kbytes sectors) is not supported.

The 64 kbytes erase command is not supported for the 512 Mbits density FS-S device.

1.2.2.5 Deep Power-Down

A Deep Power-Down (DPD) function is supported in the FS-S family devices.

1.2.2.6 WRR Single Register Write

In some legacy SPI devices, a Write Registers (WRR) command with only one data byte would update Status Register 1 and clear some bits in Configuration Register 1, including the Quad mode bit. This could result in unintended exit from Quad mode. The S25FS512S only updates Status Register 1 when a single data byte is provided. The Configuration Register 1 is not modified in this case.

1.2.2.7 Hold Input Not Supported

In some legacy SPI devices, the IO3 input has an alternate function as a HOLD# input used to pause information transfer without stopping the serial clock. This function is not supported in the FS-S family.

1.2.2.8 Separate Reset Input Not Supported

In some legacy SPI devices, a separate hardware RESET# input is supported in packages having more than eight connections. The FS-S family does not support a separate RESET# input. The FS-S family provides an alternate function for the IO3 input as a RESET# input. When the CS# signal is high and the IO3 / RESET feature is enabled, the IO3 / RESET# input is used to initiate a hardware reset when the input goes low.

1.2.2.9 Other Legacy Commands Not Supported

- Autoboot Related Commands
- Bank Address Related Commands
- Dual Output Read
- Quad Output Read
- Quad Page Program (QPP) — replaced by Page Program in QPI mode
- DDR Fast Read
- DDR Dual I/O Read

1.2.2.10 New Features

The FS-S family introduces new features to Cypress SPI category memories:

- Single 1.8V power supply for core and I/O voltage.
- Configurable initial read latency (number of dummy cycles) for faster initial access time or higher clock rate read commands.
- QPI (QPI, 4-4-4) read mode in which all transfers are 4 bits wide, including instructions.
- JEDEC JESD216 standard, Serial Flash Discoverable Parameters (SFDP) that provide device feature and configuration information.
- Evaluate Erase Status command to determine if the last erase operation on a sector completed successfully. This command can be used to detect incomplete erase due to power loss or other causes. This command can be helpful to Flash File System software in file system recovery after a power loss.
- Advanced Sector Protection (ASP) Permanent Protection. A bit is added to the ASP register to provide the option to make protection of the Persistent Protection Bits (PPB) permanent. Also, when one of the two ASP protection modes is selected, all OTP configuration bits in all registers are protected from further programming so that all OTP configuration settings are made permanent. The OTP address space is not protected by the selection of an ASP protection mode. The Freeze bit (CR1V[0]) may be used to protect the OTP Address Space.

1.3 Glossary

BCD	**Binary Coded Decimal**. A value in which each 4-bit nibble represents a decimal numeral.
Command	All information transferred between the host system and memory during one period while CS# is low. This includes the instruction (sometimes called an operation code or opcode) and any required address, mode bits, latency cycles, or data.
DDP	**Dual Die Package**. Two die stacked within the same package to increase the memory capacity of a single package. Often also referred to as a Multi-Chip Package (MCP).
DDR	**Double Data Rate**. When input and output are latched on every edge of SCK.
ECC	ECC Unit = 16 byte aligned and length data groups in the main Flash array and OTP array, each of which has its own hidden ECC syndrome to enable error correction on each group.
Flash	The name for a type of Electrical Erase Programmable Read Only Memory (EEPROM) that erases large blocks of memory bits in parallel, making the erase operation much faster than early EEPROM.
High	A signal voltage level $\geq V_{IH}$ or a logic level representing a binary one (‘1’).
Instruction	8-bit code indicating the function to be performed by a command (sometimes called an operation code or opcode). The instruction is always the first 8 bits transferred from host system to the memory in any command.
Low	A signal voltage level $\leq V_{IL}$ or a logic level representing a binary zero (‘0’).
LSB	**Least Significant Bit**. Generally the right most bit, with the lowest order of magnitude value, within a group of bits of a register or data value.
MSB	**Most Significant Bit**. Generally the left most bit, with the highest order of magnitude value, within a group of bits of a register or data value.
N/A	**Not Applicable**. A value is not relevant to situation described.
Non-Volatile	No power is needed to maintain data stored in the memory.
OPN	**Ordering Part Number**. The alphanumeric string specifying the memory device type, density, package, factory non-volatile configuration, etc. used to select the desired device.
Page	512-byte or 256-byte aligned and length group of data. The size assigned for a page depends on the Ordering Part Number.
PCB	Printed Circuit Board.
Register Bit References	Format: Register_name[bit_number] or Register_name[bit_range_MSB: bit_range_LSB].
SDR	**Single Data Rate**. When input is latched on the rising edge and output on the falling edge of SCK.
Sector	Erase unit size; depending on device model and sector location this may be 4 kbytes, 64 kbytes, or 256 kbytes.
Write	An operation that changes data within volatile or non-volatile registers bits or non-volatile flash memory. When changing non-volatile data, an erase and reprogramming of any unchanged non-volatile data is done, as part of the operation, such that the non-volatile data is modified by the write operation, in the same way that volatile data is modified – as a single operation. The non-volatile data appears to the host system to be updated by the single write command, without the need for separate commands for erase and reprogram of adjacent, but unaffected data.

1.4 Other Resources

1.4.1 Cypress Flash Memory Roadmap

www.cypress.com/product-roadmaps/cypress-flash-memory-roadmap

1.4.2 Links to Software

www.cypress.com/software-and-drivers-cypress-flash-memory

1.4.3 Links to Application Notes

www.cypress.com/appnotes

Hardware Interface

Serial Peripheral Interface with Multiple Input / Output (SPI-MIO)

Many memory devices connect to their host system with separate parallel control, address, and data signals that require a large number of signal connections and larger package size. The large number of connections increase power consumption due to so many signals switching and the larger package increases cost.

The S25FS512S reduces the number of signals for connection to the host system by serially transferring all control, address, and data information over 4 to 6 signals. This reduces the cost of the memory package, reduces signal switching power, and either reduces the host connection count or frees host connectors for use in providing other features.

The S25FS512S uses the industry standard single bit Serial Peripheral Interface (SPI) and also supports optional extension commands for two-bit (Dual) and four-bit (Quad) wide serial transfers. This multiple width interface is called SPI Multi-I/O or SPI-MIO.

2. Signal Descriptions

2.1 Input/Output Summary

Table 2.1 Signal List

Signal Name	Type	Description
SCK	Input	**Serial Clock.**
CS#	Input	**Chip Select.**
SI / IO0	I/O	**Serial Input** for single bit data commands or IO0 for Dual or Quad commands.
SO / IO1	I/O	**Serial Output** for single bit data commands. IO1 for Dual or Quad commands.
WP# / IO2	I/O	**Write Protect** when not in Quad mode (CR1V[1] = 0 and SR1NV[7] = 1). See Table 7.5, Register Descriptions on page 48. **IO2** when in Quad mode (CR1V[1] = 1). The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands or write protection. If write protection is enabled by SR1NV[7] = 1 and CR1V[1] = 0, the host system is required to drive WP# high or low during a WRR or WRAR command.
IO3 / RESET#	I/O	**IO3** in Quad-I/O mode, when Configuration Register 1 QUAD bit, CR1V[1] =1, and CS# is low. **RESET#** when enabled by CR2V[5]=1 and not in Quad-I/O mode, CR1V[1] = 0, or when enabled in quad mode, CR1V[1] = 1 and CS# is high. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad commands or RESET#.
V_{DD}	Supply	**Power Supply.**
V_{SS}	Supply	**Ground.**
NC	Unused	**Not Connected.** No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB). However, any signal connected to an NC must not have voltage levels higher than V_{DD}.
RFU	Reserved	**Reserved for Future Use.** No device internal signal is currently connected to the package connector but there is potential future use of the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.
DNU	Reserved	**Do Not Use.** A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to this connection.

2.2 Multiple Input / Output (MIO)

Traditional SPI single bit wide commands (Single or SIO) send information from the host to the memory only on the Serial Input (SI) signal. Data may be sent back to the host serially on the Serial Output (SO) signal.

Dual or Quad Input / Output (I/O) commands send instructions to the memory only on the SI / IO0 signal. Address or data is sent from the host to the memory as bit pairs on IO0 and IO1 or four-bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or four-bit (nibble) groups on IO0, IO1, IO2, and IO3.

QPI mode transfers all instructions, address, and data from the host to the memory as four-bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as four-bit (nibble) groups on IO0, IO1, IO2, and IO3.

2.3 Serial Clock (SCK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCK signal. Data output changes after the falling edge of SCK, in SDR commands, and after every edge in DDR commands.

2.4 Chip Select (CS#)

The chip select signal indicates when a command is transferring information to or from the device and the other signals are relevant for the memory device.

When the CS# signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. The device will be in the Standby Power mode, unless an internal embedded operation is in progress. An embedded operation is indicated by the Status Register 1 Write-In-Progress bit (SR1V[1]) set to 1, until the operation is completed. Some example embedded operations are: Program, Erase, or Write Registers (WRR) operations.

Driving the CS# input to the logic low state enables the device, placing it in the Active Power mode. After Power-up, a falling edge on CS# is required prior to the start of any command.

2.5 Serial Input (SI) / IO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal.

SI becomes IO0 — an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

2.6 Serial Output (SO) / IO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal.

SO becomes IO1 — an input and output during Dual and Quad commands for receiving addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

2.7 Write Protect (WP#) / IO2

When WP# is driven Low (V_{IL}), during a WRR or WRAR command and while the Status Register Write Disable (SRWD_NV) bit of Status Register 1 (SR1NV[7]) is set to a 1, it is not possible to write to Status Register 1 or Configuration Register 1 related registers. In this situation, a WRR command is ignored, a WRAR command selecting SR1NV, SR1V, CR1NV, or CR1V is ignored, and no error is set.

This prevents any alteration of the Block Protection settings. As a consequence, all the data bytes in the memory area that are protected by the Block Protection feature are also hardware protected against data modification if WP# is Low during a WRR or WRAR command with SRWD_NV set to 1.

The WP# function is not available when the Quad mode is enabled (CR1V[1]=1). The WP# function is replaced by IO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

WP# has an internal pull-up resistance; when unconnected, WP# is at V_{IH} and may be left unconnected in the host system if not used for Quad mode or protection.

2.8 IO3 / RESET#

IO3 is used for input and output during Quad mode (CR1V[1]=1) for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK, in SDR commands, and on every edge of SCK, in DDR commands).

The IO3 / RESET# signal may also be used to initiate the hardware reset function when the reset feature is enabled by writing Configuration Register 2 non-volatile bit 5 (CR2V[5]=1). The input is only treated as RESET# when the device is not in Quad-I/O mode, CR1V[1] = 0, or when CS# is high. When Quad I/O mode is in use, CR1V[1]=1, and the device is selected with CS# low, the IO3 / RESET# is used only as IO3 for information transfer. When CS# is high, the IO3 / RESET# is not in use for information transfer and is used as the RESET# input. By conditioning the reset operation on CS# high during Quad mode, the reset function remains available during Quad mode.

When the system enters a reset condition, the CS# signal must be driven high as part of the reset process and the IO3 / RESET# signal is driven low. When CS# goes high the IO3 / RESET# input transitions from being IO3 to being the RESET# input. The reset condition is then detected when CS# remains high and the IO3 / RESET# signal remains low for t_{RP}. If a reset is not intended, the system is required to actively drive IO3 / Reset# to high along with CS# being driven high at the end of a transfer of data to the memory. Following transfers of data to the host system, the memory will drive IO3 high during t_{CS}. This will ensure that IO3 / Reset is not left floating or being pulled slowly to high by the internal or an external passive pull-up. Thus, an unintended reset is not triggered by the IO3 / RESET# not being recognized as high before the end of t_{RP}.

The IO3 / RESET# signal is unused when the reset feature is disabled (CR2V[5]=0).

The IO3 / RESET# signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad mode or the reset function. The internal pull-up will hold IO3 / Reset high after the host system has actively driven the signal high and then stops driving the signal.

Note that IO3 / Reset# cannot be shared by more than one SPI-MIO memory if any of them are operating in Quad I/O mode as IO3 being driven to or from one selected memory may look like a reset signal to a second non-selected memory sharing the same IO3 / RESET# signal.

2.9 Voltage Supply (V_{DD})

V_{DD} is the voltage source for all device internal logic. It is the single voltage used for all device internal functions including read, program, and erase.

2.10 Supply and Signal Ground (V_{SS})

V_{SS} is the common voltage drain and ground reference for the device core, input signal receivers, and output drivers.

2.11 Not Connected (NC)

No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).

2.12 Reserved for Future Use (RFU)

No device internal signal is currently connected to the package connector but there is potential future use of the connector. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.

2.13 Do Not Use (DNU)

A device internal signal may be connected to the package connector. The connection may be used by Cypress for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.

2.14 Block Diagrams

Figure 2.1 Bus Master and Memory Devices on the SPI Bus — Single Bit Data Path

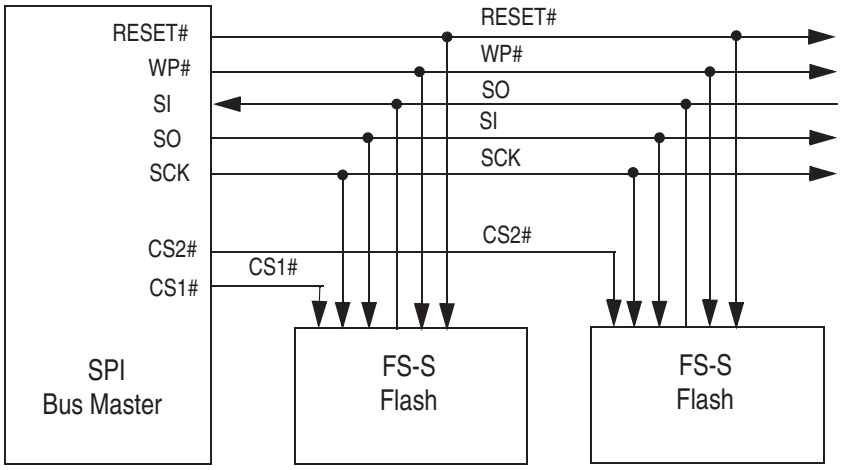


Figure 2.2 Bus Master and Memory Devices on the SPI Bus — Dual Bit Data Path

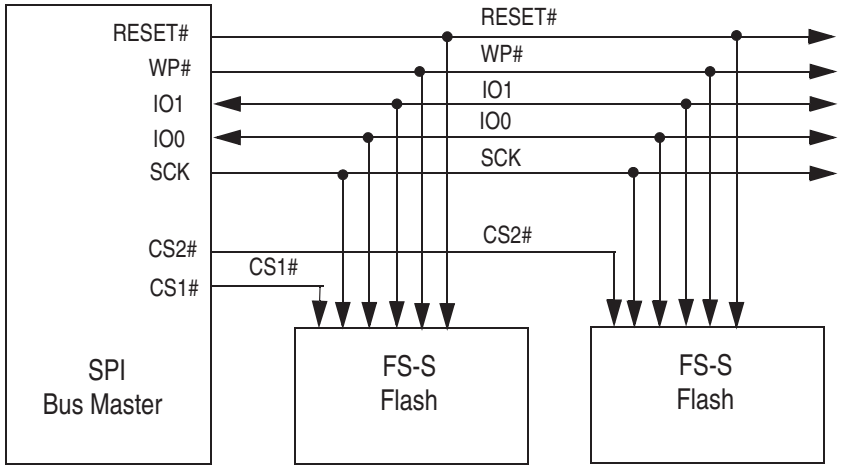
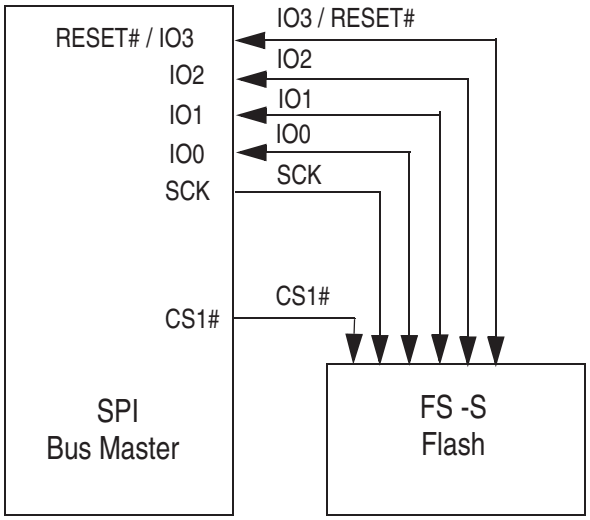


Figure 2.3 Bus Master and Memory Devices on the SPI Bus — Quad Bit Data Path



3. Signal Protocols

3.1 SPI Clock Modes

3.1.1 Single Data Rate (SDR)

The S25FS512S can be driven by an embedded microcontroller (bus master) in either of the two following clocking modes.

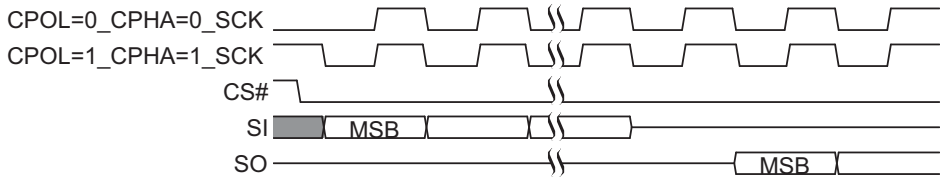
- **Mode 0** with Clock Polarity (CPOL) = 0 and, Clock Phase (CPHA) = 0
- **Mode 3** with CPOL = 1 and, CPHA = 1

For these two modes, input data into the device is always latched in on the rising edge of the SCK signal and the output data is always available from the falling edge of the SCK clock signal.

The difference between the two modes is the clock polarity when the bus master is in standby mode and not transferring any data.

- SCK will stay at logic low state with CPOL = 0, CPHA = 0
- SCK will stay at logic high state with CPOL = 1, CPHA = 1

Figure 3.1 SPI SDR Modes Supported



Timing diagrams throughout the remainder of the document are generally shown as both Mode 0 and 3 by showing SCK as both high and low at the fall of CS#. In some cases a timing diagram may show only Mode 0 with SCK low at the fall of CS#. In such a case, Mode 3 timing simply means clock is high at the fall of CS# so no SCK rising edge set up or hold time to the falling edge of CS# is needed for Mode 3.

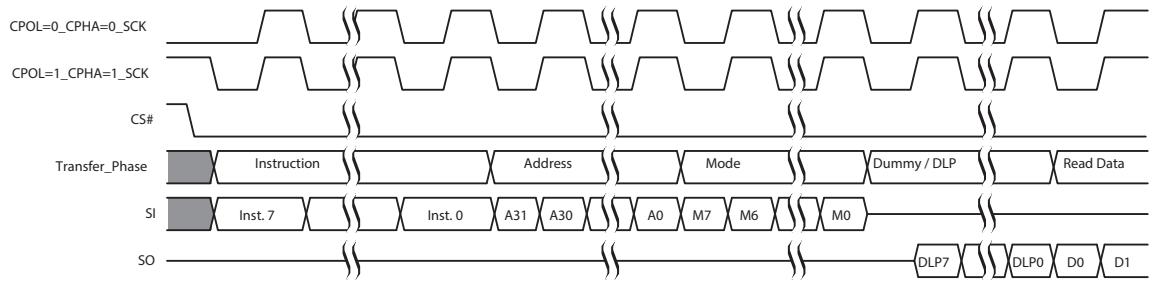
SCK cycles are measured (counted) from one falling edge of SCK to the next falling edge of SCK. In Mode 0 the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already low at the beginning of a command.

3.1.2 Double Data Rate (DDR)

Mode 0 and Mode 3 are also supported for DDR commands. In DDR commands, the instruction bits are always latched on the rising edge of clock, the same as in SDR commands. However, the address and input data that follow the instruction are latched on both the rising and falling edges of SCK. The first address bit is latched on the first rising edge of SCK following the falling edge at the end of the last instruction bit. The first bit of output data is driven on the falling edge at the end of the last access latency (dummy) cycle.

SCK cycles are measured (counted) in the same way as in SDR commands, from one falling edge of SCK to the next falling edge of SCK. In mode 0 the beginning of the first SCK cycle in a command is measured from the falling edge of CS# to the first falling edge of SCK because SCK is already low at the beginning of a command.

Figure 3.2 SPI DDR Modes Supported



3.2 Command Protocol

All communication between the host system and S25FS512S devices is in the form of units called commands.

All commands begin with an 8-bit instruction that selects the type of information transfer or device operation to be performed. Commands may also have an address, instruction modifier, latency period, data transfer to the memory, or data transfer from the memory. All instruction, address, and data information is transferred sequentially between the host system and memory device.

Command protocols are also classified by a numerical nomenclature using three numbers to reference the transfer width of three command phases:

- instruction
- address and instruction modifier (continuous read mode bits)
- data

Single-bit wide commands start with an instruction and may provide an address or data, all sent only on the SI signal. Data may be sent back to the host serially on the SO signal. This is referenced as a 1-1-1 command protocol for single-bit width instruction, single-bit width address and modifier, single-bit data.

Dual or Quad Input / Output (I/O) commands provide an address sent from the host as bit pairs on IO0 and IO1 or, four-bit (nibble) groups on IO0, IO1, IO2, and IO3. Data is returned to the host similarly as bit pairs on IO0 and IO1 or, four-bit (nibble) groups on IO0, IO1, IO2, and IO3. This is referenced as 1-2-2 for Dual I/O and 1-4-4 for Quad I/O command protocols.

The S25FS512S also supports a QPI mode in which all information is transferred in 4-bit width, including the instruction, address, modifier, and data. This is referenced as a 4-4-4 command protocol.

Commands are structured as follows:

- Each command begins with CS# going low and ends with CS# returning high. The memory device is selected by the host driving the Chip Select (CS#) signal low throughout a command.
- The serial clock (SCK) marks the transfer of each bit or group of bits between the host and memory.
- Each command begins with an eight bit (byte) instruction. The instruction selects the type of information transfer or device operation to be performed. The instruction transfers occur on SCK rising edges. However, some read commands are modified by a prior read command, such that the instruction is implied from the earlier command. This is called Continuous Read Mode. When the device is in continuous read mode, the instruction bits are not transmitted at the beginning of the command because the instruction is the same as the read command that initiated the Continuous Read Mode. In Continuous Read mode the command will begin with the read address. Thus, Continuous Read Mode removes eight instruction bits from each read command in a series of same type read commands.
- The instruction may be stand alone or may be followed by address bits to select a location within one of several address spaces in the device. The instruction determines the address space used. The address may be either a 24-bit or a 32-bit, byte boundary, address. The address transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- In legacy SPI mode, the width of all transfers following the instruction are determined by the instruction sent. Following transfers may continue to be single bit serial on only the SI or Serial Output (SO) signals, they may be done in two bit groups per (dual) transfer on the IO0 and IO1 signals, or they may be done in 4-bit groups per (quad) transfer on the IO0-IO3 signals. Within the dual or quad groups the least significant bit is on IO0. More significant bits are placed in significance order on each higher numbered IO signal. Single bits or parallel bit groups are transferred in most to least significant bit order.
- In QPI mode, the width of all transfers is a 4-bit wide (quad) transfer on the IO0-IO3 signals.
- Dual and Quad I/O read instructions send an instruction modifier called Continuous Read mode bits, following the address, to indicate whether the next command will be of the same type with an implied, rather than an explicit, instruction. These mode bits initiate or end the continuous read mode. In continuous read mode, the next command thus does not provide an instruction byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands. The mode bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- The address or mode bits may be followed by write data to be stored in the memory device or by a read latency period before read data is returned to the host.
- Write data bit transfers occur on SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.

- SCK continues to toggle during any read access latency period. The latency may be zero to several SCK cycles (also referred to as dummy cycles). At the end of the read latency cycles, the first read data bits are driven from the outputs on SCK falling edge at the end of the last read latency cycle. The first read data bits are considered transferred to the host on the following SCK rising edge. Each following transfer occurs on the next SCK rising edge, in SDR commands, or on every SCK edge, in DDR commands.
- If the command returns read data to the host, the device continues sending data transfers until the host takes the CS# signal high. The CS# signal can be driven high after any transfer in the read data sequence. This will terminate the command.
- At the end of a command that does not return data, the host drives the CS# input high. The CS# signal must go high after the eighth bit, of a stand alone instruction or, of the last write data byte that is transferred. That is, the CS# signal must be driven high when the number of bits after the CS# signal was driven low is an exact multiple of eight bits. If the CS# signal does not go high exactly at the eight-bit boundary of the instruction or write data, the command is rejected and not executed.
- All instruction, address, and mode bits are shifted into the device with the Most Significant Bits (MSB) first. The data bits are shifted in and out of the device MSB first. All data is transferred in byte units with the lowest address byte sent first. Following bytes of data are sent in lowest to highest byte address order i.e. the byte address increments.
- All attempts to read the flash memory array during a program, erase, or a write cycle (embedded operations) are ignored. The embedded operation will continue to execute without any affect. A very limited set of commands are accepted during an embedded operation. These are discussed in the individual command descriptions.
- Depending on the command, the time for execution varies. A command to read status information from an executing command is available to determine when the command completes execution and whether the command was successful.

3.2.1 Command Sequence Examples

Figure 3.3 Stand Alone Instruction Command

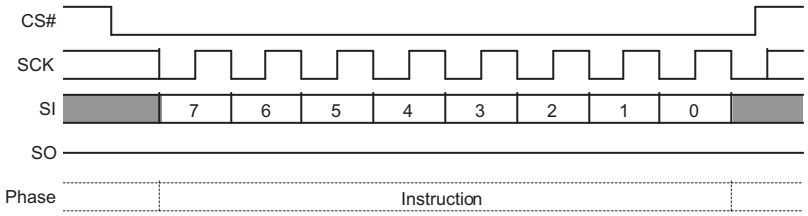


Figure 3.4 Single Bit Wide Input Command

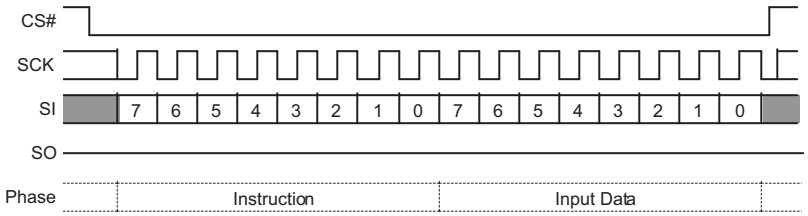


Figure 3.5 Single Bit Wide Output Command

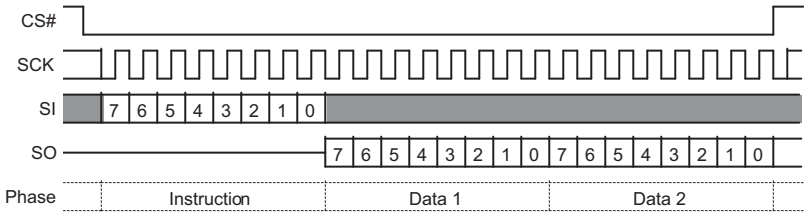


Figure 3.6 Single Bit Wide I/O Command without latency

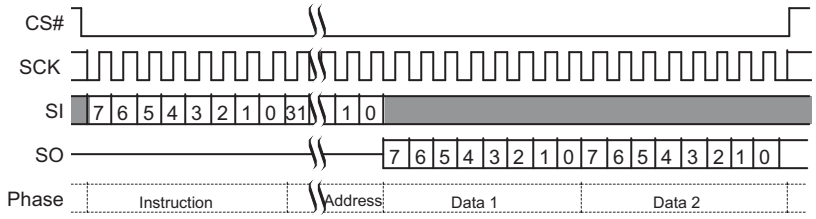


Figure 3.7 Single Bit Wide I/O Command with latency

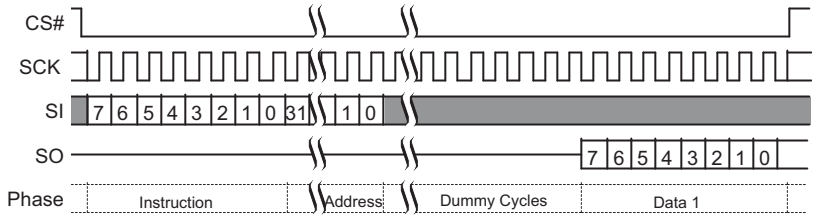


Figure 3.8 Dual I/O Command

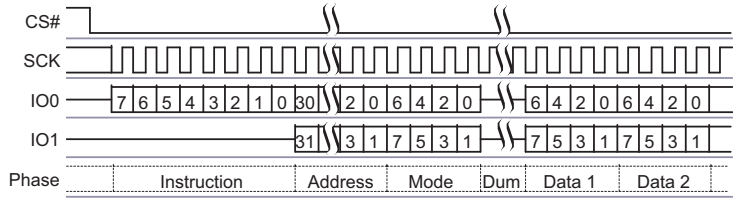


Figure 3.9 Quad I/O Command

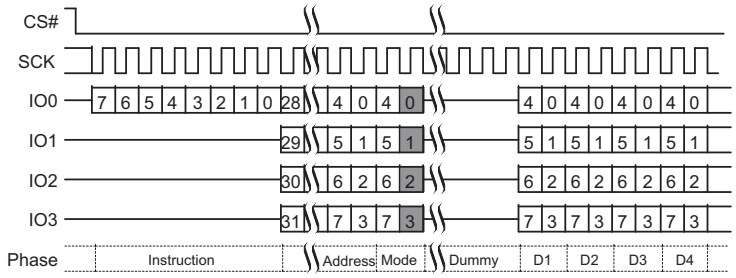


Figure 3.10 Quad I/O Read Command in QPI Mode

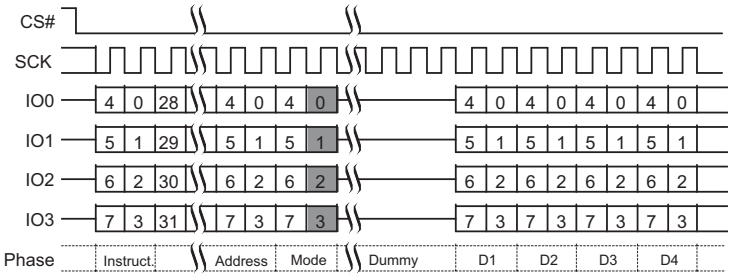


Figure 3.11 DDR Quad I/O Read

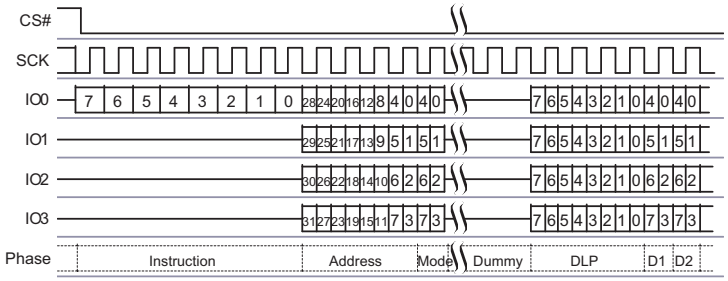
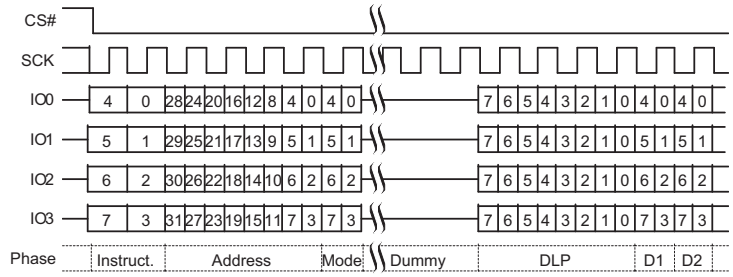


Figure 3.12 DDR Quad I/O Read in QPI Mode



Additional sequence diagrams, specific to each command, are provided in Commands on page 74.

3.3 Interface States

This section describes the input and output signal levels as related to the SPI interface behavior.

Table 3.1 Interface States Summary

Interface State	V_{DD}	SCK	CS#	IO3 / RESET#	WP# / IO2	SO / IO1	SI / IO0
Power-Off	<V_{DD} (low)	X	X	X	X	Z	X
Low Power Hardware Data Protection	<V_{DD} (cut-off)	X	X	X	X	Z	X
Power-On (Cold) Reset	≥V_{DD} (min)	X	HH	X	X	Z	X
Hardware (Warm) Reset Non-Quad Mode	≥V_{DD} (min)	X	X	HL	X	Z	X
Hardware (Warm) Reset Quad Mode	≥V_{DD} (min)	X	HH	HL	X	Z	X
Interface Standby	≥V_{DD} (min)	X	HH	X	X	Z	X
Instruction Cycle (Legacy SPI)	≥V_{DD} (min)	HT	HL	HH	HV	Z	HV
Single Input Cycle Host to Memory Transfer	≥V_{DD} (min)	HT	HL	HH	X	Z	HV
Single Latency (Dummy) Cycle	≥V_{DD} (min)	HT	HL	HH	X	Z	X
Single Output Cycle Memory to Host Transfer	≥V_{DD} (min)	HT	HL	HH	X	MV	X
Dual Input Cycle Host to Memory Transfer	≥V_{DD} (min)	HT	HL	HH	X	HV	HV
Dual Latency (Dummy) Cycle	≥V_{DD} (min)	HT	HL	HH	X	X	X
Dual Output Cycle Memory to Host Transfer	≥V_{DD} (min)	HT	HL	HH	X	MV	MV
Quad Input Cycle Host to Memory Transfer	≥V_{DD} (min)	HT	HL	HV	HV	HV	HV

Table 3.1 Interface States Summary (Continued)

Interface State	V_{DD}	SCK	CS#	IO3 / RESET#	WP# / IO2	SO / IO1	SI / IO0
Quad Latency (Dummy) Cycle	≥V_{DD} (min)	HT	HL	X	X	X	X
Quad Output Cycle Memory to Host Transfer	≥V_{DD} (min)	HT	HL	MV	MV	MV	MV
DDR Quad Input Cycle Host to Memory Transfer	≥V_{DD} (min)	HT	HL	HV	HV	HV	HV
DDR Latency (Dummy) Cycle	≥V_{DD} (min)	HT	HL	MV or Z	MV or Z	MV or Z	MV or Z
DDR Quad Output Cycle Memory to Host Transfer	≥V_{DD} (min)	HT	HL	MV	MV	MV	MV

Legend
Z = no driver – floating signal
HL = Host driving V_{IL}
HH = Host driving V_{IH}
HV = either HL or HH
X = HL or HH or Z
HT = toggling between HL and HH
ML = Memory driving V_{IL}
MH = Memory driving V_{IH},
MV = either ML or MH

3.3.1 Power-Off
When the core supply voltage is at or below the $V_{DD\ (Low)}$ voltage, the device is considered to be powered off. The device does not react to external signals, and is prevented from performing any program or erase operation.

3.3.2 Low Power Hardware Data Protection
When V_{DD} is less than $V_{DD\ (Cut\text{-}off)}$ the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

3.3.3 Power-On (Cold) Reset
When the core voltage supply remains at or below the $V_{DD\ (Low)}$ voltage for ≥ t_{PD} time, then rises to ≥ $V_{DD\ (Minimum)}$ the device will begin its Power On Reset (POR) process. POR continues until the end of t_{PU}. During t_{PU} the device does not react to external input signals nor drive any outputs. Following the end of t_{PU} the device transitions to the Interface Standby state and can accept commands. For additional information on POR see Power On (Cold) Reset on page 30.

3.3.4 Hardware (Warm) Reset
A configuration option is provided to allow IO3 to be used as a hardware reset input when the device is not in Quad mode or when it is in Quad mode and CS# is high. When IO3 / RESET# is driven low for t_{RP} time the device starts the hardware reset process. The process continues for t_{RPH} time. Following the end of both t_{RPH} and the reset hold time following the rise of RESET# (t_{RH}) the device transitions to the Interface Standby state and can accept commands.

3.3.5 Interface Standby
When CS# is high the SPI interface is in standby state. Inputs other than RESET# are ignored. The interface waits for the beginning of a new command. The next interface state is Instruction Cycle when CS# goes low to begin a new command.

While in interface standby state the memory device draws standby current (I_{SB}) if no embedded algorithm is in progress. If an embedded algorithm is in progress, the related current is drawn until the end of the algorithm when the entire device returns to standby current draw.

A Deep Power Down (DPD) mode is supported by the S25FS512S devices. If the device has been placed in DPD mode by the DPD (B9h) command, the interface standby current is (I_{DPD}). The DPD command is accepted only while the device is not performing an embedded algorithm as indicated by the Status Register-1 volatile Write In Progress (WIP) bit being cleared to zero (SR1V[0] = 0). While in DPD mode the device ignores all commands except the Release from DPD (RES ABh) command, that will return the device to the Interface Standby state after a delay of t_{RES}.

3.3.6 Instruction Cycle (Legacy SPI Mode)

When the host drives the MSB of an instruction and CS# goes low, on the next rising edge of SCK the device captures the MSB of the instruction that begins the new command. On each following rising edge of SCK the device captures the next lower significance bit of the 8-bit instruction. The host keeps CS# low, and drives the Write Protect (WP#) and IO3/RESET signals as needed for the instruction. However, WP# is only relevant during instruction cycles of a WRR or WRAR command and is otherwise ignored. IO3 / RESET# is driven high when the device is not in Quad Mode (CR1V[1]=0) or QPI Mode (CR2V[6]=0) and hardware reset is not required.

Each instruction selects the address space that is operated on and the transfer format used during the remainder of the command. The transfer format may be Single, Dual I/O, Quad I/O, or DDR Quad I/O. The expected next interface state depends on the instruction received.

Some commands are stand alone, needing no address or data transfer to or from the memory. The host returns CS# high after the rising edge of SCK for the eighth bit of the instruction in such commands. The next interface state in this case is Interface Standby.

3.3.7 Instruction Cycle (QPI Mode)

In QPI mode, when CR2V[6]=0, instructions are transferred 4 bits per cycle. In this mode instruction cycles are the same as a Quad Input Cycle. See Quad Input Cycle — Host to Memory Transfer on page 21.

3.3.8 Single Input Cycle — Host to Memory Transfer

Several commands transfer information after the instruction on the single serial input (SI) signal from host to the memory device. The host keeps RESET# high, CS# low, and drives SI as needed for the command. The memory does not drive the Serial Output (SO) signal.

The expected next interface state depends on the instruction. Some instructions continue sending address or data to the memory using additional Single Input Cycles. Others may transition to Single Latency, or directly to Single, Dual, or Quad Output cycle states.

3.3.9 Single Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR2V[3:0]). During the latency cycles, the host keeps RESET# high, CS# low. The Write Protect (WP#) signal is ignored. The host may drive the SI signal during these cycles or the host may leave SI floating. The memory does not use any data driven on SI / I/O0 or other I/O signals during the latency cycles. The memory does not drive the Serial Output (SO) or I/O signals during the latency cycles.

The next interface state depends on the command structure, i.e., the number of latency cycles, and whether the read is single, dual, or quad width.

3.3.10 Single Output Cycle — Memory to Host Transfer

Several commands transfer information back to the host on the single Serial Output (SO) signal. The host keeps RESET# high, CS# low. The Write Protect (WP#) signal is ignored. The memory ignores the Serial Input (SI) signal. The memory drives SO with data.

The next interface state continues to be Single Output Cycle until the host returns CS# to high ending the command.

3.3.11 Dual Input Cycle — Host to Memory Transfer

The Read Dual I/O command transfers two address or mode bits to the memory in each cycle. The host keeps RESET# high, CS# low. The Write Protect (WP#) signal is ignored. The host drives address on SI / IO0 and SO / IO1.

The next interface state following the delivery of address and mode bits is a Dual Latency Cycle if there are latency cycles needed or Dual Output Cycle if no latency is required.

3.3.12 Dual Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR2V[3:0]). During the latency cycles, the host keeps RESET# high, CS# low. The Write Protect (WP#) signal is ignored. The host may drive the SI / IO0 and SO / IO1 signals during these cycles or the host may leave SI / IO0 and SO / IO1 floating. The memory does not use any data driven on SI / IO0 and SO / IO1 during the latency cycles. The host must stop driving SI / IO0 and SO / IO1 on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the SI / IO0 and SO / IO1 signals during the latency cycles.

The next interface state following the last latency cycle is a Dual Output Cycle.

3.3.13 Dual Output Cycle — Memory to Host Transfer

The Read Dual Output and Read Dual I/O return data to the host two bits in each cycle. The host keeps RESET# high, CS# low. The Write Protect (WP#) signal is ignored. The memory drives data on the SI / IO0 and SO / IO1 signals during the dual output cycles.

The next interface state continues to be Dual Output Cycle until the host returns CS# to high ending the command.

3.3.14 Quad Input Cycle — Host to Memory Transfer

The Quad I/O Read command transfers four address or mode bits to the memory in each cycle. In QPI mode the Quad I/O Read and Page Program commands transfer four data bits to the memory in each cycle, including the instruction cycles. The host keeps CS# low, and drives the IO signals.

For Quad I/O Read the next interface state following the delivery of address and mode bits is a Quad Latency Cycle if there are latency cycles needed or Quad Output Cycle if no latency is required. For QPI mode Page Program, the host returns CS# high following the delivery of data to be programmed and the interface returns to standby state.

3.3.15 Quad Latency (Dummy) Cycle

Read commands may have zero to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR2V[3:0]). During the latency cycles, the host keeps CS# low. The host may drive the IO signals during these cycles or the host may leave the IO floating. The memory does not use any data driven on IO during the latency cycles. The host must stop driving the IO signals on the falling edge at the end of the last latency cycle. It is recommended that the host stop driving them during all latency cycles so that there is sufficient time for the host drivers to turn off before the memory begins to drive at the end of the latency cycles. This prevents driver conflict between host and memory when the signal direction changes. The memory does not drive the IO signals during the latency cycles.

The next interface state following the last latency cycle is a Quad Output Cycle.

3.3.16 Quad Output Cycle — Memory to Host Transfer

The Quad I/O Read returns data to the host four bits in each cycle. The host keeps CS# low. The memory drives data on IO0-IO3 signals during the Quad output cycles.

The next interface state continues to be Quad Output Cycle until the host returns CS# to high ending the command.

3.3.17 DDR Quad Input Cycle — Host to Memory Transfer

The DDR Quad I/O Read command sends address, and mode bits to the memory on all the IO signals. Four bits are transferred on the rising edge of SCK and four bits on the falling edge in each cycle. The host keeps CS# low.

The next interface state following the delivery of address and mode bits is a DDR Latency Cycle.

3.3.18 DDR Latency Cycle

DDR Read commands may have one to several latency cycles during which read data is read from the main flash memory array before transfer to the host. The number of latency cycles are determined by the Latency Code in the configuration register (CR2V[3:0]). During the latency cycles, the host keeps CS# low. The host may not drive the IO signals during these cycles. So that there is sufficient time for the host drivers to turn off before the memory begins to drive. This prevents driver conflict between host and memory when the signal direction changes. The memory has an option to drive all the IO signals with a Data Learning Pattern (DLP) during the last four latency cycles. The DLP option should not be enabled when there are fewer than five latency cycles so that there is at least one cycle of high impedance for turn around of the IO signals before the memory begins driving the DLP. When there are more than four cycles of latency the memory does not drive the IO signals until the last four cycles of latency.

The next interface state following the last latency cycle is a DDR Single, or Quad Output Cycle, depending on the instruction.

3.3.19 DDR Quad Output Cycle — Memory to Host Transfer

The DDR Quad I/O Read command returns bits to the host on all the IO signals. Four bits are transferred on the rising edge of SCK and four bits on the falling edge in each cycle. The host keeps CS# low.

The next interface state continues to be DDR Quad Output Cycle until the host returns CS# to high ending the command.

3.4 Configuration Register Effects on the Interface

The Configuration Register 2 volatile bits 3 to 0 (CR2V[3:0]) select the variable latency for all array read commands except Read and Read SDFP (RSFDP). Read always has zero latency cycles. RSFDP always has eight latency cycles. The variable latency is also used in the OTPR and RDAR commands.

The configuration register bit 1 (CR1V[1]) selects whether Quad mode is enabled to switch WP# to IO2 function, RESET# to IO3 function, and thus allow Quad I/O Read and QPI mode commands. Quad mode must also be selected to allow DDR Quad I/O Read commands.

3.5 Data Protection

Some basic protection against unintended changes to stored data are provided and controlled purely by the hardware design. These are described below. Other software managed protection methods are discussed in the software section of this document.

3.5.1 Power-Up

When the core supply voltage is at or below the $V_{DD\ (Low)}$ voltage, the device is considered to be powered off. The device does not react to external signals, and is prevented from performing any program or erase operation. Program and erase operations continue to be prevented during the Power-on Reset (POR) because no command is accepted until the exit from POR to the Interface Standby state.

3.5.2 Low Power

When V_{DD} is less than $V_{DD\ (Cut\text{-}off)}$ the memory device will ignore commands to ensure that program and erase operations can not start when the core supply voltage is out of the operating range.

3.5.3 Clock Pulse Count

The device verifies that all non-volatile memory and register data modifying commands consist of a clock pulse count that is a multiple of eight bit transfers (byte boundary) before executing them. A command not ending on an 8-bit (byte) boundary is ignored and no error status is set for the command.

3.5.4 Deep Power Down (DPD)

In DPD mode the device responds only to the Release from DPD command (RES ABh). All other commands are ignored during DPD mode, thereby protecting the memory from program and erase operations.

4. Electrical Specifications

4.1 Absolute Maximum Ratings

Storage Temperature Plastic Packages	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +150°C
V_{DD}	-0.5 V to +2.5V
Input voltage with respect to Ground (V_{SS}) (Note 1)	-0.5 V to V_{DD} + 0.5V
Output Short Circuit Current (Note 2)	100 mA

Notes:

1. *See Input Signal Overshoot on page 24 for allowed maximums during signal transition.*
2. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
3. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

4.2 Thermal Resistance

Table 4.1 Thermal Resistance

Parameter	Description	SO3016	WNH008	FAB024	Unit
Theta JA	Thermal resistance (junction to ambient)	38	18	39	°C

4.3 Latchup Characteristics

Table 4.2 Latchup Specification

Description	Min	Max	Unit
Input voltage with respect to V_{SS} on all input only connections	-1.0	V_{DD} + 1.0	V
Input voltage with respect to V_{SS} on all I/O connections	-1.0	V_{DD} + 1.0	V
V_{DD} Current	-100	+100	mA

Note:

1. *Excludes power supply V_{DD}. Test conditions: V_{DD} = 1.8 V, one connection at a time tested, connections not being tested are at V_{SS}.*

4.4 Operating Ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

4.4.1 Power Supply Voltages

V_{DD}	1.7V to 2.0V

4.4.2 Temperature Ranges

Parameter	Symbol	Devices	Spec		Unit
			Min	Max	
Ambient Temperature	T_A	Industrial (I)	-40	+85	°C
		Industrial Plus Devices (V)	-40	+105	
		Automotive, AEC-Q100 Grade 3 (A)	-40	+85	
		Automotive, AEC-Q100 Grade 2 (B)	-40	+105	
		Automotive, AEC-Q100 Grade 1 (M)	-40	+125	

Note:

1. *Industrial Plus operating and performance parameters will be determined by device characterization and may vary from standard industrial temperature range devices as currently shown in this specification.*

4.4.3 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{DD}. During voltage transitions, inputs or I/Os may overshoot V_{SS} to -1.0V or overshoot to V_{DD} +1.0V, for periods up to 20 ns.

Figure 4.1 Maximum Negative Overshoot Waveform

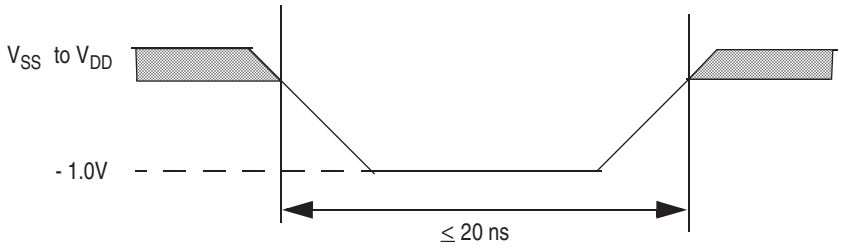
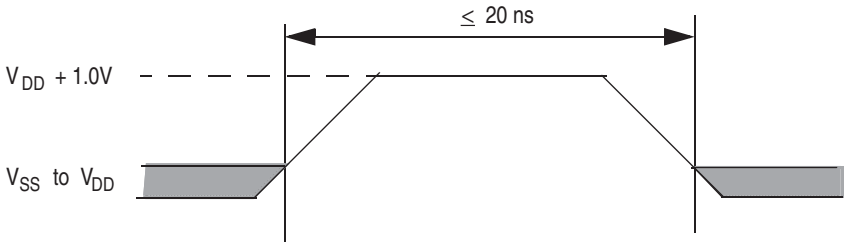


Figure 4.2 Maximum Positive Overshoot Waveform



4.5 Power-Up and Power-Down

The device must not be selected at power-up or power-down (that is, CS# must follow the voltage applied on V_{DD}) until V_{DD} reaches the correct value as follows:

- V_{DD} (min) at power-up, and then for a further delay of t_{PU}
- V_{SS} at power-down

A simple pull-up resistor on Chip Select (CS#) can usually be used to insure safe and proper power-up and power-down.

The device ignores all instructions until a time delay of t_{PU} has elapsed after the moment that V_{DD} rises above the minimum V_{DD} threshold. See Figure 4.3. However, correct operation of the device is not guaranteed if V_{DD} returns below V_{DD} (min) during t_{PU}. No command should be sent to the device until the end of t_{PU}.

The device draws I_{POR} during t_{PU}. After power-up (t_{PU}), the device is in Standby mode, draws CMOS standby current (I_{SB}), and the WEL bit is reset.

During power-down or voltage drops below V_{DD}(cut-off), the voltage must drop below V_{DD}(low) for a period of t_{PD} for the part to initialize correctly on power-up. See Figure 4.4. If during a voltage drop the V_{DD} stays above V_{DD}(cut-off) the part will stay initialized and will work correctly when V_{DD} is again above V_{DD}(min). In the event Power-on Reset (POR) did not complete correctly after power up, the assertion of the RESET# signal or receiving a software reset command (RESET) will restart the POR process.

Normal precautions must be taken for supply rail decoupling to stabilize the V_{DD} supply at the device. Each device in a system should have the V_{DD} rail decoupled by a suitable capacitor close to the package supply connection (this capacitor is generally of the order of 0.1µf).

Table 4.3 FS-S Power-Up / Power-Down Voltage and Timing

Symbol	Parameter	Min	Max	Unit
V_{DD} (min)	V_{DD} (minimum operation voltage)	1.7		V
V_{DD} (cut-off)	V_{DD} (Cut 0ff where re-initialization is needed)	1.5		V
V_{DD} (low)	V_{DD} (low voltage for initialization to occur)	0.7		V
t_{PU}	V_{DD}(min) to Read operation		300	µs
t_{PD}	V_{DD}(low) time	10.0		µs

Figure 4.3 Power-up