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S29AS016J

16 Mbit (2 M x 8-Bit/1 M x 16-Bit), 1.8 V Boot Sector Flash

Distinctive Characteristics

Architectural Advantages

- Single Power Supply Operation
  - Full voltage range: 1.65 to 1.95 volt read and write operations for battery-powered applications
- Manufactured on 110 nm Process Technology
  - Backward compatible with 0.32 µm Am29SL160C device
- Secured Silicon Sector region
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number, accessible through a command sequence
  - May be programmed and locked at the factory or by the customer
- Flexible Sector Architecture
  - Eight 8 Kbyte and thirty-one 64 Kbyte sectors (byte mode)
  - Eight 4 Kword, and thirty-one 32 Kword sectors (word mode)
- Sector Group Protection Features
  - A hardware method of locking a sector to prevent any program or erase operations within that sector
  - Sectors can be locked in-system or via programming equipment
  - Temporary Sector Group Unprotect feature allows code changes in previously locked sectors
- Unlock Bypass Program Command
  - Reduces overall programming time when issuing multiple program command sequences
- Top or Bottom Boot Block Configurations Available
- Compatibility with JEDEC standards
  - Pinout and software compatible with single-power supply Flash
  - Superior inadvertent write protection

Performance Characteristics

- High Performance
  - Access times as fast as 70 ns
  - Industrial temperature range (-40°C to +85°C)
  - Automotive In-Cabin temperature range (-40°C to +105°C)
  - Word programming time as fast as 6 µs (typical)
- Ultra Low Power Consumption (typical values at 5 MHz)
  - 15 µA Automatic Sleep mode current
  - 8 µA standby mode current
  - 8 mA read current
  - 20 mA program/erase current
- Cycling Endurance: 1,000,000 cycles per sector typical
- Data Retention: 20 years typical

Package Options

- 48-ball Fine-Pitch BGA, 8.15 mm x 6.15 mm
- 48-ball Fine-Pitch BGA, 6.0 mm x 4.0 mm
- 48-pin TSOP

Software Features

- CFI (Common Flash Interface) Compliant
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- Erase Suspend/Erase Resume
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- Data# Polling and Toggle Bits
  - Provides a software method of detecting program or erase operation completion

Hardware Features

- Ready/Busy# Pin (RY/BY#)
  - Provides a hardware method of detecting program or erase cycle completion
- Hardware Reset Pin (RESET#)
  - Hardware method to reset the device to reading array data
- WP# input pin
  - Write protect (WP#) function allows protection of two outermost boot sectors (boot sector models only), regardless of sector group protect status

General Description

The S29AS016J is a 16 Mbit, 1.8 Volt-only Flash memory organized as 2,097,152 bytes or 1,048,576 words with a x8/x16 bus and either top or bottom boot sector architecture. The device is offered in 48-pin TSOP and 48-ball FBGA packages. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device is designed to be programmed and erased in-system with the standard system 1.8 volt V_{CC} supply. A 12.0V V_{PP} or 5.0 V_{CC} are not required for program or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers access time of 70 ns allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 1.8 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The S29AS016J is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector group protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend**/**Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

Spansion's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

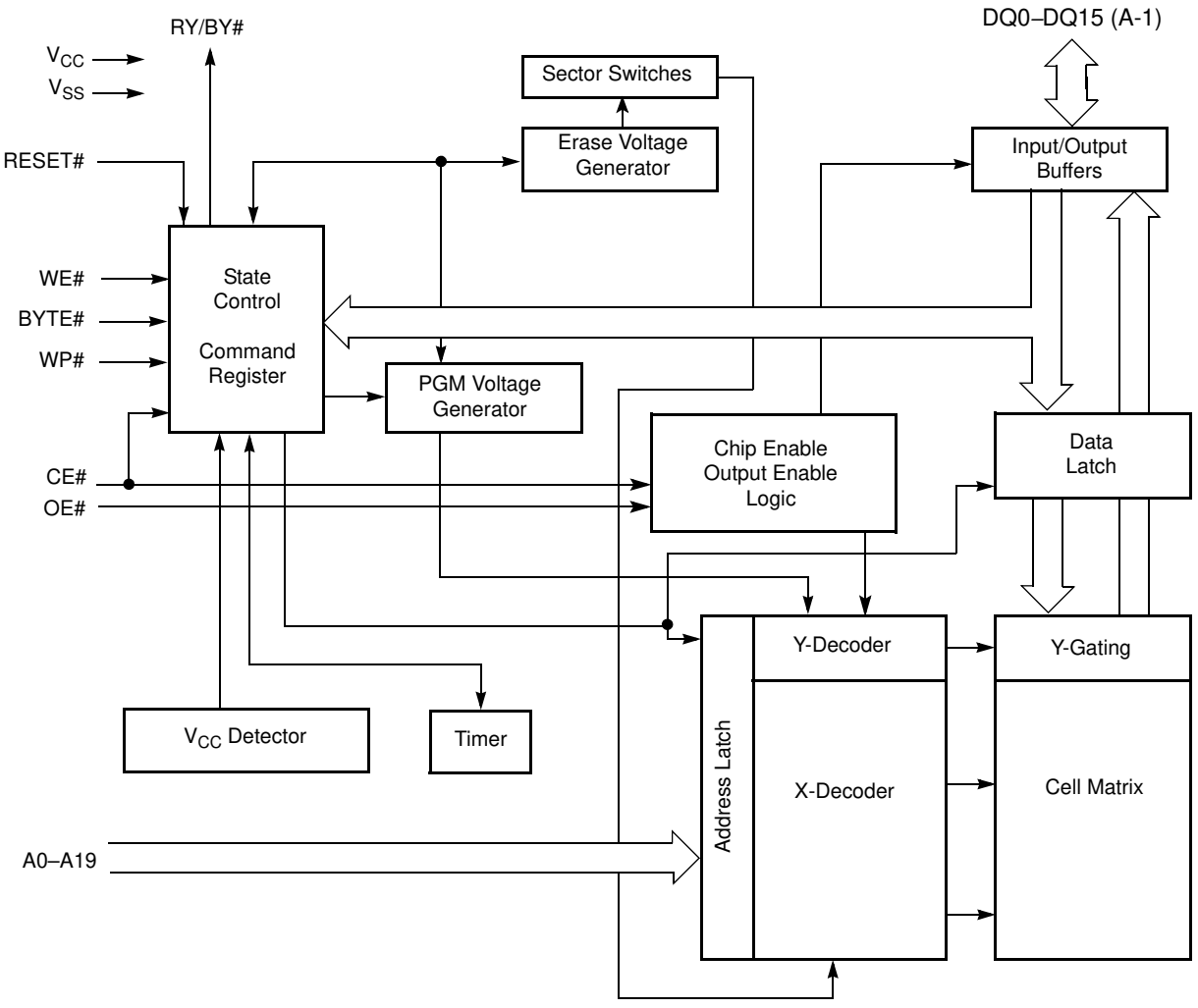
Contents

1. Product Selector Guide

Family Part Number		S29AS016J
Speed Option	Voltage Range: V_{CC} = 1.65–1.95 V	70
Max access time, ns (t_{ACC})		70
Max CE# access time, ns (t_{CE})		70
Max OE# access time, ns (t_{OE})		25

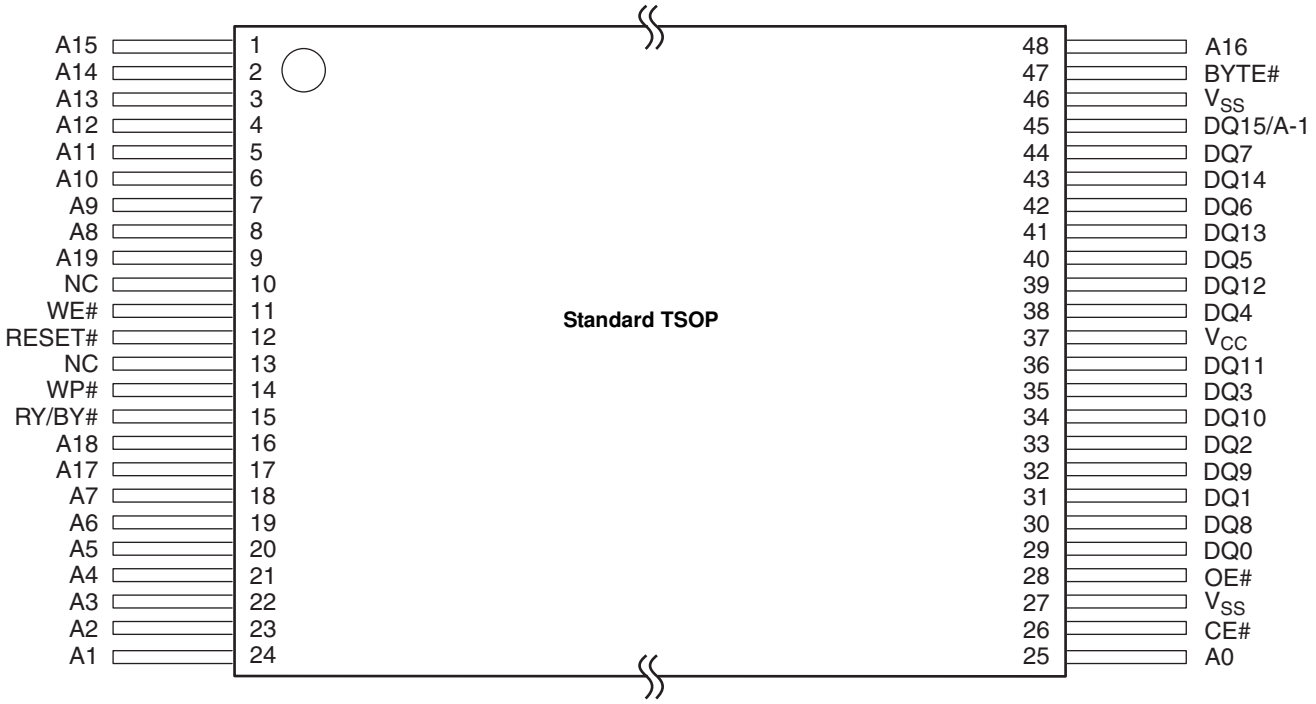
Note
See AC Characteristics on page 38 for full specifications.

2. Block Diagram



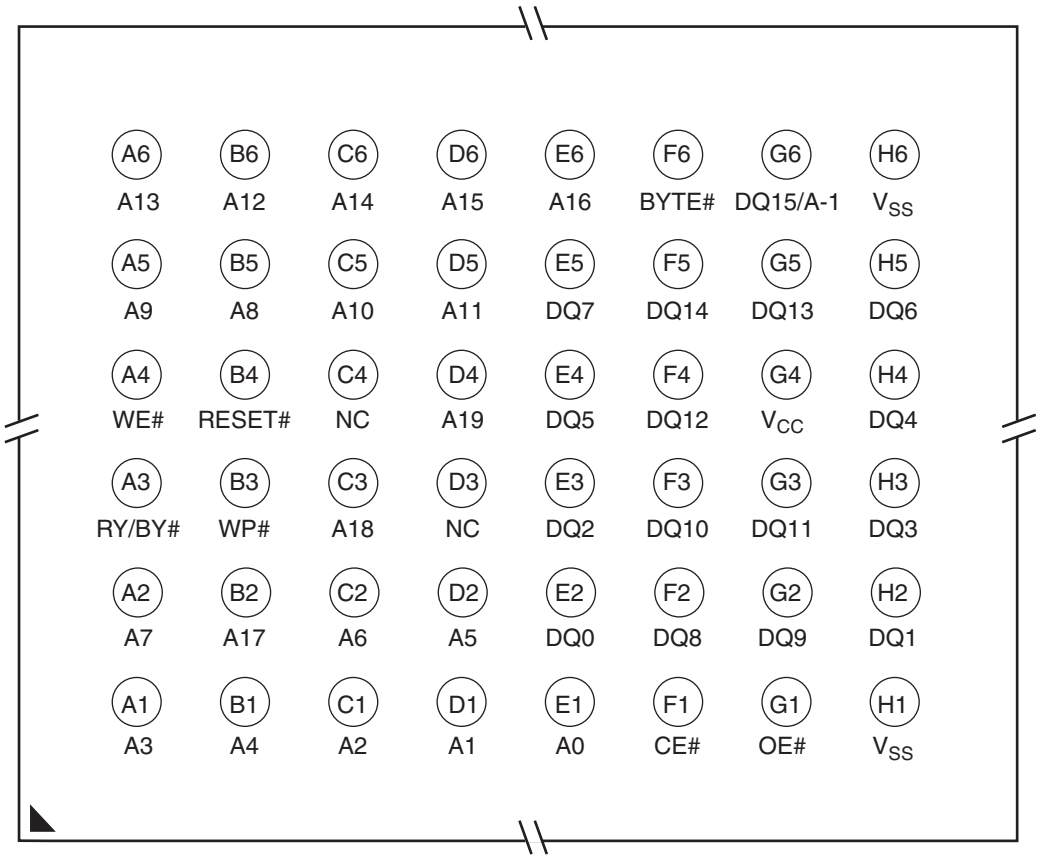
3. Connection Diagrams

3.1 Standard TSOP



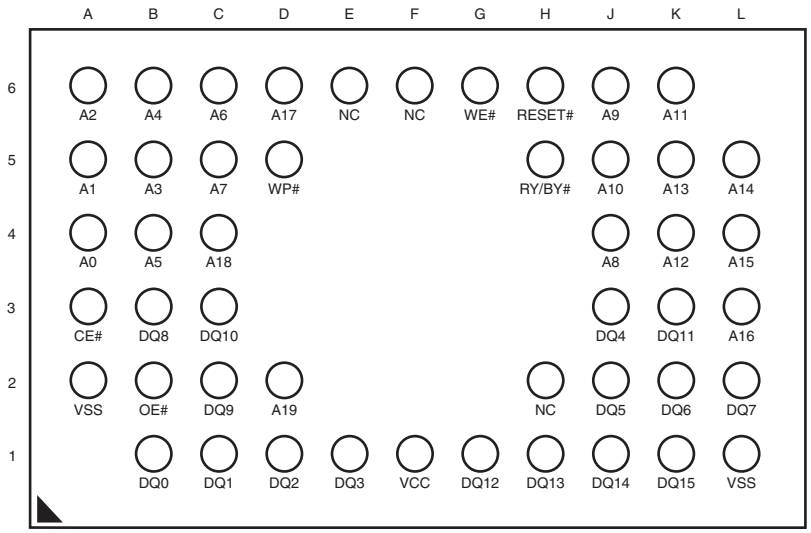
3.2 FBGA Connection Diagram, 8.15 mm x 6.15 mm (VBK048)

Fine-pitch Ball Grid Array - VBK048
Top View, Balls Facing Down



3.3 FBGA Connection Diagram, 6.0 mm x 4.0 mm (VDF048)

Fine-pitch Ball Grid Array - VDF048
Top View, Balls Facing Down



3.4 Special Handling Instructions

Special handling is required for Flash Memory products in BGA packages.

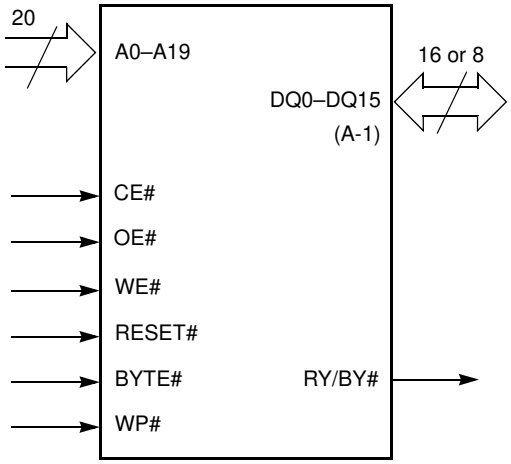
Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods.

The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

4. Pin Configuration

A0–A19	20 addresses
DQ0–DQ14	15 data inputs/outputs
DQ15/A-1	DQ15 (data input/output, word mode), A-1 (LSB address input, byte mode)
BYTE#	Selects 8-bit or 16-bit mode
CE#	Chip enable
OE#	Output enable
WE#	Write enable
WP#	Write protect: The WP# contains an internal pull-up; when unconnected, WP is at V_{IH}.
RESET#	Hardware reset pin
RY/BY#	Ready/Busy output
V_{CC}	1.8 volt-only single power supply (see *Product Selector Guide* on page 4 for speed options and voltage supply tolerances)
V_{SS}	Device ground
NC	Pin not connected internally

5. Logic Symbol



6. Ordering Information

6.1 S29AS016J Standard Products

Spansion standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

S29AS016J 70 T F I 01 0

Packing Type
0 = Tray
2 = 7" Tape and Reel
3 = 13" Tape and Reel

Model Number
01 = V_{CC} = 1.65–1.95 V, top boot sector device (Note 3)
02 = V_{CC} = 1.65–1.95 V, bottom boot sector device (Note 3)
03 = V_{CC} = 1.65–1.95 V, top boot sector device
04 = V_{CC} = 1.65–1.95 V, bottom boot sector device
F3 = V_{CC} = 1.65–1.95 V, x16 only, 6.0x4.0 mm FBGA, top boot sector device
F4 = V_{CC} = 1.65–1.95 V, x16 only, 6.0x4.0 mm FBGA, bottom boot sector device

Temperature Range
I = Industrial (-40°C to +85°C)
V = Automotive In-Cabin (-40°C to +105°C)

Package Material Set
F = Pb-Free
H = Low-Halogen, Pb-Free

Package Type
T = Thin Small Outline Package (TSOP) Standard Pinout
B = Fine-pitch Ball-Grid Array Package

Speed Option
70 = 70 ns Access Speed
90 = 90 ns Access Speed

Device Number/Description
S29AS016J
16 Megabit Flash Memory manufactured using 110 nm process technology
1.8 Volt-only Read, Program, and Erase

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S29AS016J Valid Combinations					Package Description	
Device Number	Speed Option	Package Type, Material, and Temperature Range	Model Number	Packing Type		
S29AS016J	70	TFI	01, 02, 03, 04 (Note 3)	0, 3 (Note 1)	TS048 (Note 2)	TSOP
		BFI, BHI		0, 2, 3 (Note 1)	VBK048	Fine-Pitch BGA (Note 4)
		BHI	F3, F4		VDF048	
		BFV, BHV	03, 04		VBK048	
	90	BFV, BHV	03, 04		VBK048	

Notes

1. *Type 0 is standard. Specify other options as required.*
2. *TSOP package markings omit packing type designator from ordering part number.*
3. *Model numbers 01 and 02 are deprecated. Please use the equivalent 03 and 04 model numbers instead.*
4. *BGA package marking omits leading "S29" and packing type designator from ordering part number.*

7. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

S29AS016J Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#	Addresses (Note 1)	DQ0–DQ7	DQ8–DQ15	
								BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	X	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write (Program/Erase)	L	H	L	H	(Note 3)	A_{IN}	D_{IN}	D_{IN}	
Standby	V_{CC} ± 0.2 V	X	X	V_{CC} ± 0.2 V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	X	High-Z	High-Z	High-Z
Sector Group Protect (Note 2)	L	H	L	V_{ID}	X	Sector Address, A6 = L, A3 = A2 = L, A1 = H, A0 = L	D_{IN}	X	X
Sector GroupUnprotect (Note 2)	L	H	L	V_{ID}	H	Sector Address, A6 = H, A3 = A2 = L, A1 = H, A0 = L	D_{IN}	X	X
Temporary Sector Group Unprotect	X	X	X	V_{ID}	H	A_{IN}	D_{IN}	D_{IN}	High-Z

Legend

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 9.0 - 11.0 V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes

1. *Addresses are A19:A0 in word mode (BYTE# = V_{IH}), A19:A-1 in byte mode (BYTE# = V_{IL}).*
2. *The sector group protect and sector group unprotect functions may also be implemented via programming equipment. See Sector Group Protection/Unprotection on page 15.*
3. *If WP# = V_{IL}, the two outermost boot sectors remain protected. If WP# = V_{IH}, the two outermost boot sector group protection depends on whether they were last protected or unprotected.*

7.1 Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins DQ15–DQ0 operate in the byte or word configuration. If the BYTE# pin is set at logic *1*, the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic *0*, the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

7.2 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See *Reading Array Data* on page 24 for more information. Refer to the AC *Read Operations* on page 38 for timing specifications and to Figure 18.1 on page 39 for the timing diagram. I_{CC1} in *DC Characteristics* on page 36 represents the active current specification for reading array data.

7.3 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. See *Word/Byte Configuration* on page 9 for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. *Word/Byte Program Command Sequence* on page 25 has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table on page 12 and Table on page 14 indicate the address space that each sector occupies. A “sector address” consists of the address bits required to uniquely select a sector. The *Command Definitions* on page 23 has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to *Autoselect Mode* on page 11 and *Autoselect Command Sequence* on page 24 for more information.

I_{CC2} in *DC Characteristics* on page 36 represents the active current specification for the write mode. *AC Characteristics* on page 38 contains timing specification tables and timing diagrams for write operations.

7.4 Program and Erase Operation Status

During an erase or program operation, the system may check the status of the operation by reading the status bits on DQ7–DQ0. Standard read cycle timings and I_{CC} read specifications apply. Refer to *Write Operation Status* on page 31 for more information, and to *AC Characteristics* on page 38 for timing diagrams.

7.5 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{CC} \pm 0.2$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{CC} \pm 0.2$ V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} and I_{CC4} represents the standby current specification shown in the table in *DC Characteristics* on page 36.

7.6 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC5} in the *DC Characteristics* on page 36 represents the automatic sleep mode current specification.

7.7 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the system drives the RESET# pin to V_{IL} for at least a period of t_{RP}, the device **immediately terminates** any operation in progress, tristates all data output pins, and ignores all read/write attempts for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.2 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.2 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory. Note that the CE# pin should only go to V_{IL} after RESET# has gone to V_{IH}. Keeping CE# at V_{IL} from power up through the first read could cause the first read to retrieve erroneous data.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a *0* (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is *1*), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the tables in *AC Characteristics* on page 38 for RESET# parameters and to Figure 18.2 on page 40 for the timing diagram. If V_{ID} (9.0 V – 11.0 V) is applied to the RESET# pin, the device will enter the Temporary Sector Group Unprotect mode. See *Temporary Sector Group Unprotect* on page 18 for more details on this feature.

7.8 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

7.9 Autoselect Mode

The autoselect mode provides manufacturer and device identification, sector group protection verification, and Secured Silicon Sector status through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} (9.0 V to 11.0 V) on address pin A9. Address pins A6, A3, A2, A1, and A0 must be as shown in Table . In addition, when verifying sector group protection, the sector address must appear on the appropriate highest order address bits (see Table on page 12 and Table on page 14). Table shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7-DQ0.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table on page 28. This method does not require V_{ID}. See *Command Definitions* on page 23 for details on using the autoselect mode.

S29AS016J Autoselect Codes (High Voltage Method)

Description		CE#	OE#	WE#	A19 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15		DQ7 to DQ0
														BYTE = V_{IH}	BYTE = V_{IL}	
Manufacturer ID: Spansion		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	00h	X	01h
Device ID	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22h	X	7Eh
	Cycle 2	L	L	H	X	X	V_{ID}	X	L	X	H	H	L	22h	X	03h
	Cycle 3	L	L	H	X	X	V_{ID}	X	L	X	H	H	H	22h	X	04h (Top Boot), 03h (Bottom Boot)
Sector Group Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	X	01h (protected), 00h (unprotected)
Secured Silicon Sector Indicator Bit (DQ7), WP# protects highest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	89h (factory locked), 09h (not factory locked)
Secured Silicon Sector Indicator Bit (DQ7), WP# protects lowest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	91h (factory locked), 11h (not factory locked)

Legend
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care

Note
The autoselect codes may also be accessed in-system via command sequences. See Table on page 28.

7.10 Sector Address Tables

Sector Address Tables (Top Boot Device)

Sector	A19	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
										Byte Mode (x8)	Word Mode (x16)
SA0	0	0	0	0	0	X	X	X	64/32	000000–00FFFF	00000–07FFF
SA1	0	0	0	0	1	X	X	X	64/32	010000–01FFFF	08000–0FFFF
SA2	0	0	0	1	0	X	X	X	64/32	020000–02FFFF	10000–17FFF
SA3	0	0	0	1	1	X	X	X	64/32	030000–03FFFF	18000–1FFFF
SA4	0	0	1	0	0	X	X	X	64/32	040000–04FFFF	20000–27FFF
SA5	0	0	1	0	1	X	X	X	64/32	050000–05FFFF	28000–2FFFF
SA6	0	0	1	1	0	X	X	X	64/32	060000–06FFFF	30000–37FFF
SA7	0	0	1	1	1	X	X	X	64/32	070000–07FFFF	38000–3FFFF
SA8	0	1	0	0	0	X	X	X	64/32	080000–08FFFF	40000–47FFF
SA9	0	1	0	0	1	X	X	X	64/32	090000–09FFFF	48000–4FFFF
SA10	0	1	0	1	0	X	X	X	64/32	0A0000–0AFFFF	50000–57FFF
SA11	0	1	0	1	1	X	X	X	64/32	0B0000–0BFFFF	58000–5FFFF
SA12	0	1	1	0	0	X	X	X	64/32	0C0000–0CFFFF	60000–67FFF
SA13	0	1	1	0	1	X	X	X	64/32	0D0000–0DFFFF	68000–6FFFF
SA14	0	1	1	1	0	X	X	X	64/32	0E0000–0EFFFF	70000–77FFF
SA15	0	1	1	1	1	X	X	X	64/32	0F0000–0FFFFF	78000–7FFFF
SA16	1	0	0	0	0	X	X	X	64/32	100000–10FFFF	80000–87FFF
SA17	1	0	0	0	1	X	X	X	64/32	110000–11FFFF	88000–8FFFF
SA18	1	0	0	1	0	X	X	X	64/32	120000–12FFFF	90000–97FFF
SA19	1	0	0	1	1	X	X	X	64/32	130000–13FFFF	98000–9FFFF
SA20	1	0	1	0	0	X	X	X	64/32	140000–14FFFF	A0000–A7FFF

Sector Address Tables (Top Boot Device)

Sector	A19	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
										Byte Mode (x8)	Word Mode (x16)
SA21	1	0	1	0	1	X	X	X	64/32	150000–15FFFF	A8000–AFFFF
SA22	1	0	1	1	0	X	X	X	64/32	160000–16FFFF	B0000–B7FFF
SA23	1	0	1	1	1	X	X	X	64/32	170000–17FFFF	B8000–BFFFF
SA24	1	1	0	0	0	X	X	X	64/32	180000–18FFFF	C0000–C7FFF
SA25	1	1	0	0	1	X	X	X	64/32	190000–19FFFF	C8000–CFFFF
SA26	1	1	0	1	0	X	X	X	64/32	1A0000–1AFFFF	D0000–D7FFF
SA27	1	1	0	1	1	X	X	X	64/32	1B0000–1BFFFF	D8000–DFFFF
SA28	1	1	1	0	0	X	X	X	64/32	1C0000–1CFFFF	E0000–E7FFF
SA29	1	1	1	0	1	X	X	X	64/32	1D0000–1DFFFF	E8000–EFFFF
SA30	1	1	1	1	0	X	X	X	64/32	1E0000–1EFFFF	F0000–F7FFF
SA31	1	1	1	1	1	0	0	0	8/4	1F0000–1F1FFF	F8000–F8FFF
SA32	1	1	1	1	1	0	0	1	8/4	1F2000–1F3FFF	F9000–F9FFF
SA33	1	1	1	1	1	0	1	0	8/4	1F4000–1F5FFF	FA000–FAFFF
SA34	1	1	1	1	1	0	1	1	8/4	1F6000–1F7FFF	FB000–FBFFF
SA35	1	1	1	1	1	1	0	0	8/4	1F8000–1F9FFF	FC000–FCFFF
SA36	1	1	1	1	1	1	0	1	8/4	1FA000–1FBFFF	FD000–FDFFF
SA37	1	1	1	1	1	1	1	0	8/4	1FC000–1FDFFF	FE000–FEFFF
SA38	1	1	1	1	1	1	1	1	8/4	1FE000–1FFFFF	FF000–FFFFF

Note
Address range is A19:A-1 in byte mode and A19:A0 in word mode. See *Word/Byte Configuration on page 9**.*

Sector Address Tables (Bottom Boot Device)

Sector	A19	A18	A17	A16	A15	A14	A13	A12	Sector Size (Kbytes/ Kwords)	Address Range (in hexadecimal)	
										Byte Mode (x8)	Word Mode (x16)
SA0	0	0	0	0	0	0	0	0	8/4	000000–001FFF	00000–00FFF
SA1	0	0	0	0	0	0	0	1	8/4	002000–003FFF	01000–01FFF
SA2	0	0	0	0	0	0	1	0	8/4	004000–005FFF	02000–02FFF
SA3	0	0	0	0	0	0	1	1	8/4	006000–007FFF	03000–03FFF
SA4	0	0	0	0	0	1	0	0	8/4	008000–009FFF	04000–04FFF
SA5	0	0	0	0	0	1	0	1	8/4	00A000–00BFFF	05000–05FFF
SA6	0	0	0	0	0	1	1	0	8/4	00C000–00DFFF	06000–06FFF
SA7	0	0	0	0	0	1	1	1	8/4	00E000–00FFFF	07000–07FFF
SA8	0	0	0	0	1	X	X	X	64/32	010000–01FFFF	08000–0FFFF
SA9	0	0	0	1	0	X	X	X	64/32	020000–02FFFF	10000–17FFF
SA10	0	0	0	1	1	X	X	X	64/32	030000–03FFFF	18000–1FFFF
SA11	0	0	1	0	0	X	X	X	64/32	040000–04FFFF	20000–27FFF
SA12	0	0	1	0	1	X	X	X	64/32	050000–05FFFF	28000–2FFFF
SA13	0	0	1	1	0	X	X	X	64/32	060000–06FFFF	30000–37FFF
SA14	0	0	1	1	1	X	X	X	64/32	070000–07FFFF	38000–3FFFF
SA15	0	1	0	0	0	X	X	X	64/32	080000–08FFFF	40000–47FFF
SA16	0	1	0	0	1	X	X	X	64/32	090000–09FFFF	48000–4FFFF
SA17	0	1	0	1	0	X	X	X	64/32	0A0000–0AFFFF	50000–57FFF
SA18	0	1	0	1	1	X	X	X	64/32	0B0000–0BFFFF	58000–5FFFF
SA19	0	1	1	0	0	X	X	X	64/32	0C0000–0CFFFF	60000–67FFF
SA20	0	1	1	0	1	X	X	X	64/32	0D0000–0DFFFF	68000–6FFFF
SA21	0	1	1	1	0	X	X	X	64/32	0E0000–0EFFFF	70000–77FFF
SA22	0	1	1	1	1	X	X	X	64/32	0F0000–0FFFFF	78000–7FFFF
SA23	1	0	0	0	0	X	X	X	64/32	100000–10FFFF	80000–87FFF
SA24	1	0	0	0	1	X	X	X	64/32	110000–11FFFF	88000–8FFFF
SA25	1	0	0	1	0	X	X	X	64/32	120000–12FFFF	90000–97FFF
SA26	1	0	0	1	1	X	X	X	64/32	130000–13FFFF	98000–9FFFF
SA27	1	0	1	0	0	X	X	X	64/32	140000–14FFFF	A0000–A7FFF
SA28	1	0	1	0	1	X	X	X	64/32	150000–15FFFF	A8000–AFFFF
SA29	1	0	1	1	0	X	X	X	64/32	160000–16FFFF	B0000–B7FFF
SA30	1	0	1	1	1	X	X	X	64/32	170000–17FFFF	B8000–BFFFF
SA31	1	1	0	0	0	X	X	X	64/32	180000–18FFFF	C0000–C7FFF
SA32	1	1	0	0	1	X	X	X	64/32	190000–19FFFF	C8000–CFFFF
SA33	1	1	0	1	0	X	X	X	64/32	1A0000–1AFFFF	D0000–D7FFF
SA34	1	1	0	1	1	X	X	X	64/32	1B0000–1BFFFF	D8000–DFFFF
SA35	1	1	1	0	0	X	X	X	64/32	1C0000–1CFFFF	E0000–E7FFF
SA36	1	1	1	0	1	X	X	X	64/32	1D0000–1DFFFF	E8000–EFFFF
SA37	1	1	1	1	0	X	X	X	64/32	1E0000–1EFFFF	F0000–F7FFF
SA38	1	1	1	1	1	X	X	X	64/32	1F0000–1FFFFF	F8000–FFFFF

Note
Address range is A19:A-1 in byte mode and A19:A0 in word mode. See the Word/Byte Configuration on page 9.

7.11 Sector Group Protection/Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector group (see Table on page 12 to Table on page 16). The hardware sector group unprotection feature re-enables both program and erase operations in previously protected sector groups. Sector group protection/unprotection can be implemented via two methods.

Sector group protection/unprotection requires VID on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 7.1 on page 17 shows the algorithms and Figure 18.1 on page 39 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector group unprotect, all unprotected sector groups must first be protected prior to the first sector group unprotect write cycle.

The device is shipped with all sector groups unprotected. Spansion offers the option of programming and protecting sector groups at its factory prior to shipping the device through Spansion Programming Service. Contact a Spansion representative for details.

It is possible to determine whether a sector group is protected or unprotected. See *Autoselect Mode* on page 11 for details.

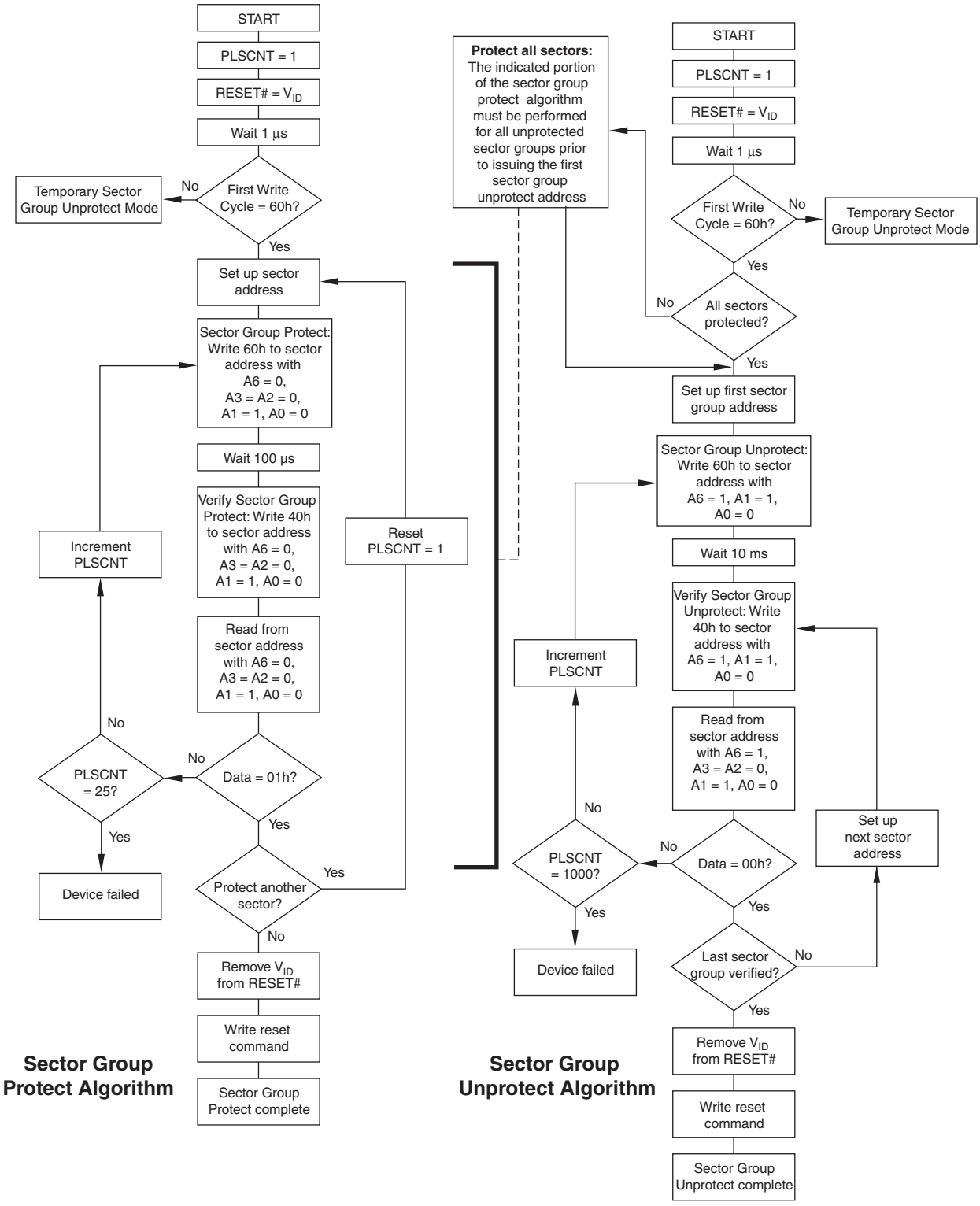
AS016J Top Boot Device Sector/Sector Group Protection

Sector / Sector Block	A19	A18	A17	A16	A15	A14	A13	A12	Sector / Sector Block Size
SA0-SA3	0	0	0	X	X	X	X	X	256 (4x64) Kbytes
SA4-SA7	0	0	1	X	X	X	X	X	256 (4x64) Kbytes
SA8-SA11	0	1	0	X	X	X	X	X	256 (4x64) Kbytes
SA12-SA15	0	1	1	X	X	X	X	X	256 (4x64) Kbytes
SA16-SA19	1	0	0	X	X	X	X	X	256 (4x64) Kbytes
SA20-SA23	1	0	1	X	X	X	X	X	256 (4x64) Kbytes
SA24-SA27	1	1	0	X	X	X	X	X	256 (4x64) Kbytes
SA28-SA29	1	1	1	0	X	X	X	X	128 (2x64) Kbytes
SA30	1	1	1	1	0	X	X	X	64 Kbytes
SA31	1	1	1	1	1	0	0	0	8 Kbytes
SA32	1	1	1	1	1	0	0	1	8 Kbytes
SA33	1	1	1	1	1	0	1	0	8 Kbytes
SA34	1	1	1	1	1	0	1	1	8 Kbytes
SA35	1	1	1	1	1	1	0	0	8 Kbytes
SA36	1	1	1	1	1	1	0	1	8 Kbytes
SA37	1	1	1	1	1	1	1	0	8 Kbytes
SA38	1	1	1	1	1	1	1	1	8 Kbytes

AS016J Bottom Boot Device Sector/Sector Group Protection

Sector / Sector Block	A19	A18	A17	A16	A15	A14	A13	A12	Sector / Sector Block Size
SA0	0	0	0	0	0	0	0	0	8 Kbytes
SA1	0	0	0	0	0	0	0	1	8 Kbytes
SA2	0	0	0	0	0	0	1	0	8 Kbytes
SA3	0	0	0	0	0	0	1	1	8 Kbytes
SA4	0	0	0	0	0	1	0	0	8 Kbytes
SA5	0	0	0	0	0	1	0	1	8 Kbytes
SA6	0	0	0	0	0	1	1	0	8 Kbytes
SA7	0	0	0	0	0	1	1	1	8 Kbytes
SA8	0	0	0	0	1	X	X	X	64 Kbytes
SA9-SA10	0	0	0	1	X	X	X	X	128 (2x64) Kbytes
SA11-SA14	0	0	1	X	X	X	X	X	256 (4x64) Kbytes
SA15-SA18	0	1	0	X	X	X	X	X	256 (4x64) Kbytes
SA19-SA22	0	1	1	X	X	X	X	X	256 (4x64) Kbytes
SA23-SA26	1	0	0	X	X	X	X	X	256 (4x64) Kbytes
SA27-SA30	1	0	1	X	X	X	X	X	256 (4x64) Kbytes
SA31-SA34	1	1	0	X	X	X	X	X	256 (4x64) Kbytes
SA35-SA38	1	1	1	X	X	X	X	X	256 (4x64) Kbytes

Figure 7.1 In-System Sector Group Protect/Unprotect Algorithms

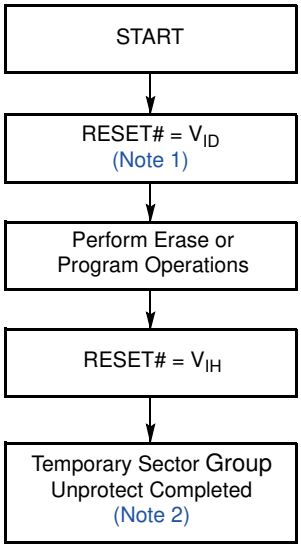


Note
If WP# = V_{IL}, the top or bottom two address sectors remains protected for boot sector devices).

7.12 Temporary Sector Group Unprotect

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Group Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 7.2 shows the algorithm, and Figure 18.10 on page 45 shows the timing diagrams, for this feature. If the WP# pin is at V_{IL}, the sectors protected by the WP# input will remain protected during the Temporary Sector Group Unprotect mode.

Figure 7.2 Temporary Sector Group Unprotect Operation



Notes

1. *All protected sector groups unprotected.*
2. *All previously protected sector groups are protected once again.*

7.13 Write Protect (WP#)

The Write Protect function provides a hardware method of protecting certain boot sectors without using VID. This function is one of two provided by the WP# pin.

If the system asserts V_{IL} on the WP# pin, the device disables program and erase functions in the two outermost 8-Kbyte boot sectors independently of whether those sectors were protected or unprotected using the method described in Section 7.11, *Sector Group Protection/Unprotection* on page 15. The two outermost 8-Kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

If the system asserts V_{IH} on the WP# pin, the device reverts to whether the two outermost 8-KByte boot sectors were last set to be protected or unprotected. That is, sector group protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in Section 7.11.

The WP# contains an internal pull-up; when unconnected, WP is at V_{IH}.

7.14 Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table on page 28 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

7.14.1 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

7.14.2 Write Pulse *Glitch* Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

7.14.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero (V_{IL}) while OE# is a logical one (V_{IH}).

7.14.4 Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to reading array data on power-up.

8. Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector feature provides a 256-byte Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector uses a Secured Silicon Sector Indicator Bit (DQ7) to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory-locked part. This ensures the security of the ESN once the product is shipped to the field.

Spansion offers the device with the Secured Silicon Sector either factory-locked or customer-lockable. The factory-locked version is always protected when shipped from the factory, and has the Secured Silicon Sector Indicator Bit permanently set to a *1*. The customer-lockable version is shipped with the Secured Silicon Sector group unprotected, allowing customers to utilize the that sector in any manner they choose. The customer-lockable version has the Secured Silicon Sector Indicator Bit permanently set to a *0*. Thus, the Secured Silicon Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The system accesses the Secured Silicon Sector through a command sequence (see *Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence* on page 24). After the system writes the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the boot sectors.

8.1 Factory Locked: Secured Silicon Sector Programmed and Protected at the Factory

In a factory locked device, the Secured Silicon Sector is protected when the device is shipped from the factory. The Secured Silicon Sector cannot be modified in any way. The device is available pre-programmed with one of the following:

- A random, secure ESN only.
- Customer code through the ExpressFlash service.
- Both a random, secure ESN and customer code through the ExpressFlash service.

In devices that have an ESN, a Bottom Boot device has the 16-byte (8-word) ESN in sector 0 at addresses 00000h–0000Fh in byte mode (or 00000h–00007h in word mode). In the Top Boot device, the ESN is in sector 38 at addresses 1FFFF0–1FFFFF in byte mode (or FFFF8–FFFFF in word mode).

Customers may opt to have their code programmed by Spansion through the Spansion ExpressFlash service. Spansion programs the customer's code, with or without the random ESN. The devices are then shipped from the Spansion factory with the Secured Silicon Sector permanently locked. Contact a Spansion representative for details on using the Spansion ExpressFlash service.

8.2 Customer Lockable: Secured Silicon Sector NOT Programmed or Protected at the Factory

The customer lockable version allows the Secured Silicon Sector to be programmed once, and then permanently locked after it ships from Spansion. Note that the unlock bypass function is not available when programming the Secured Silicon Sector.

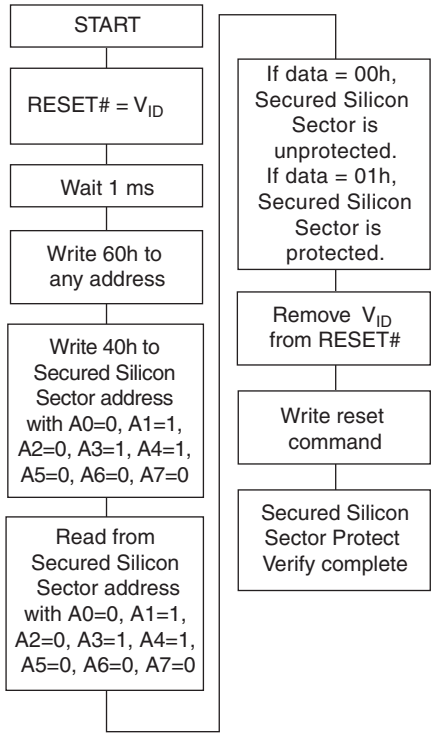
The Secured Silicon Sector area can be protected using the following procedures:

- Write the three-cycle Enter Secured Silicon Region command sequence, and then follow the in-system sector group protect algorithm as shown in Figure 7.1 on page 17, substituting the sector group address with the Secured Silicon Sector group address (A0=0, A1=1, A2=0, A3=1, A4=1, A5=0, A6=0, A7=0). This allows in-system protection of the Secured Silicon Sector without raising any device pin to a high voltage. Note that this method is only applicable to the Secured Silicon Sector.
- To verify the protect/unprotect status of the Secured Silicon Sector, follow the algorithm shown in Figure 8.1 on page 21.

Once the Secured Silicon Sector is locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing the remainder of the array.

The Secured Silicon Sector protection must be used with caution since, once protected, there is no procedure available for unprotecting the Secured Silicon Sector area, and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

Figure 8.1 Secured Silicon Sector Protect Verify



9. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Table to Table on page 23. In word mode, the upper address bits (A7–MSB) must be all zeros. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table to Table on page 23. The system must write the reset command to return the device to the autoselect mode.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/products/nvd/overview/cfi.html. Alternatively, contact a Spansion representative for copies of these documents.

CFI Query Identification String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table

CFI Query Identification String (Continued)

17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

System Interface String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
1Bh	36h	0017h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0019h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0003h	Typical timeout per single byte/word write 2^N µs
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	0009h	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0005h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Device Geometry Definition

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
27h	4Eh	0015h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0002h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	62h 64h 66h 68h	001Eh 0000h 0000h 0001h	Erase Block Region 2 Information
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information

Primary Vendor-Specific Extended Query

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0033h	Minor version number, ASCII
45h	8Ah	000Ch	Address Sensitive Unlock 0 = Required 1 = Not Required
46h	8Ch	0002h	Erase Suspend 0 = Not Supported 1 = To Read Only 2 = To Read & Write
47h	8Eh	0001h	Sector Group Protect 0 = Not Supported X= Number of sectors in smallest sector group
48h	90h	0001h	Sector Group Temporary Unprotect 00 = Not Supported 01 = Supported
49h	92h	0004h	Sector Group Protect/Unprotect scheme 01 = 29F040 mode 02 = 29F016 mode, 03 = 29F400 mode 04 = 29LV800A mode
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported 01 = Supported
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported 01 = Supported
4Ch	98h	0000h	Page Mode Type 00 = Not Supported 01 = 4 Word Page 02 = 8 Word Page
4Dh	9Ah	0000h	ACC (Acceleration) Supply Minimum 00 = Not Supported D7-D4: Volt D3-D0: 100 mV
4Eh	9Ch	0000h	ACC (Acceleration) Supply Maximum 00 = Not Supported D7-D4: Volt D3-D0: 100 mV
4Fh	9Eh	00XXh	WP# Protection 02 = Bottom Boot Device with WP Protect 03 = Top Boot Device with WP Protect
50h	A0h	0000h	Program Suspend 00 = Not Supported 01 = Supported

10. Command Definitions

Writing specific address and data commands or sequences into the command register initiates device operations. Table on page 28 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** resets the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to the appropriate timing diagrams in *AC Characteristics* on page 38.

10.1 Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See *Erase Suspend/Erase Resume Commands* on page 27 for more information on this mode.

The system *must* issue the reset command to re-enable the device for reading array data if DQ5 goes high, or while in the autoselect mode. See *Reset Command* on page 24.

See also *Requirements for Reading Array Data* on page 10 for more information. The *Read Operations* on page 38 provides the read parameters, and Figure 18.1 on page 39 shows the timing diagram.

10.2 Reset Command

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command *must* be written to return to reading array data (also applies to autoselect during Erase Suspend).

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to reading array data (also applies during Erase Suspend).

10.3 Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and devices codes, and determine whether or not a sector is protected. Table on page 28 shows the address and data requirements. This method is an alternative to that shown in Table on page 12, which is intended for PROM programmers and requires V_{ID} on address bit A9.

The autoselect command sequence is initiated by writing two unlock cycles, followed by the autoselect command. The device then enters the autoselect mode, and the system may read at any address any number of times, without initiating another command sequence.

A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h in word mode (or 04h in byte mode) returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table on page 12 and Table on page 14 for valid sector addresses.

The system must write the reset command to exit the autoselect mode and return to reading array data.

10.4 Enter Secured Silicon Sector/Exit Secured Silicon Sector Command Sequence

The Secured Silicon Sector region provides a secured data area containing a random, sixteen-byte electronic serial number (ESN). The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector command sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector command sequence. The Exit Secured Silicon Sector command sequence returns the device to normal operation. Table shows the addresses and data requirements for both command sequences. Note that the unlock bypass mode is not

available when the device enters the Secured Silicon Sector. For further information, see *Secured Silicon Sector Flash Memory Region* on page 20.

10.5 Word/Byte Program Command Sequence

The system may program the device by word or byte, depending on the state of the BYTE# pin. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table on page 28 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. See *Write Operation Status* on page 31 for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the programming operation. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from a *0* back to a *1*.** Attempting to do so may halt the operation and set DQ5 to *1*, or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still *0*. Only erase operations can convert a *0* to a *1*.

10.6 Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table on page 28 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h; the second cycle the data F0h. Addresses are don't care for both cycles. The device then returns to reading array data.

Figure 10.1 on page 26 illustrates the algorithm for the program operation. See *Erase/Program Operations* on page 42 for parameters, and to Figure 18.5 on page 42 for timing diagrams.