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S29CD032J
S29CD016J
S29CL032J
S29CL016J

32/16 Mbit, 2.6/3.3 V, Dual Boot, Simultaneous Read/Write, Burst Flash

General Description

The Spansion S29CD-J and S29CL-J devices are Floating Gate products fabricated in 110-nm process technology. These burst-mode Flash devices are capable of performing simultaneous read and write operations with zero latency on two separate banks, using separate data and address pins. These products can operate up to 75 MHz (32 Mb) or 66 MHz (16 Mb), and use a single V_{CC} of 2.5V to 2.75V (S29CD-J) or 3.0V to 3.6V (S29CL-J) that make them ideal for today's demanding automotive applications.

Distinctive Characteristics

- Single 2.6V (S29CD-J) or 3.3V (S29CL-J) for read/program/erase
- 110 nm Floating Gate Technology
- Simultaneous Read/Write operation with zero latency
- x32 Data Bus
- Dual Boot Sector Configuration (top and bottom)
- Flexible Sector Architecture
  - CD016J and CL016J: Eight 2k Double word, Thirty 16k Double word, and Eight 2k Double Word sectors
  - CD032J and CL032J: Eight 2k Double word, Sixty-two 16k Double Word, and Eight 2k Double Word sectors
- VersatileI/O™ control (1.65V to 3.6V)
- Programmable Burst Interface
  - Linear for 2, 4, and 8 double word burst with wrap around
- Secured Silicon Sector that can be either factory or customer locked
- 20 year data retention (typical)
- Cycling Endurance: 1 million write cycles per sector (typical)
- Command set compatible with JEDEC (JC42.4) standard
- Supports Common Flash Interface (CFI)
- Extended Temperature range
- Persistent and Password methods of Advanced Sector Protection
- Unlock Bypass program command to reduce programming time
- ACC input pin to reduce factory programming time
- Data Polling bits indicate program and erase operation completion
- Hardware (WP#) protection of two outermost sectors in the large bank
- Ready/Busy (RY/BY#) output indicates data available to system
- Suspend and Resume commands for Program and Erase Operation
- Offered Packages
  - 80-pin PQFP
  - 80-ball Fortified BGA (13 x 11 mm and 11 x 9mm versions)
  - Pb-free package option available
  - Known Good Die

Performance Characteristics

Read Access Times				
Speed Option (MHz)	75 (32 Mb only)	66	56	40
Max Asynch. Access Time, ns (t_{ACC})	54	54	54	54
Max Synch. Burst Access, ns (t_{BACC})	8	8	8	8
Min Initial Clock Delay (clock cycles)	5	5	5	4
Max CE# Access Time, ns (t_{CE})	54	54	54	54
Max OE# Access time, ns (t_{OE})	20	20	20	20

Current Consumption (Max values)	
Continuous Burst Read @ 75 MHz	90 mA
Program	50 mA
Erase	50 mA
Standby Mode	60 µA

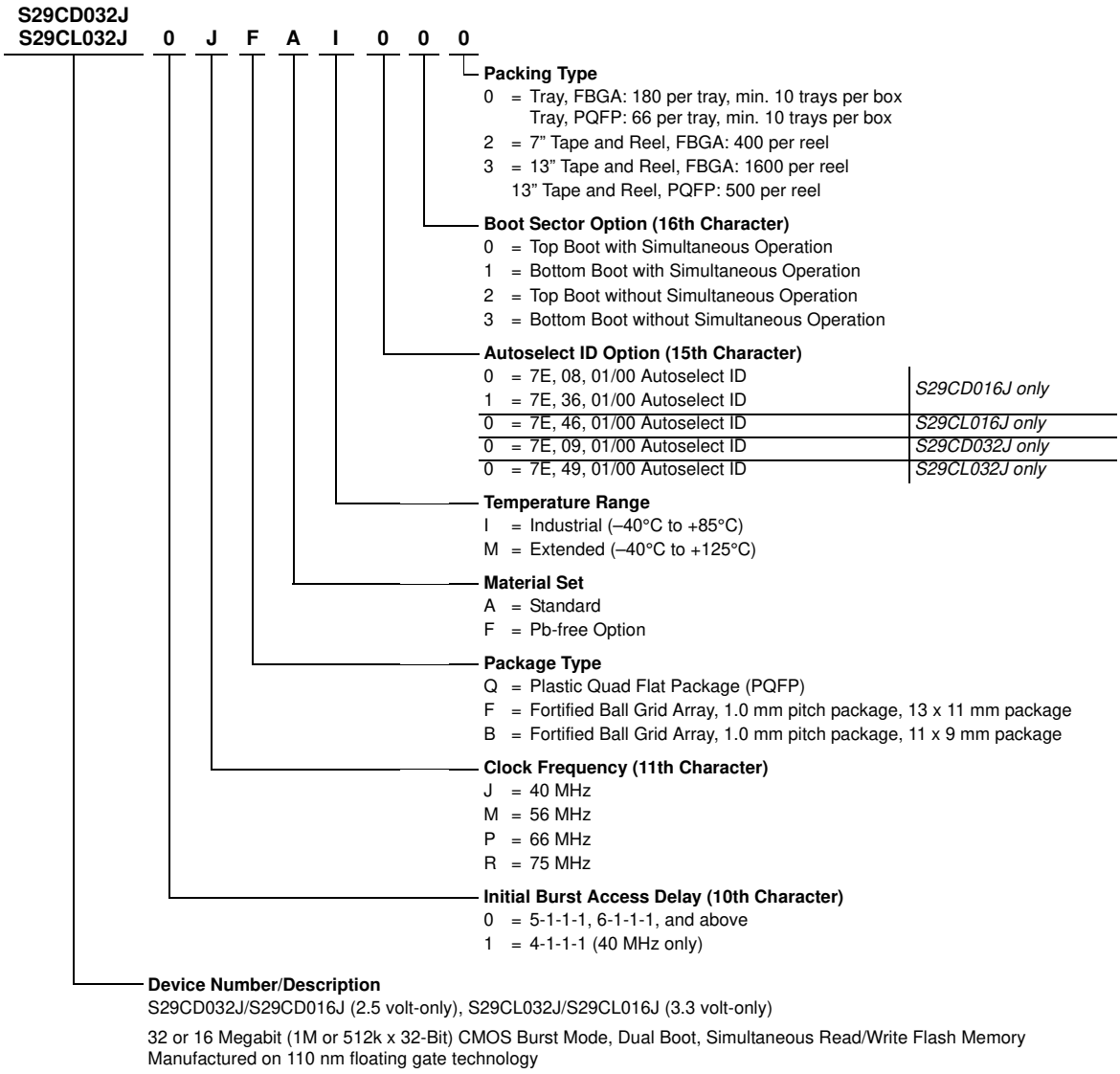
Typical Program and Erase Times	
Double Word Programming	18 µs
Sector Erase	1.0 s

Notice for the 32Mb S29CD-J and S29CL-J devices only:
Please refer to the application note "*Recommended Mode of Operation for Spansion® 110 nm S29CD032J/S29CL032J Flash Memory*" publication number *S29CD-CL032J_Recommend_AN* for programming best practices.

Contents

1. Ordering Information

The order number (Valid Combination) is formed by the following:



1.1 Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S29CD-J/CL-J Valid Combinations								
Device Number	**Initial Burst Access Delay**	**Clock Frequency**	**Package Type**	**Material Set**	**Temperature Range**	**Autoselect ID Option**	**Boot Sector Option**	**Packing Type**
S29CD016J	0, 1	J	Q	A, F	I, M	0, 1	0, 1, 2, 3	0, 3
			B, F					0, 2, 3
	0	M, P	Q					0, 3
			B, F					0, 2, 3
S29CL016J	0, 1	J	Q			0		0, 3
			B, F					0, 2, 3
	0	M, P	Q					0, 3
			B, F					0, 2, 3
S29CD032J	0, 1	J	Q					0, 3
			B, F					0, 2, 3
	0	M, P	Q					0, 3
			B, F					0, 2, 3
		R	Q				0, 1 (2)	0, 3
							2, 3	
			B, F				0, 1 (2)	0, 2, 3
							2, 3	
S29CL032J	0, 1	J	Q				0, 1, 2, 3	0, 3
			B, F					0, 2, 3
	0	M, P	Q					0, 3
			B, F					0, 2, 3
		R	Q				0, 1 (2)	0, 3
							2, 3	
			B, F				0, 1 (2)	0, 2, 3
							2, 3	

Notes:

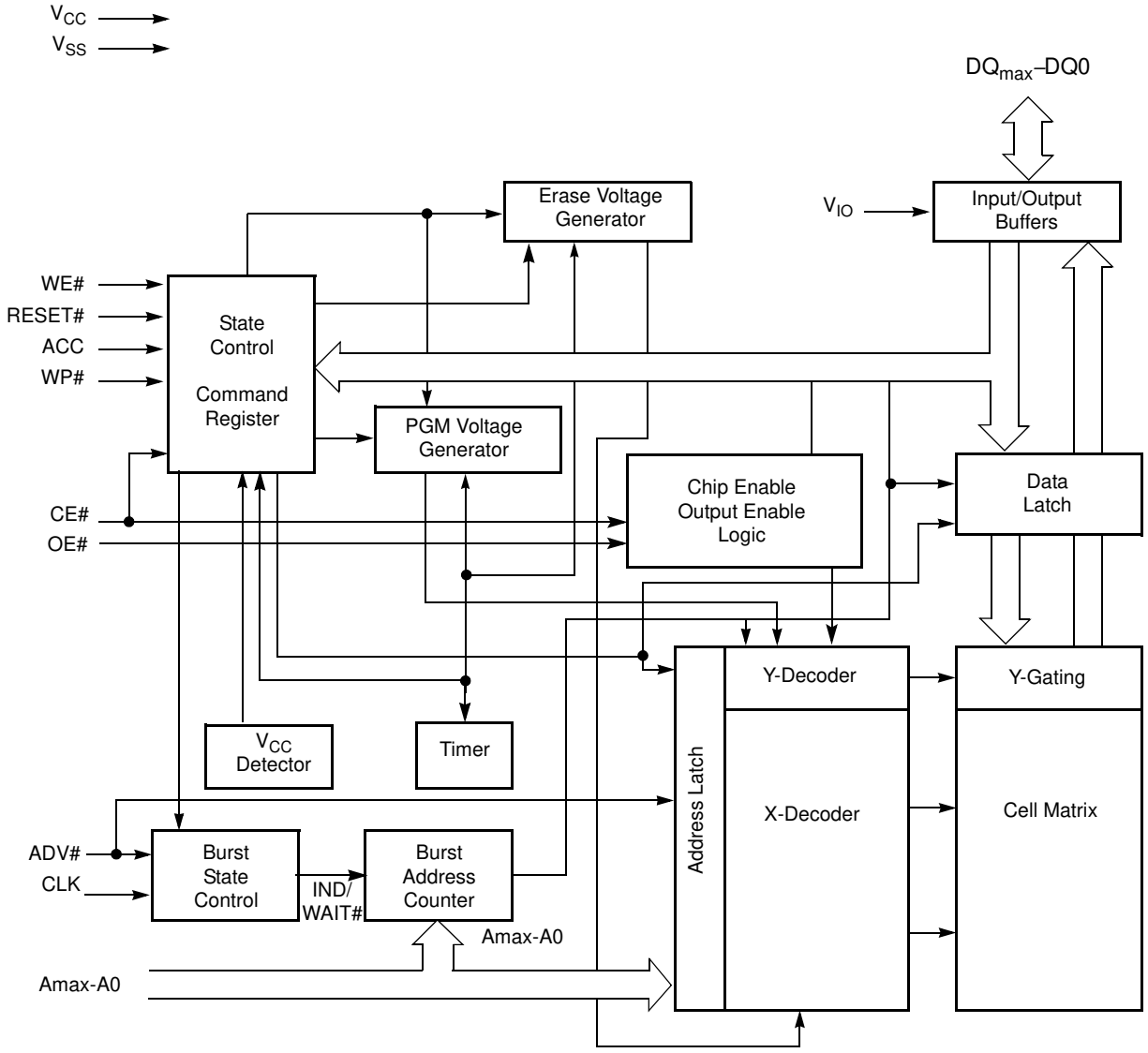
1. *The ordering part number that appears on BGA packages omits the leading "S29".*
2. *Contact factory for availability.*

2. Input/Output Descriptions and Logic Symbols

Table identifies the input and output package connections provided on the device.

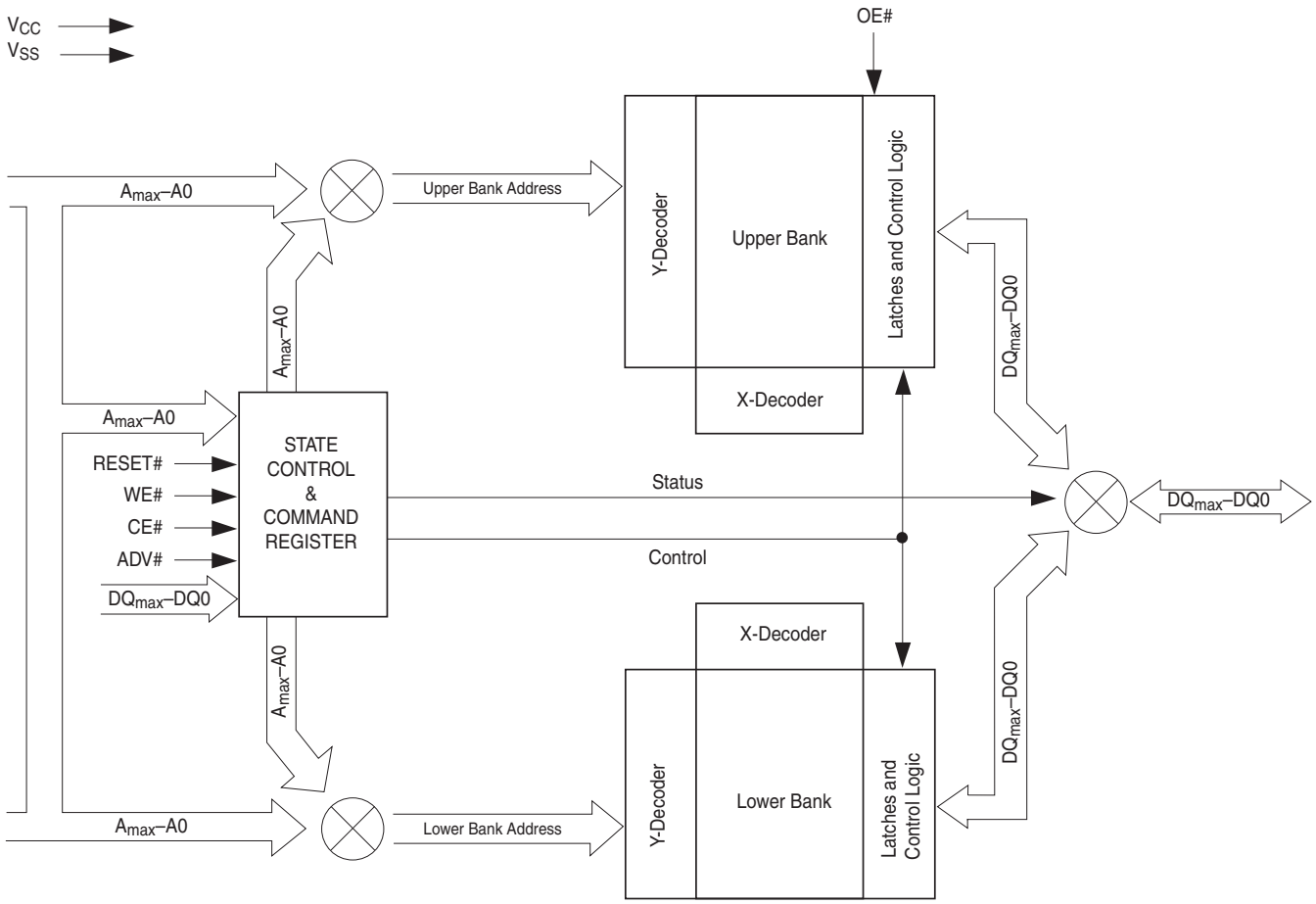
Symbol	Type	Description
A19-A0	Input	Address lines for S29CD-J and S29CL-J (A18-A0 for 16 Mb and A19-A0 for 32 Mb). A9 supports 12V autoselect input.
DQ31-DQ0	I/O	Data input/output
CE#	Input	Chip Enable. This signal is asynchronous relative to CLK for the burst mode.
OE#	Input	Output Enable. This signal is asynchronous relative to CLK for the burst mode.
WE#	Input	Write Enable
V_{CC}	Supply	Device Power Supply. This signal is asynchronous relative to CLK for the burst mode.
V_{IO}	Supply	VersatileI/O™ Input.
V_{SS}	Supply	Ground
NC	No Connect	Not connected internally
RY/BY#	Output	Ready/Busy output and open drain which require a external pull up resistor. When RY/BY# = V_{OH}, the device is ready to accept read operations and commands. When RY/BY# = V_{OL}, the device is either executing an embedded algorithm or the device is executing a hardware reset operation.
CLK	Input	Clock Input that can be tied to the system or microprocessor clock and provides the fundamental timing and internal operating frequency.
ADV#	Input	Load Burst Address input. Indicates that the valid address is present on the address inputs.
IND#	Output	End of burst indicator for finite bursts only. IND is low when the last word in the burst sequence is at the data outputs.
WAIT#	Output	Provides data valid feedback only when the burst length is set to continuous.
WP#	Input	Write Protect Input. At V_{IL}, disables program and erase functions in two outermost sectors of the large bank.
ACC	Input	Acceleration input. At V_{HH}, accelerates erasing and programming. When not used for acceleration, ACC = V_{SS} or V_{CC}.
RESET#	Input	Hardware Reset.

3. Block Diagram



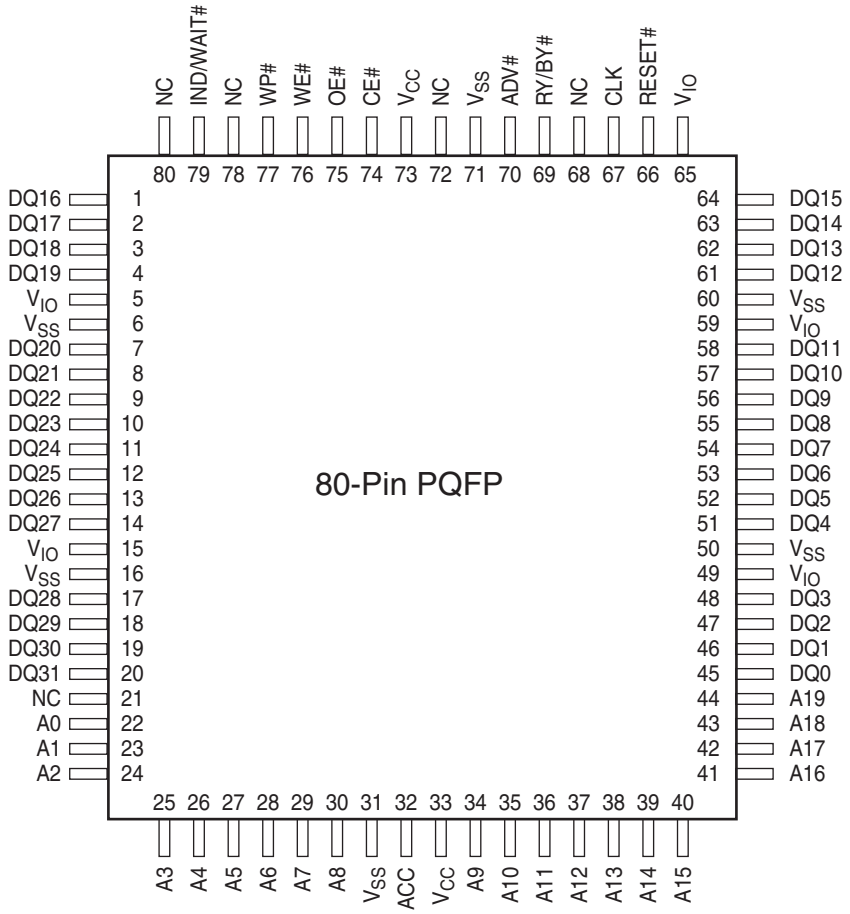
Note
Address bus is A19–A0 for 32 Mb device, A18–A0 for 16 Mb device. Data bus is D31–DQ0.

4. Block Diagram of Simultaneous Read/Write Circuit



5. Physical Dimensions/Connection Diagrams

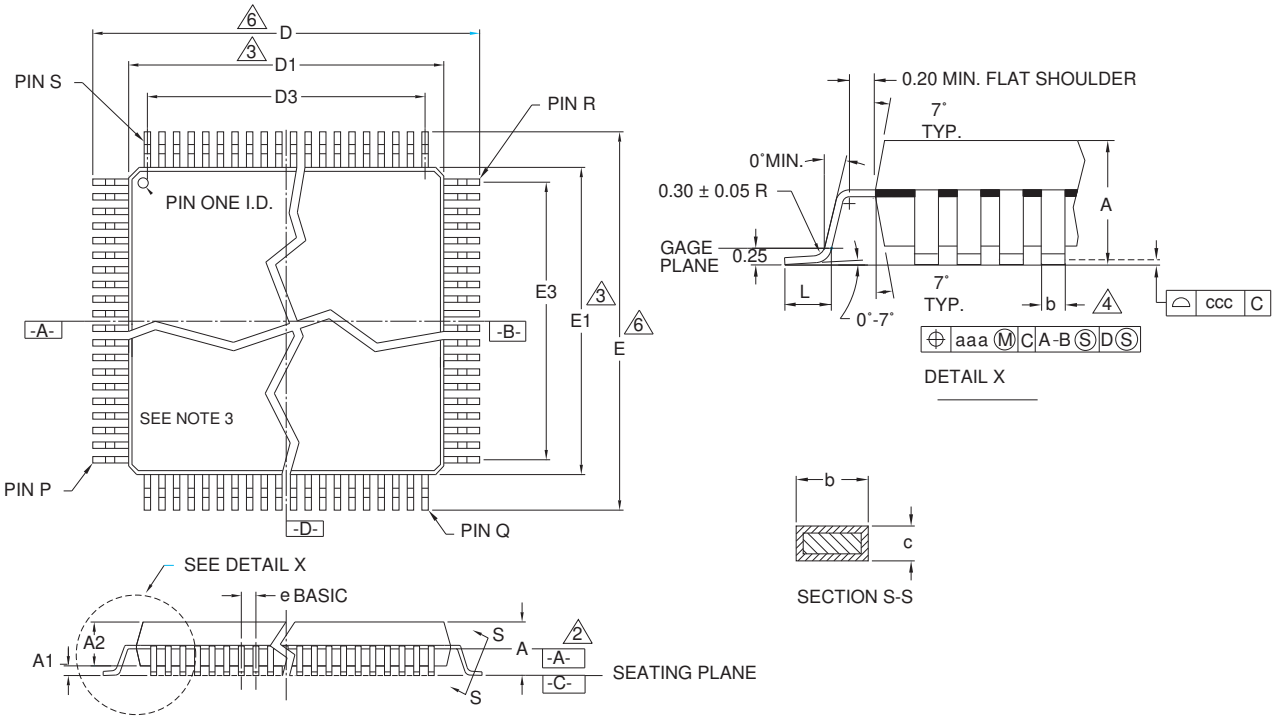
5.1 80-Pin PQFP Connection Diagram



Notes

1. *On 16 Mb device, pin 44 (A19) is NC.*
2. *Pin 69 (RY/BY#) is Open Drain and requires an external pull-up resistor.*

5.2 PQR080–80-Lead Plastic Quad Flat Package Physical Dimensions



PACKAGE	PQR 080			NOTES
JEDEC	MO-108(B)CB-1			
SYMBOL	MIN	NOM	MAX	
A	--	--	3.35	
A1	0.25	--	--	
A2	2.70	2.80	2.90	
b	0.30	--	0.45	SEE NOTE 4
c	0.15	--	0.23	
D	17.00	17.20	17.40	
D1	13.90	14.00	14.10	SEE NOTE 3
D3	--	12.0	--	REFERENCE
e	--	0.80	--	BASIC, SEE NOTE 7
E	23.00	23.20	23.40	
E1	19.90	20.00	20.10	SEE NOTE 3
E3	--	18.40	--	REFERENCE
aaa	---	0.20	---	
ccc	0.10			
L	0.73	0.88	1.03	
P	24			
Q	40			
R	64			
S	80			

NOTES:

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M-1982.
2. DATUM PLANE -A- IS LOCATED AT THE MOLD PARTING LINE AND IS COINCIDENT WITH THE BOTTOM OF THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY.
3. DIMENSIONS "D1" AND "E1" DO NOT INCLUD MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS "D1" AND "E1" INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -A-
4. DIMENSION "B" DOES NOT INCLUDE DAMBAR PROTRUSION.
5. CONTROLLING DIMENSIONS: MILLIMETER.
6. DIMENSIONS "D" AND "E" ARE MEASURED FROM BOTH INNERMOST AND OUTERMOST POINTS.
7. DEVIATION FROM LEAD-TIP TRUE POSITION SHALL BE WITHIN ±0.0076 mm FOR PITCH > 0.5 mm AND WITHIN ±0.04 FOR PITCH ≤ 0.5 mm.
8. LEAD COPLANARITY SHALL BE WITHIN: (REFER TO 06-500)
   1 - 0.10 mm FOR DEVICES WITH LEAD PITCH OF 0.65 - 0.80 mm
   2 - 0.076 mm FOR DEVICES WITH LEAD PITCH OF 0.50 mm.
   COPLANARITY IS MEASURED PER SPECIFICATION 06-500.
9. HALF SPAN (CENTER OF PACKAGE TO LEAD TIP) SHALL BE WITHIN ±0.0085".

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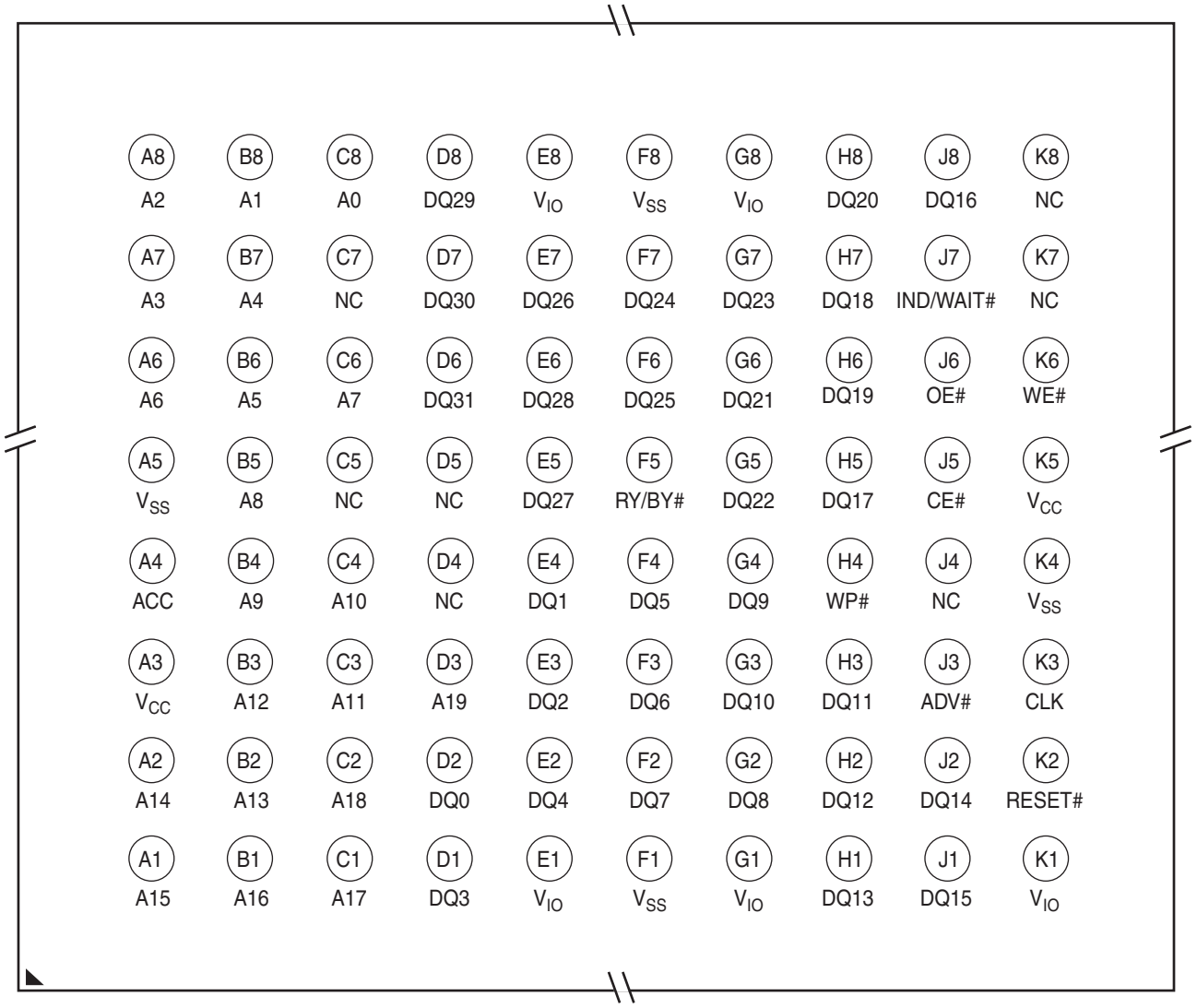
5.3 80-Ball Fortified BGA Connection Diagrams



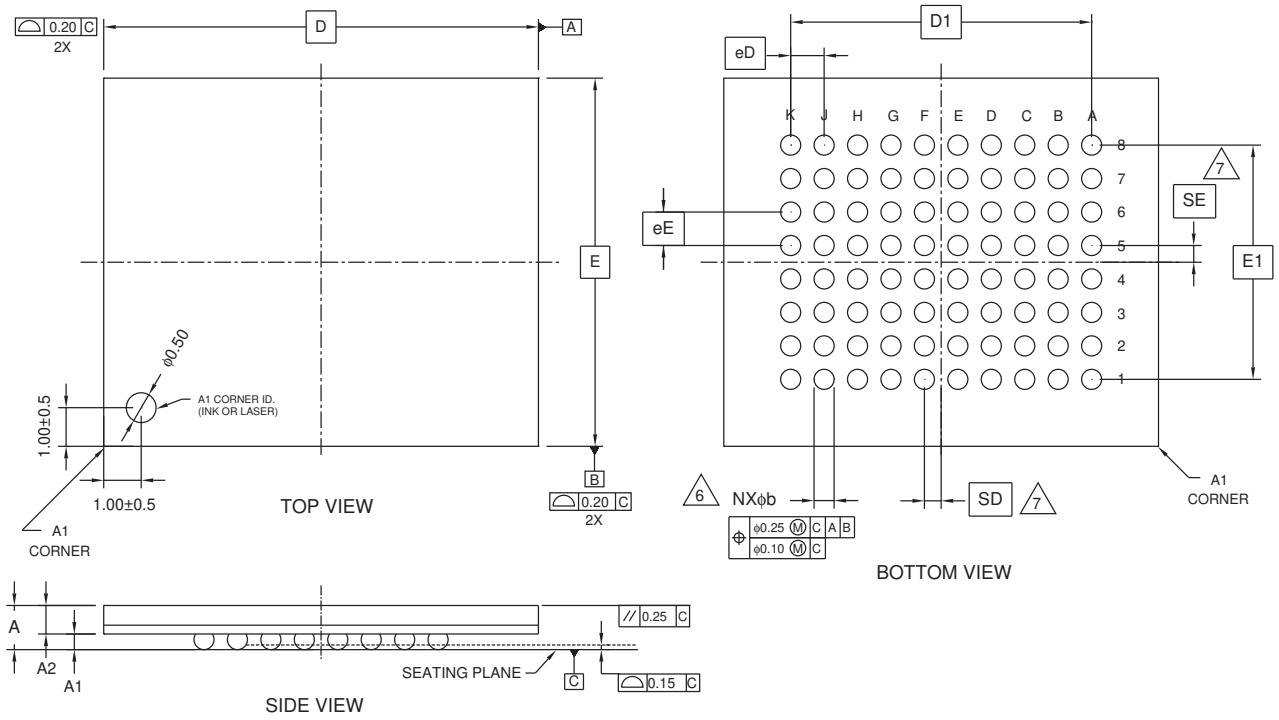
Notes

1. *On 16 Mb device, ball D3 (A19) is NC.*
2. *Ball F5 (RY/BY#) is Open Drain and requires an external pull-up resistor.*

5.4 Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (BGA). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

5.5 LAA080–80-ball Fortified Ball Grid Array (13 x 11 mm) Physical Dimensions



PACKAGE	LAA 080			NOTE
JEDEC	N/A			
	13.00 x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	--	--	1.40	PROFILE HEIGHT
A1	0.40	--	--	STANDOFF
A2	0.60	--	--	BODY THICKNESS
D	13.00 BSC.			BODY SIZE
E	11.00 BSC.			BODY SIZE
D1	9.00 BSC.			MATRIX FOOTPRINT
E1	7.00 BSC.			MATRIX FOOTPRINT
MD	10			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
N	80			BALL COUNT
φb	0.50	0.60	0.70	BALL DIAMETER
eD	1.00 BSC.			BALL PITCH - D DIRECTION
eE	1.00 BSC.			BALL PITCH - E DIRECTION
SD/SE	0.50 BSC			SOLDER BALL PLACEMENT

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION. N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW , SD OR SE = e/2
8. N/A
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

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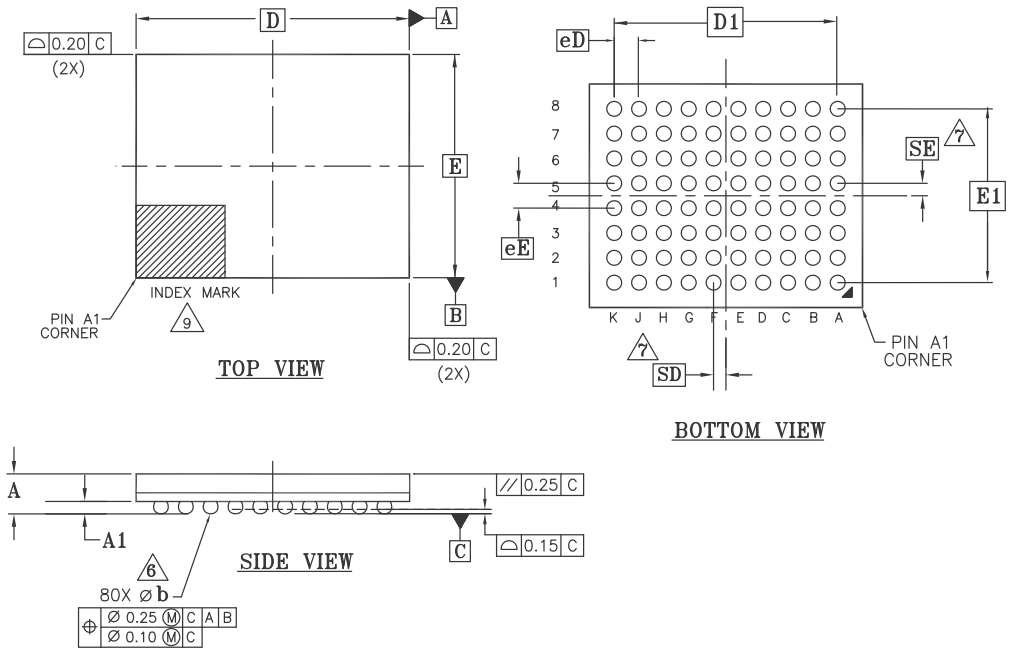
5.6 LAD080–80-ball Fortified Ball Grid Array (11 x 9 mm) Physical Dimensions



PACKAGE	LAD 080			
JEDEC	N/A			
D X E	11.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE
A1	0.35	0.45	0.55	BALL HEIGHT
D		11.00 BSC		BODY SIZE
E		9.00 BSC		BODY SIZE
D1		9.00 BSC		MATRIX FOOTPRINT
E1		7.00 BSC		MATRIX FOOTPRINT
MD		10		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
N		80		BALL COUNT
⌀b	0.55	0.65	0.75	BALL DIAMETER
eE		1.00 BSC		BALL PITCH
eD		1.00 BSC		BALL PITCH
SD / SE		0.50 BSC		SOLDER BALL PLACEMENT
		N/A		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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6. Additional Resources

Visit www.spansion.com to obtain the following related documents:

6.1 Application Notes

The following is a list of application notes related to this product. All Spansion application notes are available at http://www.spansion.com/Support/TechnicalDocuments/Pages/ApplicationNotes.aspx

- Using the Operation Status Bits in AMD Devices
- Understanding Page Mode Flash Memory Devices
- Common Flash Interface Version 1.4 Vendor Specific Extensions

6.2 Specification Bulletins

Contact your local sales office for details.

6.3 Hardware and Software Support

Downloads and related information on Flash device support is available at http://www.spansion.com/SUPPORT/Pages/Support.aspx

- Spansion low-level drivers
- Enhanced Flash drivers
- Flash file system

Downloads and related information on simulation modeling and CAD modeling support is available at http://www.spansion.com/Support/Pages/SimulationModels.aspx

VHDL and Verilog

- IBIS
- ORCAD

6.4 Contacting Spansion

Obtain the latest list of company locations and contact information on our web site at http://www.spansion.com/About/Pages/Locations.aspx

7. Product Overview

The S29CD-J and S29CL-J families consist of 32 Mb and 16 Mb, 2.6 volt-only (CD-J) or 3.3 volt-only (CL-J), simultaneous read/write, dual boot burst mode Flash devices optimized for today's automotive designs.

These devices are organized in 1,048,576 double words (32 Mb) or 524,288 double words (16 Mb) and are capable of linear burst read (2, 4, or 8 double words) with wraparound. (Note that 1 double word = 32 bits.) These products also offer single word programming with program/erase suspend and resume functionality. Additional features include:

- Advanced Sector Protection methods for protecting sectors as required.
- 256 bytes of Secured Silicon area for storing customer or factory secured information. The Secured Silicon Sector is One-Time Programmable.
- Electronic marking.

7.1 Memory Map

The S29CD-J and S29CL-J devices consist of two banks organized as shown in Table , Table , Table and Table .

S29CD016J/CL016J (Top Boot) Sector and Memory Address Map

	Sector	Sector Group	x32 Address Range (A18:A0)	Sector Size (KDwords)
Bank 0 (Note 2)	SA0 (Note 1)	SG0	00000h–007FFh	2
	SA1	SG1	00800h–00FFFh	2
	SA2	SG2	01000h–017FFh	2
	SA3	SG3	01800h–01FFFh	2
	SA4	SG4	02000h–027FFh	2
	SA5	SG5	02800h–02FFFh	2
	SA6	SG6	03000h–037FFh	2
	SA7	SG7	03800h–03FFFh	2
	SA8	SG8	04000h–07FFFh	16
	SA9		08000h–0BFFFh	16
	SA10		0C000h–0FFFFh	16
	SA11	SG9	10000h–13FFFh	16
	SA12		14000h–17FFFh	16
	SA13		18000h–1BFFFh	16
	SA14		1C000h–1FFFFh	16
Bank 1 (Note 2)	SA15	SG10	20000h–23FFFh	16
	SA16		24000h–27FFFh	16
	SA17		28000h–2BFFFh	16
	SA18		2C000h–2FFFFh	16
	SA19	SG11	30000h–33FFFh	16
	SA20		34000h–37FFFh	16
	SA21		38000h–3BFFFh	16
	SA22		3C000h–3FFFFh	16
	SA23	SG12	40000h–43FFFh	16
	SA24		44000h–47FFFh	16
	SA25		48000h–4BFFFh	16
	SA26		4C000h–4FFFFh	16
	SA27	SG13	50000h–53FFFh	16
	SA28		54000h–57FFFh	16
	SA29		58000h–5BFFFh	16
	SA30		5C000h–5FFFFh	16
	SA31	SG14	60000h–63FFFh	16
	SA32		64000h–67FFFh	16
	SA33		68000h–6BFFFh	16
	SA34		6C000h–6FFFFh	16
	SA35	SG15	70000h–73FFFh	16
	SA36		74000h–77FFFh	16
	SA37		78000h–7BFFFh	16
	SA38	SG16	7C000h–7C7FFh	2
	SA39	SG17	7C800h–7CFFFh	2
	SA40	SG18	7D000h–7D7FFh	2
	SA41	SG19	7D800h–7DFFFh	2
	SA42	SG20	7E000h–7E7FFh	2
	SA43	SG21	7E800h–7EFFFh	2
	SA44 (Note 3)	SG22	7F000h–7F7FFh	2
	SA45 (Note 3)	SG23	7F800h–7FFFFh	2

Notes

1. *Secured Silicon Sector overlays this sector when enabled.*
2. *The bank address is determined by A18 and A17. BA = 00 for Bank 0 and BA = 01, 10, or 11 for Bank 1.*
3. *This sector has the additional WP# pin sector protection feature.*

S29CD016J/CL016J (Bottom Boot) Sector and Memory Address Map

	Sector	Sector Group	x32 Address Range (A18:A0)	Sector Size (KDwords)		Sector	Sector Group	x32 Address Range (A18:A0)	Sector Size (KDwords)
Bank 0 (Note 2)	SA0 (Note 1)	SG0	00000h–007FFh	2	Bank 1 (Note 2)	SA31	SG14	60000h–63FFFh	16
	SA1 (Note 1)	SG1	00800h–00FFFh	2		SA32		64000h–67FFFh	16
	SA2	SG2	01000h–017FFh	2		SA33		68000h–6BFFFh	16
	SA3	SG3	01800h–01FFFh	2		SA34		6C000h–6FFFFh	16
	SA4	SG4	02000h–027FFh	2		SA35	SG15	70000h–73FFFh	16
	SA5	SG5	02800h–02FFFh	2		SA36		74000h–77FFFh	16
	SA6	SG6	03000h–037FFh	2		SA37		78000h–7BFFFh	16
	SA7	SG7	03800h–03FFFh	2		SA38	SG16	7C000h–7C7FFh	2
	SA8	SG8	04000h–07FFFh	16		SA39	SG17	7C800h–7CFFFh	2
	SA9		08000h–0BFFFh	16		SA40	SG18	7D000h–7D7FFh	2
	SA10		0C000h–0FFFFh	16		SA41	SG19	7D800h–7DFFFh	2
	SA11	SG9	10000h–13FFFh	16		SA42	SG20	7E000h–7E7FFh	2
	SA12		14000h–17FFFh	16		SA43	SG21	7E800h–7EFFFh	2
	SA13		18000h–1BFFFh	16		SA44	SG22	7F000h–7F7FFh	2
	SA14		1C000h–1FFFFh	16		SA45 (Note 3)	SG23	7F800h–7FFFFh	2
	SA15	SG10	20000h–23FFFh	16					
	SA16		24000h–27FFFh	16					
	SA17		28000h–2BFFFh	16					
	SA18		2C000h–2FFFFh	16					
	SA19	SG11	30000h–33FFFh	16					
	SA20		34000h–37FFFh	16					
	SA21		38000h–3BFFFh	16					
	SA22		3C000h–3FFFFh	16					
	SA23	SG12	40000h–43FFFh	16					
	SA24		44000h–47FFFh	16					
	SA25		48000h–4BFFFh	16					
	SA26		4C000h–4FFFFh	16					
	SA27	SG13	50000h–53FFFh	16					
	SA28		54000h–57FFFh	16					
	SA29		58000h–5BFFFh	16					
	SA30		5C000h–5FFFFh	16					

Notes

1. *This sector has the additional WP# pin sector protection feature.*
2. *The bank address is determined by A18 and A17. BA = 00, 01, or 10 for Bank 0 and BA = 11 for Bank 1.*
3. *Secured Silicon Sector overlays this sector when enabled.*

S29CD032J/CL032J (Top Boot) Sector and Memory Address Map

Sector	Sector Group	x32 Address Range (A19:A0)	Sector Size (KDwords)
Bank 0 (Note 2)			
SA0 (Note 1)	SG0	00000h–007FFh	2
SA1	SG1	00800h–00FFFh	2
SA2	SG2	01000h–017FFh	2
SA3	SG3	01800h–01FFFh	2
SA4	SG4	02000h–027FFh	2
SA5	SG5	02800h–02FFFh	2
SA6	SG6	03000h–037FFh	2
SA7	SG7	03800h–03FFFh	2
SA8	SG8	04000h–07FFFh	16
SA9		08000h–0BFFFh	16
SA10		0C000h–0FFFFh	16
SA11	SG9	10000h–13FFFh	16
SA12		14000h–17FFFh	16
SA13		18000h–1BFFFh	16
SA14		1C000h–1FFFFh	16
SA15	SG10	20000h–23FFFh	16
SA16		24000h–27FFFh	16
SA17		28000h–2BFFFh	16
SA18		2C000h–2FFFFh	16
SA19	SG11	30000h–33FFFh	16
SA20		34000h–37FFFh	16
SA21		38000h–3BFFFh	16
SA22		3C000h–3FFFFh	16
Bank 1 (Note 2)			
SA23	SG12	40000h–43FFFh	16
SA24		44000h–47FFFh	16
SA25		48000h–4BFFFh	16
SA26		4C000h–4FFFFh	16
SA27	SG13	50000h–53FFFh	16
SA28		54000h–57FFFh	16
SA29		58000h–5BFFFh	16
SA30		5C000h–5FFFFh	16
SA31	SG14	60000h–63FFFh	16
SA32		64000h–67FFFh	16
SA33		68000h–6BFFFh	16
SA34		6C000h–6FFFFh	16
SA35	SG15	70000h–73FFFh	16
SA36		74000h–77FFFh	16
SA37		78000h–7BFFFh	16
SA38		7C000h–7FFFFh	16

Sector	Sector Group	x32 Address Range (A19:A0)	Sector Size (KDwords)
Bank 1 continued (Note 2)			
SA39	SG16	80000h–83FFFh	16
SA40		84000h–87FFFh	16
SA41		88000h–8BFFFh	16
SA42		8C000h–8FFFFh	16
SA43	SG17	90000h–93FFFh	16
SA44		94000h–97FFFh	16
SA45		98000h–9BFFFh	16
SA46		9C000h–9FFFFh	16
SA47	SG18	A0000h–A3FFFh	16
SA48		A4000h–A7FFFh	16
SA49		A8000h–ABFFFh	16
SA50		AC000h–AFFFFh	16
SA51	SG19	B0000h–B3FFFh	16
SA52		B4000h–B7FFFh	16
SA53		B8000h–BBFFFh	16
SA54		BC000h–BFFFFh	16
SA55	SG20	C0000h–C3FFFh	16
SA56		C4000h–C7FFFh	16
SA57		C8000h–CBFFFh	16
SA58		CC000h–CFFFFh	16
SA59	SG21	D0000h–D3FFFh	16
SA60		D4000h–D7FFFh	16
SA61		D8000h–DBFFFh	16
SA62		DC000h–DFFFFh	16
SA63	SG22	E0000h–E3FFFh	16
SA64		E4000h–E7FFFh	16
SA65		E8000h–EBFFFh	16
SA66		EC000h–EFFFFh	16
SA67	SG23	F0000h–F3FFFh	16
SA68		F4000h–F7FFFh	16
SA69		F8000h–FBFFFh	16
SA70	SG24	FC000h–FC7FFh	2
SA71	SG25	FC800h–FCFFFh	2
SA72	SG26	FD000h–FD7FFh	2
SA73	SG27	FD800h–FDFFFh	2
SA74	SG28	FE000h–FE7FFh	2
SA75	SG29	FE800h–FEFFFh	2
SA76 (Note 3)	SG30	FF000h–FF7FFh	2
SA77 (Note 3)	SG31	FF800h–FFFFFh	2

Notes

1. *Secured Silicon Sector overlays this sector when enabled.*
2. *The bank address is determined by A19 and A18. BA = 00 for Bank 0 and BA = 01, 10, or 11 for Bank 1.*
3. *This sector has the additional WP# pin sector protection feature.*

S29CD032J/CL032J (Bottom Boot) Sector and Memory Address Map

Sector	Sector Group	x32 Address Range (A19:A0)	Sector Size (KDwords)
Bank 0 (Note 2)			
SA0 (Note 3)	SG0	00000h–007FFh	2
SA1 (Note 3)	SG1	00800h–00FFFh	2
SA2	SG2	01000h–017FFh	2
SA3	SG3	01800h–01FFFh	2
SA4	SG4	02000h–027FFh	2
SA5	SG5	02800h–02FFFh	2
SA6	SG6	03000h–037FFh	2
SA7	SG7	03800h–03FFFh	2
SA8	SG8	04000h–07FFFh	16
SA9		08000h–0BFFFh	16
SA10		0C000h–0FFFFh	16
SA11	SG9	10000h–13FFFh	16
SA12		14000h–17FFFh	16
SA13		18000h–1BFFFh	16
SA14		1C000h–1FFFFh	16
SA15	SG10	20000h–23FFFh	16
SA16		24000h–27FFFh	16
SA17		28000h–2BFFFh	16
SA18		2C000h–2FFFFh	16
SA19	SG11	30000h–33FFFh	16
SA20		34000h–37FFFh	16
SA21		38000h–3BFFFh	16
SA22		3C000h–3FFFFh	16
SA23	SG12	40000h–43FFFh	16
SA24		44000h–47FFFh	16
SA25		48000h–4BFFFh	16
SA26		4C000h–4FFFFh	16
SA27	SG13	50000h–53FFFh	16
SA28		54000h–57FFFh	16
SA29		58000h–5BFFFh	16
SA30		5C000h–5FFFFh	16
SA31	SG14	60000h–63FFFh	16
SA32		64000h–67FFFh	16
SA33		68000h–6BFFFh	16
SA34		6C000h–6FFFFh	16
SA35	SG15	70000h–73FFFh	16
SA36		74000h–77FFFh	16
SA37		78000h–7BFFFh	16
SA38		7C000h–7FFFFh	16

Sector	Sector Group	x32 Address Range (A19:A0)	*Sector Size (KDwords)*
Bank 0 continued (Note 2)			
SA39	SG16	80000h–83FFFh	16
SA40		84000h–87FFFh	16
SA41		88000h–8BFFFh	16
SA42		8C000h–8FFFFh	16
SA43	SG17	90000h–93FFFh	16
SA44		94000h–97FFFh	16
SA45		98000h–9BFFFh	16
SA46		9C000h–9FFFFh	16
SA47	SG18	A0000h–A3FFFh	16
SA48		A4000h–A7FFFh	16
SA49		A8000h–ABFFFh	16
SA50		AC000h–AFFFFh	16
SA51	SG19	B0000h–B3FFFh	16
SA52		B4000h–B7FFFh	16
SA53		B8000h–BBFFFh	16
SA54		BC000h–BFFFFh	16
Bank 1 (Note 2)			
SA55	SG20	C0000h–C3FFFh	16
SA56		C4000h–C7FFFh	16
SA57		C8000h–CBFFFh	16
SA58		CC000h–CFFFFh	16
SA59	SG21	D0000h–D3FFFh	16
SA60		D4000h–D7FFFh	16
SA61		D8000h–DBFFFh	16
SA62		DC000h–DFFFFh	16
SA63	SG22	E0000h–E3FFFh	16
SA64		E4000h–E7FFFh	16
SA65		E8000h–EBFFFh	16
SA66		EC000h–EFFFFh	16
SA67	SG23	F0000h–F3FFFh	16
SA68		F4000h–F7FFFh	16
SA69		F8000h–FBFFFh	16
SA70	SG24	FC000h–FC7FFh	2
SA71	SG25	FC800h–FCFFFh	2
SA72	SG26	FD000h–FD7FFh	2
SA73	SG27	FD800h–FDFFFh	2
SA74	SG28	FE000h–FE7FFh	2
SA75	SG29	FE800h–FEFFFh	2
SA76	SG30	FF000h–FF7FFh	2
SA77 (Note 1)	SG31	FF800h–FFFFFh	2

Notes
1. *This sector has the additional WP# pin sector protection feature.*
2. *The bank address is determined by A19 and A18. BA = 00, 01, or 10 for Bank 0 and BA = 11 for Bank 1.*
3. *The Secured Silicon Sector overlays this sector when enabled.*

8. Device Operations

This section describes the read, program, erase, simultaneous read/write operations, and reset features of the Flash devices.

Operations are initiated by writing specific commands or a sequence with specific address and data patterns into the command register (see Table). The command register itself does not occupy any addressable memory location; rather, it is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as input to the internal state machine; the state machine outputs dictate the function of the device. Writing incorrect address and data values or writing them in an improper sequence may place the device in an unknown state, in which case the system must write the reset command in order to return the device to the reading array data mode.

8.1 Device Operation Table

The device must be set up appropriately for each operation. Table describes the required state of each control pin for any particular operation.

Device Bus Operation

Operation	CE#	OE#	WE#	RESET#	CLK	ADV#	Addresses	Data (DQ0–DQ31)
Read	L	L	H	H	X	X	A_{IN}	D_{OUT}
Asynchronous Write	L	H	L	H	X	X	A_{IN}	D_{IN}
Synchronous Write	L	H	L	H	↑	↑	A_{IN}	D_{IN}
Standby (CE#)	H	X	X	H	H	X	X	High-Z
Output Disable	L	H	H	H	X	X	High-Z	High-Z
Reset	X	X	X	L	X	X	X	High-Z
PPB Protection Status (Note 2)	L	L	H	H	X	X	Sector Address, A9 = V_{ID}, A7 – A0 = 02h	00000001h, (protected) A6 = H 00000000h (unprotect) A6 = L
Burst Read Operations								
Load Starting Burst Address	L	X	H	H	↑	↓	A_{IN}	X
Advance Burst to next address with appropriate Data presented on the Data bus	L	L	H	H	↑	H	X	Burst Data Out
Terminate Current Burst Read Cycle	H	X	H	H	↑	X	X	High-Z
Terminate Current Burst Read Cycle with RESET#	X	X	H	L	X	X	X	High-Z
Terminate Current Burst Read Cycle; Start New Burst Read Cycle	L	H	H	H	↑	↓	A_{IN}	X

Legend
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, X = Don't care.

Notes
1. *WP# controls the two outermost sectors of the top boot block or the two outermost sectors of the bottom boot block.*
2. *DQ0 reflects the sector PPB (or sector group PPB) and DQ1 reflects the DYB.*

8.2 Asynchronous Read

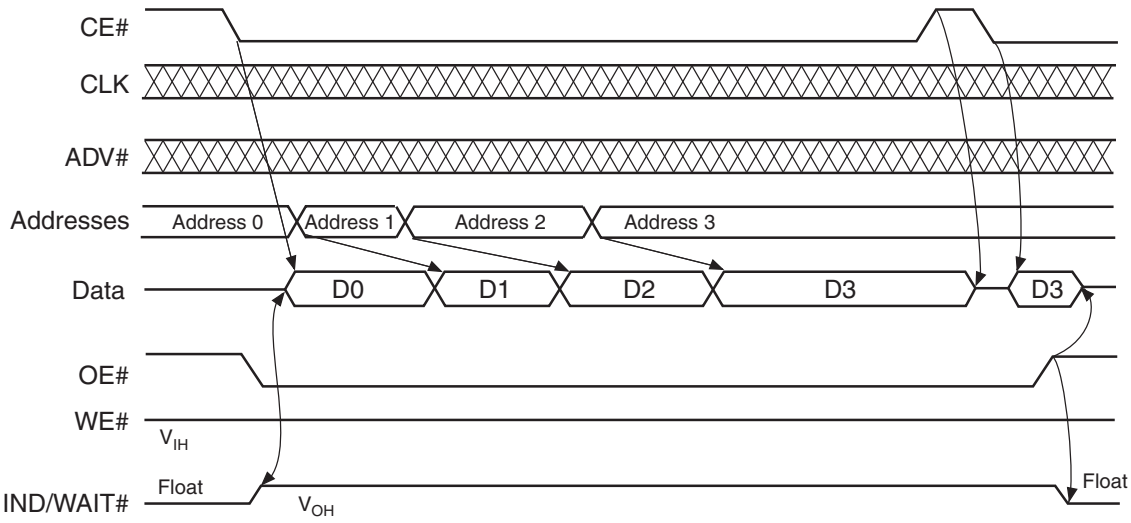
All memories require access time to output array data. In an asynchronous read operation, data is read from one memory location at a time. Addresses are presented to the device in random order, and the propagation delay through the device causes the data on its outputs to arrive asynchronously with the address on its inputs.

The internal state machine is set for asynchronously reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

The device has two control functions which must be satisfied in order to obtain data at the outputs. CE# is the power control and should be used for device selection (CE# must be set to V_{IL} to read data). OE# is the output control and should be used to gate data to the output pins if the device is selected (OE# must be set to V_{IL} in order to read data). WE# should remain at V_{IH} (when reading data).

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from the stable addresses and stable CE# to valid data at the output pins. The output enable access time (t_{OE}) is the delay from the falling edge of OE# to valid data at the output pins (assuming the addresses have been stable for at least a period of t_{ACC}-t_{OE} and CE# has been asserted for at least t_{CE}-t_{OE} time). Figure 8.1 shows the timing diagram of an asynchronous read operation.

Figure 8.1 Asynchronous Read Operation



Note
Operation is shown for the 32-bit data bus. For the 16-bit data bus, A-1 is required.

Refer to *Asynchronous Operations* on page 52 for timing specifications and to Figure 18.2, *Conventional Read Operations Timings* on page 52 for another timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

8.3 Hardware Reset (RESET#)

The RESET# pin is an active low signal that is used to reset the device under any circumstances. A logic “0” on this input forces the device out of any mode that is currently executing back to the reset state. RESET# may be tied to the system reset circuitry. A system reset would thus also reset the device. To avoid a potential bus contention during a system reset, the device is isolated from the DQ data bus by tristating the data outputs for the duration of the RESET pulse. All data outputs are “don’t care” during the reset operation.

If RESET# is asserted during a program or erase operation, the RY/BY# output remains low until the reset operation is internally complete. The RY/BY# pin can be used to determine when the reset operation is complete. Since the device offers simultaneous read/write operation, the host system may read a bank after a period of t_{READY2}, if the bank was in the read/reset mode at the time

RESET# was asserted. If one of the banks was in the middle of either a program or erase operation when RESET# was asserted, the user must wait a period of t_{READY} before accessing that bank.

Asserting RESET# during a program or erase operation leaves erroneous data stored in the address locations being operated on at the time of device reset. These locations need updating after the reset operation is complete. See *Hardware Reset (RESET#)* on page 56 for timing specifications.

Asserting RESET# active during V_{CC} and V_{IO} power-up is required to guarantee proper device initialization until V_{CC} and V_{IO} have reached their steady state voltages. See *V_{CC} and V_{IO} Power-up* on page 51.

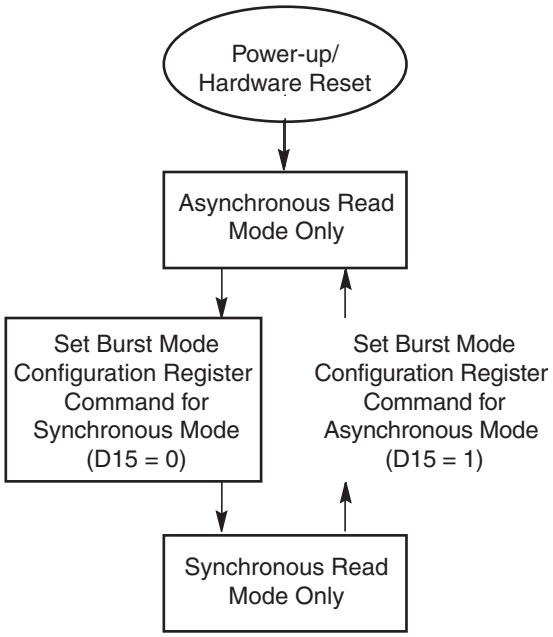
8.4 Synchronous (Burst) Read Mode and Configuration Register

When a series of adjacent addresses need to be read from the device, the synchronous (or burst read) mode can be used to significantly reduce the overall time needed for the device to output array data. After an initial access time required for the data from the first address location, subsequent data is output synchronized to a clock input provided by the system.

The device offers a linear method of burst read operation which is discussed in *2-, 4-, 8- Double Word Linear Burst Operation* on page 22.

Since the device defaults to asynchronous read mode after power-up or a hardware reset, the configuration register must be set in order to enable the burst read mode. Other Configuration Register settings include the number of wait states to insert before the initial word (t_{IACC}) of each burst access and when RDY indicates that data is ready to be read. Prior to entering the burst mode, the system first determines the configuration register settings (and read the current register settings if desired via the Read Configuration Register command sequence), then write the configuration register command sequence. See *Configuration Register* on page 24, and Table on page 71 for further details. Once the configuration register is written to enable burst mode operation, all subsequent reads from the array are returned using the burst mode protocols.

Figure 8.2 Synchronous/Asynchronous State Diagram



The device outputs the initial word subject to the following operational conditions:

- t_{IACC} specification: The time from the rising edge of the first clock cycle after addresses are latched to valid data on the device outputs.
- Configuration register setting CR13-CR10: The total number of clock cycles (wait states) that occur before valid data appears on the device outputs. The effect is that t_{IACC} is lengthened.

Like the main memory access, the Secured Silicon Sector memory is accessed with the same burst or asynchronous timing as defined in the Configuration Register. However, the user must recognize burst operations past the 256 byte Secured Silicon boundary returns invalid data.

Burst read operations occur only to the main flash memory arrays. The Configuration Register and protection bits are treated as single cycle reads, even when burst mode is enabled. Read operations to these locations results in the data remaining valid while OE# is at V_{IL}, regardless of the number of CLK cycles applied to the device.

8.4.1 2-, 4-, 8- Double Word Linear Burst Operation

In a linear burst read operation, a fixed number of words (2, 4, or 8 double words) are read from consecutive addresses that are determined by the group within which the starting address falls. Note that 1 double word = 32 bits. See Table for all valid burst output sequences.

The IND/WAIT# signal, or End of Burst Indicator signal, transitions active (V_{IL}) during the last transfer of data in a linear burst read before a wrap around. This transition indicates that the system should initiate another ADV# to start the next burst access. If the system continues to clock the device, the next access wraps around to the starting address of the previous burst access. The IND/WAIT# signal is floating when not active.

32-Bit Linear and Burst Data Order

Data Transfer Sequence	Output Data Sequence (Initial Access Address)
Two Linear Data Transfers	0-1 (A0 = 0) 1-0 (A0 = 1)
Four Linear Data Transfers	0-1-2-3 (A1-A0 = 00) 1-2-3-0 (A1-A0 = 01) 2-3-0-1 (A1-A0 = 10) 3-0-1-2 (A1-A0 = 11)
Eight Linear Data Transfers	0-1-2-3-4-5-6-7 (A2-A0 = 000) 1-2-3-4-5-6-7-0 (A2-A0 = 001) 2-3-4-5-6-7-0-1 (A2-A0 = 010) 3-4-5-6-7-0-1-2 (A2-A0 = 011) 4-5-6-7-0-1-2-3 (A2-A0 = 100) 5-6-7-0-1-2-3-4 (A2-A0 = 101) 6-7-0-1-2-3-4-5 (A2-A0 = 110) 7-0-1-2-3-4-5-6 (A2-A0 = 111)

Notes

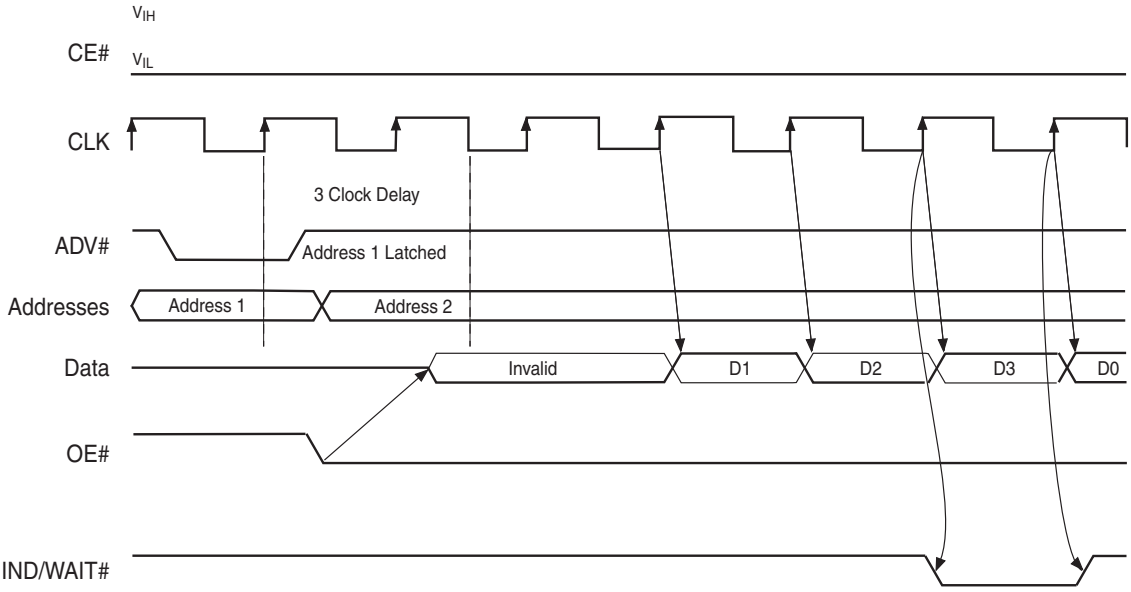
1. *The default configuration in the Control Register for Bit 6 is "1," indicating that the device delivers data on the rising edge of the CLK signal.*
2. *The device is capable of holding data for one CLK cycle.*
3. *If RESET# is asserted low during a burst access, the burst access is immediately terminated and the device defaults back to asynchronous read mode. When this happens, the DQ data bus signal floats and the Configuration Register contents are reset to their default conditions.*
4. *CE# must meet the required burst read setup times for burst cycle initiation. If CE# is taken to V_{IH} at any time during the burst linear or burst cycle, the device immediately exits the burst sequence and floats the DQ bus signal.*
5. *Restarting a burst cycle is accomplished by taking CE# and ADV# to V_{IL}.*
6. *A burst access is initiated and the address is latched on the first rising CLK edge when ADV# is active or upon a rising ADV# edge, whichever occurs first. If the ADV# signal is taken to VIL prior to the end of a linear burst sequence, the previous address is discarded and subsequent burst transfers are invalid. A new burst is initiated when ADV# transitions back to V_{IH} before a clock edge.*
7. *The OE# (Output Enable) pin is used to enable the linear burst data on the DQ data bus pin. De-asserting the OE# pin to V_{IH} during a burst operation floats the data bus, but the device continues to operate internally as if the burst sequence continues until the linear burst is complete. The OE# pin does not halt the burst sequence, The DQ bus remains in the float state until OE# is taken to V_{IL}.*
8. *Halting the burst sequence is accomplished by either taking CE# to V_{IH} or re-issuing a new ADV# pulse.*

The IND/WAIT# signal is controlled by the OE# signal. If OE# is at V_{IH}, the IND/WAIT# signal floats and is not driven. If OE# is at V_{IL}, the IND/ WAIT# signal is driven at V_{IH} until it transitions to V_{IL}, indicating the end of the burst sequence. Table lists the valid combinations of the Configuration Register bits that impact the IND/WAIT# timing. See Figure 8.3 for the IND/WAIT# timing diagram.

Valid Configuration Register Bit Definition for IND/WAIT#

CR9 (DOC)	CR8 (WC)	CR6 (CC)	Definition
0	0	1	IND/WAIT# = V_{IL} for 1-CLK cycle, Active on last transfer, Driven on rising CLK edge
0	1	1	IND/WAIT# = V_{IL} for 1-CLK cycle, Active on second to last transfer, Driven on rising CLK edge

Figure 8.3 End of Burst Indicator (IND/WAIT#) Timing for Linear 4 Double Word Burst Operation



Note
Operation is shown for the 32-bit data bus. Figure shown with 3-CLK initial access delay configuration, linear address, 4-doubleword burst, output on rising CLK edge, data hold for 1-CLK, IND/WAIT# asserted on the last transfer before wrap-around.

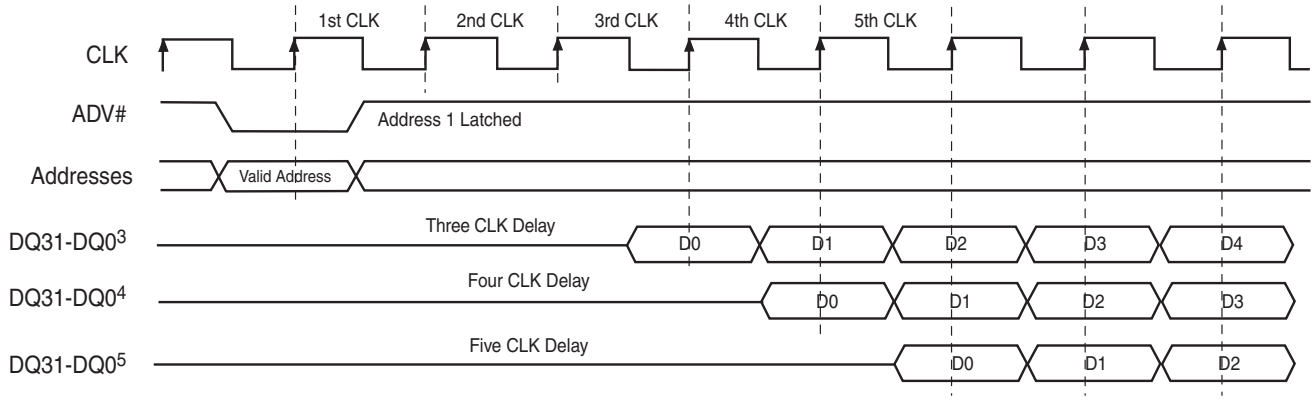
8.4.2 Initial Burst Access Delay

Initial Burst Access Delay is defined as the number of clock cycles that must elapse from the first valid clock edge after ADV# assertion (or the rising edge of ADV#) until the first valid CLK edge when the data is valid. Burst access is initiated and the address is latched on the first rising CLK edge when ADV# is active or upon a rising ADV# edge, whichever comes first. The Initial Burst Access Delay is determined in the Configuration Register (CR13-CR10). Refer to Table for the initial access delay configurations under CR13-CR10. See Figure 8.4 for the Initial Burst Delay Control timing diagram. Note that the Initial Access Delay for a burst access has no effect on asynchronous read operations.

Burst Initial Access Delay

CR13	CR12	CR11	CR10	Initial Burst Access (CLK cycles)
0	0	0	1	3
0	0	1	0	4
0	0	1	1	5
0	1	0	0	6
0	1	0	1	7
0	1	1	0	8
0	1	1	1	9

Figure 8.4 Initial Burst Delay Control



Notes

1. *Burst access starts with a rising CLK edge and when ADV# is active.*
2. *Configurations register 6 is always set to 1 (CR6 = 1). Burst starts and data outputs on the rising CLK edge.*
3. *CR [13-10] = 1 or three clock cycles.*
4. *CR [13-10] = 2 or four clock cycles.*
5. *CR [13-10] = 3 or five clock cycles.*

8.4.3 Configuration Register

The configuration register sets various operational parameters associated with burst mode. Upon power-up or hardware reset, the device defaults to the asynchronous read mode and the configuration register settings are in their default state. (See Table for the default Configuration Register settings.) The host system determines the proper settings for the entire configuration register, and then execute the Set Configuration Register command sequence before attempting burst operations. The configuration register is not reset after deasserting CE#.

The Configuration Register does not occupy any addressable memory location, but rather, is accessed by the Configuration Register commands. The Configuration Register is readable at any time, however, writing the Configuration Register is restricted to times when the Embedded Algorithm™ is not active. If the user attempts to write the Configuration Register while the Embedded Algorithm is active, the write operation is ignored and the contents of the Configuration Register remain unchanged.

The Configuration Register is a 16 bit data field which is accessed by DQ15–DQ0. During a read operation, DQ31–DQ16 returns all zeroes. Also, the Configuration Register reads operate the same as the Autoselect command reads. When the command is issued, the bank address is latched along with the command. Read operations to the bank that was specified during the Configuration Register read command return Configuration Register contents. Read operations to the other bank return flash memory data. Either bank address is permitted when writing the Configuration Register read command.

The configuration register can be read with a four-cycle command sequence. See *Command Definitions* on page 71 for sequence details.

Table describes the Configuration Register settings.

Configuration Register

Configuration Register	
CR15 = Read Mode (RM) 0 = Synchronous Burst Reads Enabled 1 = Asynchronous Reads Enabled (Default)	
CR14 = Reserved for Future Enhancements These bits are reserved for future use. Set these bits to *0*.	
CR13–CR10 = Initial Burst Access Delay Configuration (IAD3-IAD0)	
0000 = 2 CLK cycle initial burst access delay	0100 = 6 CLK cycle initial burst access delay
0001 = 3 CLK cycle initial burst access delay	0101 = 7 CLK cycle initial burst access delay
0010 = 4 CLK cycle initial burst access delay	0110 = 8 CLK cycle initial burst access delay
0011 = 5 CLK cycle initial burst access delay	0111 = 9 CLK cycle initial burst access delay—Default
CR9 = Data Output Configuration (DOC) 0 = Hold Data for 1-CLK cycle—Default 1 = Reserved	
CR8 = IND/WAIT# Configuration (WC) 0 = IND/WAIT# Asserted During Delay—Default 1 = IND/WAIT# Asserted One Data Cycle Before Delay	
CR7 = Burst Sequence (BS) 0 = Reserved 1 = Linear Burst Order—Default	
CR6 = Clock Configuration (CC) 0 = Reserved 1 = Burst Starts and Data Output on Rising Clock Edge—Default	
CR5–CR3 = Reserved For Future Enhancements (R) These bits are reserved for future use. Set these bits to *0*.	
CR2–CR0 = Burst Length (BL2–BL0) 000 = Reserved, burst accesses disabled (asynchronous reads only) 001 = 64 bit (8-byte) Burst Data Transfer - x32 Linear 010 = 128 bit (16-byte) Burst Data Transfer - x32 Linear 011 = 256 bit (32-byte) Burst Data Transfer - x32 Linear (device default) 100 = Reserved, burst accesses disabled (asynchronous reads only) 101 = Reserved, burst accesses disabled (asynchronous reads only) 110 = Reserved, burst accesses disabled (asynchronous reads only)	

Configuration Register After Device Reset

CR15	CR14	CR13	CR12	CR11	CR10	CR9	CR8
RM	**Reserve**	**IAD3**	**IAD2**	**IAD1**	**IAD0**	**DOC**	**Reserve**
1	0	0	1	1	1	0	0

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
BS	**CC**	**Reserve**	**Reserve**	**Reserve**	**BL2**	**BL1**	**BL0**
1	1	0	0	0	1	0	0

8.5 Autoselect

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be