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Continuity of Specifications

There is no change to this document as a result of offering the device as a Cypress product. Any changes that have been made are the result of normal document improvements and are noted in the document history page, where supported. Future revisions will occur when appropriate, and changes will be noted in a document history page.

Continuity of Ordering Part Numbers

Cypress continues to support existing part numbers. To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local sales office for additional information about Cypress products and solutions.

S29GL064N, S29GL032N

64 Mbit, 32 Mbit 3 V Page Mode MirrorBit Flash

Distinctive Characteristics

Architectural Advantages

- Single power supply operation
- Manufactured on 110 nm MirrorBit process technology
- Secured Silicon Sector region
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number, accessible through a command sequence
  - Programmed and locked at the factory or by the customer
- Flexible sector architecture
  - 64Mb (uniform sector models): One hundred twenty-eight 32 Kword (64 KB) sectors
  - 64 Mb (boot sector models): One hundred twenty-seven 32 Kword (64 KB) sectors + eight 4Kword (8KB) boot sectors
  - 32 Mb (uniform sector models): Sixty-four 32Kword (64 KB) sectors
  - 32 Mb (boot sector models): Sixty-three 32Kword (64 KB) sectors + eight 4Kword (8KB) boot sectors
- Enhanced VersatileI/O™ Control
  - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on V_{IO} input. V_{IO} range is 1.65 to V_{CC}
- Compatibility with JEDEC standards
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- 100,000 erase cycles typical per sector
- 20-year data retention typical

Performance Characteristics

- High performance
  - 90 ns access time
  - 8-word/16-byte page read buffer
  - 25 ns page read time
  - 16-word/32-byte write buffer which reduces overall programming time for multiple-word updates
- Low power consumption
  - 25 mA typical initial read current, 1 mA typical page read current
  - 50 mA typical erase/program current
  - 1 µA typical standby mode current
- Package options
  - 48-pin TSOP
  - 56-pin TSOP
  - 64-ball Fortified BGA
  - 48-ball fine-pitch BGA

Software & Hardware Features

- Software features
  - Advanced Sector Protection: offers Persistent Sector Protection and Password Sector Protection
  - Program Suspend & Resume: read other sectors before programming operation is completed
  - Erase Suspend & Resume: read/program other sectors before an erase operation is completed
  - Data# polling & toggle bits provide status
  - CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
  - Unlock Bypass Program command reduces overall multiple-word programming time
- Hardware features
  - WP#/ACC input accelerates programming time (when high voltage is applied) for greater throughput during system production. Protects first or last sector regardless of sector protection settings on uniform sector models
  - Hardware reset input (RESET#) resets device
  - Ready/Busy# output (RY/BY#) detects program or erase cycle

General Description

The S29GL-N family of devices are 3.0-Volt single-power Flash memory manufactured using 110 nm MirrorBit technology. The S29GL064N is a 64-Mb device organized as 4,194,304 words or 8,388,608 bytes. The S29GL032N is a 32-Mb device organized as 2,097,152 words or 4,194,304 bytes. Depending on the model number, the devices have 16-bit wide data bus only, or a 16-bit wide data bus that can also function as an 8-bit wide data bus by using the BYTE# input. The devices can be programmed either in the host system or in standard EPROM programmers.

Access times as fast as 90 ns are available. Note that each access time has a specific operating voltage range (V_{CC}) as specified in the *Product Selector Guide* and the *Ordering Information–S29GL032N*, and *Ordering Information–S29GL064N*. Package offerings include 48-pin TSOP, 56-pin TSOP, 48-ball fine-pitch BGA and 64-ball Fortified BGA, depending on model number. Each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0-Volt power supply** for both read and write functions. In addition to a V_{CC} input, a high-voltage **accelerated program (ACC)** feature provides shorter programming times through increased voltage on the WP#/ACC or ACC input. This feature is intended to facilitate factory throughput during system production, but may also be used in the field if desired.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

The **Advanced Sector Protection** features several levels of sector protection, which can disable both the program and erase operations in certain sectors. Persistent Sector Protection is a method that replaces the previous 12-volt controlled protection method. Password Sector Protection is a highly sophisticated protection method that requires a password before changes to certain sectors are permitted.

Device programming and erasure are initiated through command sequences. Once a program or erase operation begins, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses are stable for a specified period of time.

The **Write Protect (WP#)** feature protects the first or last sector by asserting a logic low on the WP#/ACC pin or WP# pin, depending on model number. The protected sector is still protected even during accelerated programming.

The **Secured Silicon Sector** provides a 128-word/256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

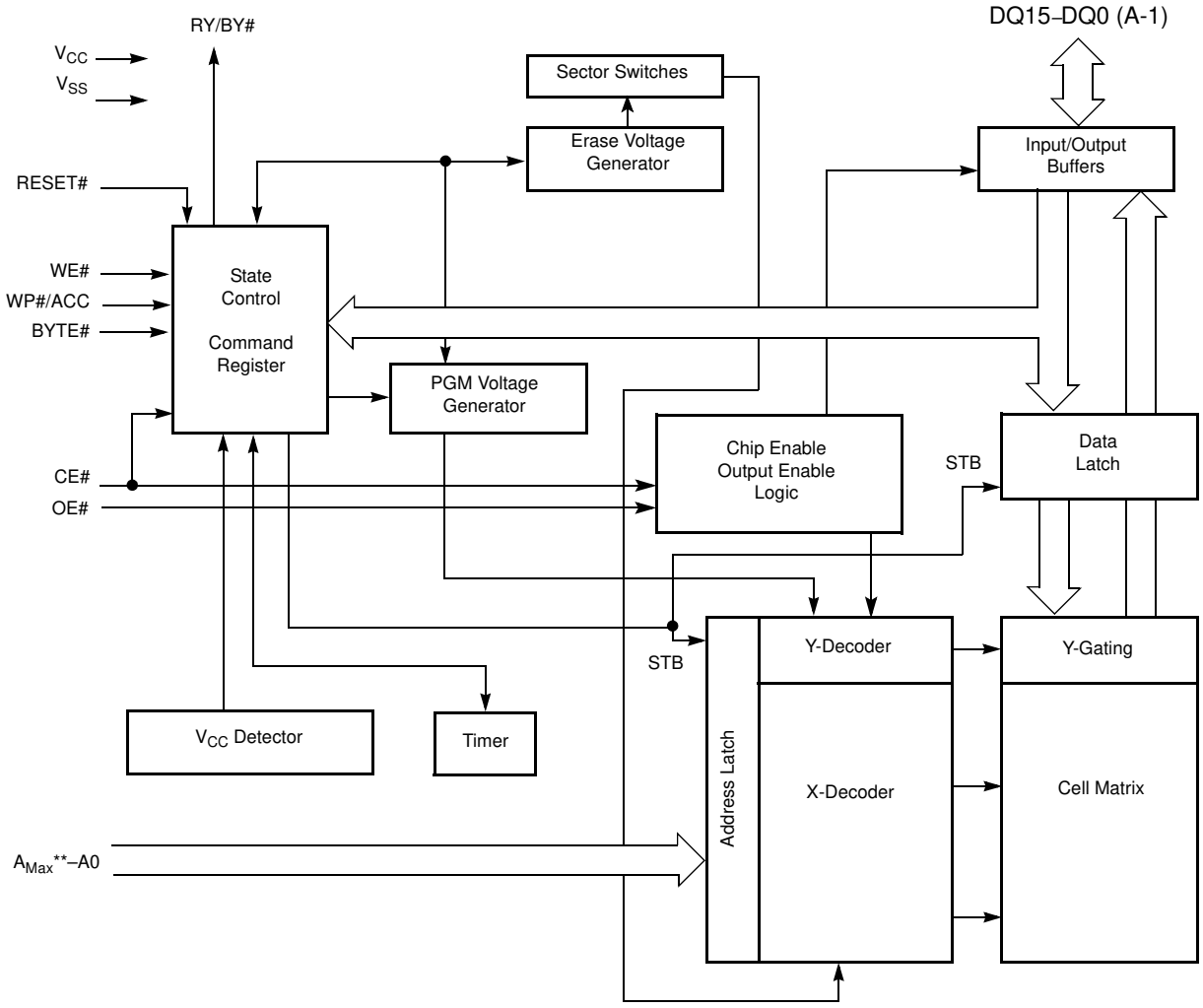
Cypress MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

Table of Contents

1. Product Selector Guide

Part Number			S29GL064N		S29GL032N	
Speed Option	V_{CC} = 2.7–3.6 V	V_{IO} = 2.7–3.6 V	**90**		**90**	
		V_{IO} = 1.65–3.6 V		**110**		**110**
Max. Access Time (ns)			90	110	90	110
Max. CE# Access Time (ns)			90	110	90	110
Max. Page Access Time (ns)			25	30	25	30
Max. OE# Access Time (ns)			25	30	25	30

2. Block Diagram



Note

***A_{MAX} GL064N = A21, GL032N = A20.*

3. Connection Diagrams

Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (TSOP and BGA). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Figure 3.1 48-Pin Standard TSOP

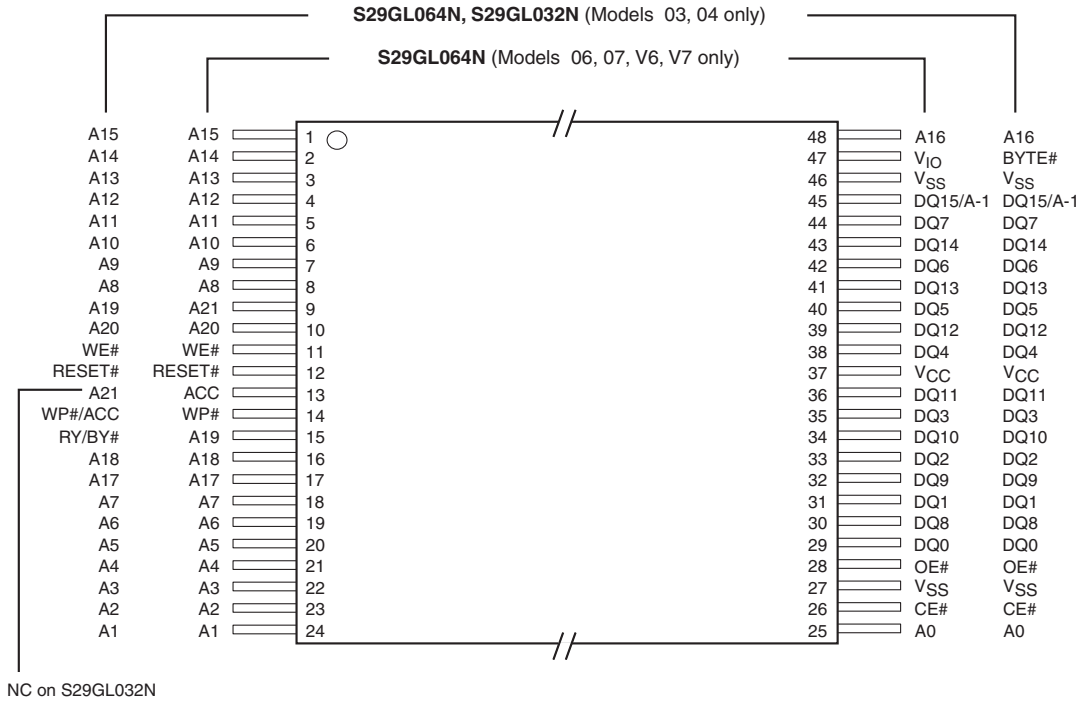


Figure 3.2 56-Pin Standard TSOP

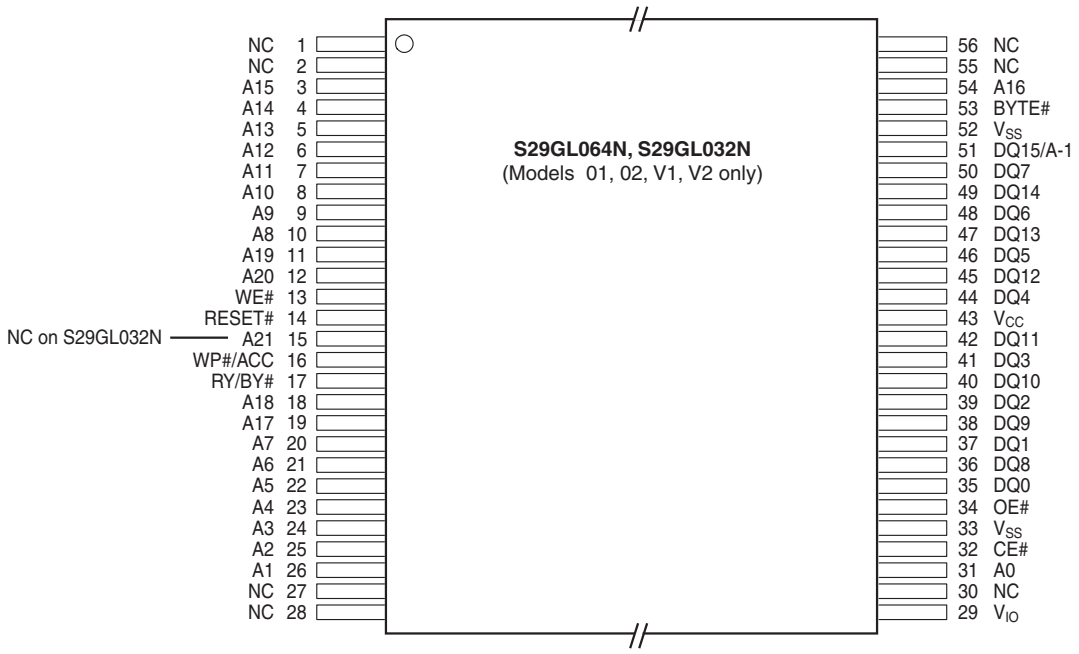


Figure 3.3 64-ball Fortified BGA

S29GL064N, S29GL032N (Models 01, 02, 03, 04, V1, V2 only)
Top View, Balls Facing Down

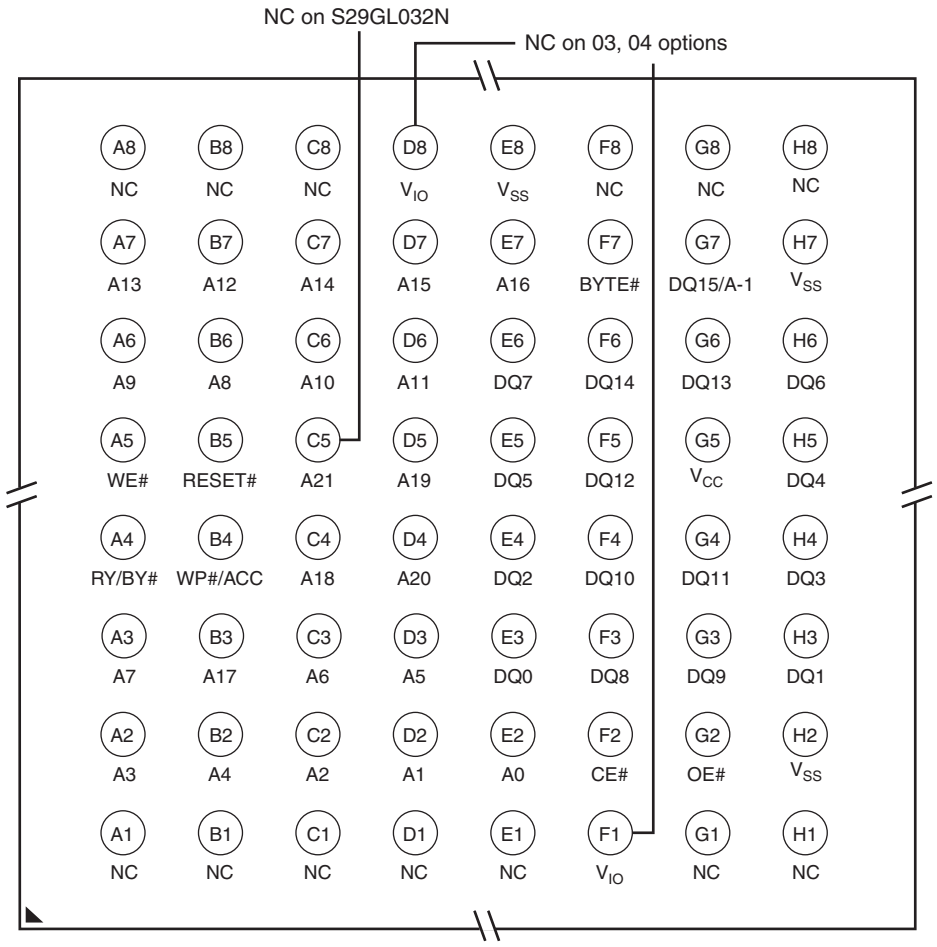
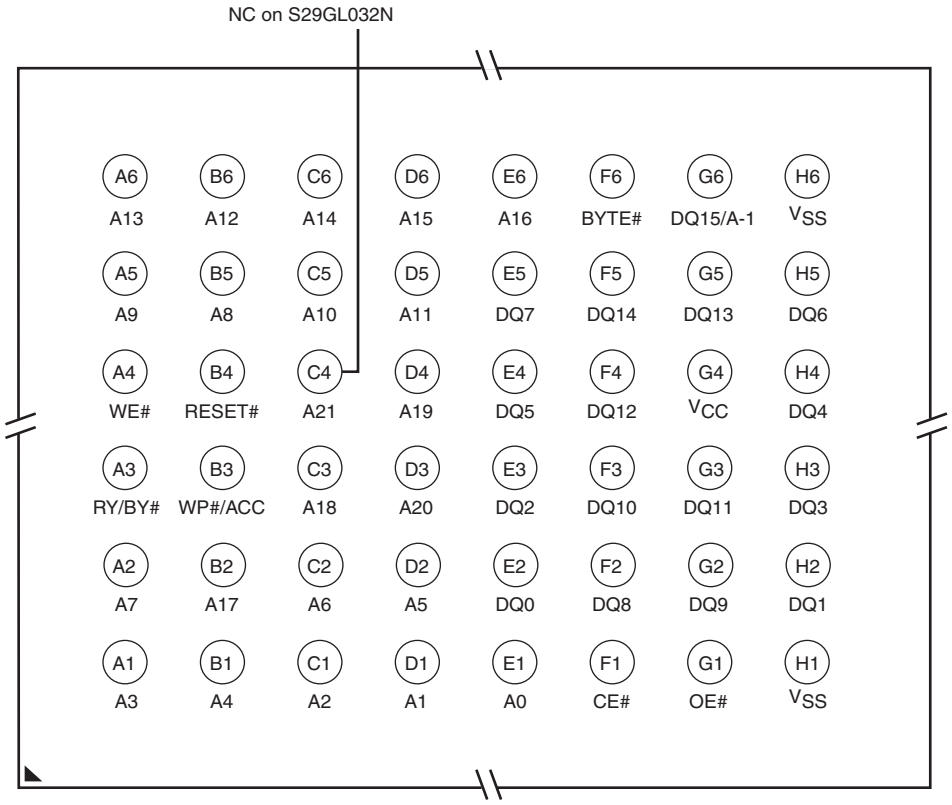


Figure 3.4 48-ball Fine-pitch BGA (VBK 048)

S29GL064N, S29GL032N (Models 03, 04 only)
Top View, Balls Facing Down



4. Pin Descriptions

Pin	Description
A21–A0	22 Address inputs (S29GL064N)
A20–A0	21 Address inputs (S29GL032N)
DQ7–DQ0	8 Data inputs/outputs
DQ14–DQ0	15 Data inputs/outputs
DQ15/A-1	DQ15 (Data input/output, word mode), A-1 (LSB Address input, byte mode)
CE#	Chip Enable input
OE#	Output Enable input
WE#	Write Enable input
WP#/ACC	Hardware Write Protect input/Programming Acceleration input
ACC	Acceleration input
WP#	Hardware Write Protect input
RESET#	Hardware Reset Pin input
RY/BY#	Ready/Busy output
BYTE#	Selects 8-bit or 16-bit mode
V_{CC}	3.0 volt-only single power supply (see *Product Selector Guide* for speed options and voltage supply tolerances)
V_{IO}	Output Buffer Power
V_{SS}	Device Ground
NC	Pin Not Connected Internally

5. Logic Symbols

Figure 5.1 S29GL064N Logic Symbol (Models 01, 02, V1, V2)

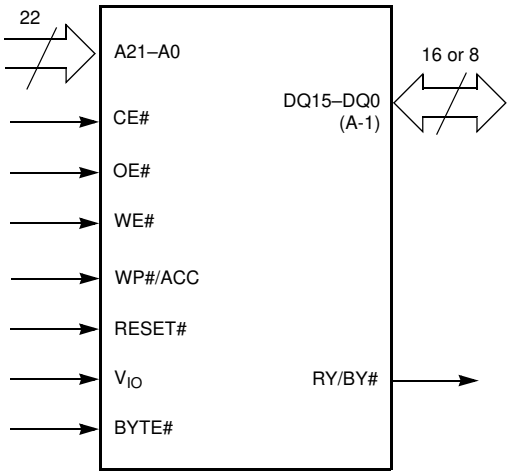


Figure 5.2 S29GL064N Logic Symbol (Models 03, 04)

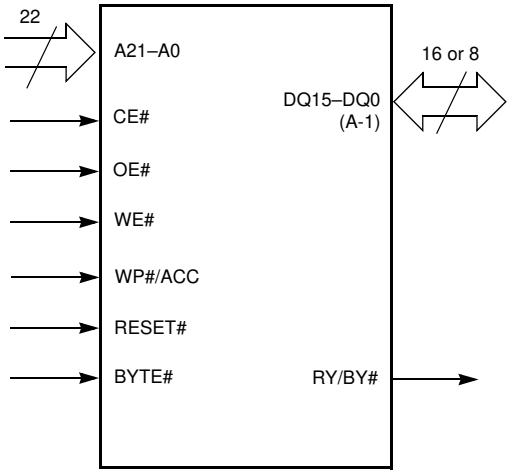


Figure 5.3 S29GL064N Logic Symbol (Models 06, 07, V6, V7)

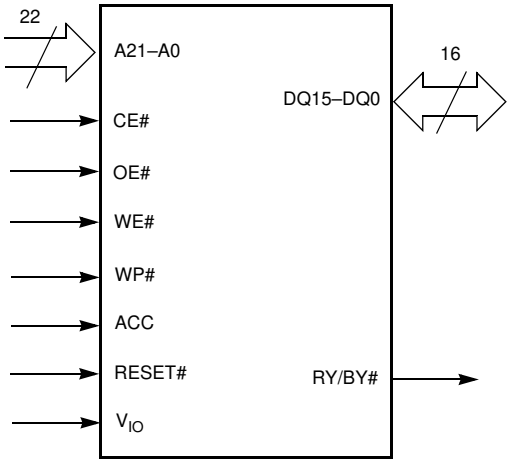


Figure 5.4 S29GL032N Logic Symbol (Models 01, 02, V1, V2)

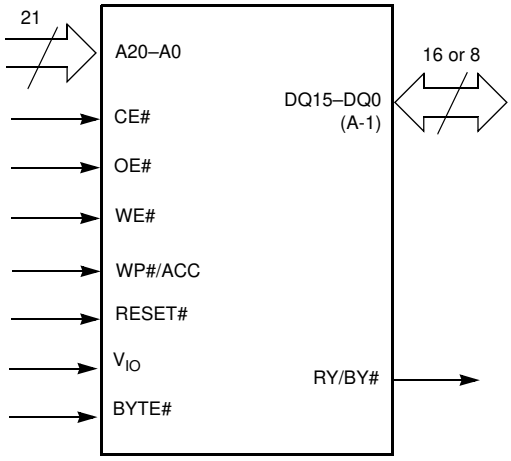
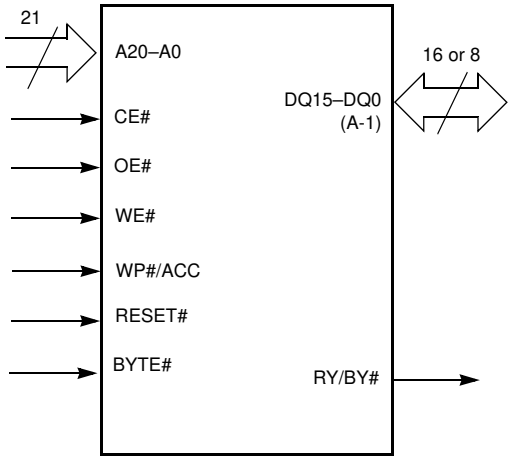


Figure 5.5 S29GL032N Logic Symbol (Models 03, 04)



6. Ordering Information–S29GL032N

S29GL032N Standard Products

Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

S29GL032N 90 T F I 01 0

PACKING TYPE
0 = Tray
2 = 7-inch Tape and Reel
3 = 13-inch Tape and Reel

MODEL NUMBER
01 = x8/x16, V_{CC}= V_{IO} = 2.7 – 3.6 V, Uniform sector, WP#/ACC = V_{IL} protects highest addressed sector
02 = x8/x16, V_{CC} = V_{IO} = 2.7 – 3.6 V, Uniform sector, WP#/ACC = V_{IL} protects lowest addressed sector
03 = x8/x16, V_{CC} = 2.7 – 3.6 V, Top boot sector, WP#/ACC = V_{IL} protects top two addressed sectors
04 = x8/x16, V_{CC} = 2.7 – 3.6 V, Bottom boot sector, WP#/ACC = V_{IL} protects bottom two addressed sectors
V1 = x8/x16, V_{CC} = 2.7 – 3.6 V, V_{IO} = 1.65 - 3.6 V, Uniform sector, WP#/ACC = V_{IL} protects highest addressed sector
V2 = x8/x16, V_{CC} = 2.7 – 3.6 V, V_{IO} = 1.65 - 3.6 V, Uniform sector, WP#/ACC = V_{IL} protects lowest addressed sector

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)

PACKAGE MATERIAL SET
A = Standard (Note 4)
F = Pb-Free

PACKAGE TYPE
B = Fine-pitch Ball-Grid Array Package
D = Fortified Ball-Grid Array Package(LAE064), 9 mm x 9 mm
F = Fortified Ball-Grid Array Package (LAA064), 13 mm x 11 mm
T = Thin Small Outline Package (TSOP) Standard Pinout

SPEED OPTION
See Product Selector Guide and Valid Combinations (90 = 90 ns, 11 = 110 ns)

DEVICE NUMBER/DESCRIPTION
S29GL032N
32 Megabit Page-Mode Flash Memory
Manufactured using 110 nm MirrorBit® Process Technology, 3.0 Volt-only Read, Program, and Erase

Table 6.1 S29GL032N Ordering Options (Note 4)

S29GL032N Valid Combinations					Package Description	
Device Number	**Speed Option**	**Package, Material, & Temperature Range**	**Model Number**	**Packing Type**		
S29GL032N	90	TFI	03, 04	0,2,3 (Note 1)	TS048 (Note 2)	TSOP
	90		01, 02		TS056 (Note 2)	
	11		V1, V2			
	90	BFI	03, 04		VBK048 (Note 3)	Fine-Pitch BGA
	90	FFI	01, 02, 03, 04		LAA064 (Note 3)	Fortified BGA
	11		V1, V2			
	90	DFI	01, 02, 03, 04		LAE064 (Note 3)	
	11		V1, V2			

Notes

1. *Type 0 is standard. Specify others as required: TSOPs can be packed in Types 0 and 3; BGAs can be packed in Types 0, 2, or 3.*
2. *TSOP package marking omits packing type designator from ordering part number.*
3. *BGA package marking omits leading* S29 *and packing type designator from ordering part number.*
4. *Contact local sales for availability for Leaded lead-frame parts.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

7. Ordering Information–S29GL064N

S29GL064N Standard Products

Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

S29GL064N 90 T F I 02 2

PACKING TYPE
0 = Tray
2 = 7-inch Tape and Reel
3 = 13-inch Tape and Reel

MODEL NUMBER
01 = x8/x16, V_{CC} = V_{IO} = 2.7 – 3.6 V, Uniform sector, WP#/ACC = V_{IL} protects highest addressed sector
02 = x8/x16, V_{CC} = V_{IO} = 2.7 – 3.6 V, Uniform sector, WP#/ACC = V_{IL} protects lowest addressed sector
03 = x8/x16, V_{CC} = 2.7 – 3.6 V, Top boot sector, WP#/ACC = V_{IL} protects top two addressed sectors
04 = x8/x16, V_{CC} = 2.7 – 3.6 V, Bottom boot sector, WP#/ACC = V_{IL} protects bottom two addressed sectors
06 = x16, V_{CC} = 2.7 – 3.6 V, Uniform sector, WP# = V_{IL} protects highest addressed sector
07 = x16, V_{CC} = 2.7 – 3.6 V, Uniform sector, WP# = V_{IL} protects lowest addressed sector
V1 = x8/x16, V_{CC} = 2.7 – 3.6 V, V_{IO} = 1.65 - 3.6 V, Uniform sector, WP#/ACC = V_{IL} protects highest addressed sector
V2 = x8/x16, V_{CC} = 2.7 – 3.6 V, V_{IO} = 1.65 - 3.6 V, Uniform sector, WP#/ACC = V_{IL} protects lowest addressed sector
V6 = x16, V_{CC} = 2.7 – 3.6 V, V_{IO} = 1.65 - 3.6 V, Uniform sector, WP# = V_{IL} protects highest addressed sector
V7 = x16, V_{CC} = 2.7 – 3.6 V, V_{IO} = 1.65 - 3.6 V, Uniform sector, WP# = V_{IL} protects lowest addressed sector

TEMPERATURE RANGE
I = Industrial (–40°C to +85°C)

PACKAGE MATERIAL SET
A = Standard (Note 4)
F = Pb-Free

PACKAGE TYPE
B = Fine-pitch Ball-Grid Array Package
D = Fortified Ball-Grid Array Package(LAE064), 9 mm x 9 mm
F = Fortified Ball-Grid Array Package (LAA064), 13 mm x 11 mm
T = Thin Small Outline Package (TSOP) Standard Pinout

SPEED OPTION
See Product Selector Guide and Valid Combinations (90 = 90 ns, 11 = 110 ns)

DEVICE NUMBER/DESCRIPTION
S29GL064N, 64 Megabit Page-Mode Flash Memory
Manufactured using 110 nm MirrorBit® Process Technology, 3.0 Volt-only Read, Program, and Erase

7.1 Valid Combinations

S29GL064N Valid Combinations					Package Description	
Device Number	**Speed Option**	**Package, Material, & Temperature Range**	**Model Number**	**Packing Type**		
S29GL064N	90	TFI	03, 04, 06, 07	0,2,3 (Note 1)	TS048 (Note 2)	TSOP
	11		V6, V7			
	90		01, 02		TS056 (Note 2)	
	11		V1, V2			
	90	BFI	03, 04		VBK048 (Note 3)	Fine-Pitch BGA
	90	FFI	01, 02, 03, 04		LAA064 (Note 3)	Fortified BGA
	11		V1, V2			
	90	DFI	01, 02, 03, 04		LAE064 (Note 3)	
	11		V1, V2			

Notes

1. *Type 0 is standard. Specify others as required: TSOPs can be packed in Types 0 and 3; BGAs can be packed in Types 0, 2, or 3.*
2. *TSOP package marking omits packing type designator from ordering part number.*
3. *BGA package marking omits leading S29 and packing type designator from ordering part number.*
4. *Contact local sales for availability for Leaded lead-frame parts.*

8. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 8.1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 8.1 Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#	ACC	Addresses	DQ0–DQ7	DQ8–DQ15	
									BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	X	X	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write (Program/Erase)	L	H	L	H	(Note 1)	X	A_{IN}	(Note 2)	(Note 2)	
Accelerated Program	L	H	L	H	(Note 1)	V_{HH}	A_{IN}	(Note 2)	(Note 2)	
Standby	$V_{CC} \pm 0.3V$	X	X	$V_{CC} \pm 0.3V$	X	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	X	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	X	X	High-Z	High-Z	High-Z

Legend

L = Logic Low = V_{IL}
H = Logic High = V_{IH}
V_{HH} = 11.5–12.5 V
X = Don't Care
A_{IN} = Address In
D_{IN} = Data In
D_{OUT} = Data Out

Notes

1. *If WP# = V_{IL}, the first or last sector remains protected (for uniform sector devices), and the two outer boot sectors are protected (for boot sector devices). If WP# = VIH, the first or last sector, or the two outer boot sectors are protected or unprotected as determined by the method described in Write Protect (WP#). All sectors are unprotected when shipped from the factory (The Secured Silicon Sector may be factory protected depending on version ordered.)*
2. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm (see Figure 10.5 on page 56).*

8.1 Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic *1*, the device is in word configuration, DQ0–DQ15 are active and controlled by CE#, WE# and OE#.

If the BYTE# pin is set at logic *0*, the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE#, WE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

8.2 Requirements for Reading Array Data

All memories require access time to output array data. In a read operation, data is read from one memory location at a time. Addresses are presented to the device in random order, and the propagation delay through the device causes the data on its outputs to arrive with the address on its inputs.

The device defaults to reading array data after device power-up or hardware reset. To read data from the memory array, the system must first assert a valid address on Amax-A0, while driving OE# and CE# to V_{IL}. WE# must remain at V_{IH}. All addresses are latched on the falling edge of CE#. Data will appear on DQ15-DQ0 after address access time (t_{ACC}), which is equal to the delay from stable addresses to valid output data. The OE# signal must be driven to V_{IL}. Data is output on DQ15-DQ0 pins after the access time (t_{OE}) has elapsed from the falling edge of OE#.

See *Reading Array Data on page 40* for more information. Refer to Table 15.1 on page 64 for timing specifications and the timing diagram. Refer to Table 13.1 on page 62 for the active current specification on reading array data.

8.2.1 Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 8 words/16 bytes. The appropriate page is selected by the higher address bits A(max)–A3. Address bits A2–A0 in word mode (A2–A-1 in byte mode) determine the specific word within a page. This is an asynchronous operation; the microprocessor supplies the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is deasserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Fast page mode accesses are obtained by keeping the *read-page addresses* constant and changing the *intra-read page* addresses.

8.3 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. The *Word Program Command Sequence* on page 41 contains details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Tables 8.2 – 8.8 indicate the address space that each sector occupies.

Refer to the DC Characteristics table for the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

8.3.1 Write Buffer

Write Buffer Programming allows the system write to a maximum of 16 words/32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms.

8.3.2 Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC or ACC pin, depending on model number. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC or ACC pin, depending on model number, returns the device to normal operation. *Note that the WP#/ACC or ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. WP# contains an internal pull-up; when unconnected, WP# is at V_{IH}.*

8.3.3 Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7-DQ0. Standard read cycle timings (t_{ACC}) apply in this mode. Refer to *Autoselect Mode* on page 28 and *Autoselect Command Sequence* on page 41 for more information.

8.4 Standby Mode

When the system is not reading or writing to the device, it can be placed in to standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{IO} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{IO} \pm 0.3$ V, the device is in the standby mode, but the standby current is greater. The device requires standard access time (t_{ACC}/t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

Refer to the *DC Characteristics* *on page 62* for the standby current specification.

8.5 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Refer to the *DC Characteristics* *on page 62* for the automatic sleep mode current specification.

8.6 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, output pins go to Hi-Z, and all read/write commands are ignored for the duration of the RESET# pulse. Program/Erase operations that were interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3$ V, the device draws CMOS standby current (I_{CC5}).

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 15.4 on page 66 for the timing diagram.

8.7 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in a high impedance state.

Table 8.2 S29GL032N (Models 01, 02, V1, V2) Sector Addresses

Sector	A20-A15	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range	Sector	A20-A15	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range
SA0	000000	64/32	000000h–00FFFFh	000000h–007FFFh	SA32	100000	64/32	200000h–20FFFFh	100000h–107FFFh
SA1	000001	64/32	010000h–01FFFFh	008000h–00FFFFh	SA33	100001	64/32	210000h–21FFFFh	108000h–10FFFFh
SA2	000010	64/32	020000h–02FFFFh	010000h–017FFFh	SA34	100010	64/32	220000h–22FFFFh	110000h–117FFFh
SA3	000011	64/32	030000h–03FFFFh	018000h–01FFFFh	SA35	100011	64/32	230000h–23FFFFh	118000h–11FFFFh
SA4	000100	64/32	040000h–04FFFFh	020000h–027FFFh	SA36	100100	64/32	240000h–24FFFFh	120000h–127FFFh
SA5	000101	64/32	050000h–05FFFFh	028000h–02FFFFh	SA37	100101	64/32	250000h–25FFFFh	128000h–12FFFFh
SA6	000110	64/32	060000h–06FFFFh	030000h–037FFFh	SA38	100110	64/32	260000h–26FFFFh	130000h–137FFFh
SA7	000111	64/32	070000h–07FFFFh	038000h–03FFFFh	SA39	100111	64/32	270000h–27FFFFh	138000h–13FFFFh
SA8	001000	64/32	080000h–08FFFFh	040000h–047FFFh	SA40	101000	64/32	280000h–28FFFFh	140000h–147FFFh
SA9	001001	64/32	090000h–09FFFFh	048000h–04FFFFh	SA41	101001	64/32	290000h–29FFFFh	148000h–14FFFFh
SA10	001010	64/32	0A0000h–0AFFFFh	050000h–057FFFh	SA42	101010	64/32	2A0000h–2AFFFFh	150000h–157FFFh
SA11	001011	64/32	0B0000h–0BFFFFh	058000h–05FFFFh	SA43	101011	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
SA12	001100	64/32	0C0000h–0CFFFFh	060000h–067FFFh	SA44	101100	64/32	2C0000h–2CFFFFh	160000h–167FFFh
SA13	001101	64/32	0D0000h–0DFFFFh	068000h–06FFFFh	SA45	101101	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
SA14	001110	64/32	0E0000h–0EFFFFh	070000h–077FFFh	SA46	101110	64/32	2E0000h–2EFFFFh	170000h–177FFFh
SA15	001111	64/32	0F0000h–0FFFFFh	078000h–07FFFFh	SA47	101111	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
SA16	010000	64/32	100000h–10FFFFh	080000h–087FFFh	SA48	110000	64/32	300000h–30FFFFh	180000h–187FFFh
SA17	010001	64/32	110000h–11FFFFh	088000h–08FFFFh	SA49	110001	64/32	310000h–31FFFFh	188000h–18FFFFh
SA18	010010	64/32	120000h–12FFFFh	090000h–097FFFh	SA50	110010	64/32	320000h–32FFFFh	190000h–197FFFh
SA19	010011	64/32	130000h–13FFFFh	098000h–09FFFFh	SA51	110011	64/32	330000h–33FFFFh	198000h–19FFFFh
SA20	010100	64/32	140000h–14FFFFh	0A0000h–0A7FFFh	SA52	110100	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
SA21	010101	64/32	150000h–15FFFFh	0A8000h–0AFFFFh	SA53	110101	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
SA22	010110	64/32	160000h–16FFFFh	0B0000h–0B7FFFh	SA54	110110	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
SA23	010111	64/32	170000h–17FFFFh	0B8000h–0BFFFFh	SA55	110111	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
SA24	011000	64/32	180000h–18FFFFh	0C0000h–0C7FFFh	SA56	111000	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
SA25	011001	64/32	190000h–19FFFFh	0C8000h–0CFFFFh	SA57	111001	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
SA26	011010	64/32	1A0000h–1AFFFFh	0D0000h–0D7FFFh	SA58	111010	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
SA27	011011	64/32	1B0000h–1BFFFFh	0D8000h–0DFFFFh	SA59	111011	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
SA28	011100	64/32	1C0000h–1CFFFFh	0E0000h–0E7FFFh	SA60	111100	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
SA29	011101	64/32	1D0000h–1DFFFFh	0E8000h–0EFFFFh	SA61	111101	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
SA30	011110	64/32	1E0000h–1EFFFFh	0F0000h–0F7FFFh	SA62	111110	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
SA31	011111	64/32	1F0000h–1FFFFFh	0F8000h–0FFFFFh	SA63	111111	64/32	3F0000h–3FFFFFh	1F8000h–1FFFFFh

Table 8.3 S29GL032N (Model 03) Top Boot Sector Addresses

Sector	A20–A12	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range	Sector	A20–A12	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range
SA0	000000xxx	64/32	000000h–00FFFFh	00000h–07FFFh	SA36	100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh
SA1	000001xxx	64/32	010000h–01FFFFh	08000h–0FFFFh	SA37	100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh
SA2	000010xxx	64/32	020000h–02FFFFh	10000h–17FFFh	SA38	100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
SA3	000011xxx	64/32	030000h–03FFFFh	18000h–1FFFFh	SA39	100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
SA4	000100xxx	64/32	040000h–04FFFFh	20000h–27FFFh	SA40	101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh
SA5	000101xxx	64/32	050000h–05FFFFh	28000h–2FFFFh	SA41	101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
SA6	000110xxx	64/32	060000h–06FFFFh	30000h–37FFFh	SA42	101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh
SA7	000111xxx	64/32	070000h–07FFFFh	38000h–3FFFFh	SA43	101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
SA8	001000xxx	64/32	080000h–08FFFFh	40000h–47FFFh	SA44	101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
SA9	001001xxx	64/32	090000h–09FFFFh	48000h–4FFFFh	SA45	101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
SA10	001010xxx	64/32	0A0000h–0AFFFFh	50000h–57FFFh	SA46	101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
SA11	001011xxx	64/32	0B0000h–0BFFFFh	58000h–5FFFFh	SA47	101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
SA12	001100xxx	64/32	0C0000h–0CFFFFh	60000h–67FFFh	SA48	110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
SA13	001101xxx	64/32	0D0000h–0DFFFFh	68000h–6FFFFh	SA49	110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh
SA14	001110xxx	64/32	0E0000h–0EFFFFh	70000h–77FFFh	SA50	110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh
SA15	001111xxx	64/32	0F0000h–0FFFFFh	78000h–7FFFFh	SA51	110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh
SA16	010000xxx	64/32	100000h–10FFFFh	80000h–87FFFh	SA52	100100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
SA17	010001xxx	64/32	110000h–11FFFFh	88000h–8FFFFh	SA53	110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
SA18	010010xxx	64/32	120000h–12FFFFh	90000h–97FFFh	SA54	110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
SA19	010011xxx	64/32	130000h–13FFFFh	98000h–9FFFFh	SA55	110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
SA20	010100xxx	64/32	140000h–14FFFFh	A0000h–A7FFFh	SA56	111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
SA21	010101xxx	64/32	150000h–15FFFFh	A8000h–AFFFFh	SA57	111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
SA22	010110xxx	64/32	160000h–16FFFFh	B0000h–B7FFFh	SA58	111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
SA23	010111xxx	64/32	170000h–17FFFFh	B8000h–BFFFFh	SA59	111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
SA24	011000xxx	64/32	180000h–18FFFFh	C0000h–C7FFFh	SA60	111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
SA25	011001xxx	64/32	190000h–19FFFFh	C8000h–CFFFFh	SA61	111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
SA26	011010xxx	64/32	1A0000h–1AFFFFh	D0000h–D7FFFh	SA62	111110xxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
SA27	011011xxx	64/32	1B0000h–1BFFFFh	D8000h–DFFFFh	SA63	111111000	8/4	3F0000h–3F1FFFh	1F8000h–1F8FFFh
SA28	011100xxx	64/32	1C0000h–1CFFFFh	E0000h–E7FFFh	SA64	111111001	8/4	3F2000h–3F3FFFh	1F9000h–1F9FFFh
SA29	011101xxx	64/32	1D0000h–1DFFFFh	E8000h–EFFFFh	SA65	111111010	8/4	3F4000h–3F5FFFh	1FA000h–1FAFFFh
SA30	011110xxx	64/32	1E0000h–1EFFFFh	F0000h–F7FFFh	SA66	111111011	8/4	3F6000h–3F7FFFh	1FB000h–1FBFFFh
SA31	011111xxx	64/32	1F0000h–1FFFFFh	F8000h–FFFFFh	SA67	111111100	8/4	3F8000h–3F9FFFh	1FC000h–1FCFFFh
SA32	100000xxx	64/32	200000h–20FFFFh	100000h–107FFFh	SA68	111111101	8/4	3FA000h–3FBFFFh	1FD000h–1FDFFFh
SA33	100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh	SA69	111111110	8/4	3FC000h–3FDFFFh	1FE000h–1FEFFFh
SA34	100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh	SA70	111111111	8/4	3FE000h–3FFFFFh	1FF000h–1FFFFFh
SA35	100011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh					

Table 8.4 S29GL032N (Model 04) Bottom Boot Sector Addresses

Sector	A20–A12	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range
SA0	000000000	8/4	000000h–001FFFh	00000h–00FFFh
SA1	000000001	8/4	002000h–003FFFh	01000h–01FFFh
SA2	000000010	8/4	004000h–005FFFh	02000h–02FFFh
SA3	000000011	8/4	006000h–007FFFh	03000h–03FFFh
SA4	000000100	8/4	008000h–009FFFh	04000h–04FFFh
SA5	000000101	8/4	00A000h–00BFFFh	05000h–05FFFh
SA6	000000110	8/4	00C000h–00DFFFh	06000h–06FFFh
SA7	000000111	8/4	00E000h–00FFFFh	07000h–07FFFh
SA8	000001xxx	64/32	010000h–01FFFFh	08000h–0FFFFh
SA9	000010xxx	64/32	020000h–02FFFFh	10000h–17FFFh
SA10	000011xxx	64/32	030000h–03FFFFh	18000h–1FFFFh
SA11	000100xxx	64/32	040000h–04FFFFh	20000h–27FFFh
SA12	000101xxx	64/32	050000h–05FFFFh	28000h–2FFFFh
SA13	000110xxx	64/32	060000h–06FFFFh	30000h–37FFFh
SA14	000111xxx	64/32	070000h–07FFFFh	38000h–3FFFFh
SA15	001000xxx	64/32	080000h–08FFFFh	40000h–47FFFh
SA16	001001xxx	64/32	090000h–09FFFFh	48000h–4FFFFh
SA17	001010xxx	64/32	0A0000h–0AFFFFh	50000h–57FFFh
SA18	001011xxx	64/32	0B0000h–0BFFFFh	58000h–5FFFFh
SA19	001100xxx	64/32	0C0000h–0CFFFFh	60000h–67FFFh
SA20	001101xxx	64/32	0D0000h–0DFFFFh	68000h–6FFFFh
SA21	001110xxx	64/32	0E0000h–0EFFFFh	70000h–77FFFh
SA22	001111xxx	64/32	0F0000h–0FFFFFh	78000h–7FFFFh
SA23	010000xxx	64/32	100000h–10FFFFh	80000h–87FFFh
SA24	010001xxx	64/32	110000h–11FFFFh	88000h–8FFFFh
SA25	010010xxx	64/32	120000h–12FFFFh	90000h–97FFFh
SA26	010011xxx	64/32	130000h–13FFFFh	98000h–9FFFFh
SA27	010100xxx	64/32	140000h–14FFFFh	A0000h–A7FFFh
SA28	010101xxx	64/32	150000h–15FFFFh	A8000h–AFFFFh
SA29	010110xxx	64/32	160000h–16FFFFh	B0000h–B7FFFh
SA30	010111xxx	64/32	170000h–17FFFFh	B8000h–BFFFFh
SA31	011000xxx	64/32	180000h–18FFFFh	C0000h–C7FFFh
SA32	011001xxx	64/32	190000h–19FFFFh	C8000h–CFFFFh
SA33	011010xxx	64/32	1A0000h–1AFFFFh	D0000h–D7FFFh
SA34	011011xxx	64/32	1B0000h–1BFFFFh	D8000h–DFFFFh
SA35	011100xxx	64/32	1C0000h–1CFFFFh	E0000h–E7FFFh
SA36	011101xxx	64/32	1D0000h–1DFFFFh	E8000h–EFFFFh
SA37	011110xxx	64/32	1E0000h–1EFFFFh	F0000h–F7FFFh
SA38	011111xxx	64/32	1F0000h–1FFFFFh	F8000h–FFFFFh
SA39	100000xxx	64/32	200000h–20FFFFh	100000h–107FFFh
SA40	100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh
SA41	100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh
SA42	100011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh
SA43	100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh
SA44	100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh
SA45	100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
SA46	100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
SA47	101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh
SA48	101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
SA49	101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh
SA50	101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
SA51	101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
SA52	101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
SA53	101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
SA54	101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
SA55	110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
SA56	110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh
SA57	110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh
SA58	110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh
SA59	110100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
SA60	110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
SA61	110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
SA62	110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
SA63	111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
SA64	111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
SA65	111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
SA66	111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
SA67	111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
SA68	111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
SA69	111110xxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
SA70	111111xxx	64/32	3F0000h–3FFFFFh	1F8000h–1FFFFFh

Table 8.5 S29GL064N (Models 01, 02, V1, V2) Sector Addresses (Sheet 1 of 2)

Sector	A21–A15	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range	Sector	A21–A15	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range
SA0	0000000	64/32	000000h–00FFFFh	000000h–007FFFh	SA64	1000000	64/32	400000h–40FFFFh	200000h–207FFFh
SA1	0000001	64/32	010000h–01FFFFh	008000h–00FFFFh	SA65	1000001	64/32	410000h–41FFFFh	208000h–20FFFFh
SA2	0000010	64/32	020000h–02FFFFh	010000h–017FFFh	SA66	1000010	64/32	420000h–42FFFFh	210000h–217FFFh
SA3	0000011	64/32	030000h–03FFFFh	018000h–01FFFFh	SA67	1000011	64/32	430000h–43FFFFh	218000h–21FFFFh
SA4	0000100	64/32	040000h–04FFFFh	020000h–027FFFh	SA68	1000100	64/32	440000h–44FFFFh	220000h–227FFFh
SA5	0000101	64/32	050000h–05FFFFh	028000h–02FFFFh	SA69	1000101	64/32	450000h–45FFFFh	228000h–22FFFFh
SA6	0000110	64/32	060000h–06FFFFh	030000h–037FFFh	SA70	1000110	64/32	460000h–46FFFFh	230000h–237FFFh
SA7	0000111	64/32	070000h–07FFFFh	038000h–03FFFFh	SA71	1000111	64/32	470000h–47FFFFh	238000h–23FFFFh
SA8	0001000	64/32	080000h–08FFFFh	040000h–047FFFh	SA72	1001000	64/32	480000h–48FFFFh	240000h–247FFFh
SA9	0001001	64/32	090000h–09FFFFh	048000h–04FFFFh	SA73	1001001	64/32	490000h–49FFFFh	248000h–24FFFFh
SA10	0001010	64/32	0A0000h–0AFFFFh	050000h–057FFFh	SA74	1001010	64/32	4A0000h–4AFFFFh	250000h–257FFFh
SA11	0001011	64/32	0B0000h–0BFFFFh	058000h–05FFFFh	SA75	1001011	64/32	4B0000h–4BFFFFh	258000h–25FFFFh
SA12	0001100	64/32	0C0000h–0CFFFFh	060000h–067FFFh	SA76	1001100	64/32	4C0000h–4CFFFFh	260000h–267FFFh
SA13	0001101	64/32	0D0000h–0DFFFFh	068000h–06FFFFh	SA77	1001101	64/32	4D0000h–4DFFFFh	268000h–26FFFFh
SA14	0001110	64/32	0E0000h–0EFFFFh	070000h–077FFFh	SA78	1001110	64/32	4E0000h–4EFFFFh	270000h–277FFFh
SA15	0001111	64/32	0F0000h–0FFFFFh	078000h–07FFFFh	SA79	1001111	64/32	4F0000h–4FFFFFh	278000h–27FFFFh
SA16	0010000	64/32	100000h–10FFFFh	080000h–087FFFh	SA80	1010000	64/32	500000h–50FFFFh	280000h–287FFFh
SA17	0010001	64/32	110000h–11FFFFh	088000h–08FFFFh	SA81	1010001	64/32	510000h–51FFFFh	288000h–28FFFFh
SA18	0010010	64/32	120000h–12FFFFh	090000h–097FFFh	SA82	1010010	64/32	520000h–52FFFFh	290000h–297FFFh
SA19	0010011	64/32	130000h–13FFFFh	098000h–09FFFFh	SA83	1010011	64/32	530000h–53FFFFh	298000h–29FFFFh
SA20	0010100	64/32	140000h–14FFFFh	0A0000h–0A7FFFh	SA84	1010100	64/32	540000h–54FFFFh	2A0000h–2A7FFFh
SA21	0010101	64/32	150000h–15FFFFh	0A8000h–0AFFFFh	SA85	1010101	64/32	550000h–55FFFFh	2A8000h–2AFFFFh
SA22	0010110	64/32	160000h–16FFFFh	0B0000h–0B7FFFh	SA86	1010110	64/32	560000h–56FFFFh	2B0000h–2B7FFFh
SA23	0010111	64/32	170000h–17FFFFh	0B8000h–0BFFFFh	SA87	1010111	64/32	570000h–57FFFFh	2B8000h–2BFFFFh
SA24	0011000	64/32	180000h–18FFFFh	0C0000h–0C7FFFh	SA88	1011000	64/32	580000h–58FFFFh	2C0000h–2C7FFFh
SA25	0011001	64/32	190000h–19FFFFh	0C8000h–0CFFFFh	SA89	1011001	64/32	590000h–59FFFFh	2C8000h–2CFFFFh
SA26	0011010	64/32	1A0000h–1AFFFFh	0D0000h–0D7FFFh	SA90	1011010	64/32	5A0000h–5AFFFFh	2D0000h–2D7FFFh
SA27	0011011	64/32	1B0000h–1BFFFFh	0D8000h–0DFFFFh	SA91	1011011	64/32	5B0000h–5BFFFFh	2D8000h–2DFFFFh
SA28	0011100	64/32	1C0000h–1CFFFFh	0E0000h–0E7FFFh	SA92	1011100	64/32	5C0000h–5CFFFFh	2E0000h–2E7FFFh
SA29	0011101	64/32	1D0000h–1DFFFFh	0E8000h–0EFFFFh	SA93	1011101	64/32	5D0000h–5DFFFFh	2E8000h–2EFFFFh
SA30	0011110	64/32	1E0000h–1EFFFFh	0F0000h–0F7FFFh	SA94	1011110	64/32	5E0000h–5EFFFFh	2F0000h–2F7FFFh
SA31	0011111	64/32	1F0000h–1FFFFFh	0F8000h–0FFFFFh	SA95	1011111	64/32	5F0000h–5FFFFFh	2F8000h–2FFFFFh
SA32	0100000	64/32	200000h–20FFFFh	100000h–107FFFh	SA96	1100000	64/32	600000h–60FFFFh	300000h–307FFFh
SA33	0100001	64/32	210000h–21FFFFh	108000h–10FFFFh	SA97	1100001	64/32	610000h–61FFFFh	308000h–30FFFFh
SA34	0100010	64/32	220000h–22FFFFh	110000h–117FFFh	SA98	1100010	64/32	620000h–62FFFFh	310000h–317FFFh
SA35	0100011	64/32	230000h–23FFFFh	118000h–11FFFFh	SA99	1100011	64/32	630000h–63FFFFh	318000h–31FFFFh
SA36	0100100	64/32	240000h–24FFFFh	120000h–127FFFh	SA100	1100100	64/32	640000h–64FFFFh	320000h–327FFFh
SA37	0100101	64/32	250000h–25FFFFh	128000h–12FFFFh	SA101	1100101	64/32	650000h–65FFFFh	328000h–32FFFFh
SA38	0100110	64/32	260000h–26FFFFh	130000h–137FFFh	SA102	1100110	64/32	660000h–66FFFFh	330000h–337FFFh
SA39	0100111	64/32	270000h–27FFFFh	138000h–13FFFFh	SA103	1100111	64/32	670000h–67FFFFh	338000h–33FFFFh
SA40	0101000	64/32	280000h–28FFFFh	140000h–147FFFh	SA104	1101000	64/32	680000h–68FFFFh	340000h–347FFFh
SA41	0101001	64/32	290000h–29FFFFh	148000h–14FFFFh	SA105	1101001	64/32	690000h–69FFFFh	348000h–34FFFFh
SA42	0101010	64/32	2A0000h–2AFFFFh	150000h–157FFFh	SA106	1101010	64/32	6A0000h–6AFFFFh	350000h–357FFFh
SA43	0101011	64/32	2B0000h–2BFFFFh	158000h–15FFFFh	SA107	1101011	64/32	6B0000h–6BFFFFh	358000h–35FFFFh

Table 8.5 S29GL064N (Models 01, 02, V1, V2) Sector Addresses (Sheet 2 of 2)

Sector	A21–A15	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range	Sector	A21–A15	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range
SA44	0101100	64/32	2C0000h–2CFFFFh	160000h–167FFFh	SA108	1101100	64/32	6C0000h–6CFFFFh	360000h–367FFFh
SA45	0101101	64/32	2D0000h–2DFFFFh	168000h–16FFFFh	SA109	1101101	64/32	6D0000h–6DFFFFh	368000h–36FFFFh
SA46	0101110	64/32	2E0000h–2EFFFFh	170000h–177FFFh	SA110	1101110	64/32	6E0000h–6EFFFFh	370000h–377FFFh
SA47	0101111	64/32	2F0000h–2FFFFFh	178000h–17FFFFh	SA111	1101111	64/32	6F0000h–6FFFFFh	378000h–37FFFFh
SA48	0110000	64/32	300000h–30FFFFh	180000h–187FFFh	SA112	1110000	64/32	700000h–70FFFFh	380000h–387FFFh
SA49	0110001	64/32	310000h–31FFFFh	188000h–18FFFFh	SA113	1110001	64/32	710000h–71FFFFh	388000h–38FFFFh
SA50	0110010	64/32	320000h–32FFFFh	190000h–197FFFh	SA114	1110010	64/32	720000h–72FFFFh	390000h–397FFFh
SA51	0110011	64/32	330000h–33FFFFh	198000h–19FFFFh	SA115	1110011	64/32	730000h–73FFFFh	398000h–39FFFFh
SA52	0110100	64/32	340000h–34FFFFh	1A0000h–1A7FFFh	SA116	1110100	64/32	740000h–74FFFFh	3A0000h–3A7FFFh
SA53	0110101	64/32	350000h–35FFFFh	1A8000h–1AFFFFh	SA117	1110101	64/32	750000h–75FFFFh	3A8000h–3AFFFFh
SA54	0110110	64/32	360000h–36FFFFh	1B0000h–1B7FFFh	SA118	1110110	64/32	760000h–76FFFFh	3B0000h–3B7FFFh
SA55	0110111	64/32	370000h–37FFFFh	1B8000h–1BFFFFh	SA119	1110111	64/32	770000h–77FFFFh	3B8000h–3BFFFFh
SA56	0111000	64/32	380000h–38FFFFh	1C0000h–1C7FFFh	SA120	1111000	64/32	780000h–78FFFFh	3C0000h–3C7FFFh
SA57	0111001	64/32	390000h–39FFFFh	1C8000h–1CFFFFh	SA121	1111001	64/32	790000h–79FFFFh	3C8000h–3CFFFFh
SA58	0111010	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh	SA122	1111010	64/32	7A0000h–7AFFFFh	3D0000h–3D7FFFh
SA59	0111011	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh	SA123	1111011	64/32	7B0000h–7BFFFFh	3D8000h–3DFFFFh
SA60	0111100	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh	SA124	1111100	64/32	7C0000h–7CFFFFh	3E0000h–3E7FFFh
SA61	0111101	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh	SA125	1111101	64/32	7D0000h–7DFFFFh	3E8000h–3EFFFFh
SA62	0111110	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh	SA126	1111110	64/32	7E0000h–7EFFFFh	3F0000h–3F7FFFh
SA63	0111111	64/32	3F0000h–3FFFFFh	1F8000h–1FFFFFh	SA127	1111111	64/32	7F0000h–7FFFFFh	3F8000h–3FFFFFh

Table 8.6 S29GL064N (Model 03) Top Boot Sector Addresses (Sheet 1 of 3)

Sector	A21–A12	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range	Sector	A21–A12	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range
SA0	0000000xxx	64/32	000000h–00FFFFh	000000h–007FFFh	SA68	1000100xxx	64/32	440000h–44FFFFh	220000h–227FFFh
SA1	0000001xxx	64/32	010000h–01FFFFh	008000h–00FFFFh	SA69	1000101xxx	64/32	450000h–45FFFFh	228000h–22FFFFh
SA2	0000010xxx	64/32	020000h–02FFFFh	010000h–017FFFh	SA70	1000110xxx	64/32	460000h–46FFFFh	230000h–237FFFh
SA3	0000011xxx	64/32	030000h–03FFFFh	018000h–01FFFFh	SA71	1000111xxx	64/32	470000h–47FFFFh	238000h–23FFFFh
SA4	0000100xxx	64/32	040000h–04FFFFh	020000h–027FFFh	SA72	1001000xxx	64/32	480000h–48FFFFh	240000h–247FFFh
SA5	0000101xxx	64/32	050000h–05FFFFh	028000h–02FFFFh	SA73	1001001xxx	64/32	490000h–49FFFFh	248000h–24FFFFh
SA6	0000110xxx	64/32	060000h–06FFFFh	030000h–037FFFh	SA74	1001010xxx	64/32	4A0000h–4AFFFFh	250000h–257FFFh
SA7	0000111xxx	64/32	070000h–07FFFFh	038000h–03FFFFh	SA75	1001011xxx	64/32	4B0000h–4BFFFFh	258000h–25FFFFh
SA8	0001000xxx	64/32	080000h–08FFFFh	040000h–047FFFh	SA76	1001100xxx	64/32	4C0000h–4CFFFFh	260000h–267FFFh
SA9	0001001xxx	64/32	090000h–09FFFFh	048000h–04FFFFh	SA77	1001101xxx	64/32	4D0000h–4DFFFFh	268000h–26FFFFh
SA10	0001010xxx	64/32	0A0000h–0AFFFFh	050000h–057FFFh	SA78	1001110xxx	64/32	4E0000h–4EFFFFh	270000h–277FFFh
SA11	0001011xxx	64/32	0B0000h–0BFFFFh	058000h–05FFFFh	SA79	1001111xxx	64/32	4F0000h–4FFFFFh	278000h–27FFFFh
SA12	0001100xxx	64/32	0C0000h–0CFFFFh	060000h–067FFFh	SA80	1010000xxx	64/32	500000h–50FFFFh	280000h–287FFFh
SA13	0001101xxx	64/32	0D0000h–0DFFFFh	068000h–06FFFFh	SA81	1010001xxx	64/32	510000h–51FFFFh	288000h–28FFFFh
SA14	0001110xxx	64/32	0E0000h–0EFFFFh	070000h–077FFFh	SA82	1010010xxx	64/32	520000h–52FFFFh	290000h–297FFFh
SA15	0001111xxx	64/32	0F0000h–0FFFFFh	078000h–07FFFFh	SA83	1010011xxx	64/32	530000h–53FFFFh	298000h–29FFFFh
SA16	0010000xxx	64/32	100000h–10FFFFh	080000h–087FFFh	SA84	1010100xxx	64/32	540000h–54FFFFh	2A0000h–2A7FFFh
SA17	0010001xxx	64/32	110000h–11FFFFh	088000h–08FFFFh	SA85	1010101xxx	64/32	550000h–55FFFFh	2A8000h–2AFFFFh
SA18	0010010xxx	64/32	120000h–12FFFFh	090000h–097FFFh	SA86	1010110xxx	64/32	560000h–56FFFFh	2B0000h–2B7FFFh

Table 8.6 S29GL064N (Model 03) Top Boot Sector Addresses (Sheet 2 of 3)

Sector	A21–A12	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range	Sector	A21–A12	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range
SA19	0010011xxx	64/32	130000h–13FFFFh	098000h–09FFFFh	SA87	1010111xxx	64/32	570000h–57FFFFh	2B8000h–2BFFFFh
SA20	0010100xxx	64/32	140000h–14FFFFh	0A0000h–0A7FFFh	SA88	1011000xxx	64/32	580000h–58FFFFh	2C0000h–2C7FFFh
SA21	0010101xxx	64/32	150000h–15FFFFh	0A8000h–0AFFFFh	SA89	1011001xxx	64/32	590000h–59FFFFh	2C8000h–2CFFFFh
SA22	0010110xxx	64/32	160000h–16FFFFh	0B0000h–0B7FFFh	SA90	1011010xxx	64/32	5A0000h–5AFFFFh	2D0000h–2D7FFFh
SA23	0010111xxx	64/32	170000h–17FFFFh	0B8000h–0BFFFFh	SA91	1011011xxx	64/32	5B0000h–5BFFFFh	2D8000h–2DFFFFh
SA24	0011000xxx	64/32	180000h–18FFFFh	0C0000h–0C7FFFh	SA92	1011100xxx	64/32	5C0000h–5CFFFFh	2E0000h–2E7FFFh
SA25	0011001xxx	64/32	190000h–19FFFFh	0C8000h–0CFFFFh	SA93	1011101xxx	64/32	5D0000h–5DFFFFh	2E8000h–2EFFFFh
SA26	0011010xxx	64/32	1A0000h–1AFFFFh	0D0000h–0D7FFFh	SA94	1011110xxx	64/32	5E0000h–5EFFFFh	2F0000h–2F7FFFh
SA27	0011011xxx	64/32	1B0000h–1BFFFFh	0D8000h–0DFFFFh	SA95	1011111xxx	64/32	5F0000h–5FFFFFh	2F8000h–2FFFFFh
SA28	0011100xxx	64/32	1C0000h–1CFFFFh	0E0000h–0E7FFFh	SA96	1100000xxx	64/32	600000h–60FFFFh	300000h–307FFFh
SA29	0011101xxx	64/32	1D0000h–1DFFFFh	0E8000h–0EFFFFh	SA97	1100001xxx	64/32	610000h–61FFFFh	308000h–30FFFFh
SA30	0011110xxx	64/32	1E0000h–1EFFFFh	0F0000h–0F7FFFh	SA98	1100010xxx	64/32	620000h–62FFFFh	310000h–317FFFh
SA31	0011111xxx	64/32	1F0000h–1FFFFFh	0F8000h–0FFFFFh	SA99	1100011xxx	64/32	630000h–63FFFFh	318000h–31FFFFh
SA32	0100000xxx	64/32	200000h–20FFFFh	100000h–107FFFh	SA100	1100100xxx	64/32	640000h–64FFFFh	320000h–327FFFh
SA33	0100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh	SA101	1100101xxx	64/32	650000h–65FFFFh	328000h–32FFFFh
SA34	0100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh	SA102	1100110xxx	64/32	660000h–66FFFFh	330000h–337FFFh
SA35	0101011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh	SA103	1100111xxx	64/32	670000h–67FFFFh	338000h–33FFFFh
SA36	0100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh	SA104	1101000xxx	64/32	680000h–68FFFFh	340000h–347FFFh
SA37	0100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh	SA105	1101001xxx	64/32	690000h–69FFFFh	348000h–34FFFFh
SA38	0100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh	SA106	1101010xxx	64/32	6A0000h–6AFFFFh	350000h–357FFFh
SA39	0100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh	SA107	1101011xxx	64/32	6B0000h–6BFFFFh	358000h–35FFFFh
SA40	0101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh	SA108	1101100xxx	64/32	6C0000h–6CFFFFh	360000h–367FFFh

Table 8.6 S29GL064N (Model 03) Top Boot Sector Addresses (Sheet 3 of 3)

Sector	A21–A12	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range	Sector	A21–A12	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range
SA41	0101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh	SA109	1101101xxx	64/32	6D0000h–6DFFFFh	368000h–36FFFFh
SA42	0101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh	SA110	1101110xxx	64/32	6E0000h–6EFFFFh	370000h–377FFFh
SA43	0101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh	SA111	1101111xxx	64/32	6F0000h–6FFFFFh	378000h–37FFFFh
SA44	0101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh	SA112	1110000xxx	64/32	700000h–70FFFFh	380000h–387FFFh
SA45	0101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh	SA113	1110001xxx	64/32	710000h–71FFFFh	388000h–38FFFFh
SA46	0101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh	SA114	1110010xxx	64/32	720000h–72FFFFh	390000h–397FFFh
SA47	0101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh	SA115	1110011xxx	64/32	730000h–73FFFFh	398000h–39FFFFh
SA48	0110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh	SA116	1110100xxx	64/32	740000h–74FFFFh	3A0000h–3A7FFFh
SA49	0110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh	SA117	1110101xxx	64/32	750000h–75FFFFh	3A8000h–3AFFFFh
SA50	0110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh	SA118	1110110xxx	64/32	760000h–76FFFFh	3B0000h–3B7FFFh
SA51	0110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh	SA119	1110111xxx	64/32	770000h–77FFFFh	3B8000h–3BFFFFh
SA52	0110100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh	SA120	1111000xxx	64/32	780000h–78FFFFh	3C0000h–3C7FFFh
SA53	0110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh	SA121	1111001xxx	64/32	790000h–79FFFFh	3C8000h–3CFFFFh
SA54	0110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh	SA122	1111010xxx	64/32	7A0000h–7AFFFFh	3D0000h–3D7FFFh
SA55	0110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh	SA123	1111011xxx	64/32	7B0000h–7BFFFFh	3D8000h–3DFFFFh
SA56	0111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh	SA124	1111100xxx	64/32	7C0000h–7CFFFFh	3E0000h–3E7FFFh
SA57	0111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh	SA125	1111101xxx	64/32	7D0000h–7DFFFFh	3E8000h–3EFFFFh
SA58	0111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh	SA126	1111110xxx	64/32	7E0000h–7EFFFFh	3F0000h–3F7FFFh
SA59	0111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh	SA127	1111111000	8/4	7F0000h–7F1FFFh	3F8000h–3F8FFFh
SA60	0111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh	SA128	1111111001	8/4	7F2000h–7F3FFFh	3F9000h–3F9FFFh
SA61	0111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh	SA129	1111111010	8/4	7F4000h–7F5FFFh	3FA000h–3FAFFFh
SA62	0111110xxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh	SA130	1111111011	8/4	7F6000h–7F7FFFh	3FB000h–3FBFFFh
SA63	0111111xxx	64/32	3F0000h–3FFFFFh	1F8000h–1FFFFFh	SA131	1111111100	8/4	7F8000h–7F9FFFh	3FC000h–3FCFFFh
SA64	1000000xxx	64/32	400000h–40FFFFh	200000h–207FFFh	SA132	1111111101	8/4	7FA000h–7FBFFFh	3FD000h–3FDFFFh
SA65	1000001xxx	64/32	410000h–41FFFFh	208000h–20FFFFh	SA133	1111111110	8/4	7FC000h–7FDFFFh	3FE000h–3FEFFFh
SA66	1000010xxx	64/32	420000h–42FFFFh	210000h–217FFFh	SA134	1111111111	8/4	7FE000h–7FFFFFh	3FF000h–3FFFFFh
SA67	1000011xxx	64/32	430000h–43FFFFh	218000h–21FFFFh					

Table 8.7 S29GL064N (Model 04) Bottom Boot Sector Addresses (Sheet 1 of 3)

Sector	A21–A12	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range	Sector	A21–A12	Sector Size (KB/ Kwords)	8-bit Address Range	16-bit Address Range
SA0	0000000000	8/4	000000h–001FFFh	000000h–000FFFh	SA45	0100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
SA1	0000000001	8/4	002000h–003FFFh	001000h–001FFFh	SA46	0100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
SA2	0000000010	8/4	004000h–005FFFh	002000h–002FFFh	SA47	0101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh
SA3	0000000011	8/4	006000h–007FFFh	003000h–003FFFh	SA48	0101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
SA4	0000000100	8/4	008000h–009FFFh	004000h–004FFFh	SA49	0101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh
SA5	0000000101	8/4	00A000h–00BFFFh	005000h–005FFFh	SA50	0101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
SA6	0000000110	8/4	00C000h–00DFFFh	006000h–006FFFh	SA51	0101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
SA7	0000000111	8/4	00E000h–00FFFFh	007000h–007FFFh	SA52	0101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
SA8	0000001xxx	64/32	010000h–01FFFFh	008000h–00FFFFh	SA53	0101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
SA9	0000010xxx	64/32	020000h–02FFFFh	010000h–017FFFh	SA54	0101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
SA10	0000011xxx	64/32	030000h–03FFFFh	018000h–01FFFFh	SA55	0110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
SA11	0000100xxx	64/32	040000h–04FFFFh	020000h–027FFFh	SA56	0110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh