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S29GL064S

64 Mbit (8 Mbyte) 3.0 V Flash Memory

Distinctive Characteristics

- CMOS 3.0 Volt Core with Versatile I/O

Architectural Advantages

- Single Power Supply Operation
- Manufactured on 65 nm MirrorBit Process Technology
- Secure Silicon Region
  - 128-word / 256-byte sector for permanent, secure identification through an 8-word / 16-byte random Electronic Serial Number, accessible through a command sequence
  - Programmed and locked at the factory or by the customer
- Flexible Sector Architecture
  - 64 Mb (uniform sector models): One hundred twenty-eight 32-kword (64-kB) sectors
  - 64 Mb (boot sector models): One hundred twenty-seven 32-kword (64-kB) sectors + eight 4kword (8kB) boot sectors
- Automatic Error Checking and Correction (ECC) - internal hardware ECC with single bit error correction
- Enhanced VersatileI/O Control
  - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on V_{IO} input. V_{IO} range is 1.65 to V_{CC}
- Compatibility with JEDEC Standards
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- 100,000 Erase Cycles per Sector Minimum
- 20-year Data Retention Typical

Performance Characteristics

- High Performance
  - 70 ns access time
  - 8-word / 16-byte page read buffer
  - 15 ns page read time
  - 128-word / 256-byte write buffer which reduces overall programming time for multiple-word updates
- Low Power Consumption
  - 25 mA typical initial read current @ 5 MHz
  - 7.5 mA typical page read current @ 33 MHz
  - 50 mA typical erase / program current
  - 40 µA typical standby mode current
- Package Options
  - 48-pin TSOP
  - 56-pin TSOP
  - 64-ball Fortified BGA (LAA064 13 mm x 11 mm x 1.4 mm) (LAE064 9 mm x 9 mm x 1.4 mm)
  - 48-ball fine-pitch BGA (VBK048 8.15 mm x 6.15 mm x 1.0 mm)
- Temperature Range
  - Industrial (-40°C to +85°C)
  - Industrial Plus (-40°C to +105°C)
  - Automotive, AEC-Q100 Grade 3 (-40°C to +85°C)
  - Automotive, AEC-Q100 Grade 2(-40°C to +105°C)

Software and Hardware Features

- Software Features
  - Advanced Sector Protection: offers Persistent Sector Protection and Password Sector Protection
  - Program Suspend and Resume: read other sectors before programming operation is completed
  - Erase Suspend and Resume: read / program other sectors before an erase operation is completed
  - Data# polling and toggle bits provide status
  - CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
  - Unlock Bypass Program command reduces overall multiple-word programming time
- Hardware Features
  - WP#/ACC input supports manufacturing programming operations (when high voltage is applied). Protects first or last sector regardless of sector protection settings on uniform sector models
  - Hardware reset input (RESET#) resets device
  - Ready/Busy# output (RY/BY#) detects program or erase cycle completion

General Description

The S29GL-S mid density family of devices are 3.0-volt single-power flash memory manufactured using 65 nm MirrorBit technology. The S29GL064S is a 64-Mb device organized as 4,194,304 words or 8,388,608 bytes. Depending on the model number, the devices have 16-bit wide data bus only, or a 16-bit wide data bus that can also function as an 8-bit wide data bus by using the BYTE# input. The devices can be programmed either in the host system or in standard EPROM programmers.

Access times as fast as 70 ns are available. Note that each access time has a specific operating voltage range (V_{CC}) as specified in the *Product Selector Guide* and *Ordering Information*. Package offerings include 48-pin TSOP, 56-pin TSOP, 48-ball fine-pitch BGA, and 64-ball Fortified BGA, depending on model number. Each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0-volt power supply** for both read and write functions. In addition to a V_{CC} input, a high-voltage **accelerated program (ACC)** feature is supported through increased voltage on the WP#/ACC or ACC input. This feature is intended to facilitate system production.

The device is entirely command set compatible with the **JEDEC single-power-supply flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

The **Advanced Sector Protection** features several levels of sector protection, which can disable both the program and erase operations in certain sectors. Persistent Sector Protection is a method that replaces the previous 12-volt controlled protection method. Password Sector Protection is a highly sophisticated protection method that requires a password before changes to certain sectors are permitted.

Device programming and erasure are initiated through command sequences. Once a program or erase operation begins, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready**/**Busy# (RY**/**BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** / **Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend** / **Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses are stable for a specified period of time.

The **Write Protect (WP#)** feature protects the first or last sector by asserting a logic low on the WP#/ACC pin or WP# pin, depending on model number. The protected sector is still protected even during accelerated programming.

The **Secure Silicon Region** provides a 128-word / 256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

Cypress MirrorBit flash technology combines years of flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

Contents

1. Product Selector Guide

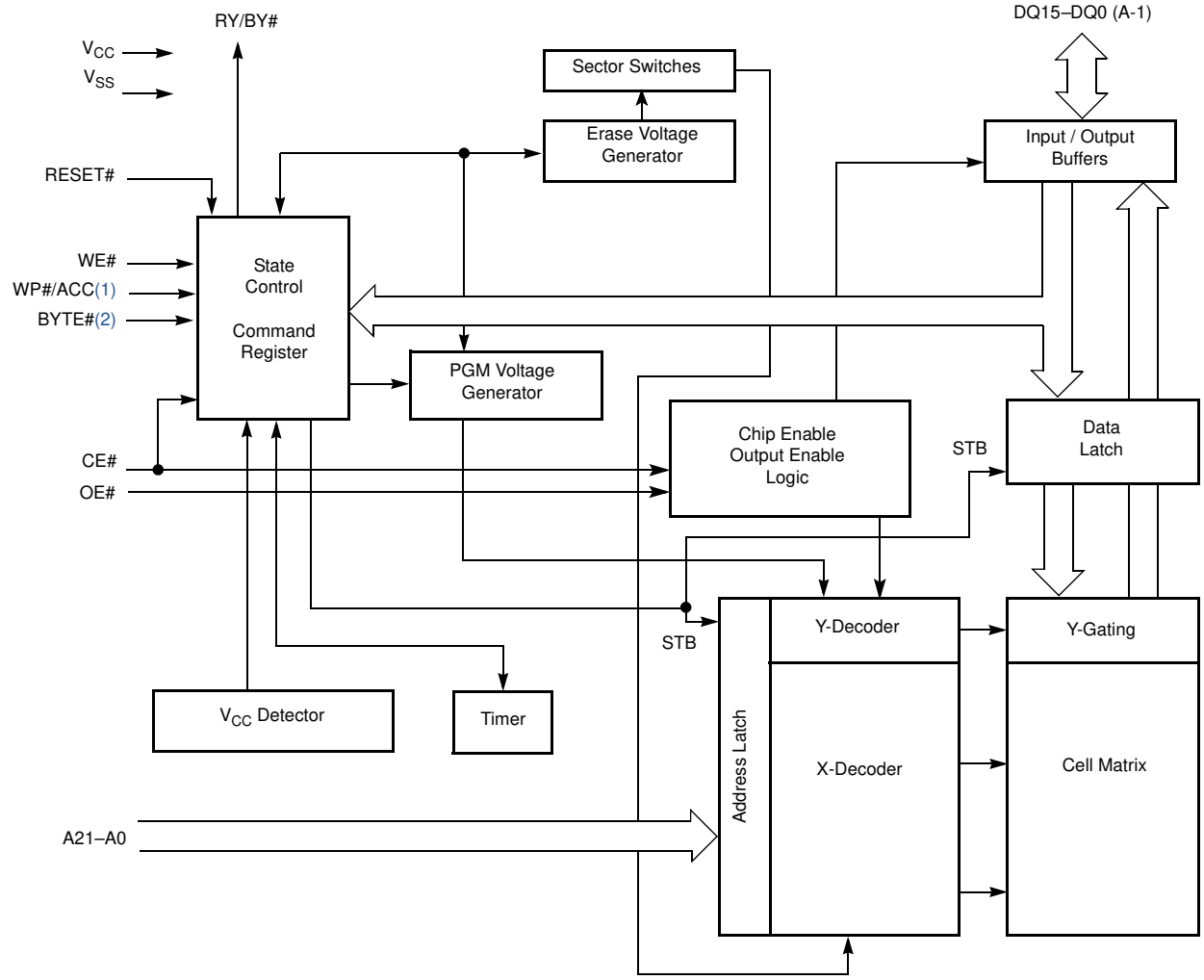
Table 1.1 Product Selector Guide for Industrial Temperature Range (-40°C to +85°C)

Part Number			**S29GL064S**	
Speed Option	V_{CC} = 2.7–3.6V	V_{IO} = 2.7–3.6V	70	
		V_{IO} = 1.65–3.6V		80
Max. Access Time (ns)			70	80
Max. CE# Access Time (ns)			70	80
Max. Page Access Time (ns)			15	25
Max. OE# Access Time (ns)			15	25

Table 1.2 Product Selector Guide for Industrial Plus Temperature Range (-40°C to +105°C)

Part Number			**S29GL064S**	
Speed Option	V_{CC} = 2.7–3.6V	V_{IO} = 2.7–3.6V	80	
		V_{IO} = 1.65–3.6V		90
Max. Access Time (ns)			80	90
Max. CE# Access Time (ns)			80	90
Max. Page Access Time (ns)			15	25
Max. OE# Access Time (ns)			15	25

2. Block Diagram



Notes:

1. *Available on separate pins for models 06, 07, V6, V7.*
2. *Available only on X8/x16 devices.*

3. Connection Diagrams

Special Package Handling Instructions

Special handling is required for flash memory products in molded packages (TSOP and BGA). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

Figure 3.1 48-Pin Standard TSOP

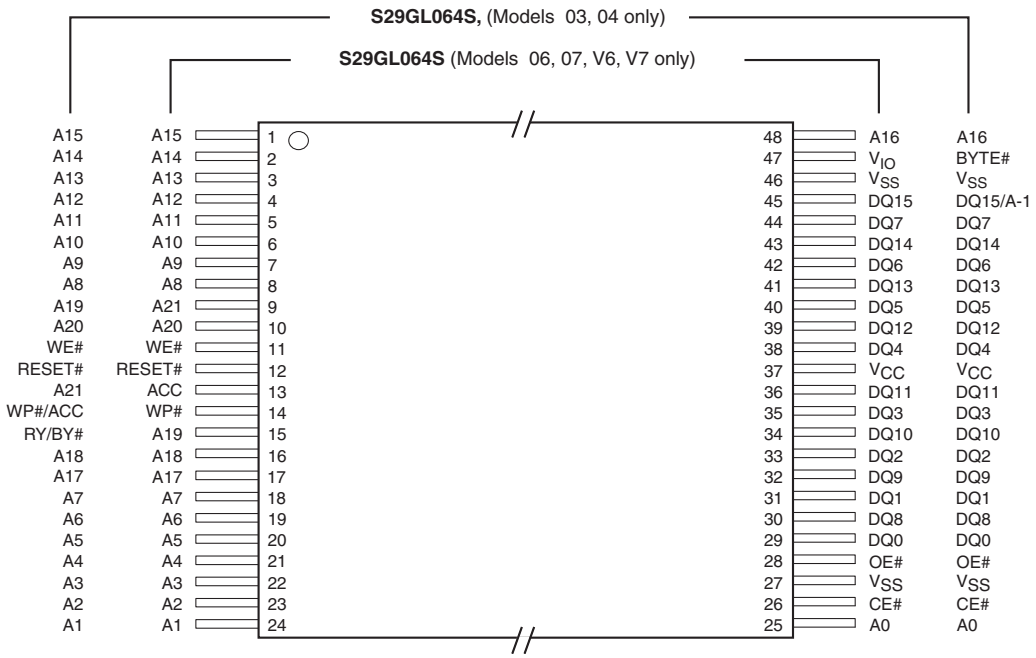
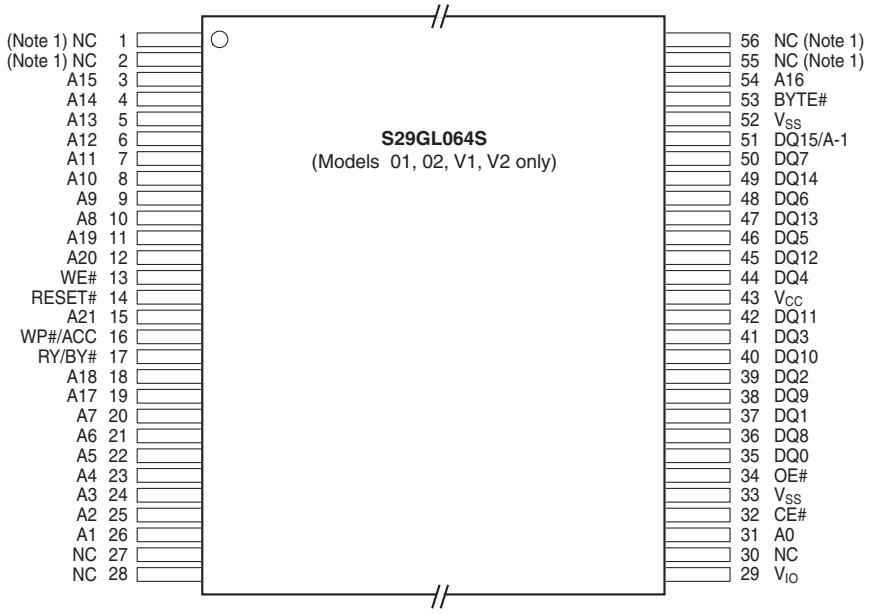


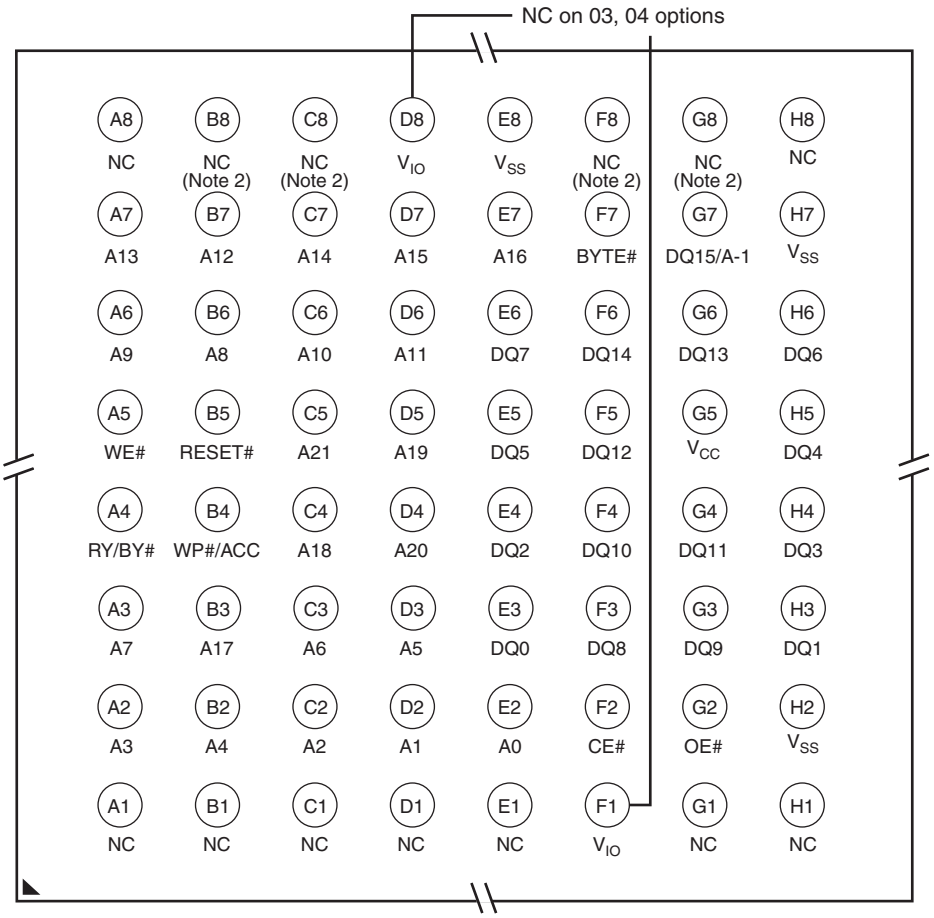
Figure 3.2 56-Pin Standard TSOP



Note:

1. These pins are NC on the S29GL064S, however, are used by 128-Mbit –1-Gbit density GL devices as the high order address inputs.

Figure 3.3 64-Ball Fortified BGA

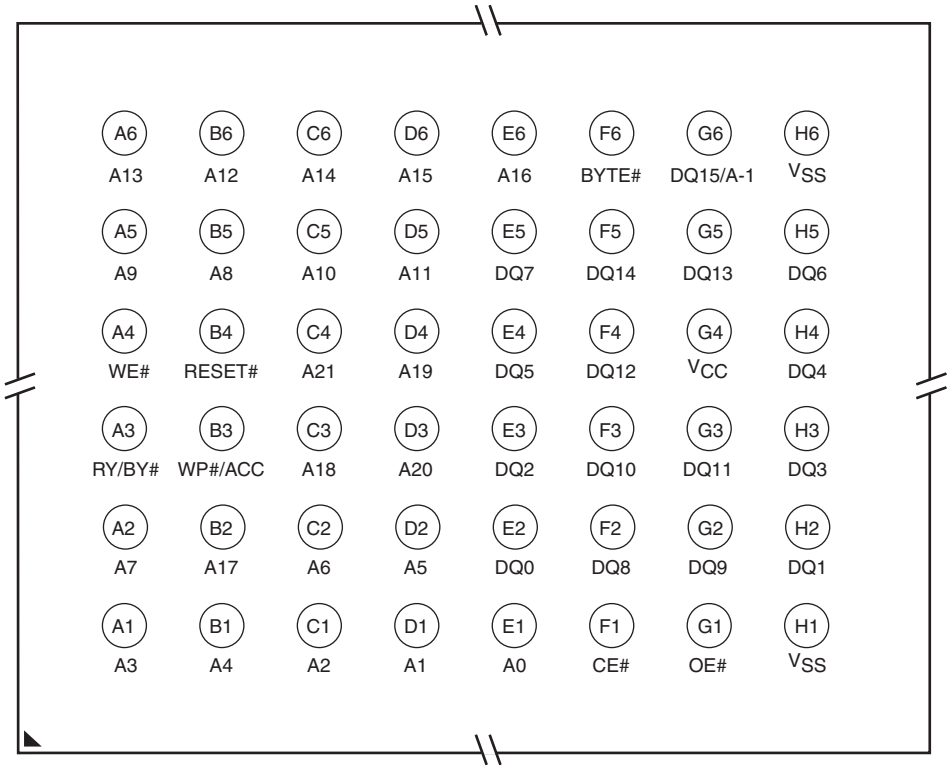


Notes:

1. *S29GL064S (Models 01, 02, 03, 04, V1, V2).*
2. *These balls are NC on the S29GL064S, however, are used by 128- Mbit – 1-Gbit density GL devices as the high order address inputs.*

Figure 3.4 48-Ball Fine-Pitch BGA (VBK 048)

S29GL064S (Models 03, 04 only)
Top View, Balls Facing Down



4. Pin Descriptions

Pin	Description
A21–A0	22 Address inputs (S29GL064S)
DQ7–DQ0	8 Data inputs / outputs
DQ14–DQ0	15 Data inputs / outputs
DQ15/A-1	DQ15 (Data input / output, word mode), A-1 (LSB Address input, byte mode)
CE#	Chip Enable input
OE#	Output Enable input
WE#	Write Enable input
WP#/ACC	Hardware Write Protect input / Programming Acceleration input
ACC	Programming Acceleration input
WP#	Hardware Write Protect input
RESET#	Hardware Reset Pin input
RY/BY#	Ready/Busy output
BYTE#	Selects 8-bit or 16-bit mode
VCC	3.0 volt-only single power supply (see *Product Selector Guide* on page 4 for speed options and voltage supply tolerances)
VIO	Output Buffer Power
VSS	Device Ground
NC	Pin Not Connected Internally
RFU	Reserved for Future Use. Not currently connected internally but the pin/ball location should be left unconnected and unused by PCB routing channel for future compatibility. The pin/ball may be used by a signal in the future.

5. S29GL064S Logical Symbols

Figure 5.1 S29GL064S Logic Symbol (Models 01, 02, V1, V2)

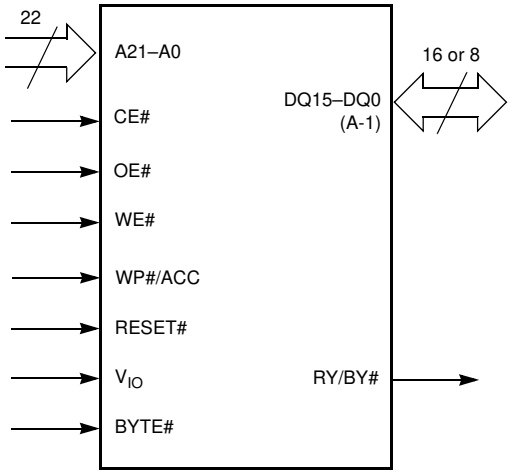


Figure 5.2 S29GL064S Logic Symbol (Models 03, 04)

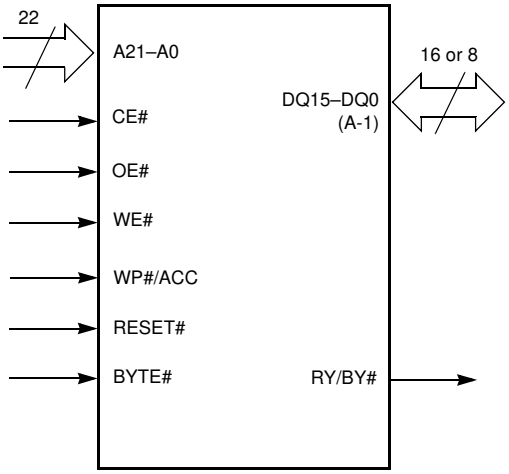
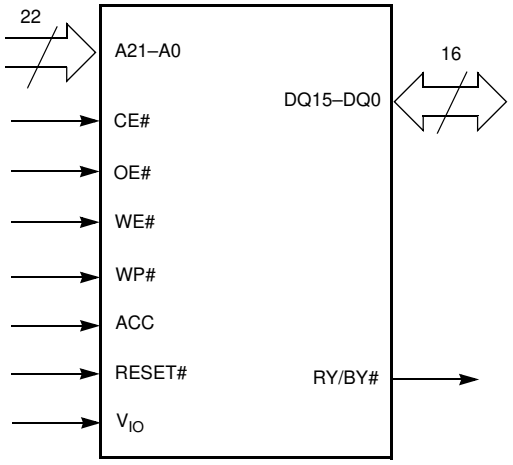


Figure 5.3 S29GL064S Logic Symbol (Models 06, 07, V6, V7)



6. Ordering Information

Standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:

S29GL064S 70 T F I 01 0

Packing Type
0 = Tray
3 = 13-inch Tape and Reel

Model Number
01 = x8/x16, V_{CC} = V_{IO} = 2.7 – 3.6V, Uniform Sector, WP#/ACC = V_{IL} protects highest addressed sector
02 = x8/x16, V_{CC} = V_{IO} = 2.7 – 3.6V, Uniform Sector, WP#/ACC = V_{IL} protects lowest addressed sector
03 = x8/x16, V_{CC} = V_{IO} = 2.7 – 3.6V, Top Boot Sector, WP#/ACC = V_{IL} protects top two addressed sectors (1)
04 = x8/x16, V_{CC} = V_{IO} = 2.7 – 3.6V, Bottom Boot Sector, WP#/ACC = V_{IL} protects bottom two addressed sectors (1)
06 = x16, V_{CC} = V_{IO} = 2.7 – 3.6V, Uniform Sector, WP# = V_{IL} protects highest addressed sector
07 = x16, V_{CC} = V_{IO} = 2.7 – 3.6V, Uniform Sector, WP# = V_{IL} protects lowest addressed sector
V1 = x8/x16, V_{CC} = 2.7 – 3.6V, V_{IO} = 1.65 - 3.6V, Uniform Sector, WP#/ACC = V_{IL} protects highest addressed sector
V2 = x8/x16, V_{CC} = 2.7 – 3.6V, V_{IO} = 1.65 - 3.6V, Uniform Sector, WP#/ACC = V_{IL} protects lowest addressed sector
V6 = x16, V_{CC} = 2.7 – 3.6V, V_{IO} = 1.65 - 3.6V, Uniform Sector, WP# = V_{IL} protects highest addressed sector
V7 = x16, V_{CC} = 2.7 – 3.6V, V_{IO} = 1.65 - 3.6V, Uniform Sector, WP# = V_{IL} protects lowest addressed sector

Temperature Range
I = Industrial (–40°C to +85°C)
V = Industrial Plus (–40°C to +105°C)
A = Automotive, AEC-Q100 Grade 3 (–40°C to +85°C)
B = Automotive, AEC-Q100 Grade 2 (–40°C to +105°C)

Package Material Set
F = Pb-Free
H = Low Halogen, Pb-Free

Package Type
B = Fine-pitch Ball-Grid Array Package (VBK048), 8.15 mm x 6.16 mm
D = Fortified Ball-Grid Array Package (LAE064), 9 mm x 9 mm
F = Fortified Ball-Grid Array Package (LAA064), 13 mm x 11 mm
T = Thin Small Outline Package (TSOP) Standard Pinout

Speed Option
See Product Selector Guide and Valid Combinations (70 = 70 ns, 80 = 80 ns, 90 = 90 ns)

Device Number / Description
S29GL064S, 64-Megabit Page-Mode Flash Memory
Manufactured using 65 nm MirrorBit Process Technology, 3.0 Volt-Only Read, Program, and Erase

Note:
1. V_{IO} is tied internally to V_{CC}.

6.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations. Table 6.1 and Table 6.2 list configurations that are standard units and Automotive Grade / AEC-Q100 qualified units.

Production Part Approval Process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements. AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 6.1 Industrial (-40°C to +85°C)

S29GL064S Valid Combinations					Package Description	
Device Number	**Speed Option**	**Package, Material, and Temperature Range**	**Model Number**	**Packing Type**		
S29GL064S	70	TFI, TFA	03, 04, 06, 07	0,3 (Note 1)	TS048 (Note 2)	TSOP
	80		V6, V7			
	70		01, 02		TS056 (Note 2)	
	80		V1, V2			
	70	BHI, BHA	03, 04		VBK048 (Note 3)	Fine-Pitch BGA
	70	FHI, FHA	01, 02, 03, 04		LAA064 (Note 3)	Fortified BGA
	80		V1, V2			
	70	DHI, FHA	01, 02, 03, 04		LAE064 (Note 3)	
	80		V1, V2			

Notes:

1. *Type 0 is standard. Specify others as required.*
2. *TSOP package marking omits packing type designator from ordering part number.*
3. *BGA package marking omits leading* S29 *and packing type designator from ordering part number.*

Table 6.2 Industrial Plus (-40°C to +105°C)

S29GL064S Valid Combinations					Package Description	
Device Number	**Speed Option**	**Package, Material, and Temperature Range**	**Model Number**	**Packing Type**		
S29GL064S	80	TFV, TFB	03, 04, 06, 07	0,3 (Note 1)	TS048 (Note 2)	TSOP
	90		V6, V7			
	80		01, 02		TS056 (Note 2)	
	90		V1, V2			
	80	BHV, BHB	03, 04		VBK048 (Note 3)	Fine-Pitch BGA
	80	FHV, FHB	01, 02, 03, 04		LAA064 (Note 3)	Fortified BGA
	90		V1, V2			
	80	DHV, DHB	01, 02, 03, 04		LAE064 (Note 3)	
	90		V1, V2			

Notes:

1. *Type 0 is standard. Specify others as required.*
2. *TSOP package marking omits packing type designator from ordering part number.*
3. *BGA package marking omits leading* S29 *and packing type designator from ordering part number.*

7. Other Resources

7.1 Cypress Flash Memory Roadmap

http://www.cypress.com/Flash-Roadmap

7.2 Links to Software

http://www.cypress.com/software-and-drivers-spansion-flash-memory

7.3 Links to Application Notes

http://www.cypress.com/cypressappnotes

8. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 8.1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 8.1 Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	BYTE# (Note 4)	WP#	ACC	Addresses	DQ0–DQ7	DQ8–DQ15	
										BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	L or H	X	X	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Autoselect (HV)	L	L	H	H	L or H	X	H	A_{IN} (Note 3)	D_{OUT}	D_{OUT}	
Write (Program / Erase)	L	H	L	H	L or H	(Note 1)	X	A_{IN}	(Note 2)	(Note 2)	
Accelerated Program	L	H	L	H	L or H	(Note 1)	V_{HH}	A_{IN}	(Note 2)	(Note 2)	
Standby	$V_{IO} \pm 0.3V$	X	X	$V_{IO} \pm 0.3V$	L or H	X	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L or H	X	X	X	High-Z	High-Z	High-Z
	H	X	X								
Reset	X	X	X	L	L or H	X	X	X	High-Z	High-Z	High-Z

Legend:

L = Logic Low = V_{IL}
H = Logic High = V_{IH}
V_{HH} = Voltage for ACC Program Acceleration
V_{ID} = Voltage for Autoselect
X = Don't Care
A_{IN} = Address In
D_{IN} = Data In
D_{OUT} = Data Out

Notes:

1. *If WP# = V_{IL}, the first or last sector remains protected (for uniform sector devices), and the two outer boot sectors are protected (for boot sector devices). If WP# = V_{IH}, the first or last sector, or the two outer boot sectors are protected or unprotected as determined by the method described in Write Protect (WP#). All sectors are unprotected when shipped from the factory (The Secure Silicon Region may be factory protected depending on version ordered.)*
2. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm (see Figure 12.1 on page 54).*
3. *A9 is raised to V_{ID} to enable Autoselect reads.*
4. *V_{IL} = V_{SS} and V_{IH} = V_{IO}.*

8.1 Word / Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic 1, the device is in word configuration, DQ0–DQ15 are active and controlled by CE#, WE# and OE#.

If the BYTE# pin is set at logic 0, the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE#, WE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

The BYTE# pin must be driven set to a logic 0 or 1 state prior to CE# being driven low. The BYTE# pin should not change logic state while CE# is low.

8.2 Requirements for Reading Array Data

All memories require access time to output array data. In a read operation, data is read from one memory location at a time. Addresses are presented to the device in random order, and the propagation delay through the device causes the data on its outputs to arrive with the address on its inputs.

The device defaults to reading array data after device power-up or hardware reset. To read data from the memory array, the system must first assert a valid address on Amax-A0, while driving OE# and CE# to V_{IL}. WE# must remain at V_{IH}. Data will appear on DQ15-DQ0 after address access time (t_{ACC}), which is equal to the delay from stable addresses to valid output data. The OE# signal must be driven to V_{IL}. Data is output on DQ15-DQ0 pins after the access time (t_{OE}) has elapsed from the falling edge of OE#.

See *Reading Array Data* on page 31 for more information. Refer to Table 17.1 on page 86 and Table 17.2 on page 87 for timing specifications and the timing diagram. Refer to Table 15.1 on page 79 and Table 15.2 on page 80 for the active current specification on reading array data.

8.2.1 Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 8 words / 16 bytes. The appropriate page is selected by the higher address bits A(max)–A3. Address bits A2–A0 in word mode (A2–A-1 in byte mode) determine the specific word within a page. This is an asynchronous operation; the microprocessor supplies the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is deasserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Fast page mode accesses are obtained by keeping the *read-page addresses* constant and changing the intra-read *page* addresses.

8.3 Writing Commands / Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. The on page 33 contains details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Tables 8.2 – 8.5 indicate the address space that each sector occupies.

Refer to *DC Characteristics* on page 79 for the active current specification for the write mode. The *AC Characteristics* section contains timing specification tables and timing diagrams for write operations.

8.3.1 Write Buffer

Write Buffer Programming allows the system write to a maximum of 128 words / 256 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms.

8.3.2 Accelerated Program Operation

The device offers program operations through the ACC function. This is one of two functions provided by the WP#/ACC or ACC pin, depending on model number. This function is primarily intended to support manufacturing programming operations at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the Unlock Bypass mode, protected sectors will remain protected. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC or ACC pin, depending on model number, returns the device to normal operation. *Note that the WP#/ACC or ACC pin must be raised to V_{HH} prior to any accelerated operation and should return to V_{IL}/V_{IH} after the completion of the accelerated operation. It should not be at V_{HH} for operations other than accelerated programming, or device damage may result. WP# contains an internal pull-up; when unconnected, WP# is at V_{IH}.*

8.3.3 Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7-DQ0. Standard read cycle timings (t_{ACC}) apply in this mode. Refer to *Autoselect Mode* on page 19 and *Autoselect Command Sequence* on page 32 for more information.

8.4 Automatic ECC

8.4.1 ECC Overview

The Automatic ECC feature works transparently with normal program, erase, and read operations. As the device transfers each page of data from the Write Buffer to the memory array, internal ECC logic programs the ECC code for that page into a portion of the memory array that is not visible to the host system. The device evaluates the page data and the ECC code during each initial page access. If needed, the internal ECC logic will correct a single bit error during the initial access.

Programming more than once to a particular page will disable the ECC function for that page. The ECC function for that page will remain disabled until the next time the host system erases the sector containing that page. The host system may read data stored in that page following multiple programming operations; however, ECC remains disables and the device will not detect or correct an error in that page.

8.4.2 Program and Erase Summary

For performance and reliability reasons, the device performs reading and programming operations on full 32-byte pages in parallel. Internal device logic provides ECC on each page by adding an ECC code when the page is first programmed.

8.4.3 ECC Implementation

Each 32-byte page in the main flash array, as well as each 32-byte OTP region, features an associated ECC code. Internal ECC logic is able to detect and correct any single bit error found in a page or the associated ECC code during a read access. The first Write Buffer program operation applied to a page programs the ECC code for that page. Subsequent programming operations that occur more than once on a particular page will disable the ECC function for that page. This allows bit or word programming; however, multiple programming operations to the same page will disable the ECC function on the page where incremental programming occurs. An erase of the sector containing the page with ECC disabled will re-enable the ECC function for that Page.

The ECC function is automatic and transparent to the user. The transparency of the Automatic ECC function enhances data integrity for typical programming operations that write data once to each page. The ECC function also facilitates software compatibility to previous generations of GL Family products by allowing single word programming and bit-walking where the user programs the same page or word more than once. When a page has Automatic ECC disabled, the ECC function will not detect or correct any errors upon a data read from that page.

8.4.4 Word Programming

A word programming operation programs a single word anywhere in the main memory array. Programming multiple words within the same 32-byte page disables the Automatic ECC function for that page. An erase of the sector containing that page will re-enable Automatic ECC following multiple word programming operation on that page.

8.4.5 Write Buffer Programming

Each Write Buffer program operation allows the user to program a single bit up to 512 bytes. A 32-byte page is the smallest program granularity that features Automatic ECC protection. Programming to the same page more than once will disable the Automatic ECC function for that page. Cypress recommends the use of a Write Buffer programming operation to program multiple pages in an operation and to write each page only once. This keeps the Automatic ECC function enabled on each page. For the very best performance, program in full lines of 512 bytes aligned on 512-byte boundaries.

8.5 Standby Mode

When the system is not reading or writing to the device, it can be placed in to standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{IO} \pm 0.3V$. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{IO} \pm 0.3V$, the device is in the standby mode, but the standby current is greater. The device requires standard access time (t_{ACC}/t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

Refer to the *DC Characteristics* on page 79, for the standby current specification.

8.6 Automatic Sleep Mode

The automatic sleep mode reduces device interface energy consumption to the sleep level (I_{CC6}) following the completion of a random read access time. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. While in sleep mode, output data is latched and always available to the system. Output of the data depends on the level of the OE# signal but, the automatic sleep mode current is independent of the OE# signal level. Standard address access timings (t_{ACC} or t_{PACC}) provide new data when addresses are changed. Refer to the *DC Characteristics* on page 79 for the automatic sleep mode current specification I_{CC6}.

Automatic sleep helps reduce current consumption especially when the host system clock is slowed for power reduction. During slow system clock periods, read and write cycles may extend many times their length versus when the system is operating at high speed. Even though CE# may be Low throughout these extended data transfer cycles, the memory device host interface will go to the Automatic Sleep current at t_{ACC} + 30 ns. The device will remain at the Automatic Sleep current for t_{ASSB}. Then the device will transition to the standby current level. This keeps the memory at the Automatic Sleep or standby power level for most of the long duration data transfer cycles, rather than consuming full read power all the time that the memory device is selected by the host system.

However, the EAC operates independent of the automatic sleep mode of the host interface and will continue to draw current during an active Embedded Algorithm. Only when both the host interface and EAC are in their standby states is the standby level current achieved.

8.7 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, output pins go to High-Z, and all read / write commands are ignored for the duration of the RESET# pulse. Program / Erase operations that were interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3V$ long enough, the device draws CMOS standby current (I_{CC5}).

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the flash memory, enabling the system to read the boot-up firmware from the flash memory.

Refer to the *AC Characteristics* on page 86 for RESET# parameters and to Figure 16.4 on page 85 for the timing diagram.

8.8 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in a high impedance state.

8.9 Memory Map

Table 8.2 S29GL064S (Models 01, 02, V1, V2) Sector Addresses

Sector	A21–A15	Sector Size (kB/ kwords)	8-bit Address Range	16-bit Address Range	Sector	A21–A15	Sector Size (kB/ kwords)	8-bit Address Range	16-bit Address Range
SA0	0000000	64/32	000000h–00FFFFh	000000h–007FFFh	...	...	...	...	...
SA1	0000001	64/32	010000h–01FFFFh	008000h–00FFFFh	SA118	1110110	64/32	760000h–76FFFFh	3B0000h–3B7FFFh
SA2	0000010	64/32	020000h–02FFFFh	010000h–017FFFh	SA119	1110111	64/32	770000h–77FFFFh	3B8000h–3BFFFFh
SA3	0000011	64/32	030000h–03FFFFh	018000h–01FFFFh	SA120	1111000	64/32	780000h–78FFFFh	3C0000h–3C7FFFh
SA4	0000100	64/32	040000h–04FFFFh	020000h–027FFFh	SA121	1111001	64/32	790000h–79FFFFh	3C8000h–3CFFFFh
SA5	0000101	64/32	050000h–05FFFFh	028000h–02FFFFh	SA122	1111010	64/32	7A0000h–7AFFFFh	3D0000h–3D7FFFh
SA6	0000110	64/32	060000h–06FFFFh	030000h–037FFFh	SA123	1111011	64/32	7B0000h–7BFFFFh	3D8000h–3DFFFFh
SA7	0000111	64/32	070000h–07FFFFh	038000h–03FFFFh	SA124	1111100	64/32	7C0000h–7CFFFFh	3E0000h–3E7FFFh
SA8	0001000	64/32	080000h–08FFFFh	040000h–047FFFh	SA125	1111101	64/32	7D0000h–7DFFFFh	3E8000h–3EFFFFh
SA9	0001001	64/32	090000h–09FFFFh	048000h–04FFFFh	SA126	1111110	64/32	7E0000h–7EFFFFh	3F0000h–3F7FFFh
...	...	...	...	...	SA127	1111111	64/32	7F0000h–7FFFFFh	3F8000h–3FFFFFh

Table 8.3 S29GL064S (Model 03) Top Boot Sector Addresses

Sector	A21–A12	Sector Size (kB/ kwords)	8-bit Address Range	16-bit Address Range	Sector	A21–A12	Sector Size (kB/ kwords)	8-bit Address Range	16-bit Address Range
SA0	0000000xxx	64/32	000000h–00FFFFh	000000h–007FFFh	...	...	...	...	...
SA1	0000001xxx	64/32	010000h–01FFFFh	008000h–00FFFFh	SA125	1111101xxx	64/32	7D0000h–7DFFFFh	3E8000h–3EFFFFh
SA2	0000010xxx	64/32	020000h–02FFFFh	010000h–017FFFh	SA126	1111110xxx	64/32	7E0000h–7EFFFFh	3F0000h–3F7FFFh
SA3	0000011xxx	64/32	030000h–03FFFFh	018000h–01FFFFh	SA127	1111111000	8/4	7F0000h–7F1FFFh	3F8000h–3F8FFFh
SA4	0000100xxx	64/32	040000h–04FFFFh	020000h–027FFFh	SA128	1111111001	8/4	7F2000h–7F3FFFh	3F9000h–3F9FFFh
SA5	0000101xxx	64/32	050000h–05FFFFh	028000h–02FFFFh	SA129	1111111010	8/4	7F4000h–7F5FFFh	3FA000h–3FAFFFh
SA6	0000110xxx	64/32	060000h–06FFFFh	030000h–037FFFh	SA130	1111111011	8/4	7F6000h–7F7FFFh	3FB000h–3FBFFFh
SA7	0000111xxx	64/32	070000h–07FFFFh	038000h–03FFFFh	SA131	1111111100	8/4	7F8000h–7F9FFFh	3FC000h–3FCFFFh
SA8	0001000xxx	64/32	080000h–08FFFFh	040000h–047FFFh	SA132	1111111101	8/4	7FA000h–7FBFFFh	3FD000h–3FDFFFh
SA9	0001001xxx	64/32	090000h–09FFFFh	048000h–04FFFFh	SA133	1111111110	8/4	7FC000h–7FDFFFh	3FE000h–3FEFFFh
...	...	...	...	...	SA134	1111111111	8/4	7FE000h–7FFFFFh	3FF000h–3FFFFFh

Table 8.4 S29GL064S (Model 04) Bottom Boot Sector Addresses

Sector	A21–A12	Sector Size (kB/ kwords)	8-bit Address Range	16-bit Address Range
SA0	0000000000	8/4	000000h–001FFFh	000000h–000FFFh
SA1	0000000001	8/4	002000h–003FFFh	001000h–001FFFh
SA2	0000000010	8/4	004000h–005FFFh	002000h–002FFFh
SA3	0000000011	8/4	006000h–007FFFh	003000h–003FFFh
SA4	0000000100	8/4	008000h–009FFFh	004000h–004FFFh
SA5	0000000101	8/4	00A000h–00BFFFh	005000h–005FFFh
SA6	0000000110	8/4	00C000h–00DFFFh	006000h–006FFFh
SA7	0000000111	8/4	00E000h–00FFFFh	007000h–007FFFh
SA8	0000001xxx	64/32	010000h–01FFFFh	008000h–00FFFFh
SA9	0000010xxx	64/32	020000h–02FFFFh	010000h–017FFFh
...	...	...	...	...

Sector	A21–A12	Sector Size (kB/ kwords)	8-bit Address Range	16-bit Address Range
...	...	...	...	...
SA125	1110110xxx	64/32	760000h–76FFFFh	3B0000h–3B7FFFh
SA126	1110111xxx	64/32	770000h–77FFFFh	3B8000h–3BFFFFh
SA127	1111000xxx	64/32	780000h–78FFFFh	3C0000h–3C7FFFh
SA128	1111001xxx	64/32	790000h–79FFFFh	3C8000h–3CFFFFh
SA129	1111010xxx	64/32	7A0000h–7AFFFFh	3D0000h–3D7FFFh
SA130	1111011xxx	64/32	7B0000h–7BFFFFh	3D8000h–3DFFFFh
SA131	1111100xxx	64/32	7C0000h–7CFFFFh	3E0000h–3E7FFFh
SA132	1111101xxx	64/32	7D0000h–7DFFFFh	3E8000h–3EFFFFh
SA133	1111110xxx	64/32	7E0000h–7EFFFFh	3F0000h–3F7FFFh
SA134	1111111xxx	64/32	7F0000h–7FFFFFh	3F8000h–3FFFFFh

Table 8.5 S29GL064S (Models 06, 07, V6, V7) Sector Addresses

Sector	A21–A15	Sector Size (kB/ kwords)	16-bit Address Range
SA0	0000000	64/32	000000–007FFF
SA1	0000001	64/32	008000–00FFFF
SA2	0000010	64/32	010000–017FFF
SA3	0000011	64/32	018000–01FFFF
SA4	0000100	64/32	020000–027FFF
SA5	0000101	64/32	028000–02FFFF
SA6	0000110	64/32	030000–037FFF
SA7	0000111	64/32	038000–03FFFF
SA8	0001000	64/32	040000–047FFF
SA9	0001001	64/32	048000–04FFFF
...	...	...	...

Sector	A21–A15	Sector Size (kB/ kwords)	16-bit Address Range
...	...	...	...
SA118	1110110	64/32	3B0000–3B7FFF
SA119	1110111	64/32	3B8000–3BFFFF
SA120	1111000	64/32	3C0000–3C7FFF
SA121	1111001	64/32	3C8000–3CFFFF
SA122	1111010	64/32	3D0000–3D7FFF
SA123	1111011	64/32	3D8000–3DFFFF
SA124	1111100	64/32	3E0000–3E7FFF
SA125	1111101	64/32	3E8000–3EFFFF
SA126	1111110	64/32	3F0000–3F7FFF
SA127	1111111	64/32	3F8000–3FFFFF

8.10 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins A6, A3, A2, A1, and A0 must be as shown in Table 8.6 on page 20. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table 8.2 - 8.5). Table 8.6 shows the remaining address bits that are don't care. When all necessary bits are set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0. *Note that the A9 pin must not be at V_{ID} for operations other than Autoselect, or device damage may result. Autoselect using V_{ID} is supported at room temperature only. It must be raised to V_{ID} prior to any autoselect operations and should return to V_{IL}/V_{IH} after the completion of the autoselect operation. It should not be at V_{ID} for operations other than autoselect, or device damage may result.*

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table 10.5 on page 43 and Table 10.7 on page 47. This method does not require V_{ID}. Refer to the *Autoselect Command Sequence* on page 32 for more information.

ID-CFI Location 02h displays sector protection status for the sector selected by the sector address (SA) used in the ID-CFI enter command. To read the protection status of more than one sector it is necessary to exit the ID ASO and enter the ID ASO using the new SA. The access time to read location 02h is always t_{ACC} and a read of this location requires CE# to go High before the read and return Low to initiate the read (asynchronous read access). Page mode read between location 02h and other ID locations is not supported. Page mode read between ID locations other than 02h is supported.

In x8 mode, address A-1 is ignored and the lower 8 bits of data will be returned for both address.

Table 8.6 Autoselect Codes, (High Voltage Method)

Description		CE#	OE#	WE#	A_{max} to A15	A14 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15		DQ7 to DQ0		
																Model Number		
														BYTE# = V_{IH}	BYTE# = V_{IL}	01, 02 V1, V2	03, 04	06, 07, V6, V7
Manufacturer ID: Cypress Products		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	00	X	01h	01h	01h
S29GL064S	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh	7Eh	7Eh
	Cycle 2										H	H	L	22	X	0Ch	10h	13h
	Cycle 3										H	H	H	22	X	01h	00h (04, bottom boot) 01h (03, top boot)	01h
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	X	01h (protected), 00h (unprotected)		
Secure Silicon Region Indicator Bit (DQ7), WP# protects highest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	9A (factory locked), 1A (not factory locked)		
Secure Silicon Region Indicator Bit (DQ7), WP# protects lowest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	8A (factory locked), 0A (not factory locked)		

Legend:
L = Logic Low = V_{IL}
H = Logic High = V_{IH}
SA = Sector Address
X = Don't care

8.11 Advanced Sector Protection

The device features several levels of sector protection, which can disable both the program and erase operations in certain sectors.

8.11.1 Persistent Sector Protection

A command sector protection method that replaces the old 12V controlled protection method.

8.11.2 Password Sector Protection

A highly sophisticated protection method that requires a password before changes to certain sectors are permitted.

8.11.3 WP# Hardware Protection

A write protect pin that can prevent program or erase operations in the outermost sectors.

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

8.11.4 Selecting a Sector Protection Mode

All parts default to operate in the Persistent Sector Protection mode. The user must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method is used. If the user decides to continue using the Persistent Sector Protection method, they must set the Persistent Sector Protection Mode Locking Bit. This permanently sets the part to operate only using Persistent Sector Protection. If the user decides to use the password method, they must set the Password Mode Locking Bit. This permanently sets the part to operate only using password sector protection.

It is important to remember that setting either the Persistent Sector Protection Mode Locking Bit or the Password Mode Locking Bit permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit is set. **It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone.** This is so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The device is shipped with all sectors unprotected. Cypress offers the option of programming and protecting sectors at the factory prior to shipping the device through the ExpressFlash™ Service. Contact your sales representative for details.

It is possible to determine whether a sector is protected or unprotected. See *Autoselect Command Sequence* on page 32 for details.

8.12 Lock Register

The Lock Register consists of 3 bits (DQ2, DQ1, and DQ0). These DQ2, DQ1, DQ0 bits of the Lock Register are programmable by the user. Users are not allowed to program both DQ2 and DQ1 bits of the Lock Register to the 00 state. If the user tries to program DQ2 and DQ1 bits of the Lock Register to the 00 state, the device aborts the Lock Register back to the default 11 state. Once either DQ2 and DQ1 bits of the Lock Register are programmed than no further changes are allow on DQ2 and DQ1. The programming time of the Lock Register is same as the typical word programming time (t_{WHWH1}) without utilizing the Write Buffer of the device. During a Lock Register programming sequence execution, the DQ6 Toggle Bit I toggles until the programming of the Lock Register has completed to indicate programming status. All Lock Register bits are readable to allow users to verify Lock Register statuses.

The Customer Secure Silicon Region Protection Bit is DQ0, Persistent Protection Mode Lock Bit is DQ1, and Password Protection Mode Lock Bit is DQ2 are accessible by all users. Each of these bits are non-volatile. DQ15-DQ3 are reserved and must be 1's when the user tries to program the DQ2, DQ1, and DQ0 bits of the Lock Register. The user is not required to program DQ2, DQ1 and DQ0 bits of the Lock Register at the same time. This allows users to lock the Secure Silicon Region and then set the device either permanently into Password Protection Mode or Persistent Protection Mode and then lock the Secure Silicon Region at separate instances and time frames.

- Secure Silicon Region Protection allows the user to lock the Secure Silicon Region area.
- Persistent Protection Mode Lock Bit allows the user to set the device permanently to operate in the Persistent Protection Mode.
- Password Protection Mode Lock Bit allows the user to set the device permanently to operate in the Password Protection Mode.

Table 8.7 Lock Register

Bit	DQ15-6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Name	Don't Care	Reserved	Reserved	Reserved	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	Secure Silicon Region Protection Bit
Default Value	1	1	1	1	1	1	0

8.13 Persistent Sector Protection

The Persistent Sector Protection method replaces the old 12V controlled protection method while at the same time enhancing flexibility by providing three different sector protection states

Dynamically Locked	The sector is protected and can be changed by a simple command.
Persistently Locked	A sector is protected and cannot be changed.
Unlocked	The sector is unprotected and can be changed by a simple command.

To achieve these states, three types of “bits” are used:

8.13.1 Dynamic Protection Bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYB bits are in the “unprotected state”. Each DYB is individually modifiable through the DYB Set Command and DYB Clear Command. The DYB bits and Persistent Protect Bits (PPB) Lock bit are defaulted to power up in the cleared state or unprotected state - meaning the all PPB bits are changeable.

The Protection State for each sector is determined by the logical OR of the PPB and the DYB related to that sector. For the sectors that have the PPB bits cleared, the DYB bits control whether or not the sector is protected or unprotected. By issuing the DYB Set and DYB Clear command sequences, the DYB bits is protected or unprotected, thus placing each sector in the protected or unprotected state. These are the so-called Dynamic Locked or Unlocked states. They are called dynamic states because it is very easy to switch back and forth between the protected and un-protected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed.

The DYB bits maybe set or cleared as often as needed. The PPB bits allow for a more static, and difficult to change, level of protection. The PPB bits retain their state across power cycles because they are Non-Volatile. Individual PPB bits are set with a program command but must all be cleared as a group through an erase command.

The PPB Lock Bit adds an additional level of protection. Once all PPB bits are programmed to the desired settings, the PPB Lock Bit may be set to the ‘freeze state’. Setting the PPB Lock Bit to the freeze state disables all program and erase commands to the Non-Volatile PPB bits. In effect, the PPB Lock Bit locks the PPB bits into their current state. The only way to clear the PPB Lock Bit to the ‘unfreeze state’ is to go through a power cycle, or hardware reset. The Software Reset command does not clear the PPB Lock Bit to the unfreeze state. System boot code can determine if any changes to the PPB bits are needed e.g., to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB Lock Bit to disable any further changes to the PPB bits during system operation.

The WP# write protect pin adds a final level of hardware protection. When this pin is low it is not possible to change the contents of the WP# protected sectors. These sectors generally hold system boot code. So, the WP# pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Set command sequence is all that is necessary. The DYB Set and DYB Clear commands for the dynamic sectors switch the DYB bits to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB Lock Bit must be disabled to the unfreeze state by either putting the device through a power-cycle, or hardware reset. The PPB bits can then be changed to reflect the desired settings. Setting the PPB Lock Bit once again to the freeze state locks the PPB bits, and the device operates normally again.

To achieve the best protection, execute the PPB Lock Bit Set command early in the boot code, and protect the boot code by holding WP# = V_{IL}.

8.13.2 Persistent Protection Bit (PPB)

A single Persistent (non-volatile) Protection Bit is assigned to each sector. If a PPB is programmed to the protected state through the PPB Program command, that sector is protected from program or erase operations and is therefor read-only. If a PPB requires erasure, all of the sector PPB bits must first be erased in parallel through the All PPB Erase command. The All PPB Erase command preprograms all PPB bits prior to PPB erasing. All PPB bits erase in parallel, unlike programming where individual PPB bits are programmable. The PPB bits are limited to the same number of cycles as a flash memory sector.

Programming the PPB bit requires the typical word programming time without utilizing the Write Buffer. During a PPB bit programming and all PPB bit erasing sequence executions, the DQ6 Toggle Bit I toggles until the programming of the PPB bit or erasing of all PPB bits has completed to indicate programming and erasing status. Erasing all of the PPB bits at once requires typical sector erase time. During the erasing of all PPB bits, the DQ3 Sector Erase Timer bit outputs a 1 to indicate the erasure of all PPB bits are in progress. Reading the PPB Status bit requires the initial access time of the device.

8.13.3 Persistent Protection Bit Lock (PPB Lock Bit)

A global volatile bit. When set to the freeze state, the PPB bits cannot be changed. When cleared to the unfreeze state, the PPB bits are changeable. There is only one PPB Lock Bit per device. The PPB Lock Bit is cleared to the unfreeze state at power-up or hardware reset.

Configuring the PPB Lock Bit to the freeze state requires approximately t_{WC}. Reading the PPB Lock Status bit requires the initial access time (t_{ACC}) of the device.

Table 8.8 Sector Protection Schemes

Protection States			Sector State
DYB Bit	PPB Bit	PPB Lock Bit	
Unprotect	Unprotect	Unfreeze	Unprotected – PPB and DYB are changeable
Unprotect	Unprotect	Freeze	Unprotected – PPB not changeable, DYB is changeable
Unprotect	Protect	Unfreeze	Protected – PPB and DYB are changeable
Unprotect	Protect	Freeze	Protected – PPB not changeable, DYB is changeable
Protect	Unprotect	Unfreeze	Protected – PPB and DYB are changeable
Protect	Unprotect	Freeze	Protected – PPB not changeable, DYB is changeable
Protect	Protect	Unfreeze	Protected – PPB and DYB are changeable
Protect	Protect	Freeze	Protected – PPB not changeable, DYB is changeable

Table 8.8 contains all possible combinations of the DYB bit, PPB bit, and PPB Lock Bit relating to the status of the sector. In summary, if the PPB bit is set, and the PPB Lock Bit is set, the sector is protected and the protection cannot be removed until the next power cycle or hardware reset clears the PPB Lock Bit to unfreeze state. If the PPB bit is cleared, the sector can be dynamically locked or unlocked. The DYB bit then controls whether or not the sector is protected or unprotected. If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program or erase command to a protected sector enables status polling for t_{DP} before the device returns to read mode without having modified the contents of the protected sector. The programming of the DYB bit, PPB bit, and PPB Lock Bit for a given sector can be verified by writing a DYB Status Read, PPB Status Read, and PPB Lock Status Read commands to the device.

The Autoselect Sector Protection Verification outputs the OR function of the DYB bit and PPB bit per sector basis. When the OR function of the DYB bit and PPB bit is a 1, the sector is either protected by DYB or PPB or both. When the OR function of the DYB bit and PPB bit is a 0, the sector is unprotected through both the DYB and PPB.

8.14 Password Sector Protection

The Password Sector Protection method allows an even higher level of security than the Persistent Sector Protection method. There are two main differences between the Persistent Sector Protection and the Password Sector Protection methods:

- When the device is first powered on, or comes out of a reset cycle, the PPB Lock Bit is set to the locked state, or the freeze state, rather than cleared to the unlocked state, or the unfreeze state.
- The only means to clear and unfreeze the PPB Lock Bit is by writing a unique 64-bit Password to the device.

The Password Sector Protection method is otherwise identical to the Persistent Sector Protection method.

A 64-bit password is the only additional tool utilized in this method.

The password is stored in a one-time programmable (OTP) region outside of the flash memory. Once the Password Protection Mode Lock Bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear and unfreeze the PPB Lock Bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB Lock Bit is cleared to the unfreezed *state*, and the PPB bits can be altered. If they do not match, the flash device does nothing. There is a built-in t_{PPB} delay for each password check after the valid 64-bit password is entered for the PPB Lock Bit to be cleared to the unfreezed state. This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

8.15 Password and Password Protection Mode Lock Bit

In order to select the Password Sector Protection method, the user must first program the password. Cypress recommends that the password be somehow correlated to the unique Electronic Serial Number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform Password Read operations. Once the desired password is programmed in, the customer must then set the Password Protection Mode Lock Bit. This operation achieves two objectives:

1. It permanently sets the device to operate using the Password Protection Mode. It is not possible to reverse this function.
2. It also disables all further commands to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the Password Sector Protection method is desired when programming the Password Protection Mode Lock Bit. More importantly, the user must be sure that the password is correct when the Password Protection Mode Lock Bit is programmed. Due to the fact that read operations are disabled, there is no means to read what the password is afterwards. If the password is lost after programming the Password Protection Mode Lock Bit, there is no way to clear and unfreeze the PPB Lock Bit. The Password Protection Mode Lock Bit, once programmed, prevents reading the 64-bit password on the DQ bus and further password programming. The Password Protection Mode Lock Bit is not erasable. Once Password Protection Mode Lock Bit is programmed, the Persistent Protection Mode Lock Bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

8.15.1 64-Bit Password

The 64-bit password is located in its own memory space and is accessible through the use of the Password Program and Password Read commands. The password function works in conjunction with the Password Protection Mode Lock Bit, which when programmed, prevents the Password Read command from reading the contents of the password on the pins of the device.

8.16 Persistent Protection Bit Lock (PPB Lock Bit)

A global volatile bit. The PPB Lock Bit is a volatile bit that reflects the state of the Password Protection Mode Lock Bit after power-up reset. If the Password Protection Mode Lock Bit is also programmed after programming the Password, the Password Unlock command must be issued to clear and unfreeze the PPB Lock Bit after a hardware reset (RESET# asserted) or a power-up reset. Successful execution of the Password Unlock command clears and unfreezes the PPB Lock Bit, allowing for sector PPB bits to be modified. Without issuing the Password Unlock command, while asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB Lock Bit to a the freeze state.

If the Password Protection Mode Lock Bit is not programmed, the device defaults to Persistent Protection Mode. In the Persistent Protection Mode, the PPB Lock Bit is cleared to the unfreeze state after power-up or hardware reset. The PPB Lock Bit is set to the freeze state by issuing the PPB Lock Bit Set command. Once set to the freeze state the only means for clearing the PPB Lock Bit to the unfreeze state is by issuing a hardware or power-up reset. The Password Unlock command is ignored in Persistent Protection Mode.

Reading the PPB Lock Bit requires the initial access time (t_{ACC}) of the device.

8.17 Secure Silicon Region Flash Memory

The Secure Silicon Region feature provides a flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secure Silicon Region is 256 bytes in length, and uses a Secure Silicon Region Indicator Bit (DQ7) in Autoselect Mode to indicate whether or not the Secure Silicon Region is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The factory offers the device with the Secure Silicon Region either customer lockable (standard shipping option) or factory locked (contact a sales representative for ordering information). The customer-lockable version is shipped with the Secure Silicon Region unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also has the Secure Silicon Region Indicator Bit permanently set to a 0. The factory-locked version is always protected when shipped from the factory, and has the Secure Silicon Region Indicator Bit permanently set to a 1. Thus, the Secure Silicon Region Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The Secure Silicon Region address space in this device is allocated as follows:

Secure Silicon Region Address Range	Customer Lockable	ESN Factory Locked	ExpressFlash Factory Locked
000000h–000007h	Determined by customer	ESN	ESN or determined by customer
000008h–00007Fh		Unavailable	Determined by customer

The system accesses the Secure Silicon Region through a command sequence (see Table 10.5 and Table 10.7). After the system has written the Enter Secure Silicon Region command sequence, it may read the Secure Silicon Region by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit Secure Silicon Region command sequence, Reset / ASO Exit command, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.