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S29GL01GP
S29GL512P
S29GL256P
S29GL128P

1 Gbit, 512, 256, 128 Mbit, 3 V, Page Flash with 90 nm MirrorBit Process Technology

General Description

The Spansion S29GL01G/512/256/128P are Mirrorbit® Flash products fabricated on 90 nm process technology. These devices offer a fast page access time of 25 ns with a corresponding random access time as fast as 90 ns. They feature a Write Buffer that allows a maximum of 32 words/64 bytes to be programmed in one operation, resulting in faster effective programming time than standard programming algorithms. This makes these devices ideal for today's embedded applications that require higher density, better performance and lower power consumption.

Distinctive Characteristics

- Single 3V read/program/erase (2.7-3.6 V)
- Enhanced VersatileI/O™ control
  - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on V_{IO} input. V_{IO} range is 1.65 to V_{CC}
- 90 nm MirrorBit process technology
- 8-word/16-byte page read buffer
- 32-word/64-byte write buffer reduces overall programming time for multiple-word updates
- Secured Silicon Sector region
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number
  - Can be programmed and locked at the factory or by the customer
- Uniform 64 Kword/128 Kbyte Sector Architecture
  - S29GL01GP: One thousand twenty-four sectors
  - S29GL512P: Five hundred twelve sectors
  - S29GL256P: Two hundred fifty-six sectors
  - S29GL128P: One hundred twenty-eight sectors
- 100,000 erase cycles per sector typical
- 20-year data retention typical
- Offered Packages
  - 56-pin TSOP
  - 64-ball Fortified BGA
- Suspend and Resume commands for Program and Erase operations
- Write operation status bits indicate program and erase operation completion
- Unlock Bypass Program command to reduce programming time
- Support for CFI (Common Flash Interface)
- Persistent and Password methods of Advanced Sector Protection
- WP#/ACC input
  - Accelerates programming time (when V_{HH} is applied) for greater throughput during system production
  - Protects first or last sector regardless of sector protection settings
- Hardware reset input (RESET#) resets device
- Ready/Busy# output (RY/BY#) detects program or erase cycle completion

Performance Characteristics

Maximum Read Access Times (ns)					
Density	**Voltage Range (1)**	**Random Access Time (t_{ACC})**	**Page Access Time (t_{PACC})**	**CE# Access Time (t_{CE})**	**OE# Access Time (t_{OE})**
128 & 256 Mb	Regulated V_{CC}	90	25	90	25
	Full V_{CC}	100/110		100/110	
	VersatileIO V_{IO}	110		110	
512 Mb	Regulated V_{CC}	100	25	100	25
	Full V_{CC}	110		110	
	VersatileIO V_{IO}	120		120	
1 Gb	Regulated V_{CC}	110	25	110	25
	Full V_{CC}	120		120	
	VersatileIO V_{IO}	130		130	

Notes

1. *Access times are dependent on V_{CC} and V_{IO} operating ranges.*
   See Ordering Information page for further details.
   Regulated V_{CC}: *V_{CC} = 3.0–3.6 V.*
   Full V_{CC}: *V_{CC} = V_{IO} = 2.7–3.6 V.*
   VersatileIO V_{IO}: *V_{IO} = 1.65–V_{CC}, V_{CC} = 2.7–3.6 V.*
2. *Contact a sales representative for availability.*

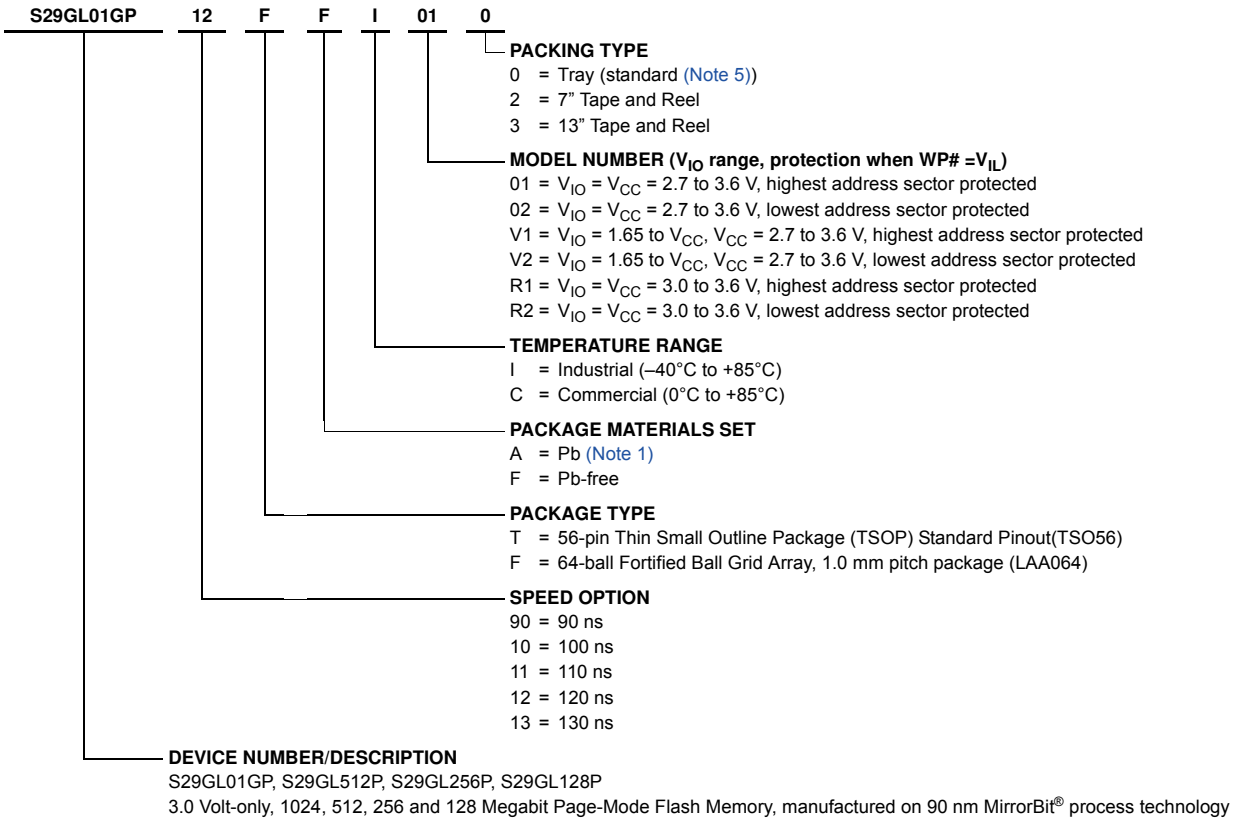
Current Consumption (typical values)	
Random Access Read (*f* = 5 MHz)	30 mA
8-Word Page Read (*f* = 10 MHz)	1 mA
Program/Erase	50 mA
Standby	1 µA

Program & Erase Times (typical values)	
Single Word Programming	60 µs
Effective Write Buffer Programming (V_{CC}) Per Word	15 µs
Effective Write Buffer Programming (V_{HH}) Per Word	13.5 µs
Sector Erase Time (64 Kword Sector)	0.5 s

Contents

1. Ordering Information

The ordering part number is formed by a valid combination of the following:



Recommended Combinations

Recommended Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific recommended combinations and to check on newly released combinations.

S29GL-P Valid Combinations					
Base Part Number	**Speed**	**Package** (2)(3)	**Temperature** (4)	**Model Number**	**Packing Type** (5)
S29GL01GP	11	TA (1), TF	I, C	R1, R2	0, 3
	12		I	01, 02	
	13			V1, V2	
	11	FA (1), FF	I, C	R1, R2	0, 2, 3
	12		I	01, 02	
	13			V1, V2	
S29GL512P	10	TA (1), TF	I, C	R1, R2	0, 3
	11		I	01, 02	
	12			V1, V2	
	10	FA (1), FF	I, C	R1, R2	0, 2, 3
	11		I	01, 02	
	12			V1, V2	
S29GL128P, S29GL256P	90	TA (1), TF	I, C	R1, R2	0, 3
	10, 11		I	01, 02	
	11			V1, V2	
	90	FA (1), FF	I, C	R1, R2	0, 2, 3
	10, 11		I	01, 02	
	11			V1, V2	

Notes

1. *Contact a local sales representative for availability.*
2. *TSOP package marking omits packing type designator from ordering part number.*
3. *BGA package marking omits leading "S29" and packing type designator from ordering part number.*
4. *Operating Temperature range: I = Industrial (–40°C to +85°C)*
   C = Commercial (0°C to +85°C)
5. *Type 0 is standard. Specify other options as required.*

2. Input/Output Descriptions & Logic Symbol

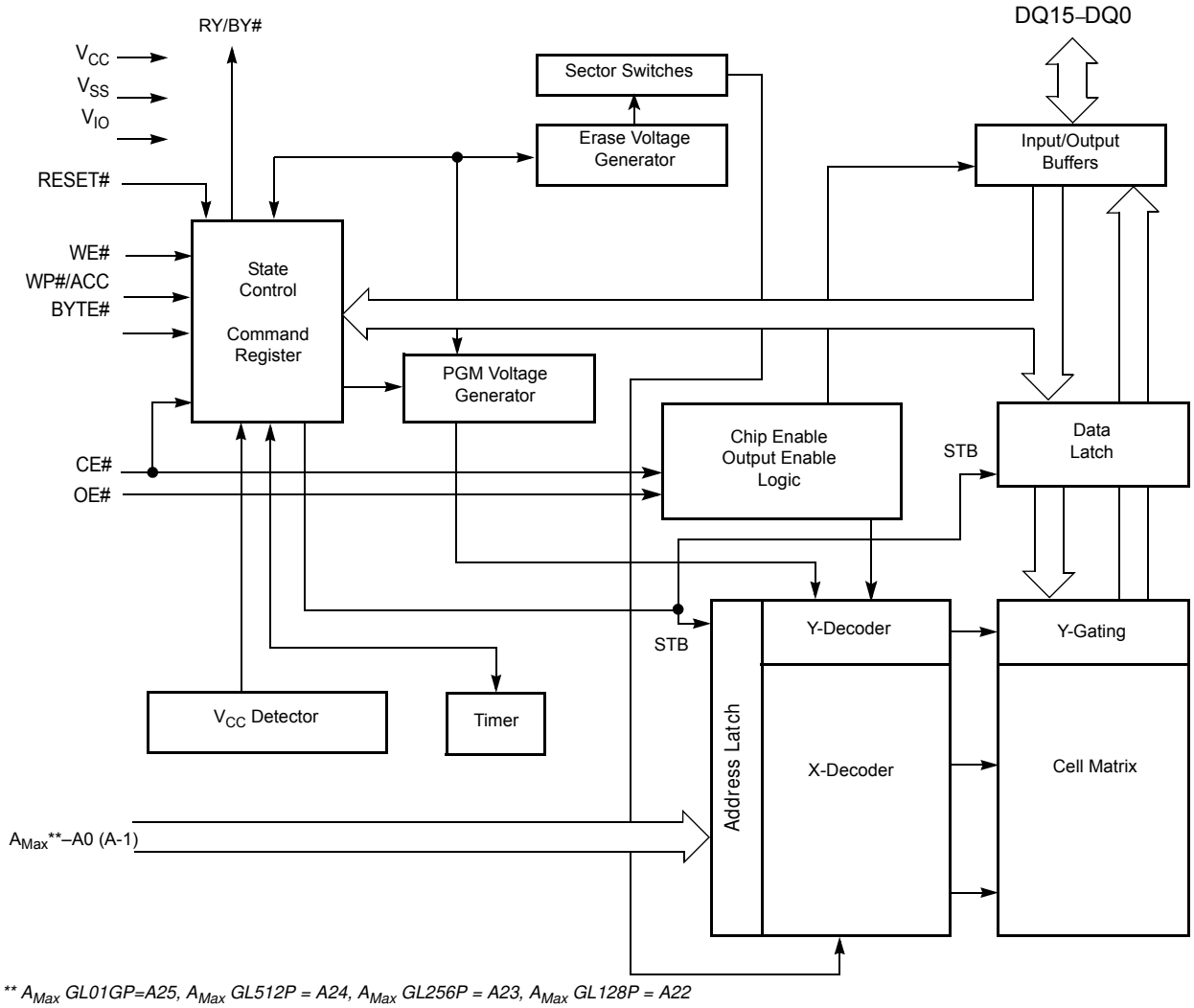
Table identifies the input and output package connections provided on the device.

Input/Output Descriptions

Symbol	Type	Description
A25–A0	Input	Address lines for GL01GP A24–A0 for GL512P A23–A0 for GL256P, A22–A0 for GL128P.
DQ14–DQ0	I/O	Data input/output.
DQ15/A-1	I/O	DQ15: Data input/output in word mode. A-1: LSB address input in byte mode.
CE#	Input	Chip Enable.
OE#	Input	Output Enable.
WE#	Input	Write Enable.
V_{CC}	Supply	Device Power Supply.
V_{IO}	Supply	Versatile IO Input.
V_{SS}	Supply	Ground.
NC	No Connect	Not connected internally.
RY/BY#	Output	Ready/Busy. Indicates whether an Embedded Algorithm is in progress or complete. At V_{IL}, the device is actively erasing or programming. At High Z, the device is in ready.
BYTE#	Input	Selects data bus width. At VIL, the device is in byte configuration and data I/O pins DQ0-DQ7 are active and DQ15/A-1 becomes the LSB address input. At VIH, the device is in word configuration and data I/O pins DQ0-DQ15 are active.
RESET#	Input	Hardware Reset. Low = device resets and returns to reading array data.
WP#/ACC	Input	Write Protect/Acceleration Input. At V_{IL}, disables program and erase functions in the outermost sectors. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. Should be at V_{IH} for all other conditions. WP# has an internal pull-up; when unconnected, WP# is at V_{IH}.

3. Block Diagram

Figure 3.1 S29GL-P Block Diagram



*** A_{Max} GL01GP=A25, A_{Max} GL512P = A24, A_{Max} GL256P = A23, A_{Max} GL128P = A22*

4. Physical Dimensions/Connection Diagrams

This section shows the I/O designations and package specifications for the S29GL-P family.

4.1 Related Documents

The following documents contain information relating to the S29GL-P devices. Click on the title or go to www.spansion.com download the PDF file, or request a copy from your sales office.

- Considerations for X-ray Inspection of Surface-Mounted Flash Integrated Circuits

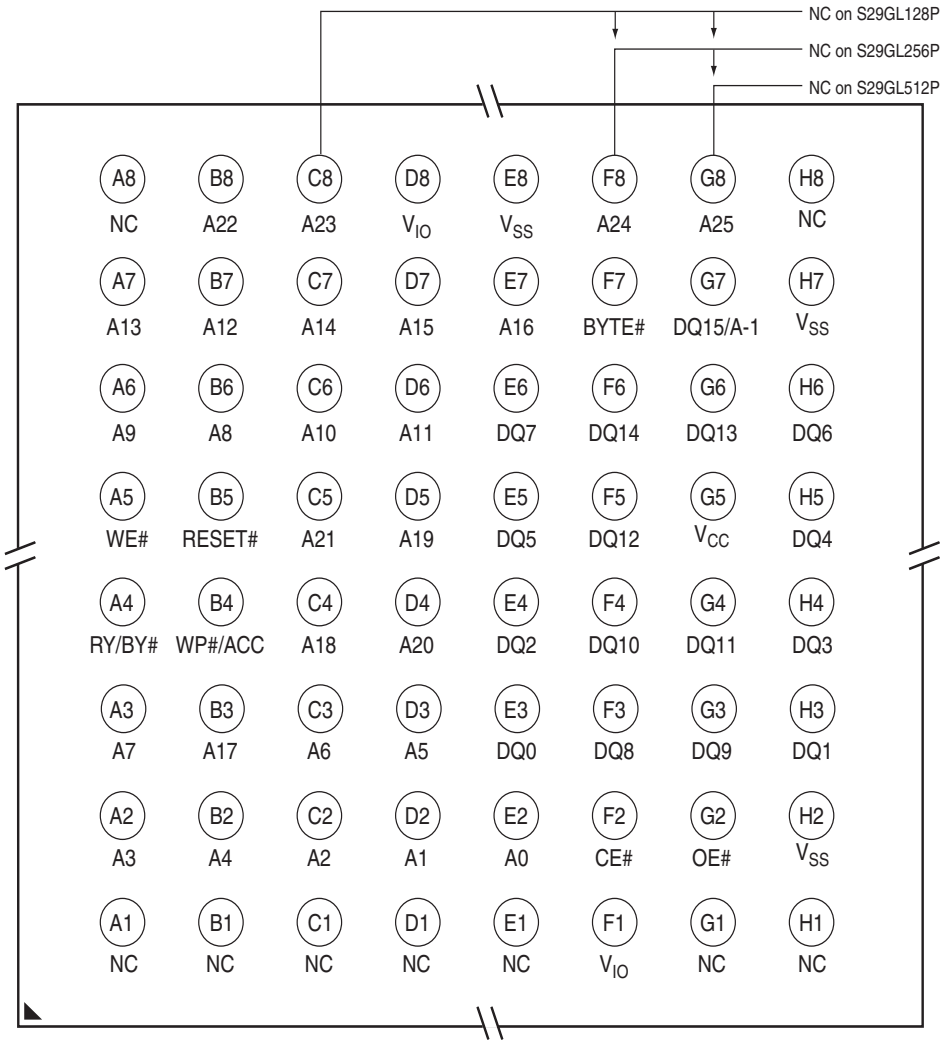
4.2 Special Handling Instructions for BGA Package

Special handling is required for Flash Memory products in BGA packages.

Flash memory devices in BGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

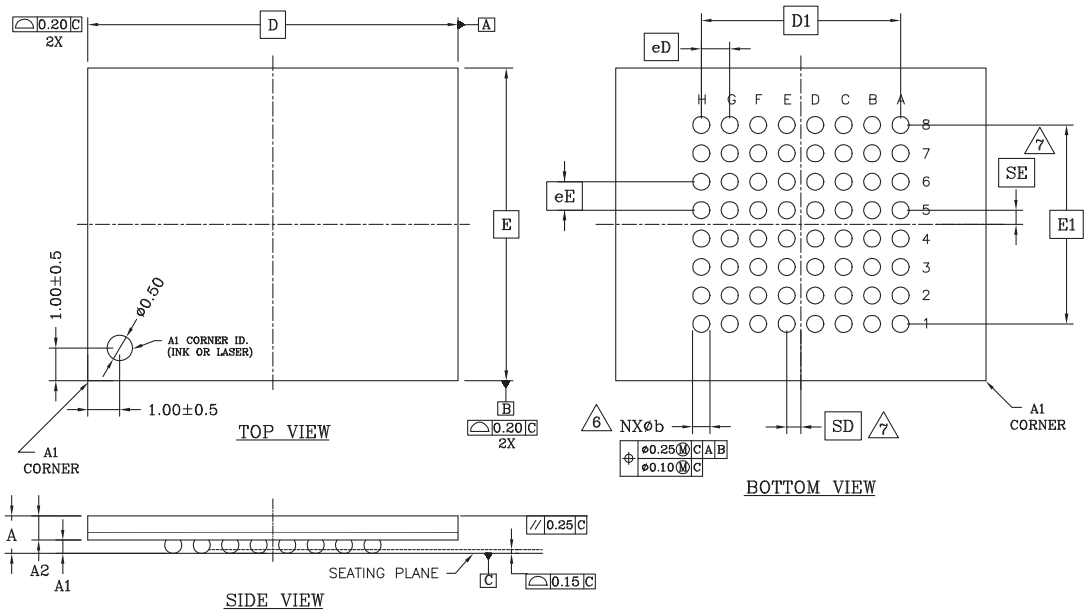
Figure 4.1 64-ball Fortified Ball Grid Array

Top View, Balls Facing Down



4.3 LAA064—64 ball Fortified Ball Grid Array, 11 x 13 mm

Figure 4.2 LAA064—64ball Fortified Ball Grid Array (FBGA), 11 x 13 mm



PACKAGE	LAA 064			
JEDEC	N/A			
	13.00 mm x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE HEIGHT
A1	0.40	---	---	STANDOFF
A2	0.60	---	---	BODY THICKNESS
D		13.00 BSC.		BODY SIZE
E		11.00 BSC.		BODY SIZE
D1		7.00 BSC.		MATRIX FOOTPRINT
E1		7.00 BSC.		MATRIX FOOTPRINT
MD		8		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
N		64		BALL COUNT
ϕb	0.50	0.60	0.70	BALL DIAMETER
eD		1.00 BSC.		BALL PITCH - D DIRECTION
eE		1.00 BSC.		BALL PITCH - E DIRECTION
SD / SE		0.50 BSC.		SOLDER BALL PLACEMENT
		NONE		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

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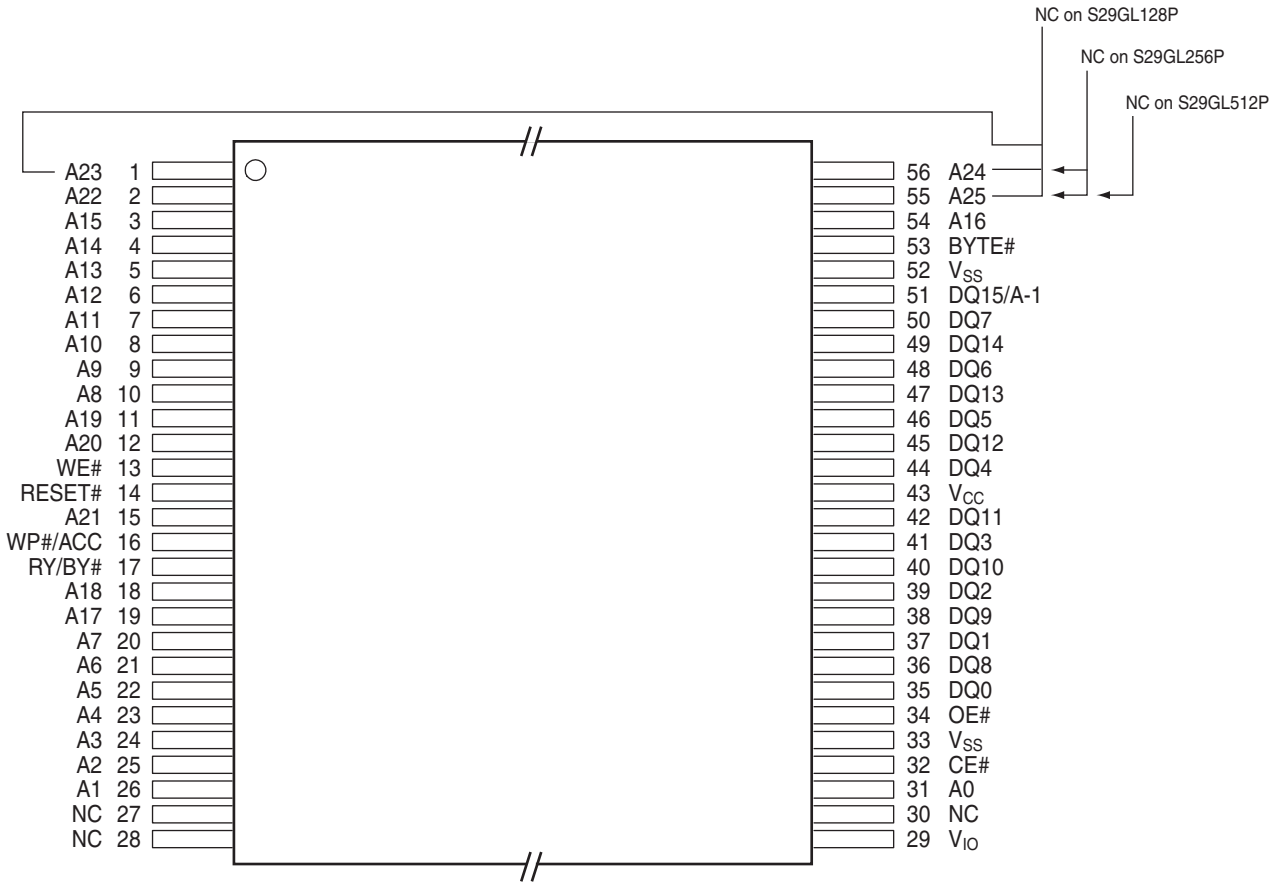
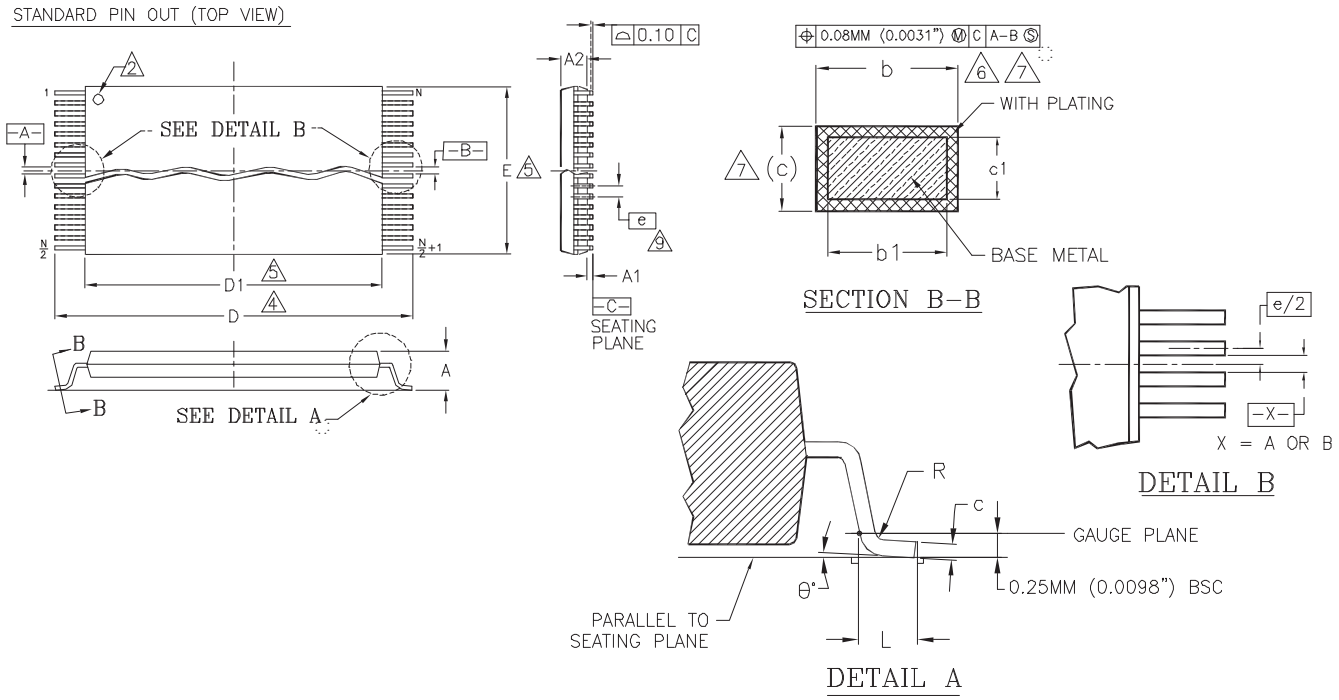
Figure 4.3 56-pin Standard TSOP (Top View)



4.4 TS056—56-Pin Standard Thin Small Outline Package (TSOP)

Figure 4.4 56-Pin Thin Small Outline Package (TSOP), 14 x 20 mm



PACKAGE	TS 56		
JEDEC	MO-142 (B) EC		
SYMBOL	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	---	0.16
c	0.10	---	0.21
D	19.80	20.00	20.20
D1	18.30	18.40	18.50
E	13.90	14.00	14.10
e	0.50 BASIC		
L	0.50	0.60	0.70
Ø	0°	-	8°
R	0.08	---	0.20
N	56		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (mm). (DIMENSIONING AND TOLERANCING CONFORMS TO ANSI Y14.5M-1982.)
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
4. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTUSION IS 0.15 mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTUSION. ALLOWABLE DAMBAR PROTUSION SHALL BE 0.08 mm TOTAL IN EXCESS OF b DIMENSION AT MAX MATERIAL CONDITION. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07 mm.
6. THESE DIMESIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
7. LEAD COPLANARITY SHALL BE WITHIN 0.10 mm AS MEASURED FROM THE SEATING PLANE.
8. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

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5. Additional Resources

Visit www.spansion.com to obtain the following related documents:

5.1 Application Notes

The following is a list of application notes related to this product. All Spansion application notes are available at http://www.spansion.com/Support/TechnicalDocuments/Pages/ApplicationNotes.aspx

- Using the Operation Status Bits in AMD Devices
- Understanding Page Mode Flash Memory Devices
- MirrorBit® Flash Memory Write Buffer Programming and Page Buffer Read
- Common Flash Interface Version 1.4 Vendor Specific Extensions
- MirrorBit® Flash Memory Write Buffer Programming and Page Buffer Read
- Taking Advantage of Page Mode Read on the MCF5407 Coldfire
- Migration to S29GL128N and S29GL256N based on 110nm MirrorBit® Technology
- Optimizing Program/Erase Times
- Practical Guide to Endurance and Data Retention
- Configuring FPGAs using Spansion S29GL-N Flash
- Connecting Spansion™ Flash Memory to a System Address Bus
- Connecting Unused Data Lines of MirrorBit® Flash
- Reset Voltage and Timing Requirements for MirrorBit® Flash
- Versatile IO: DQ and Enhanced

5.2 Specification Bulletins

Contact your local sales office for details.

5.3 Hardware and Software Support

Downloads and related information on Flash device support is available at http://www.spansion.com/Support/Pages/DriversSoftware.aspx

- Spansion low-level drivers
- Enhanced Flash drivers
- Flash file system

Downloads and related information on simulation modeling and CAD modeling support is available at http://www.spansion.com/Support/Pages/SimulationModels.aspx

- VHDL and Verilog
- IBIS
- ORCAD

5.4 Contacting Spansion

Obtain the latest list of company locations and contact information on our web site at http://www.spansion.com/About/Pages/Locations.aspx

6. Product Overview

The S29GL-P family consists of 1 Gb, 512 Mb, 256 Mb and 128 Mb, 3.0-volt-only, page mode Flash devices optimized for today's embedded designs that demand a large storage array and rich functionality. These devices are manufactured using 90 nm MirrorBit technology. These products offer uniform 64 Kword (128 Kbyte) uniform sectors and feature VersatileIO control, allowing control and I/O signals to operate from 1.65 V to V_{CC}. Additional features include:

- Single word programming or a 32-word programming buffer for an increased programming speed
- Program Suspend/Resume and Erase Suspend/Resume
- Advanced Sector Protection methods for protecting sectors as required
- 128 words/256 bytes of Secured Silicon area for storing customer and factory secured information. The Secured Silicon Sector is One Time Programmable.

6.1 Memory Map

The S29GL-P devices consist of uniform 64 Kword (128 Kbyte) sectors organized as shown in Table –Table .

S29GL01GP Sector & Memory Address Map

Uniform Sector Size	Sector Count	Sector Range	Address Range (16-bit)	Notes
64 Kword/ 128 Kbyte	1024	SA00	0000000h - 000FFFFh	Sector Starting Address
		:	:	
		SA1023	3FF0000H - 3FFFFFFh	Sector Ending Address

Note
This table has been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA001-SA1022) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 Kb sectors have the pattern xxx0000h-xxxFFFFh.

S29GL512P Sector & Memory Address Map

Uniform Sector Size	Sector Count	Sector Range	Address Range (16-bit)	Notes
64 Kword/ 128 Kbyte	512	SA00	0000000h - 000FFFFh	Sector Starting Address
		:	:	
		SA511	1FF0000H - 1FFFFFFh	Sector Ending Address

Note
This table has been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA001-SA510) have sector starting and ending addresses that the same pattern as all other sectors of that size. For example, all 128 Kb sectors have the pattern xxx0000h-xxxFFFFh.

S29GL256P Sector & Memory Address Map

Uniform Sector Size	Sector Count	Sector Range	Address Range (16-bit)	Notes
64 Kword/ 128 Kbyte	256	SA00	0000000h - 000FFFFh	Sector Starting Address
		:	:	
		SA255	0FF0000H - 0FFFFFFh	Sector Ending Address

Note
This table has been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA001-SA254) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 Kb sectors have the pattern xxx0000h-xxxFFFFh.

S29GL128P Sector & Memory Address Map

Uniform Sector Size	Sector Count	Sector Range	Address Range (16-bit)	Notes
64 Kword/ 128 Kbyte	128	SA00	0000000h - 000FFFFh	Sector Starting Address
		:	:	
		SA127	07F0000 - 7FFFFF	Sector Ending Address

Note
This table has been condensed to show sector-related information for an entire device on a single page. Sectors and their address ranges that are not explicitly listed (such as SA001-SA510) have sector starting and ending addresses that form the same pattern as all other sectors of that size. For example, all 128 Kb sectors have the pattern xxx0000h-xxxFFFFh.

7. Device Operations

This section describes the read, program, erase, handshaking, and reset features of the Flash devices.

Operations are initiated by writing specific commands or a sequence with specific address and data patterns into the command registers (see Table through Table). The command register itself does not occupy any addressable memory location; rather, it is composed of latches that store the commands, along with the address and data information needed to execute the command. The contents of the register serve as input to the internal state machine and the state machine outputs dictate the function of the device. Writing incorrect address and data values or writing them in an improper sequence may place the device in an unknown state, in which case the system must pull the RESET# pin low or power cycle the device to return the device to the reading array data mode.

7.1 Device Operation Table

The device must be setup appropriately for each operation. Table describes the required state of each control pin for any particular operation.

Device Operations

Operation	CE#	OE#	WE#	RESET#	WP#/ACC	Addresses (Note 1)	DQ0–DQ7	DQ8–DQ15	
								BYTE#= V_{IH}	BYTE#= V_{IL}
Read	L	L	H	H	X	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write (Program/Erase)	L	H	L	H	(Note 2)	A_{IN}	(Note 3)	(Note 3)	
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	(Note 3)	(Note 3)	
Standby	V_{CC} ± 0.3 V	X	X	V_{CC} ± 0.3 V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	X	High-Z	High-Z	High-Z

Legend
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{HH} = 11.5–12.5V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out

Notes
1. *Addresses are AMax:A0 in word mode; A_{Max}:A-1 in byte mode.*
2. *If WP# = V_{IL}, on the outermost sector remains protected. If WP# = V_{IH}, the outermost sector is unprotected. WP# has an internal pull-up; when unconnected, WP# is at V_{IH}. All sectors are unprotected when shipped from the factory (The Secured Silicon Sector can be factory protected depending on version ordered.)*
3. *D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm.*

7.2 Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ0-DQ15 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0-DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8-DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

7.3 VersatileIO™ (V_{IO}) Control

The VersatileIO™ (V_{IO}) control allows the host system to set the voltage levels that the device generates and tolerates on all inputs and outputs (address, control, and DQ signals). V_{IO} range is 1.65 to V_{CC}. See *Ordering Information* on page 4 for V_{IO} options on this device.

For example, a V_{IO} of 1.65-3.6 volts allows for I/O at the 1.8 or 3 volt levels, driving and receiving signals to and from other 1.8 or 3 V devices on the same data bus.

7.4 Read

All memories require access time to output array data. In a read operation, data is read from one memory location at a time. Addresses are presented to the device in random order, and the propagation delay through the device causes the data on its outputs to arrive with the address on its inputs.

The device defaults to reading array data after device power-up or hardware reset. To read data from the memory array, the system must first assert a valid address on Amax-A0, while driving OE# and CE# to V_{IL}. WE# must remain at V_{IH}. All addresses are latched on the falling edge of CE#. Data will appear on DQ15-DQ0 after address access time (t_{ACC}), which is equal to the delay from stable addresses to valid output data. The OE# signal must be driven to V_{IL}. Data is output on DQ15-DQ0 pins after the access time (t_{OE}) has elapsed from the falling edge of OE#, assuming the t_{ACC} access time has been meet.

7.5 Page Read Mode

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 8 words/16 bytes. The appropriate page is selected by the higher address bits A(max)-A3. Address bits A2-A0 in word mode (A2 to A-1 in byte mode) determine the specific word within a page. The microprocessor supplies the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is de-asserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Fast page mode accesses are obtained by keeping the "read-page addresses" constant and changing the "intra-read page" addresses.

7.6 Autoselect

The Autoselect mode provides manufacturer ID, Device identification, and sector protection information, through identifier codes output from the internal register (separate from the memory array) on DQ7-DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm (see Table). The Autoselect codes can also be accessed in-system.

There are two methods to access autoselect codes. One uses the autoselect command, the other applies V_{ID} on address pin A9.

When using programming equipment, the autoselect mode requires V_{ID} (11.5 V to 12.5 V) on address pin A9. Address pins must be as shown in Table .

- To access Autoselect mode without using high voltage on A9, the host system must issue the Autoselect command.
- The Autoselect command sequence may be written to an address within a sector that is either in the read or erase-suspend-read mode.
- The Autoselect command may not be written while the device is actively programming or erasing.
- The system must write the reset command to return to the read mode (or erase-suspend-read mode if the sector was previously in Erase Suspend).
- It is recommended that A9 apply V_{ID} after power-up sequence is completed. In addition, it is recommended that A9 apply from V_{ID} to V_{IH}/V_{IL} before power-down the V_{CC}/V_{IO}.
- See Table on page 64 for command sequence details.
- When verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table to Table). The remaining address bits are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15-DQ0. The Autoselect codes can also be accessed in-system through the command register.

Autoselect Codes, (High Voltage Method)

Description		CE#	OE#	WE#	Amax to A16	A14 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15		DQ7 to DQ0
														BYTE# = V_{IH}	BYTE# = V_{IL}	
Manufacturer ID: Spansion Product		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	00	X	01h
Device ID S29GL01GP	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh
	Cycle 2										H	H	L	22	X	28h
	Cycle 3										H	H	H	22	X	01h
Device ID S29GL512P	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh
	Cycle 2										H	H	L	22	X	23h
	Cycle 3										H	H	H	22	X	01h
Device ID S29GL256P	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh
	Cycle 2										H	H	L	22	X	22h
	Cycle 3										H	H	H	22	X	01h
Device ID S29GL128P	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh
	Cycle 2										H	H	L	22	X	21h
	Cycle 3										H	H	H	22	X	01h
Sector Group Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	X	01h (protected), 00h (unprotected)
Secured Silicon Sector Indicator Bit (DQ7), WP# protects highest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	99h (factory locked), 19h (not factory locked)
Secured Silicon Sector Indicator Bit (DQ7), WP# protects lowest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	89h (factory locked), 09h (not factory locked)

Legend

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care. V_{ID} = 11.5V to 12.5V

Autoselect Addresses in System

Description	Address	Read Data (word/byte mode)
Manufacturer ID	Base + 00h	xx01h/1h
Device ID, Word 1	Base + 01h	227Eh/7Eh
Device ID, Word 2	Base + 0Eh	2228h/28h (GL01GP) 2223h/23h (GL512P) 2222h/22h (GL256P) 2221h/21h (GL128P)
Device ID, Word 3	Base + 0Fh	2201h/01h
Secure Device Verify	Base + 03h	For S29GLxxxPH: XX19h/19h = Not Factory Locked. XX99h/99h = Factory Locked. For S29GLxxxPL: XX09h/09h = Not Factory Locked. XX89h/89h = Factory Locked.
Sector Protect Verify	(SA) + 02h	xx01h/01h = Locked, xx00h/00h = Unlocked

Software Functions and Sample Code

Autoselect Entry in System

(LLD Function = lld_AutoselectEntryCmd)

Cycle	Operation	Byte Address	Word Address	Data
Unlock Cycle 1	Write	Base + AAAh	Base + 555h	0x00AAh
Unlock Cycle 2	Write	Base + 555h	Base + 2AAh	0x0055h
Autoselect Command	Write	Base + AAAh	Base + 555h	0x0090h

Autoselect Exit

(LLD Function = lld_AutoselectExitCmd)

Cycle	Operation	Byte Address	Word Address	Data
Autoselect Exit Command	Write	base + XXXh	base + XXXh	0x00F0h

Note

1. *Any offset within the device works.*
2. *base = base address.*

The following is a C source code example of using the autoselect function to read the manufacturer ID. Refer to the *Spansion Low Level Driver User's Guide* (available on www.spansion.com) for general information on Spansion Flash memory software development guidelines.

```
/* Here is an example of Autoselect mode (getting manufacturer ID) */
/* Define UINT16 example: typedef unsigned short UINT16; */

UINT16 manuf_id;

/* Auto Select Entry */

*( (UINT16 *)base_addr + 0x555 ) = 0x00AA; /* write unlock cycle 1 */
*( (UINT16 *)base_addr + 0x2AA ) = 0x0055; /* write unlock cycle 2 */
*( (UINT16 *)base_addr + 0x555 ) = 0x0090; /* write autoselect command */


/* multiple reads can be performed after entry */

manuf_id = *( (UINT16 *)base_addr + 0x000 ); /* read manuf. id */

/*  Autoselect exit */

*( (UINT16 *)base_addr + 0x000 ) = 0x00F0; /* exit autoselect (write reset command) */
```

7.7 Program/Erase Operations

These devices are capable of several modes of programming and or erase operations which are described in detail in the following sections.

During a write operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when providing address, command, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE#.

The Unlock Bypass feature allows the host system to send program commands to the Flash device without first writing unlock cycles within the command sequence. See Section 7.7.8 for details on the Unlock Bypass function.

Note the following:

- When the Embedded Program algorithm is complete, the device returns to the read mode.
- The system can determine the status of the program operation by reading the DQ status bits. Refer to the *Write Operation Status* on page 31 for information on these status bits.
- An “0” cannot be programmed back to a “1.” A succeeding read shows that the data is still “0.”
- Only erase operations can convert a “0” to a “1.”
- Any commands written to the device during the Embedded Program/Erase are ignored except the Suspend commands.
- Secured Silicon Sector, Autoselect, and CFI functions are unavailable when a program operation is in progress.
- A hardware reset and/or power removal immediately terminates the Program/Erase operation and the Program/Erase command sequence should be reinitiated once the device has returned to the read mode to ensure data integrity.
- Programming is allowed in any sequence and across sector boundaries for single word programming operation. See *Write Buffer Programming* on page 21 when using the write buffer.
- Programming to the same word address multiple times without intervening erases is permitted.

7.7.1 Single Word Programming

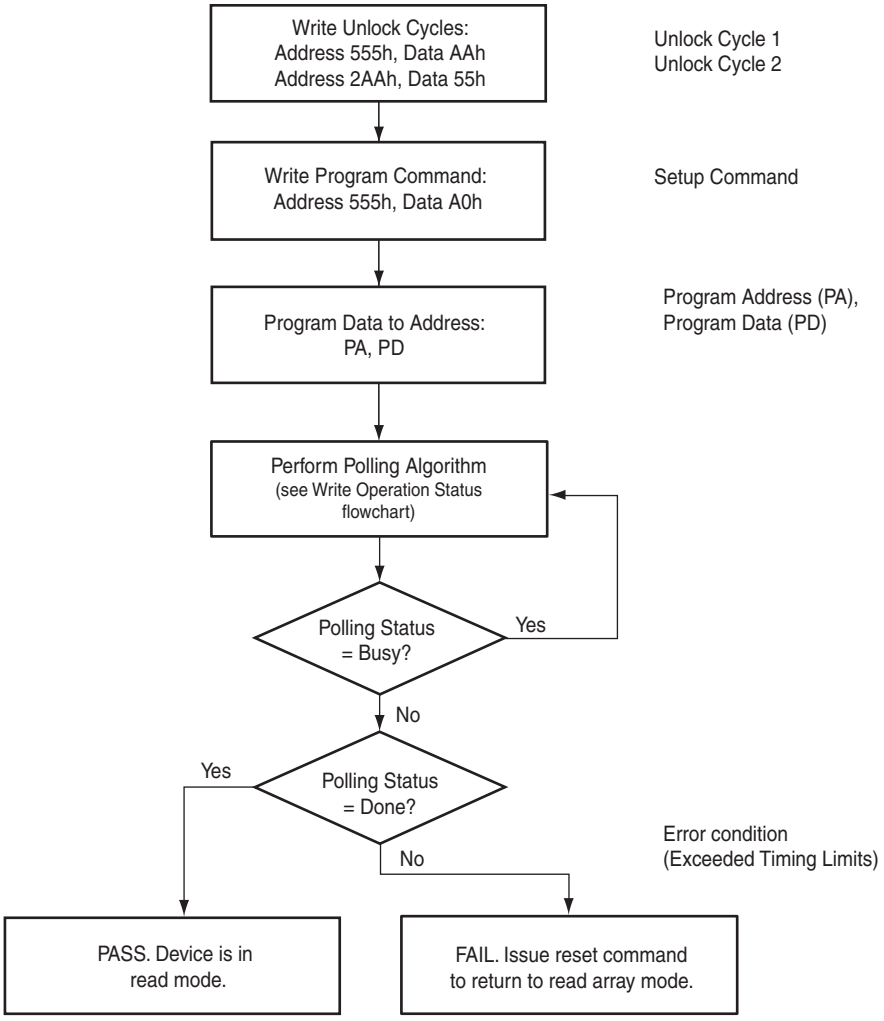
Single word programming mode is one method of programming the Flash. In this mode, four Flash command write cycles are used to program an individual Flash address. The data for this programming operation could be 8 or 16-bits wide.

While the single word programming method is supported by most Spansion devices, in general Single Word Programming is not recommended for devices that support Write Buffer Programming. See Table on page 64 for the required bus cycles and Figure 7.1 for the flowchart.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by reading the DQ status bits. Refer to *Write Operation Status* on page 31 for information on these status bits.

- During programming, any command (except the Suspend Program command) is ignored.
- The Secured Silicon Sector, Autoselect, and CFI functions are unavailable when a program operation is in progress.
- A hardware reset immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.
- Programming to the same address multiple times continuously (for example, “walking” a bit within a word) is permitted.

Figure 7.1 Single Word Program



Software Functions and Sample Code

Single Word/Byte Program

(LLD Function = lld_ProgramCmd)

Cycle	Operation	Byte Address	Word Address	Data
Unlock Cycle 1	Write	Base + AAAh	Base + 555h	00AAh
Unlock Cycle 2	Write	Base + 555h	Base + 2AAh	0055h
Program Setup	Write	Base + AAAh	Base + 555h	00A0h
Program	Write	Byte Address	Word Address	Data

Note
Base = Base Address.

The following is a C source code example of using the single word program function. Refer to the *Spansion Low Level Driver User's Guide* (available on www.spansion.com) for general information on Spansion Flash memory software development guidelines.

```
/* Example: Program Command    */
  *( (UINT16 *)base_addr + 0x555 ) = 0x00AA;   /* write unlock cycle 1            */
  *( (UINT16 *)base_addr + 0x2AA ) = 0x0055;   /* write unlock cycle 2            */
  *( (UINT16 *)base_addr + 0x555 ) = 0x00A0;   /* write program setup command     */
  *( (UINT16 *)pa )                = data;     /* write data to be programmed     */
/* Poll for program completion */
```

7.7.2 Write Buffer Programming

Write Buffer Programming allows the system to write a maximum of 32 words in one programming operation. This results in a faster effective word programming time than the standard "word" programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming occurs. At this point, the system writes the number of "word locations minus 1" that are loaded into the page buffer at the Sector Address in which programming occurs. This tells the device how many write buffer addresses are loaded with data and therefore when to expect the "Program Buffer to Flash" confirm command. The number of locations to program cannot exceed the size of the write buffer or the operation aborts. (Number loaded = the number of locations to program minus 1. For example, if the system programs 6 address locations, then 05h should be written to the device.)

The system then writes the starting address/data combination. This starting address is the first address/data pair to be programmed, and selects the "write-buffer-page" address. All subsequent address/data pairs must fall within the elected write-buffer-page.

The "write-buffer-page" is selected by using the addresses A_{MAX}–A5.

The "write-buffer-page" addresses must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple "write-buffer-pages." This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected "write-buffer-page", the operation ABORTs.)

After writing the Starting Address/Data pair, the system then writes the remaining address/data pairs into the write buffer.

Note that if a Write Buffer address location is loaded multiple times, the "address/data pair" counter is decremented for every data load operation. Also, the last data loaded at a location before the "Program Buffer to Flash" confirm command is the data programmed into the device. It is the software's responsibility to comprehend ramifications of loading a write-buffer location more than once. The counter decrements for each data load operation, NOT for each unique write-buffer-address location. Once the specified number of write buffer locations have been loaded, the system must then write the "Program Buffer to Flash" command at the Sector Address. Any other address/data write combinations abort the Write Buffer Programming operation. The Write Operation Status bits should be used while monitoring the last address location loaded into the write buffer. This eliminates the need to store an address in memory because the system can load the last address location, issue the program confirm command at the last loaded address location, and then check the write operation status at that same address. DQ7, DQ6, DQ5, DQ2, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer "embedded" programming operation can be suspended using the standard suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device returns to READ mode.

The Write Buffer Programming Sequence is ABORTED under any of the following conditions:

- Load a value that is greater than the page buffer size during the “Number of Locations to Program” step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the “Starting Address” during the “write buffer data loading” stage of the operation.
- Writing anything other than the *Program to Buffer Flash* Command after the specified number of “data load” cycles.

The ABORT condition is indicated by DQ1 = 1, DQ7 = DATA# (for the “last address location loaded”), DQ6 = TOGGLE, DQ5 = 0. This indicates that the Write Buffer Programming Operation was ABORTED. A “Write-to-Buffer-Abort reset” command sequence is required when using the write buffer Programming features in Unlock Bypass mode. Note that the Secured Silicon sector, autoselect, and CFI functions are unavailable when a program operation is in progress.

Write buffer programming is allowed in any sequence of memory (or address) locations. These flash devices are capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases.

Use of the write buffer is strongly recommended for programming when multiple words are to be programmed.

Software Functions and Sample Code

Write Buffer Program

(LLD Functions Used = lld_WriteToBufferCmd, lld_ProgramBufferToFlashCmd)

Cycle	Description	Operation	Byte Address	Word Address	Data
1	Unlock	Write	Base + AAAh	Base + 555h	00AAh
2	Unlock	Write	Base + 555h	Base + 2AAh	0055h
3	Write Buffer Load Command	Write	Sector Address		0025h
4	Write Word Count	Write	Sector Address		Word Count (N–1)h
Number of words (N) loaded into the write buffer can be from 1 to 32 words (1 to 64 bytes).					
5 to 36	Load Buffer Word N	Write	Program Address, Word N		Word N
Last	Write Buffer to Flash	Write	Sector Address		0029h

Notes

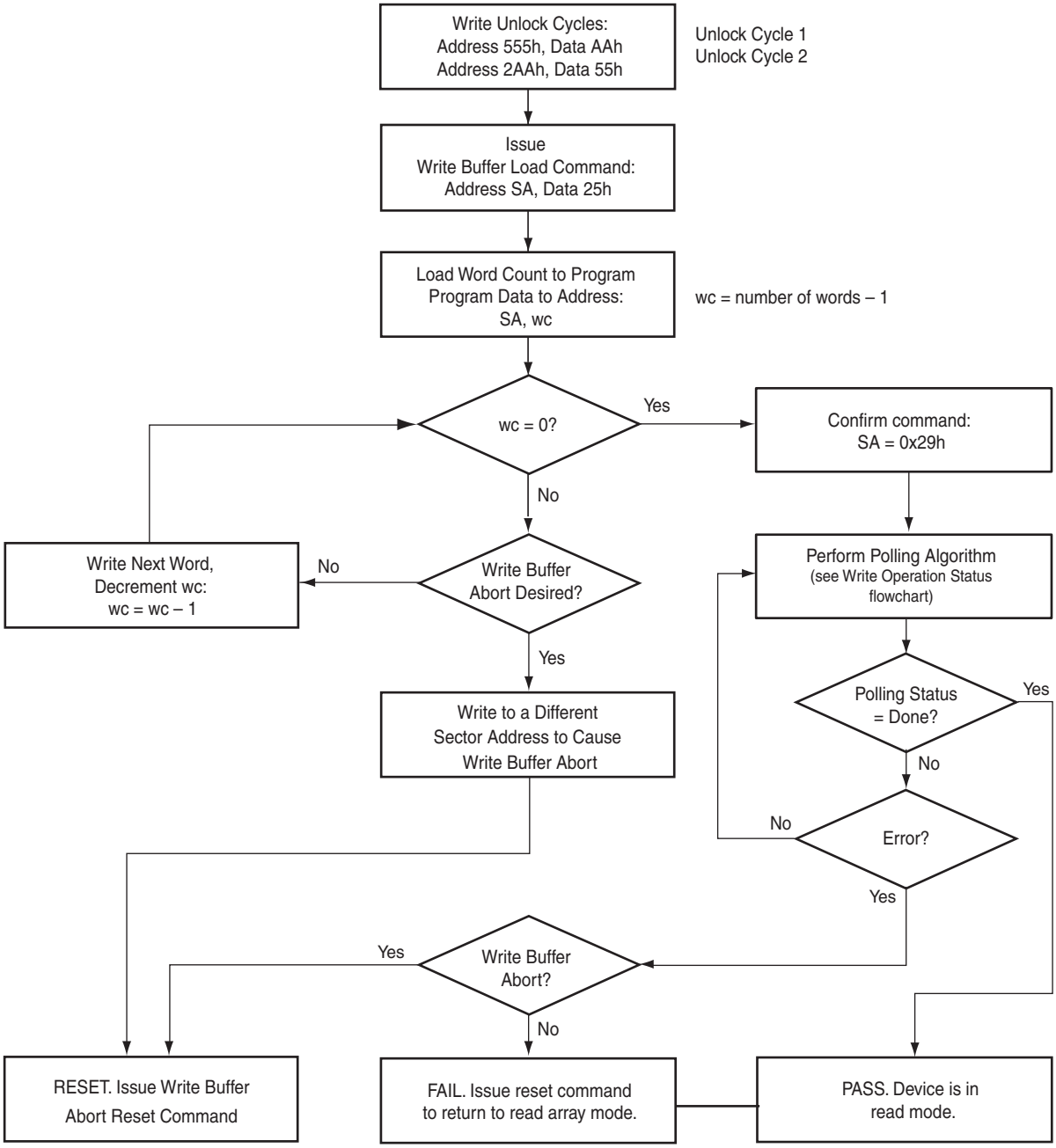
1. *Base = Base Address.*
2. *Last = Last cycle of write buffer program operation; depending on number of words written, the total number of cycles may be from 6 to 37.*
3. *For maximum efficiency, it is recommended that the write buffer be loaded with the highest number of words (N words) possible.*

The following is a C source code example of using the write buffer program function. Refer to the *Spansion Low Level Driver User's Guide* (available on www.spansion.com) for general information on Spansion Flash memory software development guidelines.

```
/* Example: Write Buffer Programming Command            */
/* NOTES: Write buffer programming limited to 16 words. */
/*        All addresses to be written to the flash in   */
/*        one operation must be within the same flash   */
/*        page. A flash page begins at addresses       */
/*        evenly divisible by 0x20.                     */
  UINT16 *src = source_of_data;               /* address of source data          */
  UINT16 *dst = destination_of_data;          /* flash destination address       */
  UINT16 wc   = words_to_program -1;          /* word count (minus 1)            */
  *( (UINT16 *)base_addr + 0x555 ) = 0x00AA;  /* write unlock cycle 1            */
  *( (UINT16 *)base_addr + 0x2AA ) = 0x0055;  /* write unlock cycle 2            */
  *( (UINT16 *)sector_address )    = 0x0025;  /* write write buffer load command */
  *( (UINT16 *)sector_address )    = wc;      /* write word count (minus 1)      */
for (i=0;i<=wc;i++)
{
*dst++ = *src++; /* ALL dst MUST BE in same Write Buffer */
}
*( (UINT16 *)sector_address )    = 0x0029;  /* write confirm command           */
  /* poll for completion */


/* Example: Write Buffer Abort Reset */
  *( (UINT16 *)addr + 0x555 ) = 0x00AA;   /* write unlock cycle 1            */
  *( (UINT16 *)addr + 0x2AA ) = 0x0055;   /* write unlock cycle 2            */
  *( (UINT16 *)addr + 0x555 ) = 0x00F0;   /* write buffer abort reset        */
```

Figure 7.2 Write Buffer Programming Operation



7.7.3 Sector Erase

The sector erase function erases one or more sectors in the memory array. (See Table on page 64 and Figure 7.3.) The device does not require the system to preprogram a sector prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory to an all zero data pattern prior to electrical erase. After a successful sector erase, all locations within the erased sector contain FFFFh. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, the sector erase time-out t_{SEA} (50 µs) occurs. During the time-out period, additional sector addresses may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs. Any sector erase address and command following the exceeded time-out (50 µs) may or may not be accepted. Any command other than Sector Erase or Erase Suspend during the time-out period resets that sector to the read mode. The system can monitor DQ3 to determine if the sector erase timer has timed out (See Section 7.8.6.) The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the sector returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7 or DQ6/DQ2 in the erasing sector. Refer to Section 7.8 for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that sector has returned to reading array data, to ensure the sector is properly erased.

The Unlock Bypass feature allows the host system to send program commands to the Flash device without first writing unlock cycles within the command sequence. See Section 7.7.8 for details on the Unlock Bypass function.

Figure 7.3 illustrates the algorithm for the erase operation. Refer to Section 11.7.5 for parameters and timing diagrams.

Software Functions and Sample Code

Sector Erase

(LLD Function = lld_SectorEraseCmd)

Cycle	Description	Operation	Byte Address	Word Address	Data
1	Unlock	Write	Base + AAAh	Base + 555h	00AAh
2	Unlock	Write	Base + 555h	Base + 2AAh	0055h
3	Setup Command	Write	Base + AAAh	Base + 555h	0080h
4	Unlock	Write	Base + AAAh	Base + 555h	00AAh
5	Unlock	Write	Base + 555h	Base + 2AAh	0055h
6	Sector Erase Command	Write	Sector Address	Sector Address	0030h
Unlimited additional sectors may be selected for erase; command(s) must be written within 50 µs.					

The following is a C source code example of using the sector erase function. Refer to the *Spansion Low Level Driver User's Guide* (available on www.spansion.com) for general information on Spansion Flash memory software development guidelines.

```
/* Example: Sector Erase Command */
  *( (UINT16 *)base_addr + 0x555 ) = 0x00AA;   /* write unlock cycle 1           */
  *( (UINT16 *)base_addr + 0x2AA ) = 0x0055;   /* write unlock cycle 2           */
  *( (UINT16 *)base_addr + 0x555 ) = 0x0080;   /* write setup command            */
  *( (UINT16 *)base_addr + 0x555 ) = 0x00AA;   /* write additional unlock cycle 1 */
  *( (UINT16 *)base_addr + 0x2AA ) = 0x0055;   /* write additional unlock cycle 2 */
  *( (UINT16 *)sector_address )    = 0x0030;   /* write sector erase command     */
```