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S29JL032J

32 Mbit (4M x 8-Bit/2M x 16-Bit), 3 V Simultaneous Read/Write Flash

Distinctive Characteristics

Architectural Advantages

- Simultaneous Read/Write operations
  - Data can be continuously read from one bank while executing erase/program functions in another bank.
  - Zero latency between read and write operations
- Multiple bank architecture
  - Four bank architectures available (refer to Table on page 12).
- Boot sectors
  - Top or bottom boot sector configurations available
  - Any combination of sectors can be erased
- Manufactured on 0.11 µm Process Technology
- Secured Silicon Region: **Extra 256 byte sector**
  - Factory locked and identifiable: 16 bytes available for secure, random factory Electronic Serial Number; verifiable as factory locked through autoselect function
  - *Customer lockable:* One-time programmable only. Once locked, data cannot be changed
- Zero power operation
  - Sophisticated power management circuits reduce power consumed during inactive periods to nearly zero.
- Compatible with JEDEC standards
  - Pinout and software compatible with single-power-supply flash standard

Package Options

- 48-ball Fine-pitch BGA
- 48-pin TSOP

Performance Characteristics

- High performance
  - Access time as fast as 60 ns
  - Program time: 6 µs/word typical using accelerated programming function
- Ultra low power consumption (typical values)
  - 2 mA active read current at 1 MHz
  - 10 mA active read current at 5 MHz
  - 200 nA in standby or automatic sleep mode
- Cycling endurance: 1 million cycles per sector typical
- Data retention: 20 years typical

Software Features

- Supports Common Flash Memory Interface (CFI)
- Erase suspend/Erase resume
  - Suspends erase operations to read data from, or program data to, a sector that is not being erased, then resumes the erase operation.
- Data# polling and toggle bits
  - Provides a software method of detecting the status of program or erase operations
- Unlock bypass program command
  - Reduces overall programming time when issuing multiple program command sequences

Hardware Features

- Ready/Busy# output (RY/BY#)
  - Hardware method for detecting program or erase cycle completion
- Hardware reset pin (RESET#)
  - Hardware method of resetting the internal state machine to the read mode
- WP#/ACC input pin
  - Write protect (WP#) function protects the two outermost boot sectors regardless of sector protect status
  - Acceleration (ACC) function accelerates program timing
- Sector protection
  - Hardware method to prevent any program or erase operation within a sector
  - Temporary Sector Unprotect allows changing data in protected sectors in-system

General Description

The S29JL032J is a 32 Mbit, 3.0 volt-only flash memory device, organized as 2,097,152 words of 16 bits each or 4,194,304 bytes of 8 bits each. Word mode data appears on DQ15–DQ0; byte mode data appears on DQ7–DQ0. The device is designed to be programmed in-system with the standard 3.0 volt V_{CC} supply, and can also be programmed in standard EPROM programmers. The device is available with an access time of 60, or 70 ns and is offered in a 48-ball FBGA or a 48-pin TSOP package. Standard control pins—chip enable (CE#), write enable (WE#), and output enable (OE#)—control normal read and write operations, and avoid bus contention issues. The device requires only a single 3.0 volt power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

Contents

1. Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into separate banks (see Table on page 12). Sector addresses are fixed, system software can be used to form user-defined bank groups.

During an Erase/Program operation, any of the non-busy banks may be read from. *Note that only two banks can operate simultaneously.* The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The S29JL032J can be organized with either a top or bottom boot sector configuration.

1.1 S29JL032J Features

The **Secured Silicon Region** is an extra 256 byte sector capable of being permanently locked by the customer. The Secured Silicon Customer Indicator Bit (DQ6) is permanently set to 1 if the part has been locked and is 0 if lockable.

Customers may utilize the Secured Silicon Region as bonus space, reading and writing like any other flash sector, or may permanently lock their own code there.

The device offers complete compatibility with the **JEDEC 42.4 single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by using the device **status bits:** RY/BY# pin, DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to the read mode.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the Secured Silicon Region area (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

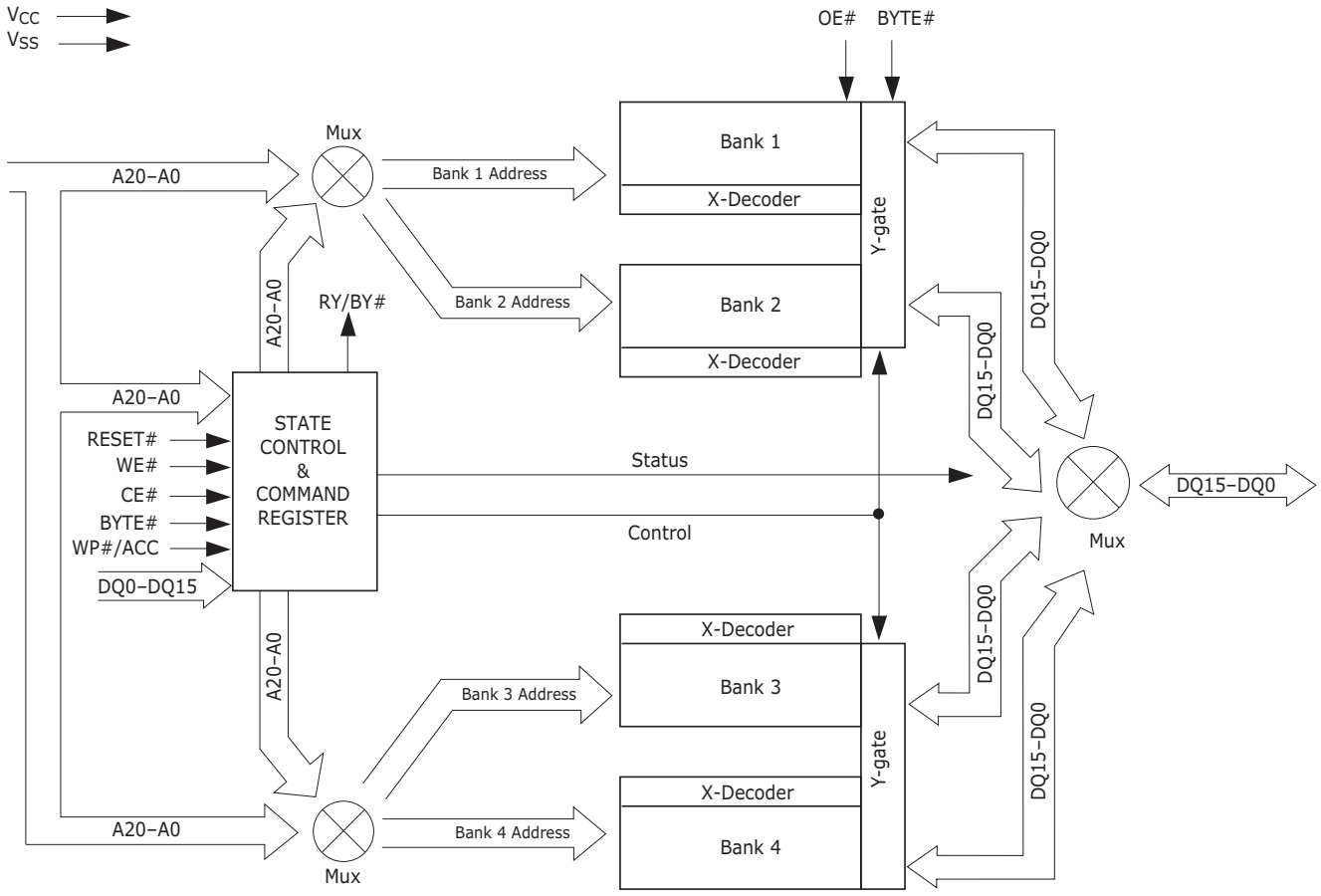
The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

2. Product Selector Guide

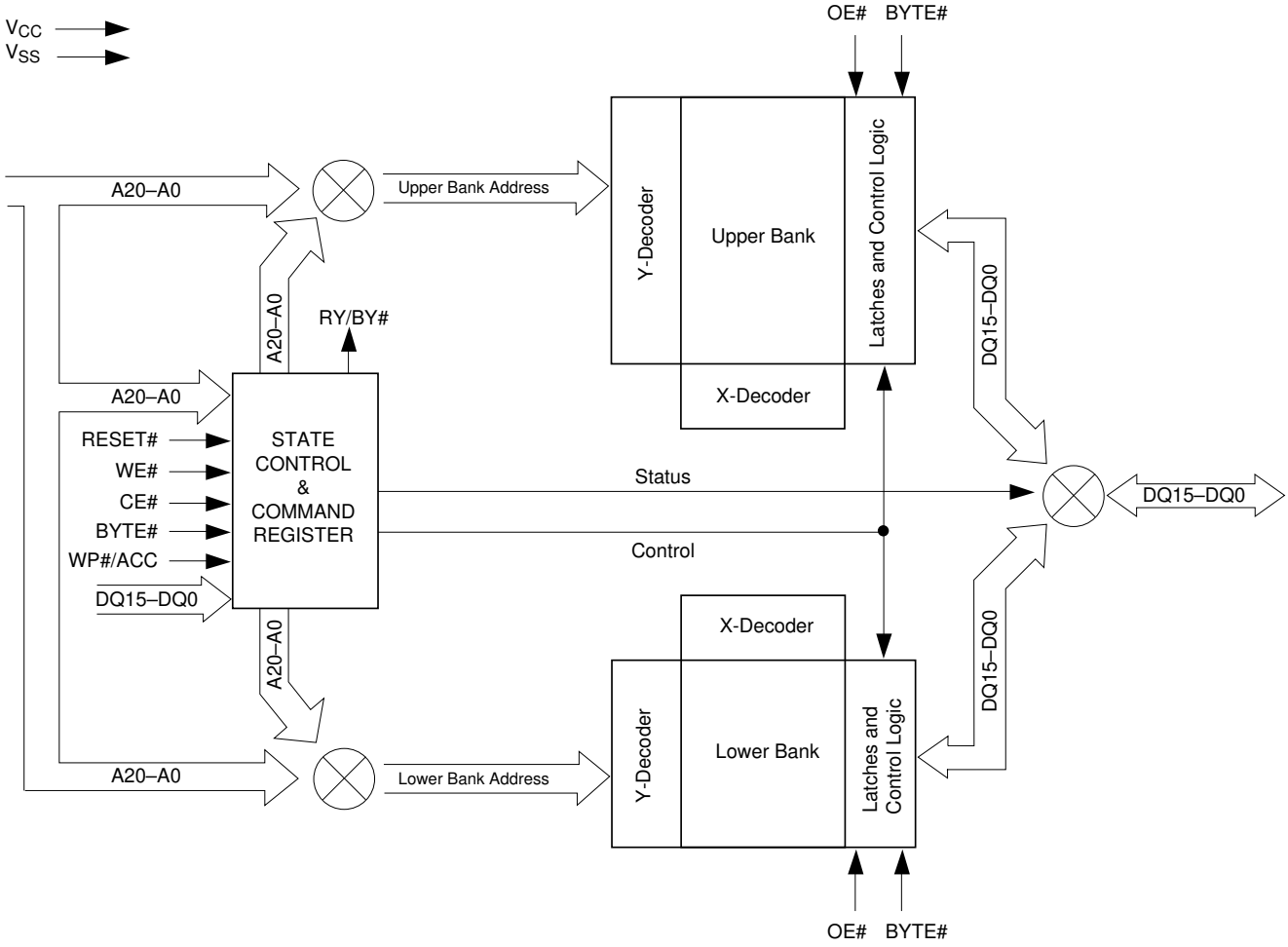
Part Number		S29JL032J	
Speed Option	Standard Voltage Range: V_{CC} = 3.0–3.6V	60	
	Standard Voltage Range: V_{CC} = 2.7–3.6V		70
Max Access Time (ns), t_{ACC}		60	70
CE# Access (ns), t_{CE}		60	70
OE# Access (ns), t_{OE}		25	30

3. Block Diagram

3.1 4-Bank Device

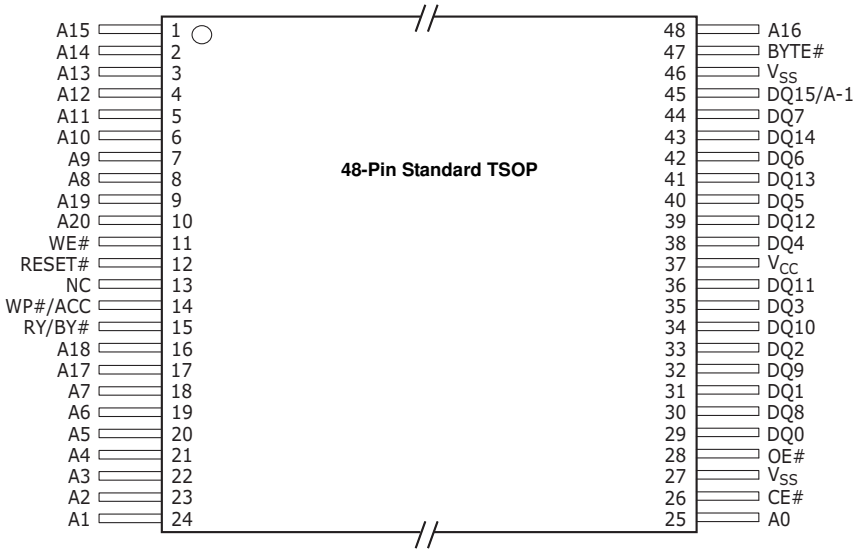


3.2 2-Bank Device

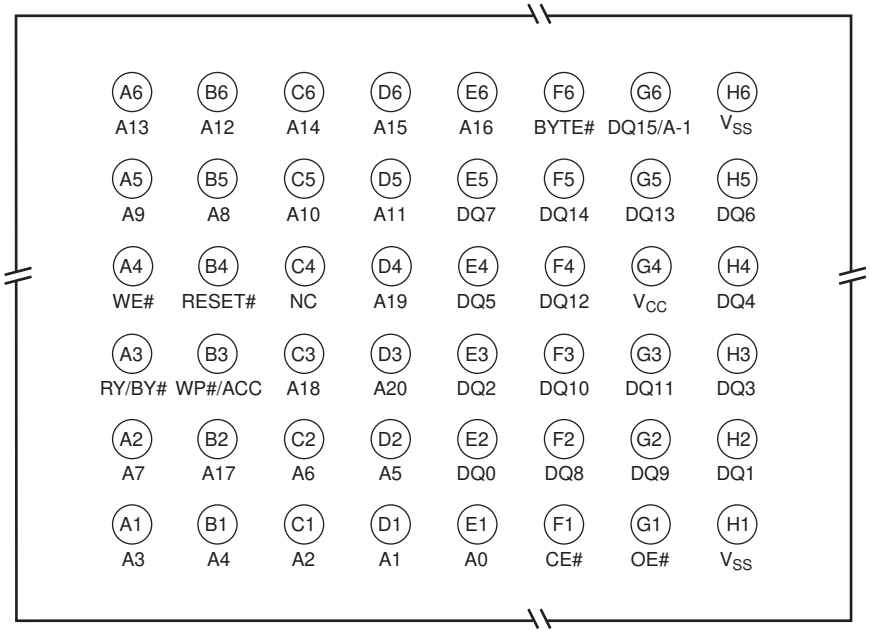


4. Connection Diagrams

4.1 48-pin TSOP Package



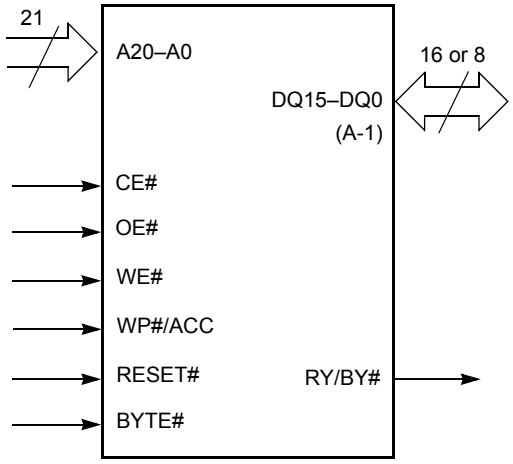
4.2 48-ball FBGA Package



5. Pin Description

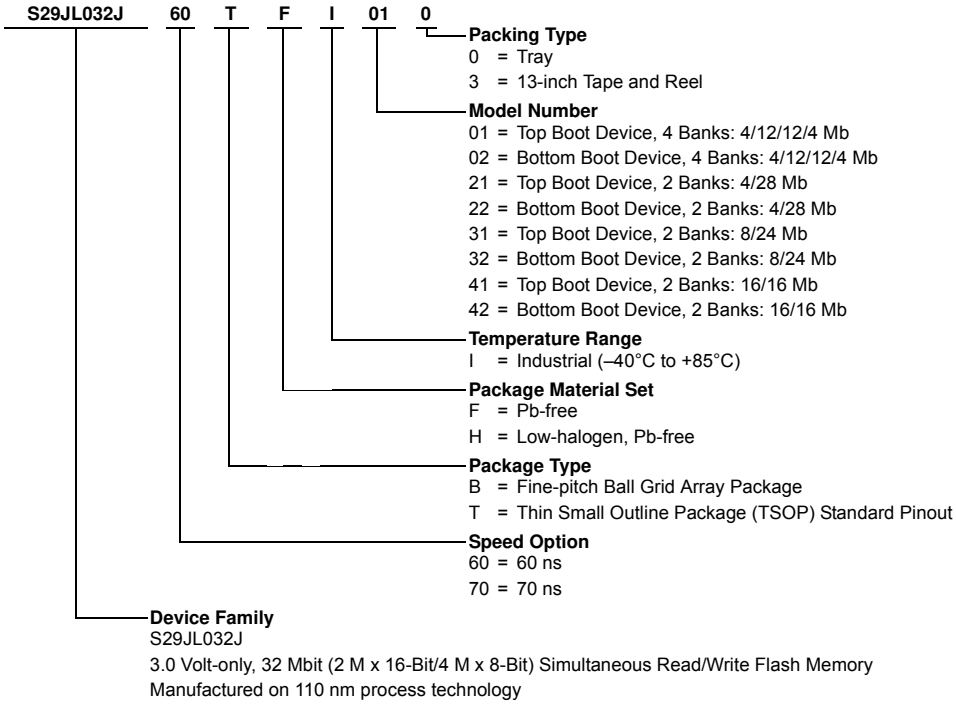
A20–A0	21 Address Pins
DQ14–DQ0	15 Data Inputs/Outputs (x16-only devices)
DQ15/A-1	DQ15 (Data Input/Output, word mode), A-1 (LSB Address Input, byte mode)
CE#	Chip Enable, Active Low
OE#	Output Enable, Active Low
WE#	Write Enable, Active Low
WP#/ACC	Hardware Write Protect/Acceleration Pin.
RESET#	Hardware Reset Pin, Active Low
BYTE#	Selects 8-bit or 16-bit mode, Active Low
RY/BY#	Ready/Busy Output, Active Low
V_{CC}	3.0 volt-only single power supply (see *Product Selector Guide* *on page 4* for speed options and voltage supply tolerances)
V_{SS}	Device Ground
NC	Not Connected – No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).

6. Logic Symbol



7. Ordering Information

The order number (Valid Combination) is formed by the following:



S29JL032J Valid Combinations							
Device Number/ Description	**Speed (ns)**	**Package Type**	**Temperature Range**	**Additional Ordering Options**	**Packing Type**	**Package Description**	
S29JL032J	60, 70	TF	I	01, 02, 21, 22, 31, 32, 41, 42	0, 3 (1)	TS048	TSOP
		BH		31, 32		VBK048	FBGA

Note:

1. Type 0 is standard. Specify others as required.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local Spansion sales office to confirm availability of specific valid combinations and to check on newly released combinations.

8. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

S29JL032J Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#/ACC	Addresses (Note 1)	DQ15–DQ8		DQ7–DQ0
							BYTE# = V_{IH}	BYTE# = V_{IL}	
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	DQ14–DQ8 = High-Z, DQ15 = A-1	D_{OUT}
Write	L	H	L	H	(Note 3)	A_{IN}	D_{IN}		D_{IN}
Standby	$V_{CC} \pm 0.3V$	X	X	$V_{CC} \pm 0.3V$	L/H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	L/H	SA, A6 = L, A1 = H, A0 = L	X	X	D_{IN}
Sector Unprotect (Note 2)	L	H	L	V_{ID}	(Note 3)	SA, A6 = H, A1 = H, A0 = L	X	X	D_{IN}
Temporary Sector Unprotect	X	X	X	V_{ID}	(Note 3)	A_{IN}	D_{IN}	High-Z	D_{IN}

Legend:
L = Logic Low = V_{IL}
H = Logic High = V_{IH}
V_{ID} = 8.5–12.5V
V_{HH} = 9.0 ± 0.5V
X = Don't Care
SA = Sector Address
A_{IN} = Address In
D_{IN} = Data In
D_{OUT} = Data Out

Notes:
1. *Addresses are A20:A0 in word mode (BYTE# = V_{IH}), A20:A-1 in byte mode (BYTE# = V_{IL}).*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See Boot Sector/Sector Block Protection and Unprotection on page 18.*
3. *If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, protection on the two outermost boot sectors depends on whether they were last protected or unprotected using the method described in Boot Sector/Sector Block Protection and Unprotection on page 18. If WP#/ACC = V_{HH}, all sectors will be unprotected.*

8.1 Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ7–DQ0 are active and controlled by CE# and OE#. The data I/O pins DQ14–DQ8 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

8.2 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

Refer to the *Read-Only Operations* on page 44 for timing specifications and to Figure 17.1 on page 44 for the timing diagram. I_{CC1} in *DC Characteristics* on page 40 represents the active current specification for reading array data.

8.3 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to *Word/Byte Configuration* on page 9 for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. *Byte/Word Program Command Sequence* on page 28 has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table on page 13 and Table on page 15 indicate the address space that each sector occupies. Similarly, a “sector address” is the address bits required to uniquely select a sector. *Command Definitions* on page 27 has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

The device address space is divided into four banks. A “bank address” is the address bits required to uniquely select a bank.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. *AC Characteristics* on page 44 contains timing specification tables and timing diagrams for write operations.

8.3.1 Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that V_{HH} must not be asserted on WP#/ACC for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result. See Write Protect (WP#) on page 20 for related information.*

8.3.2 Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. Refer to *Autoselect Mode* on page 17 and *Autoselect Command Sequence* on page 28 for more information.

8.4 Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in another bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 17.8 on page 49 shows how read and write cycles may be initiated for simultaneous operation with zero latency. I_{CC6} and I_{CC7} in *DC Characteristics on page 40* represent the current specifications for read-while-program and read-while-erase, respectively.

8.5 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{CC} ± 0.3V. *Note that this is a more restricted voltage range than V_{IH}.* If CE# and RESET# are held at V_{IH}, but not within V_{CC} ± 0.3V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in *DC Characteristics on page 40* represents the standby current specification.

8.6 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC5} in *DC Characteristics on page 40* represents the automatic sleep mode current specification.

8.7 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to *Hardware Reset (RESET#) on page 45* for RESET# parameters and to Figure 17.2 on page 45 for the timing diagram.

8.8 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

S29JL032J Bank Architecture

Device Model Number	Bank 1		Bank 2		Bank 3		Bank 4	
	Mbit	Sector Size	Mbit	Sector Size	Mbit	Sector Size	Mbit	Sector Size
01, 02	4 Mbit	Eight 8 kbyte/ 4 kword, seven 64 kbyte/ 32 kword	12 Mbit	Twenty-four 64 kbyte/ 32 kword	12 Mbit	Twenty-four 64 kbyte/ 32 kword	4 Mbit	Eight 64 kbyte/ 32 kword

Device Model Number	Bank 1		Bank 2	
	Mbits	Sector Size	Mbit	Sector Size
21, 22	4 Mbit	Eight 8 kbyte/4 kword, seven 64 kbyte/32 kword	28 Mbit	Fifty-six 64 kbyte/32 kword
31, 32	8 Mbit	Eight 8 kbyte/4 kword, fifteen 64 kbyte/32 kword	24 Mbit	Forty-eight 64 kbyte/32 kword
41, 42	16 Mbit	Eight 8 kbyte/4 kword, thirty-one 64 kbyte/32 kword	16 Mbit	Thirty-two 64 kbyte/32 kword

S29JL032J Sector Addresses - Top Boot Devices (Sheet 1 of 2)

S29JL032J (Model 41)	S29JL032J (Model 31)	S29JL032J (Model 21)	S29JL032J (Model 01)	Sector	Sector Address A20–A12	Sector Size (kbytes/kwords)	(x8) Address Range	(x16) Address Range
Bank 2	Bank 2	Bank 2	Bank 4	SA0	000000xxx	64/32	000000h-00FFFFh	000000h-07FFFh
				SA1	000001xxx	64/32	010000h-01FFFFh	008000h-0FFFFh
				SA2	000010xxx	64/32	020000h-02FFFFh	010000h-17FFFh
				SA3	000011xxx	64/32	030000h-03FFFFh	018000h-01FFFFh
				SA4	000100xxx	64/32	040000h-04FFFFh	020000h-027FFFh
				SA5	000101xxx	64/32	050000h-05FFFFh	028000h-02FFFFh
				SA6	000110xxx	64/32	060000h-06FFFFh	030000h-037FFFh
				SA7	000111xxx	64/32	070000h-07FFFFh	038000h-03FFFFh
			Bank 3	SA8	001000xxx	64/32	080000h-08FFFFh	040000h-047FFFh
				SA9	001001xxx	64/32	090000h-09FFFFh	048000h-04FFFFh
				SA10	001010xxx	64/32	0A0000h-0AFFFFh	050000h-057FFFh
				SA11	001011xxx	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
				SA12	001100xxx	64/32	0C0000h-0CFFFFh	060000h-067FFFh
				SA13	001101xxx	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
				SA14	001110xxx	64/32	0E0000h-0EFFFFh	070000h-077FFFh
				SA15	001111xxx	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
				SA16	010000xxx	64/32	100000h-10FFFFh	080000h-087FFFh
				SA17	010001xxx	64/32	110000h-11FFFFh	088000h-08FFFFh
				SA18	010010xxx	64/32	120000h-12FFFFh	090000h-097FFFh
				SA19	010011xxx	64/32	130000h-13FFFFh	098000h-09FFFFh
				SA20	010100xxx	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
				SA21	010101xxx	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
				SA22	010110xxx	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
				SA23	010111xxx	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
				SA24	011000xxx	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
				SA25	011001xxx	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
				SA26	011010xxx	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
				SA27	011011xxx	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
				SA28	011100xxx	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
				SA29	011101xxx	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
				SA30	011110xxx	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
				SA31	011111xxx	64/32	1F0000h-1FFFFFh	0F8000h-0FFFFFh

S29JL032J Sector Addresses - Top Boot Devices (Sheet 2 of 2)

S29JL032J (Model 41)	S29JL032J (Model 31)	S29JL032J (Model 21)	S29JL032J (Model 01)	Sector	Sector Address A20–A12	Sector Size (kbytes/kwords)	(x8) Address Range	(x16) Address Range
Bank 1	Bank 2 (continued)	Bank 2 (continued)	Bank 2	SA32	100000xxx	64/32	200000h-20FFFFh	100000h-107FFFh
				SA33	100001xxx	64/32	210000h-21FFFFh	108000h-10FFFFh
				SA34	100010xxx	64/32	220000h-22FFFFh	110000h-117FFFh
				SA35	100011xxx	64/32	230000h-23FFFFh	118000h-11FFFFh
				SA36	100100xxx	64/32	240000h-24FFFFh	120000h-127FFFh
				SA37	100101xxx	64/32	250000h-25FFFFh	128000h-12FFFFh
				SA38	100110xxx	64/32	260000h-26FFFFh	130000h-137FFFh
				SA39	100111xxx	64/32	270000h-27FFFFh	138000h-13FFFFh
				SA40	101000xxx	64/32	280000h-28FFFFh	140000h-147FFFh
				SA41	101001xxx	64/32	290000h-29FFFFh	148000h-14FFFFh
				SA42	101010xxx	64/32	2A0000h-2AFFFFh	150000h-157FFFh
				SA43	101011xxx	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
				SA44	101100xxx	64/32	2C0000h-2CFFFFh	160000h-167FFFh
				SA45	101101xxx	64/32	2D0000h-2DFFFFh	168000h-16FFFFh
				SA46	101110xxx	64/32	2E0000h-2EFFFFh	170000h-177FFFh
				SA47	101111xxx	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
	Bank 1			SA48	110000xxx	64/32	300000h-30FFFFh	180000h-187FFFh
				SA49	110001xxx	64/32	310000h-31FFFFh	188000h-18FFFFh
				SA50	110010xxx	64/32	320000h-32FFFFh	190000h-197FFFh
				SA51	110011xxx	64/32	330000h-33FFFFh	198000h-19FFFFh
				SA52	110100xxx	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
				SA53	110101xxx	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
				SA54	110110xxx	64/32	360000h-36FFFFh	1B0000h-1BFFFFh
				SA55	110111xxx	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
		Bank 1	Bank 1	SA56	111000xxx	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
				SA57	111001xxx	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
				SA58	111010xxx	64/32	3A0000h-3AFFFFh	1D0000h-1DFFFFh
				SA59	111011xxx	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
				SA60	111100xxx	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
				SA61	111101xxx	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
				SA62	111110xxx	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
				SA63	111111000	8/4	3F0000h-3F1FFFh	1F8000h-1F8FFFh
				SA64	111111001	8/4	3F2000h-3F3FFFh	1F9000h-1F9FFFh
				SA65	111111010	8/4	3F4000h-3F5FFFh	1FA000h-1FAFFFh
				SA66	111111011	8/4	3F6000h-3F7FFFh	1FB000h-1FBFFFh
				SA67	111111100	8/4	3F8000h-3F9FFFh	1FC000h-1FCFFFh
				SA68	111111101	8/4	3FA000h-3FBFFFh	1FD000h-1FDFFFh
				SA69	111111110	8/4	3FC000h-3FDFFFh	1FE000h-1FEFFFh
				SA70	111111111	8/4	3FE000h-3FFFFFh	1FF000h-1FFFFFh

S29JL032J Sector Addresses - Bottom Boot Devices (Sheet 1 of 2)

S29JL032J (Model 42)	S29JL032J (Model 32)	S29JL032J (Model 22)	S29JL032J (Model 02)	Sector	Sector Address A20–A12	Sector Size (kbytes/kwords)	(x8) Address Range	(x16) Address Range
Bank 1	Bank 1	Bank 1	Bank 1	SA0	000000000	8/4	000000h-001FFFh	000000h-000FFFh
				SA1	000000001	8/4	002000h-003FFFh	001000h-001FFFh
				SA2	000000010	8/4	004000h-005FFFh	002000h-002FFFh
				SA3	000000011	8/4	006000h-007FFFh	003000h-003FFFh
				SA4	000000100	8/4	008000h-009FFFh	004000h-004FFFh
				SA5	000000101	8/4	00A000h-00BFFFh	005000h-005FFFh
				SA6	000000110	8/4	00C000h-00DFFFh	006000h-006FFFh
				SA7	000000111	8/4	00E000h-00FFFFh	007000h-007FFFh
				SA8	000001xxx	64/32	010000h-01FFFFh	008000h-00FFFFh
				SA9	000010xxx	64/32	020000h-02FFFFh	010000h-017FFFh
				SA10	000011xxx	64/32	030000h-03FFFFh	018000h-01FFFFh
				SA11	000100xxx	64/32	040000h-04FFFFh	020000h-027FFFh
				SA12	000101xxx	64/32	050000h-05FFFFh	028000h-02FFFFh
				SA13	000110xxx	64/32	060000h-06FFFFh	030000h-037FFFh
				SA14	000111xxx	64/32	070000h-07FFFFh	038000h-03FFFFh
		Bank 2	Bank 2	SA15	001000xxx	64/32	080000h-08FFFFh	040000h-047FFFh
				SA16	001001xxx	64/32	090000h-09FFFFh	048000h-04FFFFh
				SA17	001010xxx	64/32	0A0000h-0AFFFFh	050000h-057FFFh
				SA18	001011xxx	64/32	0B0000h-0BFFFFh	058000h-05FFFFh
				SA19	001100xxx	64/32	0C0000h-0CFFFFh	060000h-067FFFh
				SA20	001101xxx	64/32	0D0000h-0DFFFFh	068000h-06FFFFh
				SA21	001110xxx	64/32	0E0000h-0EFFFFh	070000h-077FFFh
				SA22	001111xxx	64/32	0F0000h-0FFFFFh	078000h-07FFFFh
	Bank 2			SA23	010000xxx	64/32	100000h-10FFFFh	080000h-087FFFh
				SA24	010001xxx	64/32	110000h-11FFFFh	088000h-08FFFFh
				SA25	010010xxx	64/32	120000h-12FFFFh	090000h-097FFFh
				SA26	010011xxx	64/32	130000h-13FFFFh	098000h-09FFFFh
				SA27	010100xxx	64/32	140000h-14FFFFh	0A0000h-0A7FFFh
				SA28	010101xxx	64/32	150000h-15FFFFh	0A8000h-0AFFFFh
				SA29	010110xxx	64/32	160000h-16FFFFh	0B0000h-0B7FFFh
				SA30	010111xxx	64/32	170000h-17FFFFh	0B8000h-0BFFFFh
				SA31	011000xxx	64/32	180000h-18FFFFh	0C0000h-0C7FFFh
				SA32	011001xxx	64/32	190000h-19FFFFh	0C8000h-0CFFFFh
				SA33	011010xxx	64/32	1A0000h-1AFFFFh	0D0000h-0D7FFFh
				SA34	011011xxx	64/32	1B0000h-1BFFFFh	0D8000h-0DFFFFh
				SA35	011100xxx	64/32	1C0000h-1CFFFFh	0E0000h-0E7FFFh
				SA36	011101xxx	64/32	1D0000h-1DFFFFh	0E8000h-0EFFFFh
				SA37	011110xxx	64/32	1E0000h-1EFFFFh	0F0000h-0F7FFFh
				SA38	011111xxx	64/32	1F0000h-1FFFFFh	0F8000h-0FFFFFh

S29JL032J Sector Addresses - Bottom Boot Devices (Sheet 2 of 2)

S29JL032J (Model 42)	S29JL032J (Model 32)	S29JL032J (Model 22)	S29JL032J (Model 02)	Sector	Sector Address A20–A12	Sector Size (kbytes/kwords)	(x8) Address Range	(x16) Address Range
Bank 2	Bank 2 (continued)	Bank 2 (continued)	Bank 3	SA39	100000xxx	64/32	200000h-20FFFFh	100000h-107FFFh
				SA40	100001xxx	64/32	210000h-21FFFFh	108000h-10FFFFh
				SA41	100010xxx	64/32	220000h-22FFFFh	110000h-117FFFh
				SA42	100011xxx	64/32	230000h-23FFFFh	118000h-11FFFFh
				SA43	100100xxx	64/32	240000h-24FFFFh	120000h-127FFFh
				SA44	100101xxx	64/32	250000h-25FFFFh	128000h-12FFFFh
				SA45	100110xxx	64/32	260000h-26FFFFh	130000h-137FFFh
				SA46	100111xxx	64/32	270000h-27FFFFh	138000h-13FFFFh
				SA47	101000xxx	64/32	280000h-28FFFFh	140000h-147FFFh
				SA48	101001xxx	64/32	290000h-29FFFFh	148000h-14FFFFh
				SA49	101010xxx	64/32	2A0000h-2AFFFFh	150000h-157FFFh
				SA50	101011xxx	64/32	2B0000h-2BFFFFh	158000h-15FFFFh
				SA51	101100xxx	64/32	2C0000h-2CFFFFh	160000h-167FFFh
				SA52	101101xxx	64/32	2D0000h-2DFFFFh	168000h-16FFFFh
				SA53	101110xxx	64/32	2E0000h-2EFFFFh	170000h-177FFFh
				SA54	111111xxx	64/32	2F0000h-2FFFFFh	178000h-17FFFFh
				SA55	111000xxx	64/32	300000h-30FFFFh	180000h-187FFFh
				SA56	110001xxx	64/32	310000h-31FFFFh	188000h-18FFFFh
				SA57	110010xxx	64/32	320000h-32FFFFh	190000h-197FFFh
				SA58	110011xxx	64/32	330000h-33FFFFh	198000h-19FFFFh
				SA59	110100xxx	64/32	340000h-34FFFFh	1A0000h-1A7FFFh
				SA60	110101xxx	64/32	350000h-35FFFFh	1A8000h-1AFFFFh
				SA61	110110xxx	64/32	360000h-36FFFFh	1B0000h-1B7FFFh
				SA62	110111xxx	64/32	370000h-37FFFFh	1B8000h-1BFFFFh
			Bank 4	SA63	111000xxx	64/32	380000h-38FFFFh	1C0000h-1C7FFFh
				SA64	111001xxx	64/32	390000h-39FFFFh	1C8000h-1CFFFFh
				SA65	111010xxx	64/32	3A0000h-3AFFFFh	1D0000h-1D7FFFh
				SA66	111011xxx	64/32	3B0000h-3BFFFFh	1D8000h-1DFFFFh
				SA67	111100xxx	64/32	3C0000h-3CFFFFh	1E0000h-1E7FFFh
				SA68	111101xxx	64/32	3D0000h-3DFFFFh	1E8000h-1EFFFFh
				SA69	111110xxx	64/32	3E0000h-3EFFFFh	1F0000h-1F7FFFh
				SA70	111111xxx	64/32	3F0000h-3F1FFFh	1F8000h-1FFFFFh

8.9 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins must be as shown in Table . In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits. Table shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0. However, the autoselect codes can also be accessed in-system through the command register, for instances when the S29JL032J is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table on page 33. *Note that if a Bank Address (BA) on address bits A20, A19 and A18 is asserted during the third write cycle of the autoselect command, the host system can read autoselect data from that bank and then immediately read array data from another bank, without exiting the autoselect mode.*

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table on page 33. This method does not require V_{ID}. Refer to *Autoselect Command Sequence on page 28* for more information.

S29JL032J Autoselect Codes (High Voltage Method)

Description	CE#	OE#	WE#	A20 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A4	A3	A2	A1	A0	DQ15 to DQ8		DQ7 to DQ0
														BYTE# = V_{IH}	BYTE# = V_{IL}	
Manufacturer ID: Spansion Products	L	L	H	BA	X	V_{ID}	X	L	X	L	L	L	L	X	X	01h
Device ID (Models 01, 02) Read Cycle 1	L	L	H	BA	X	V_{ID}	X	L	X	L	L	L	H	22h	X	7Eh
Device ID (Models 01, 02) Read Cycle 2								L		H	H	H	L	22h		0Ah
Device ID (Models 01, 02) Read Cycle 3								L		H	H	H	H	22h		00h (bottom boot) 01h (top boot)
Device ID (Models 21, 22)	L	L	H	BA	X	V_{ID}	X	L	X	X	X	L	H	22h	X	56h (bottom boot) 55h (top boot)
Device ID (Models 31, 32)	L	L	H	BA	X	V_{ID}	X	L	X	X	X	L	H	22h	X	53h (bottom boot) 50h (top boot)
Device ID (Models 41, 42)	L	L	H	BA	X	V_{ID}	X	L	X	X	X	L	H	22h	X	5Fh (bottom boot) 5Ch (top boot)
Sector Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	L	L	H	L	X	X	01h (protected), 00h (unprotected)
Secured Silicon Indicator Bit (DQ6, DQ7)	L	L	H	BA	X	V_{ID}	X	L	X	L	L	H	H	X	X	82h (Factory Locked), 42h (Customer Locked), 02h (Not Locked)

Legend:
L = Logic Low = V_{IL}
H = Logic High = V_{IH}
BA = Bank Address
SA = Sector Address
X = Don't care.

8.10 Boot Sector/Sector Block Protection and Unprotection

Note: For the following discussion, the term "sector" applies to both boot sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table).

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented via two methods.

S29JL032J Boot Sector/Sector Block Addresses for Protection/Unprotection (Top Boot Devices)

Sector	A20-A12	Sector/ Sector Block Size
SA0	000000XXX	64 kbytes
SA1-SA3	000001XXX 000010XXX 000011XXX	192 (3X64) kbytes
SA4-SA7	0001XXXXX	256 (4X64) kbytes
SA8-SA11	0010XXXXX	256 (4X64) kbytes
SA12-SA15	0011XXXXX	256 (4X64) kbytes
SA16-SA19	0100XXXXX	256 (4X64) kbytes
SA20-SA23	0101XXXXX	256 (4X64) kbytes
SA24-SA27	0110XXXXX	256 (4X64) kbytes
SA28-SA31	0111XXXXX	256 (4X64) kbytes
SA32-SA35	1000XXXXX	256 (4X64) kbytes
SA36-SA39	1001XXXXX	256 (4X64) kbytes
SA40-SA43	1010XXXXX	256 (4X64) kbytes
SA44-SA47	1011XXXXX	256 (4X64) kbytes
SA48-SA51	1100XXXXX	256 (4X64) kbytes
SA52-SA55	1101XXXXX	256 (4X64) kbytes
SA56-SA59	1110XXXXX	256 (4X64) kbytes
SA60-SA62	111100XXX 111101XXX 111110XXX	192 (3X64) kbytes
SA63	111111000	8 kbytes
SA64	111111001	8 kbytes
SA65	111111010	8 kbytes
SA66	111111011	8 kbytes
SA67	111111100	8 kbytes
SA68	111111101	8 kbytes
SA69	111111110	8 kbytes
SA70	111111111	8 kbytes

S29JL032J Sector/Sector Block Addresses for Protection/Unprotection (Bottom Boot Devices)

Sector	A20-A12	Sector/ Sector Block Size
SA70	111111XXX	64 kbytes
SA69-SA67	111110XXX 111101XXX 111100XXX	192 (3X64) kbytes
SA66-SA63	1110XXXXX	256 (4X64) kbytes
SA62-SA59	1101XXXXX	256 (4X64) kbytes
SA58-SA55	1100XXXXX	256 (4X64) kbytes
SA54-SA51	1011XXXXX	256 (4X64) kbytes
SA50-SA47	1010XXXXX	256 (4X64) kbytes
SA46-SA43	1001XXXXX	256 (4X64) kbytes
SA42-SA39	1000XXXXX	256 (4X64) kbytes
SA38-SA35	0111XXXXX	256 (4X64) kbytes
SA34-SA31	0110XXXXX	256 (4X64) kbytes
SA30-SA27	0101XXXXX	256 (4X64) kbytes
SA26-SA23	0100XXXXX	256 (4X64) kbytes
SA22-SA19	0011XXXXX	256 (4X64) kbytes
SA18-SA15	0010XXXXX	256 (4X64) kbytes
SA14-SA11	0001XXXXX	256 (4X64) kbytes
SA10-SA8	000011XXX 000010XXX 000001XXX	192 (3X64) kbytes
SA7	000000111	8 kbytes
SA6	000000110	8 kbytes
SA5	000000101	8 kbytes
SA4	000000100	8 kbytes
SA3	000000011	8 kbytes
SA2	000000010	8 kbytes
SA1	000000001	8 kbytes
SA0	000000000	8 kbytes

Sector Protect/Sector Unprotect requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 8.2 on page 21 shows the algorithms and Figure 17.13 on page 52 shows the timing diagram. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle. *Note that the sector unprotect algorithm unprotects all sectors in parallel.* All previously protected sectors must be individually re-protected. To change data in protected sectors efficiently, the temporary sector unprotect function is available. See *Temporary Sector Unprotect on page 20.*

The device is shipped with all sectors unprotected. Optional Spansion programming service enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for details.

It is possible to determine whether a sector is protected or unprotected. See *Autoselect Mode on page 17* for details.

8.11 Write Protect (WP#)

The Write Protect function provides a hardware method of protecting certain boot sectors without using V_{ID}. This function is one of two provided by the WP#/ACC pin.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the two outermost 8 kbyte boot sectors independently of whether those sectors were protected or unprotected using the method described in *Boot Sector/Sector Block Protection and Unprotection on page 18*. The two outermost 8 kbyte boot sectors are the two sectors containing the lowest addresses in a bottom-boot-configured device, or the two sectors containing the highest addresses in a top-boot-configured device.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the two outermost 8K Byte boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these two sectors depends on whether they were last protected or unprotected using the method described in *Boot Sector/Sector Block Protection and Unprotection on page 18*.

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

WP#/ACC Modes

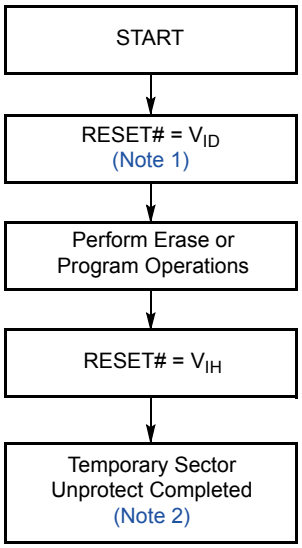
WP# Input Voltage	Device Mode
V_{IL}	Disables programming and erasing in the two outermost boot sectors
V_{IH}	Enables programming and erasing in the two outermost boot sectors, dependent on whether they were last protected or unprotected
V_{HH}	Enables accelerated programming (ACC). See *Accelerated Program Operation on page 10*.

8.12 Temporary Sector Unprotect

Note: For the following discussion, the term "sector" applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table on page 18 and Table on page 19).

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Temporary Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 8.1 shows the algorithm, and Figure 17.12 on page 51 shows the timing diagrams, for this feature. If the WP#/ACC pin is at V_{IL}, the two outermost boot sectors will remain protected during the Temporary sector Unprotect mode.

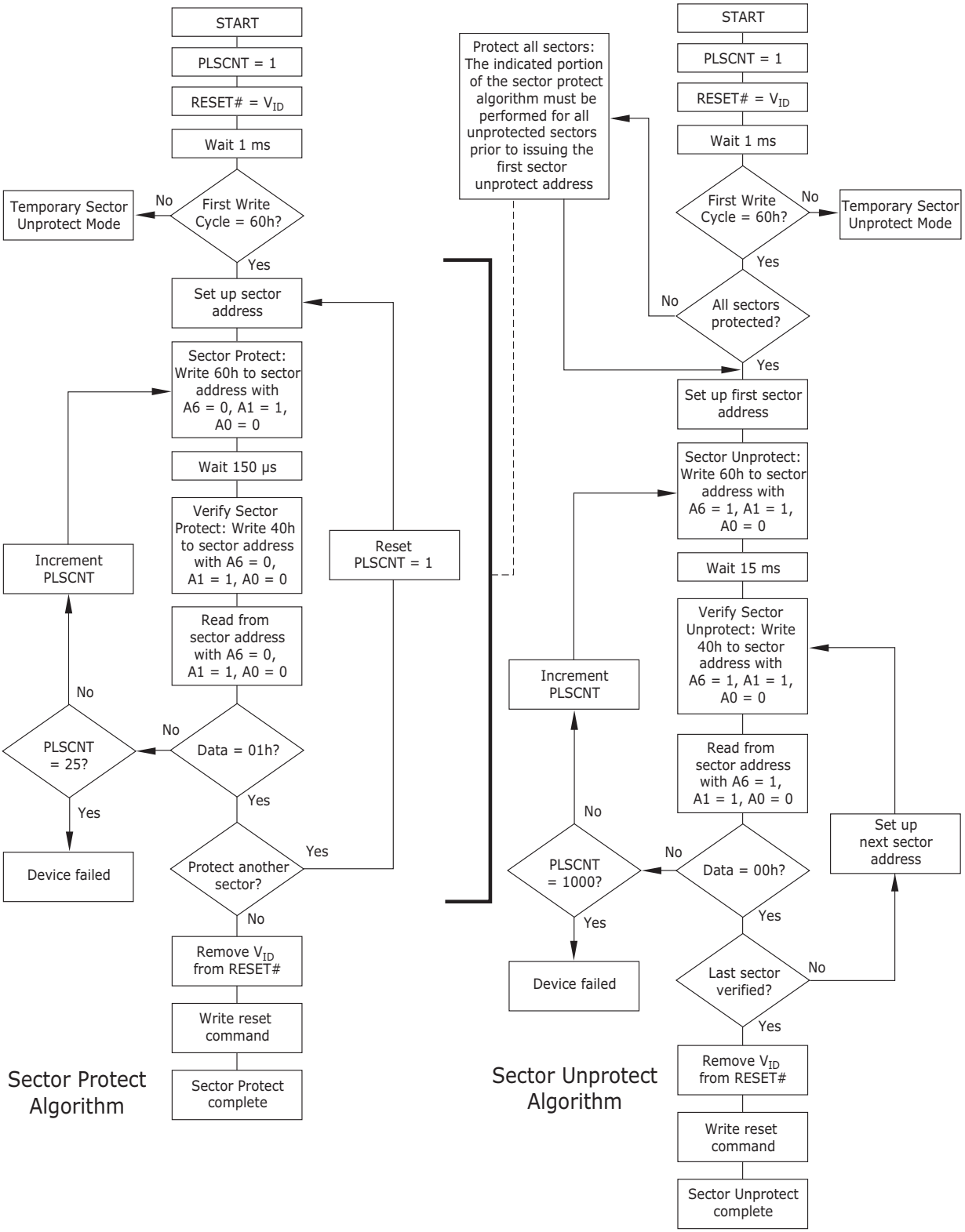
Figure 8.1 Temporary Sector Unprotect Operation



Notes:

1. *All protected sectors unprotected (If WP#/ACC = V_{IL}, the outermost two boot sectors will remain protected).*
2. *All previously protected sectors are protected once again.*

Figure 8.2 In-System Sector Protect/Unprotect Algorithms



8.13 Secured Silicon Region

The Secured Silicon Region feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Region is 256 bytes in length, and may shipped unprotected, allowing customers to utilize that sector in any manner they choose, or may shipped locked at the factory (upon customer request). The Secured Silicon Indicator Bit data will be 82h if factory locked, 42h if customer locked, or 02h if neither. Refer to Table on page 17 for more details.

The system accesses the Secured Silicon through a command sequence (see *Enter Secured Silicon Region/Exit Secured Silicon Region Command Sequence on page 28*). After the system has written the Enter Secured Silicon Region command sequence, it may read the Secured Silicon Region by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit Secured Silicon Region command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the first 256 bytes of Sector 0. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Region is enabled.*

8.13.1 Factory Locked: Secured Silicon Region Programmed and Protected At the Factory

In a factory locked device, the Secured Silicon Region is protected when the device is shipped from the factory. The Secured Silicon Region cannot be modified in any way. The device is preprogrammed with both a random number and a secure ESN. The 8-word random number is at addresses 000000h-000007h in word mode (or 000000h-00000Fh in byte mode). The secure ESN is programmed in the next 8 words at addresses 000008h-00000Fh (or 000010h-00001Fh in byte mode). The device is available preprogrammed with one of the following:

- A random, secure ESN only
- Customer code through Spansion programming services
- Both a random, secure ESN and customer code through Spansion programming services

Contact an your local sales office for details on using Spansion programming services.

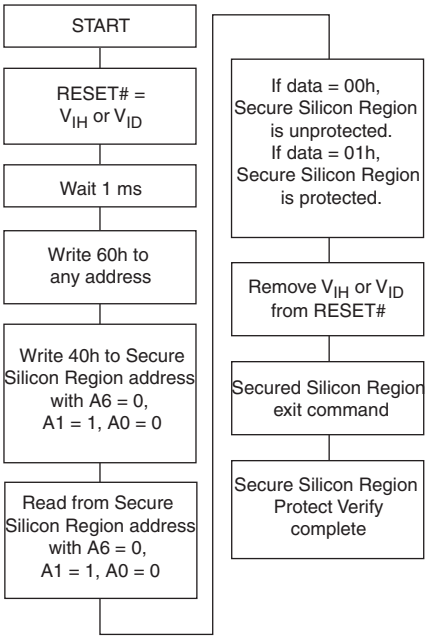
8.13.2 Customer Lockable: Secured Silicon Region NOT Programmed or Protected At the Factory

If the security feature is not required, the Secured Silicon Region can be treated as an additional Flash memory space. The Secured Silicon Region can be read any number of times, but can be programmed and locked only once. *Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the Secured Silicon Region.*

- Write the three-cycle Enter Secured Silicon Region command sequence, and then follow the insystem sector protect algorithm as shown in Figure 8.2 on page 21, except that RESET# may be at either V_{IH} or V_{ID}. This allows in-system protection of the Secured Silicon Region without raising any device pin to a high voltage. *Note that this method is only applicable to the Secured Silicon Region.*
- To verify the protect/unprotect status of the Secured Silicon Region, follow the algorithm shown in Figure 8.3 on page 23.

Once the Secured Silicon Region is locked and verified, the system must write the Exit Secured Silicon Region command sequence to return to reading and writing the remainder of the array. The Secured Silicon Region lock must be used with caution since, once locked, there is no procedure available for unlocking the Secured Silicon Region area and none of the bits in the Secured Silicon Region memory space can be modified in any way.

Figure 8.3 Secured Silicon Region Protect Verify



8.14 Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table on page 33 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

8.14.1 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

8.14.2 Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

8.14.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

8.14.4 Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

9. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Table . To terminate reading CFI data, the system must write the reset command. The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode via the command register only (high voltage method does not apply). The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table . The system must write the reset command to return to reading array data.

For further information, please refer to the CFI Specification and *CFI Publication 100*. Contact your local sales office for copies of these documents.

CFI Query Identification String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

System Interface String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0003h	Typical timeout per single byte/word write 2^N µs
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	0009h	Typical timeout per individual block erase 2^N ms
22h	44h	000Fh	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0004h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Device Geometry Definition

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
27h	4Eh	0016h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0002h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	62h 64h 66h 68h	003Eh 0000h 0000h 0001h	Erase Block Region 2 Information (refer to the CFI specification or CFI publication 100)
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information (refer to the CFI specification or CFI publication 100)
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to the CFI specification or CFI publication 100)