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S29JL064J

64 Mbit (8 M x 8-Bit/4 M x 16-Bit), 3 V Simultaneous Read/Write Flash

Distinctive Characteristics

Architectural Advantages

- Simultaneous Read/Write operations
  - Data can be continuously read from one bank while executing erase/program functions in another bank
  - Zero latency between read and write operations
- Flexible bank architecture
  - Read may occur in any of the three banks not being programmed or erased
  - Four banks may be grouped by customer to achieve desired bank divisions
- Boot sectors
  - Top and bottom boot sectors in the same device
  - Any combination of sectors can be erased
- Manufactured on 0.11 µm Process Technology
- Secured Silicon Region: **Extra 256-byte sector**
  - *Factory locked and identifiable:* 16 bytes available for secure, random factory Electronic Serial Number; verifiable as factory locked through autoselect function
  - *Customer lockable:* One-time programmable only. Once locked, data cannot be changed
- Zero power operation
  - Sophisticated power management circuits reduce power consumed during inactive periods to nearly zero
- Compatible with JEDEC standards
  - Pinout and software compatible with single-power-supply flash standard

Package Options

- 48-ball Fine-pitch BGA
- 48-pin TSOP

Performance Characteristics

- High performance
  - Access time as fast as 55 ns
  - Program time: 7 µs/word typical using accelerated programming function
- Ultra low power consumption (typical values)
  - 2 mA active read current at 1 MHz
  - 10 mA active read current at 5 MHz
  - 200 nA in standby or automatic sleep mode
- Cycling endurance: 1 million cycles per sector typical
- Data retention: 20 years typical

Software Features

- Supports Common Flash Memory Interface (CFI)
- Erase suspend/erase resume
  - Suspends erase operations to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- Data# polling and toggle bits
  - Provides a software method of detecting the status of program or erase operations
- Unlock bypass program command
  - Reduces overall programming time when issuing multiple program command sequences

Hardware Features

- Ready/Busy# output (RY/BY#)
  - Hardware method for detecting program or erase cycle completion
- Hardware reset pin (RESET#)
  - Hardware method of resetting the internal state machine to the read mode
- WP#/ACC input pin
  - Write protect (WP#) function protects sectors 0, 1, 140, and 141, regardless of sector protect status
  - Acceleration (ACC) function accelerates program timing
- Sector Protection
  - Hardware method to prevent any program or erase operation within a sector
  - Temporary Sector Unprotect allows changing data in protected sectors in-system

General Description

The S29JL064J is a 64 Mbit, 3.0 volt-only flash memory device, organized as 4,194,304 words of 16 bits each or 8,388,608 bytes of 8 bits each. Word mode data appears on DQ15–DQ0; byte mode data appears on DQ7–DQ0. The device is designed to be programmed in-system with the standard 3.0 volt V_{CC} supply, and can also be programmed in standard EPROM programmers. The device is available with an access time of 55, 60, 70 ns and is offered in a 48-ball FBGA or 48-pin TSOP package. Standard control pins—chip enable (CE#), write enable (WE#), and output enable (OE#)—control normal read and write operations, and avoid bus contention issues. The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

Contents

1. Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into **four banks,** two 8 Mb banks with small and large sectors, and two 24 Mb banks of large sectors. Sector addresses are fixed, system software can be used to form user-defined bank groups.

During an Erase/Program operation, any of the three non-busy banks may be read from. Note that only two banks can operate simultaneously. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The S29JL064J is organized as a dual boot device with both top and bottom boot sectors.

Bank	Mbits	Sector Sizes
Bank 1	8 Mb	Eight 8 kbyte/4 kword, Fifteen 64 kbyte/32 kword
Bank 2	24 Mb	Forty-eight 64 kbyte/32 kword
Bank 3	24 Mb	Forty-eight 64 kbyte/32 kword
Bank 4	8 Mb	Eight 8 kbyte/4 kword, Fifteen 64 kbyte/32 kword

1.1 S29JL064J Features

The **Secured Silicon Region** is an extra 256 byte sector capable of being permanently locked by Spansion or customers. The Secured Silicon Customer Indicator Bit (DQ6) is permanently set to 1 if the part has been customer locked, and permanently set to 0 if the part has been factory locked. This way, customer lockable parts can never be used to replace a factory locked part.

Factory locked parts provide several options. The Secured Silicon Region may store a secure, random 16 byte ESN (Electronic Serial Number), customer code (programmed through Spansion programming services), or both. Customer Lockable parts may utilize the Secured Silicon Region as bonus space, reading and writing like any other flash sector, or may permanently lock their own code there.

The device offers complete compatibility with the **JEDEC 42.4 single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by using the device **status bits:** RY/BY# pin, DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to the read mode.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

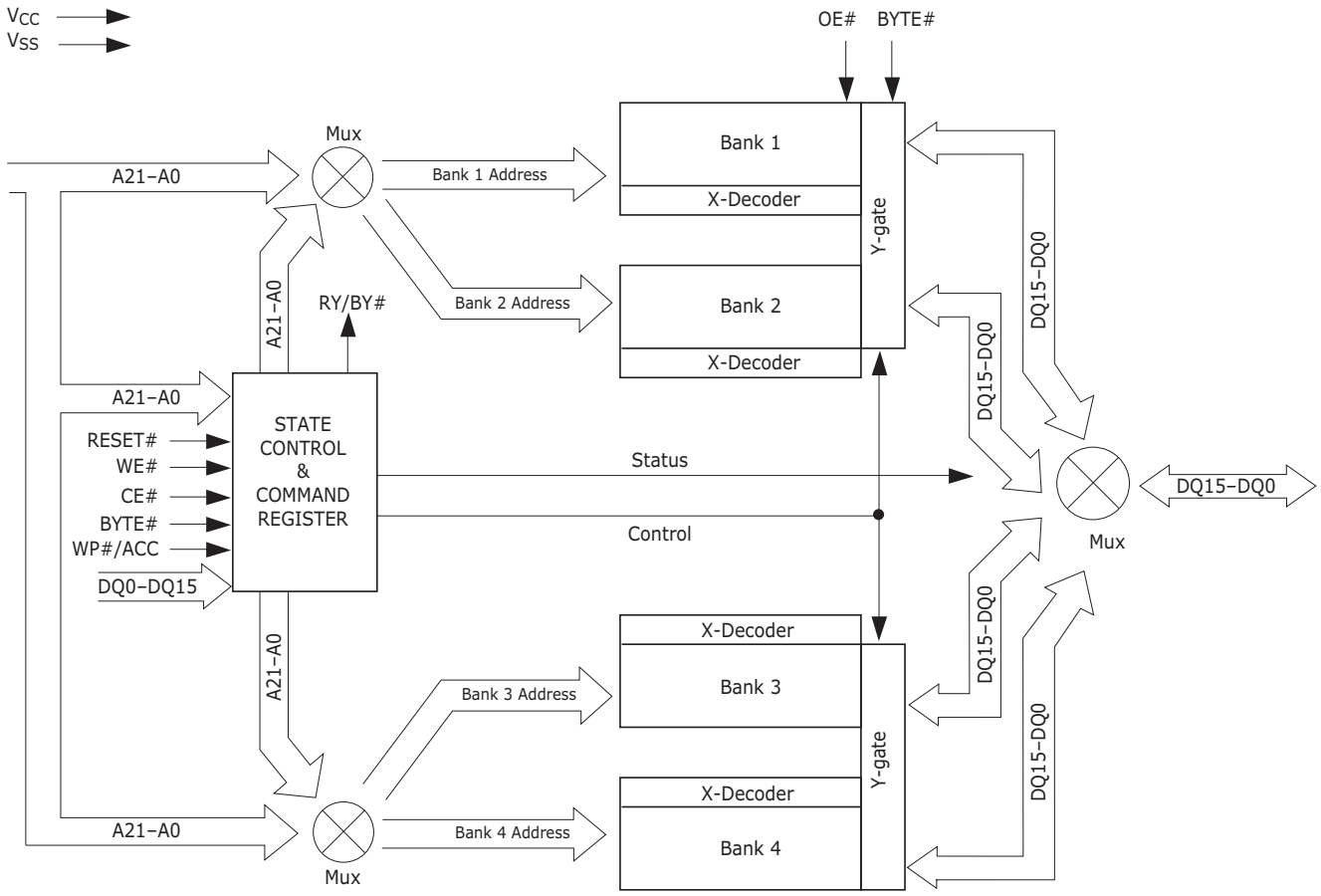
The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved. If a read is needed from the Secured Silicon Region (One Time Program area) after an erase suspend, then the user must use the proper command sequence to enter and exit this region.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

2. Product Selector Guide

Part Number		S29JL064J		
Speed Option	Standard Voltage Range: V_{CC} = 2.7–3.6V	55	60	70
Max Access Time (ns), t_{ACC}		55	60	70
CE# Access (ns), t_{CE}		55	60	70
OE# Access (ns), t_{OE}		25	25	30

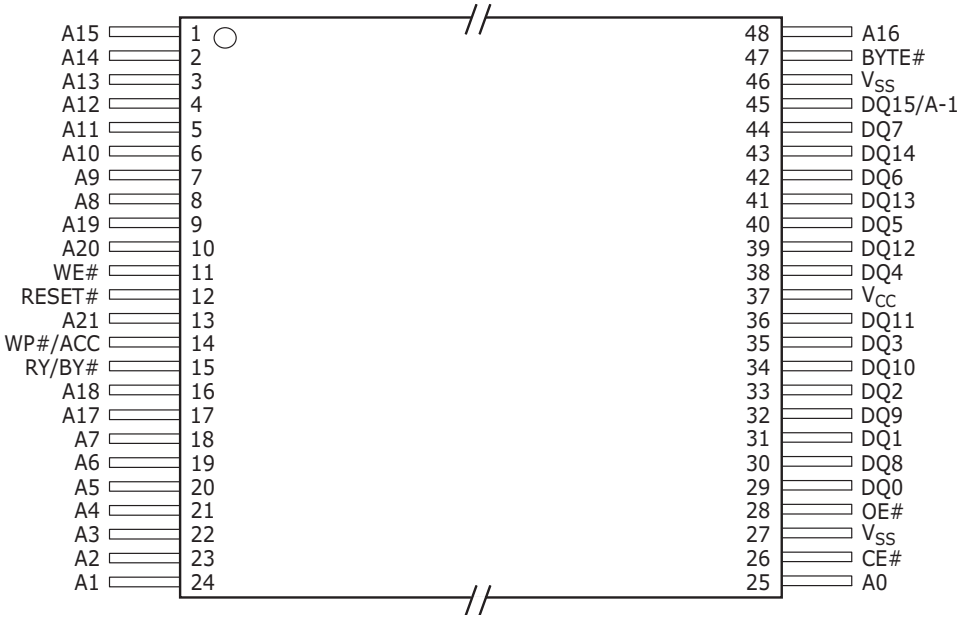
3. Block Diagram



4. Connection Diagrams

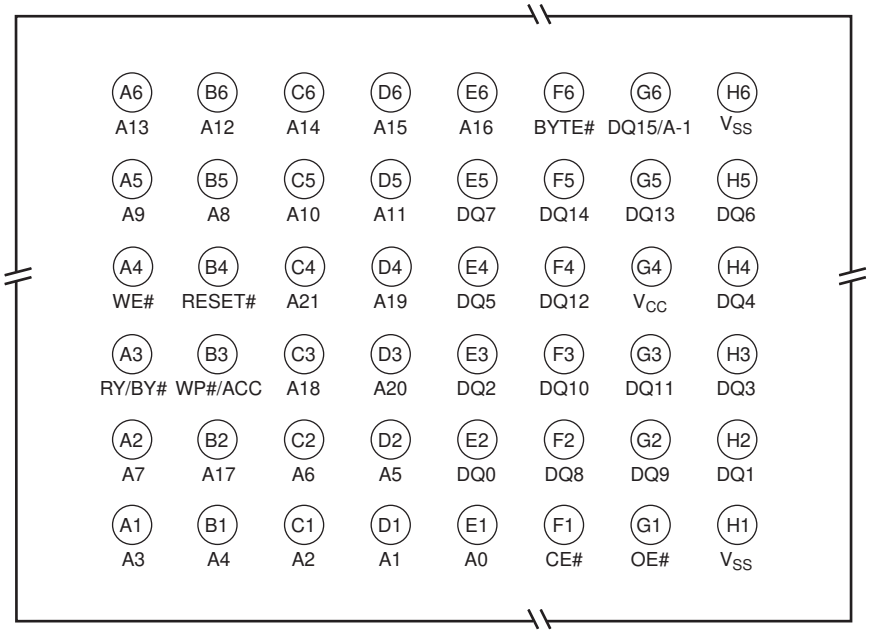
4.1 48-pin TSOP Package

Figure 4.1 48-Pin Standard TSOP



4.2 48-ball FBGA Package

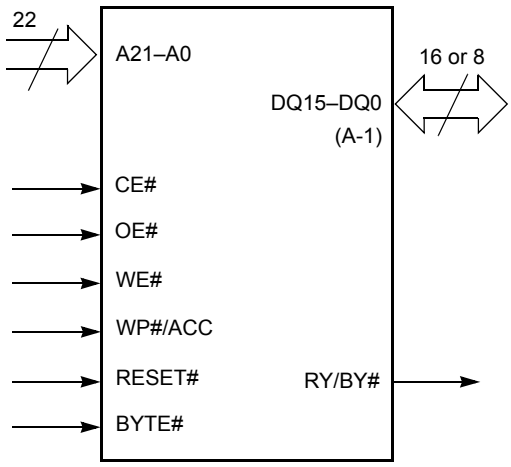
Figure 4.2 48-ball FBGA



5. Pin Description

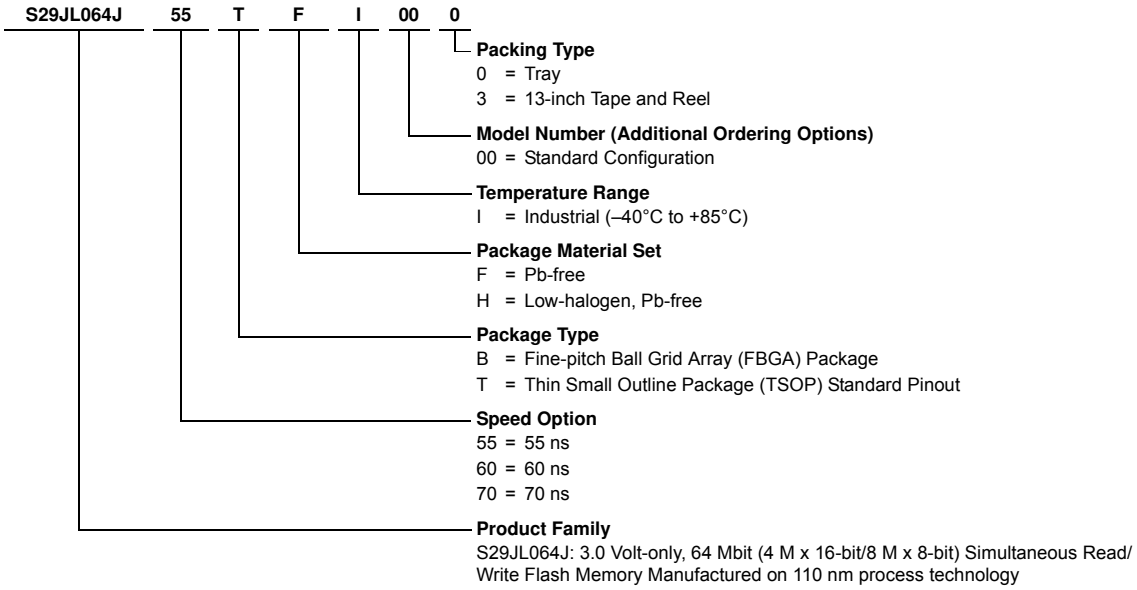
A21–A0	22 Address pins
DQ14–DQ0	15 Data Inputs/Outputs (x16-only devices)
DQ15/A-1	DQ15 (Data Input/Output, word mode), A-1 (LSB Address Input, byte mode)
CE#	Chip Enable, Active Low
OE#	Output Enable, Active Low
WE#	Write Enable, Active Low
WP#/ACC	Hardware Write Protect/Acceleration Pin
RESET#	Hardware Reset Pin, Active Low
BYTE#	Selects 8-bit or 16-bit mode, Active Low
RY/BY#	Ready/Busy Output, Active Low
V_{CC}	3.0 volt-only single power supply (see *Product Selector Guide* on page 4 for speed options and voltage supply tolerances)
V_{SS}	Device Ground
NC	Not Connected. No device internal signal is connected to the package connector nor is there any future plan to use the connector for a signal. The connection may safely be used for routing space for a signal on a Printed Circuit Board (PCB).
DNU	Do Not Use. A device internal signal may be connected to the package connector. The connection may be used by Spansion for test or other purposes and is not intended for connection to any host system signal. Any DNU signal related function will be inactive when the signal is at V_{IL}. The signal has an internal pull-down resistor and may be left unconnected in the host system or may be tied to V_{SS}. Do not use these connections for PCB signal routing channels. Do not connect any host system signal to these connections.
RFU	Reserved for Future Use. No device internal signal is currently connected to the package connector but there is potential future use for the connector for a signal. It is recommended to not use RFU connectors for PCB routing channels so that the PCB may take advantage of future enhanced features in compatible footprint devices.

6. Logic Symbol



7. Ordering Information

The order number is formed by a valid combination of the following:



S29JL064J Valid Combinations							
Device Number/ Description	**Speed (ns)**	**Package Type & Material**	**Temperature Range**	**Model Number**	**Packing Type**	**Package Description**	
S29JL064J	55, 60, 70	TF	I	00	0, 3 (1)	TS048	TSOP
		BH				VBK048	FBGA

Note:

1. Packing type 0 is standard. Specify other options as required.

8. Device Bus Operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

S29JL064J Device Bus Operations

Operation	CE#	OE#	WE#	RESET#	WP#/ ACC	Addresses (Note 1)	DQ15–DQ8		DQ7–DQ0
							BYTE# = V_{IH}	BYTE# = V_{IL}	
Read	L	L	H	H	L/H	A_{IN}	D_{OUT}	DQ14–DQ8 = High-Z, DQ15 = A-1	D_{OUT}
Write	L	H	L	H	(Note 3)	A_{IN}	D_{IN}		D_{IN}
Standby	$V_{CC} \pm 0.3V$	X	X	$V_{CC} \pm 0.3V$	L/H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L/H	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	L/H	X	High-Z	High-Z	High-Z
Sector Protect (Note 2)	L	H	L	V_{ID}	L/H	SA, A6 = L, A1 = H, A0 = L	X	X	D_{IN}
Sector Unprotect (Note 2)	L	H	L	V_{ID}	(Note 3)	SA, A6 = H, A1 = H, A0 = L	X	X	D_{IN}
Temporary Sector Unprotect	X	X	X	V_{ID}	(Note 3)	A_{IN}	D_{IN}	High-Z	D_{IN}

Legend

L = Logic Low = V_{IL}
H = Logic High = V_{IH}
V_{ID} = 11.5–12.5V
V_{HH} = 9.0 ± 0.5V
X = Don't Care
SA = Sector Address
A_{IN} = Address In
D_{IN} = Data In
D_{OUT} = Data Out

Notes:

1. *Addresses are A21:A0 in word mode (BYTE# = V_{IH}), A21:A-1 in byte mode (BYTE# = V_{IL}).*
2. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See Boot Sector/Sector Block Protection and Unprotection on page 17.*
3. *If WP#/ACC = V_{IL}, sectors 0, 1, 140, and 141 remain protected. If WP#/ACC = V_{IH}, protection on sectors 0, 1, 140, and 141 depends on whether they were last protected or unprotected using the method described in Boot Sector/Sector Block Protection and Unprotection on page 17. If WP#/ACC = V_{HH}, all sectors will be unprotected.*

8.1 Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ15–DQ0 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ7–DQ0 are active and controlled by CE# and OE#. The data I/O pins DQ14–DQ8 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

8.2 Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The BYTE# pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

Refer to *Read-Only Operations* on page 42 for timing specifications and to Figure 17.1 on page 42 for the timing diagram. I_{CC1} in *DC Characteristics* on page 38 represents the active current specification for reading array data.

8.3 Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

For program operations, the BYTE# pin determines whether the device accepts program data in bytes or words. Refer to *Word/Byte Configuration* on page 9 for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. *Byte/Word Program Command Sequence* on page 27 has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table on page 15 indicates the address space that each sector occupies. Similarly, a *sector address* is the address bits required to uniquely select a sector. *Command Definitions* on page 26 has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

The device address space is divided into four banks. A *bank address* is the address bits required to uniquely select a bank.

I_{CC2} in the *DC Characteristics* on page 38 represents the active current specification for the write mode. *AC Characteristics* on page 42 contains timing specification tables and timing diagrams for write operations.

8.3.1 Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. Note that V_{HH} must not be asserted on WP#/ACC for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result. See *Write Protect (WP#)* on page 18 for related information.

8.3.2 Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. Refer to *Autoselect Mode* on page 16 and *Autoselect Command Sequence* on page 27 for more information.

8.4 Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in another bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 17.8 on page 47 shows how read and write cycles may be initiated for simultaneous operation with zero latency. I_{CC6} and I_{CC7} in the *DC Characteristics* on page 38 represent the current specifications for read-while-program and read-while-erase, respectively.

8.5 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at V_{CC} ± 0.3V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within V_{CC} ± 0.3V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3} in *DC Characteristics* on page 38 represents the standby current specification.

8.6 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC5} in *DC Characteristics* on page 38 represents the automatic sleep mode current specification.

8.7 RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS} ±0.3V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS} ±0.3V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to *Hardware Reset (RESET#)* on page 43 for RESET# parameters and to Figure 17.2 on page 43 for the timing diagram.

8.8 Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

S29JL064J Sector Architecture (Sheet 1 of 4)

Bank	Sector	Sector Address A21–A12	Sector Size (kbytes/kwords)	(x8) Address Range	(x16) Address Range
Bank 1	SA0	0000000000	8/4	000000h–001FFFh	00000h–00FFFh
	SA1	0000000001	8/4	002000h–003FFFh	01000h–01FFFh
	SA2	0000000010	8/4	004000h–005FFFh	02000h–02FFFh
	SA3	0000000011	8/4	006000h–007FFFh	03000h–03FFFh
	SA4	0000000100	8/4	008000h–009FFFh	04000h–04FFFh
	SA5	0000000101	8/4	00A000h–00BFFFh	05000h–05FFFh
	SA6	0000000110	8/4	00C000h–00DFFFh	06000h–06FFFh
	SA7	0000000111	8/4	00E000h–00FFFFh	07000h–07FFFh
	SA8	0000001xxx	64/32	010000h–01FFFFh	08000h–0FFFFh
	SA9	0000010xxx	64/32	020000h–02FFFFh	10000h–17FFFh
	SA10	0000011xxx	64/32	030000h–03FFFFh	18000h–1FFFFh
	SA11	0000100xxx	64/32	040000h–04FFFFh	20000h–27FFFh
	SA12	0000101xxx	64/32	050000h–05FFFFh	28000h–2FFFFh
	SA13	0000110xxx	64/32	060000h–06FFFFh	30000h–37FFFh
	SA14	0000111xxx	64/32	070000h–07FFFFh	38000h–3FFFFh
	SA15	0001000xxx	64/32	080000h–08FFFFh	40000h–47FFFh
	SA16	0001001xxx	64/32	090000h–09FFFFh	48000h–4FFFFh
	SA17	0001010xxx	64/32	0A0000h–0AFFFFh	50000h–57FFFh
	SA18	0001011xxx	64/32	0B0000h–0BFFFFh	58000h–5FFFFh
	SA19	0001100xxx	64/32	0C0000h–0CFFFFh	60000h–67FFFh
	SA20	0001101xxx	64/32	0D0000h–0DFFFFh	68000h–6FFFFh
	SA21	0001110xxx	64/32	0E0000h–0EFFFFh	70000h–77FFFh
	SA22	0001111xxx	64/32	0F0000h–0FFFFFh	78000h–7FFFFh

S29JL064J Sector Architecture (Sheet 2 of 4)

Bank	Sector	Sector Address A21–A12	Sector Size (kbytes/kwords)	(x8) Address Range	(x16) Address Range
Bank 2	SA23	0010000xxx	64/32	100000h–10FFFFh	80000h–87FFFh
	SA24	0010001xxx	64/32	110000h–11FFFFh	88000h–8FFFFh
	SA25	0010010xxx	64/32	120000h–12FFFFh	90000h–97FFFh
	SA26	0010011xxx	64/32	130000h–13FFFFh	98000h–9FFFFh
	SA27	0010100xxx	64/32	140000h–14FFFFh	A0000h–A7FFFh
	SA28	0010101xxx	64/32	150000h–15FFFFh	A8000h–AFFFFh
	SA29	0010110xxx	64/32	160000h–16FFFFh	B0000h–B7FFFh
	SA30	0010111xxx	64/32	170000h–17FFFFh	B8000h–BFFFFh
	SA31	0011000xxx	64/32	180000h–18FFFFh	C0000h–C7FFFh
	SA32	0011001xxx	64/32	190000h–19FFFFh	C8000h–CFFFFh
	SA33	0011010xxx	64/32	1A0000h–1AFFFFh	D0000h–D7FFFh
	SA34	0011011xxx	64/32	1B0000h–1BFFFFh	D8000h–DFFFFh
	SA35	0011000xxx	64/32	1C0000h–1CFFFFh	E0000h–E7FFFh
	SA36	0011101xxx	64/32	1D0000h–1DFFFFh	E8000h–EFFFFh
	SA37	0011110xxx	64/32	1E0000h–1EFFFFh	F0000h–F7FFFh
	SA38	0011111xxx	64/32	1F0000h–1FFFFFh	F8000h–FFFFFh
	SA39	0100000xxx	64/32	200000h–20FFFFh	100000h–107FFFh
	SA40	0100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh
	SA41	0100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh
	SA42	0101011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh
	SA43	0100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh
	SA44	0100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh
	SA45	0100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
	SA46	0100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
	SA47	0101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh
	SA48	0101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
	SA49	0101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh
	SA50	0101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
	SA51	0101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
	SA52	0101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
	SA53	0101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
	SA54	0101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
	SA55	0110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
	SA56	0110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh
	SA57	0110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh
	SA58	0110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh
	SA59	0110100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh
	SA60	0110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
	SA61	0110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
	SA62	0110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
	SA63	0111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
	SA64	0111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
	SA65	0111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
	SA66	0111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
	SA67	0111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
	SA68	0111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh

S29JL064J Sector Architecture (Sheet 3 of 4)

Bank	Sector	Sector Address A21–A12	Sector Size (kbytes/kwords)	(x8) Address Range	(x16) Address Range
Bank 3	SA71	1000000xxx	64/32	400000h–40FFFFh	200000h–207FFFh
	SA72	1000001xxx	64/32	410000h–41FFFFh	208000h–20FFFFh
	SA73	1000010xxx	64/32	420000h–42FFFFh	210000h–217FFFh
	SA74	1000011xxx	64/32	430000h–43FFFFh	218000h–21FFFFh
	SA75	1000100xxx	64/32	440000h–44FFFFh	220000h–227FFFh
	SA76	1000101xxx	64/32	450000h–45FFFFh	228000h–22FFFFh
	SA77	1000110xxx	64/32	460000h–46FFFFh	230000h–237FFFh
	SA78	1000111xxx	64/32	470000h–47FFFFh	238000h–23FFFFh
	SA79	1001000xxx	64/32	480000h–48FFFFh	240000h–247FFFh
	SA80	1001001xxx	64/32	490000h–49FFFFh	248000h–24FFFFh
	SA81	1001010xxx	64/32	4A0000h–4AFFFFh	250000h–257FFFh
	SA82	1001011xxx	64/32	4B0000h–4BFFFFh	258000h–25FFFFh
	SA83	1001100xxx	64/32	4C0000h–4CFFFFh	260000h–267FFFh
	SA84	1001101xxx	64/32	4D0000h–4DFFFFh	268000h–26FFFFh
	SA85	1001110xxx	64/32	4E0000h–4EFFFFh	270000h–277FFFh
	SA86	1001111xxx	64/32	4F0000h–4FFFFFh	278000h–27FFFFh
	SA87	1010000xxx	64/32	500000h–50FFFFh	280000h–28FFFFh
	SA88	1010001xxx	64/32	510000h–51FFFFh	288000h–28FFFFh
	SA89	1010010xxx	64/32	520000h–52FFFFh	290000h–297FFFh
	SA90	1010011xxx	64/32	530000h–53FFFFh	298000h–29FFFFh
	SA91	1010100xxx	64/32	540000h–54FFFFh	2A0000h–2A7FFFh
	SA92	1010101xxx	64/32	550000h–55FFFFh	2A8000h–2AFFFFh
	SA93	1010110xxx	64/32	560000h–56FFFFh	2B0000h–2B7FFFh
	SA94	1010111xxx	64/32	570000h–57FFFFh	2B8000h–2BFFFFh
	SA95	1011000xxx	64/32	580000h–58FFFFh	2C0000h–2C7FFFh
	SA96	1011001xxx	64/32	590000h–59FFFFh	2C8000h–2CFFFFh
	SA97	1011010xxx	64/32	5A0000h–5AFFFFh	2D0000h–2D7FFFh
	SA98	1011011xxx	64/32	5B0000h–5BFFFFh	2D8000h–2DFFFFh
	SA99	1011100xxx	64/32	5C0000h–5CFFFFh	2E0000h–2E7FFFh
	SA100	1011101xxx	64/32	5D0000h–5DFFFFh	2E8000h–2EFFFFh
	SA101	1011110xxx	64/32	5E0000h–5EFFFFh	2F0000h–2FFFFFh
	SA102	1011111xxx	64/32	5F0000h–5FFFFFh	2F8000h–2FFFFFh
	SA103	1100000xxx	64/32	600000h–60FFFFh	300000h–307FFFh
	SA104	1100001xxx	64/32	610000h–61FFFFh	308000h–30FFFFh
	SA105	1100010xxx	64/32	620000h–62FFFFh	310000h–317FFFh
	SA106	1100011xxx	64/32	630000h–63FFFFh	318000h–31FFFFh
	SA107	1100100xxx	64/32	640000h–64FFFFh	320000h–327FFFh
	SA108	1100101xxx	64/32	650000h–65FFFFh	328000h–32FFFFh
	SA109	1100110xxx	64/32	660000h–66FFFFh	330000h–337FFFh
	SA110	1100111xxx	64/32	670000h–67FFFFh	338000h–33FFFFh
	SA111	1101000xxx	64/32	680000h–68FFFFh	340000h–347FFFh
	SA112	1101001xxx	64/32	690000h–69FFFFh	348000h–34FFFFh
	SA113	1101010xxx	64/32	6A0000h–6AFFFFh	350000h–357FFFh
	SA114	1101011xxx	64/32	6B0000h–6BFFFFh	358000h–35FFFFh
	SA115	1101100xxx	64/32	6C0000h–6CFFFFh	360000h–367FFFh
	SA116	1101101xxx	64/32	6D0000h–6DFFFFh	368000h–36FFFFh

S29JL064J Sector Architecture (Sheet 4 of 4)

Bank	Sector	Sector Address A21–A12	Sector Size (kbytes/kwords)	(x8) Address Range	(x16) Address Range
Bank 4	SA119	1110000xxx	64/32	700000h–70FFFFh	380000h–387FFFh
	SA120	1110001xxx	64/32	710000h–71FFFFh	388000h–38FFFFh
	SA121	1110010xxx	64/32	720000h–72FFFFh	390000h–397FFFh
	SA122	1110011xxx	64/32	730000h–73FFFFh	398000h–39FFFFh
	SA123	1110100xxx	64/32	740000h–74FFFFh	3A0000h–3A7FFFh
	SA124	1110101xxx	64/32	750000h–75FFFFh	3A8000h–3AFFFFh
	SA125	1110110xxx	64/32	760000h–76FFFFh	3B0000h–3B7FFFh
	SA126	1110111xxx	64/32	770000h–77FFFFh	3B8000h–3BFFFFh
	SA127	1111000xxx	64/32	780000h–78FFFFh	3C0000h–3C7FFFh
	SA128	1111001xxx	64/32	790000h–79FFFFh	3C8000h–3CFFFFh
	SA129	1111010xxx	64/32	7A0000h–7AFFFFh	3D0000h–3D7FFFh
	SA130	1111011xxx	64/32	7B0000h–7BFFFFh	3D8000h–3DFFFFh
	SA131	1111100xxx	64/32	7C0000h–7CFFFFh	3E0000h–3E7FFFh
	SA132	1111101xxx	64/32	7D0000h–7DFFFFh	3E8000h–3EFFFFh
	SA133	1111110xxx	64/32	7E0000h–7EFFFFh	3F0000h–3F7FFFh
	SA134	1111111000	8/4	7F0000h–7F1FFFh	3F8000h–3F8FFFh
	SA135	1111111001	8/4	7F2000h–7F3FFFh	3F9000h–3F9FFFh
	SA136	1111111010	8/4	7F4000h–7F5FFFh	3FA000h–3FAFFFh
	SA137	1111111011	8/4	7F6000h–7F7FFFh	3FB000h–3FBFFFh
	SA138	1111111100	8/4	7F8000h–7F9FFFh	3FC000h–3FCFFFh
	SA139	1111111101	8/4	7FA000h–7FBFFFh	3FD000h–3FDFFFh
	SA140	1111111110	8/4	7FC000h–7FDFFFh	3FE000h–3FEFFFh
	SA141	1111111111	8/4	7FE000h–7FFFFFh	3FF000h–3FFFFFh

Note:
The address range is A21:A-1 in byte mode (BYTE# = V_{IL}) or A21:A0 in word mode (BYTE# = V_{IH}).

Bank Address

Bank	A21–A19
1	000
2	001, 010, 011
3	100, 101, 110
4	111

Secured Silicon Region Addresses

Device	Sector Size	(x8) Address Range	(x16) Address Range
S29JL064J	256 bytes	000000h–0000FFh	000000h–00007Fh

8.9 Autoselect Mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins must be as shown in Table . In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see Table on page 15). Table shows the remaining address bits that are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0. However, the autoselect codes can also be accessed in-system through the command register, for instances when the S29JL064J is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table on page 31. *Note that if a Bank Address (BA) on address bits A21, A20, and A19 is asserted during the third write cycle of the autoselect command, the host system can read autoselect data from that bank and then immediately read array data from another bank, without exiting the autoselect mode.*

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in Table on page 31. This method does not require V_{ID}. Refer to *Autoselect Command Sequence* on page 27 for more information.

S29JL064J Autoselect Codes, (High Voltage Method)

Description		CE#	OE#	WE#	A21 to A12	A11 to A10	A9	A8 to A7	A6	A5 to A4	A3	A2	A1	A0	DQ15 to DQ8		DQ7 to DQ0
															BYTE# = V_{IH}	BYTE# = V_{IL}	
Manufacturer ID: Spansion Products		L	L	H	BA	X	V_{ID}	X	L	X	L	L	L	L	X	X	01h
Device ID	Read Cycle 1	L	L	H	BA	X	V_{ID}	X	L	X	L	L	L	H	22h	X	7Eh
	Read Cycle 2								L		H	H	H	L	22h		02h
	Read Cycle 3								L		H	H	H	H	22h		01h
Sector Protection Verification		L	L	H	SA	X	V_{ID}	X	L	X	L	L	H	L	X	X	01h (protected), 00h (unprotected)
Secured Silicon Indicator Bit (DQ6, DQ7)		L	L	H	BA	X	V_{ID}	X	L	X	L	L	H	H	X	X	81h (Factory Locked), 41h (Customer Locked), 01h (Not Locked)

Legend

L = Logic Low = V_{IL}
H = Logic High = V_{IH}
BA = Bank Address
SA = Sector Address
X = Don't care.

8.10 Boot Sector/Sector Block Protection and Unprotection

Note: For the following discussion, the term *sector* applies to both boot sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table).

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented via two methods.

S29JL064J Boot Sector/Sector Block Addresses for Protection/Unprotection (Sheet 1 of 2)

Sector	A21–A12	Sector/Sector Block Size
SA0	0000000000	8 kbytes
SA1	0000000001	8 kbytes
SA2	0000000010	8 kbytes
SA3	0000000011	8 kbytes
SA4	0000000100	8 kbytes
SA5	0000000101	8 kbytes
SA6	0000000110	8 kbytes
SA7	0000000111	8 kbytes
SA8–SA10	0000001XXX, 0000010XXX, 0000011XXX,	192 (3x64) kbytes
SA11–SA14	00001XXXXX	256 (4x64) kbytes
SA15–SA18	00010XXXXX	256 (4x64) kbytes
SA19–SA22	00011XXXXX	256 (4x64) kbytes
SA23–SA26	00100XXXXX	256 (4x64) kbytes
SA27-SA30	00101XXXXX	256 (4x64) kbytes
SA31-SA34	00110XXXXX	256 (4x64) kbytes
SA35-SA38	00111XXXXX	256 (4x64) kbytes
SA39-SA42	01000XXXXX	256 (4x64) kbytes
SA43-SA46	01001XXXXX	256 (4x64) kbytes
SA47-SA50	01010XXXXX	256 (4x64) kbytes
SA51-SA54	01011XXXXX	256 (4x64) kbytes
SA55–SA58	01100XXXXX	256 (4x64) kbytes
SA59–SA62	01101XXXXX	256 (4x64) kbytes
SA63–SA66	01110XXXXX	256 (4x64) kbytes
SA67–SA70	01111XXXXX	256 (4x64) kbytes
SA71–SA74	10000XXXXX	256 (4x64) kbytes
SA75–SA78	10001XXXXX	256 (4x64) kbytes
SA79–SA82	10010XXXXX	256 (4x64) kbytes
SA83–SA86	10011XXXXX	256 (4x64) kbytes
SA87–SA90	10100XXXXX	256 (4x64) kbytes
SA91–SA94	10101XXXXX	256 (4x64) kbytes
SA95–SA98	10110XXXXX	256 (4x64) kbytes
SA99–SA102	10111XXXXX	256 (4x64) kbytes
SA103–SA106	11000XXXXX	256 (4x64) kbytes
SA107–SA110	11001XXXXX	256 (4x64) kbytes
SA111–SA114	11010XXXXX	256 (4x64) kbytes
SA115–SA118	11011XXXXX	256 (4x64) kbytes
SA119–SA122	11100XXXXX	256 (4x64) kbytes
SA123–SA126	11101XXXXX	256 (4x64) kbytes

S29JL064J Boot Sector/Sector Block Addresses for Protection/Unprotection (Sheet 2 of 2)

Sector	A21–A12	Sector/Sector Block Size
SA127–SA130	11110XXXXX	256 (4x64) kbytes
SA131–SA133	1111100XXX, 1111101XXX, 1111110XXX	192 (3x64) kbytes
SA134	1111111000	8 kbytes
SA135	1111111001	8 kbytes
SA136	1111111010	8 kbytes
SA137	1111111011	8 kbytes
SA138	1111111100	8 kbytes
SA139	1111111101	8 kbytes
SA140	1111111110	8 kbytes
SA141	1111111111	8 kbytes

Sector Protect/Sector Unprotect requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 8.2 on page 20 shows the algorithms and Figure 17.13 on page 50 shows the timing diagram. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle. *Note that the sector unprotect algorithm unprotects all sectors in parallel. All previously protected sectors must be individually re-protected.* To change data in protected sectors efficiently, the temporary sector unprotect function is available. See *Temporary Sector Unprotect* on page 19.

The device is shipped with all sectors unprotected. Optional Spansion programming service enable programming and protecting sectors at the factory prior to shipping the device. Contact your local sales office for details.

It is possible to determine whether a sector is protected or unprotected. See *Autoselect Mode* on page 16 for details.

8.11 Write Protect (WP#)

The Write Protect function provides a hardware method of protecting without using V_{ID}. This function is one of two provided by the WP#/ACC pin.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in sectors 0, 1, 140, and 141, independently of whether those sectors were protected or unprotected using the method described in *Boot Sector/Sector Block Protection and Unprotection* on page 17.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether sectors 0, 1, 140, and 141 were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected using the method described in *Boot Sector/Sector Block Protection and Unprotection* on page 17.

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

WP#/ACC Modes

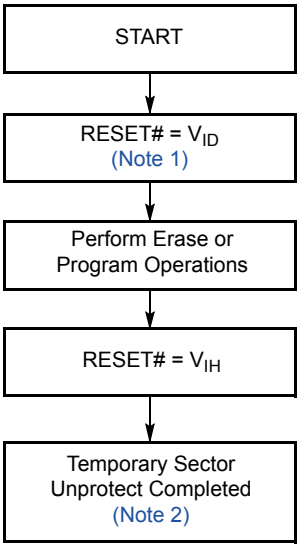
WP# Input Voltage	Device Mode
V_{IL}	Disables programming and erasing in SA0, SA1, SA140, and SA141
V_{IH}	Enables programming and erasing in SA0, SA1, SA140, and SA141, dependent on whether they were last protected or unprotected.
V_{HH}	Enables accelerated programming (ACC). See *Accelerated Program Operation* on page 10.

8.12 Temporary Sector Unprotect

Note: For the following discussion, the term *sector* applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table on page 17).

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Temporary Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 8.1 shows the algorithm, and Figure 17.12 on page 49 shows the timing diagrams, for this feature. If the WP#/ACC pin is at V_{IL}, sectors 0, 1, 140, and 141 will remain protected during the Temporary sector Unprotect mode.

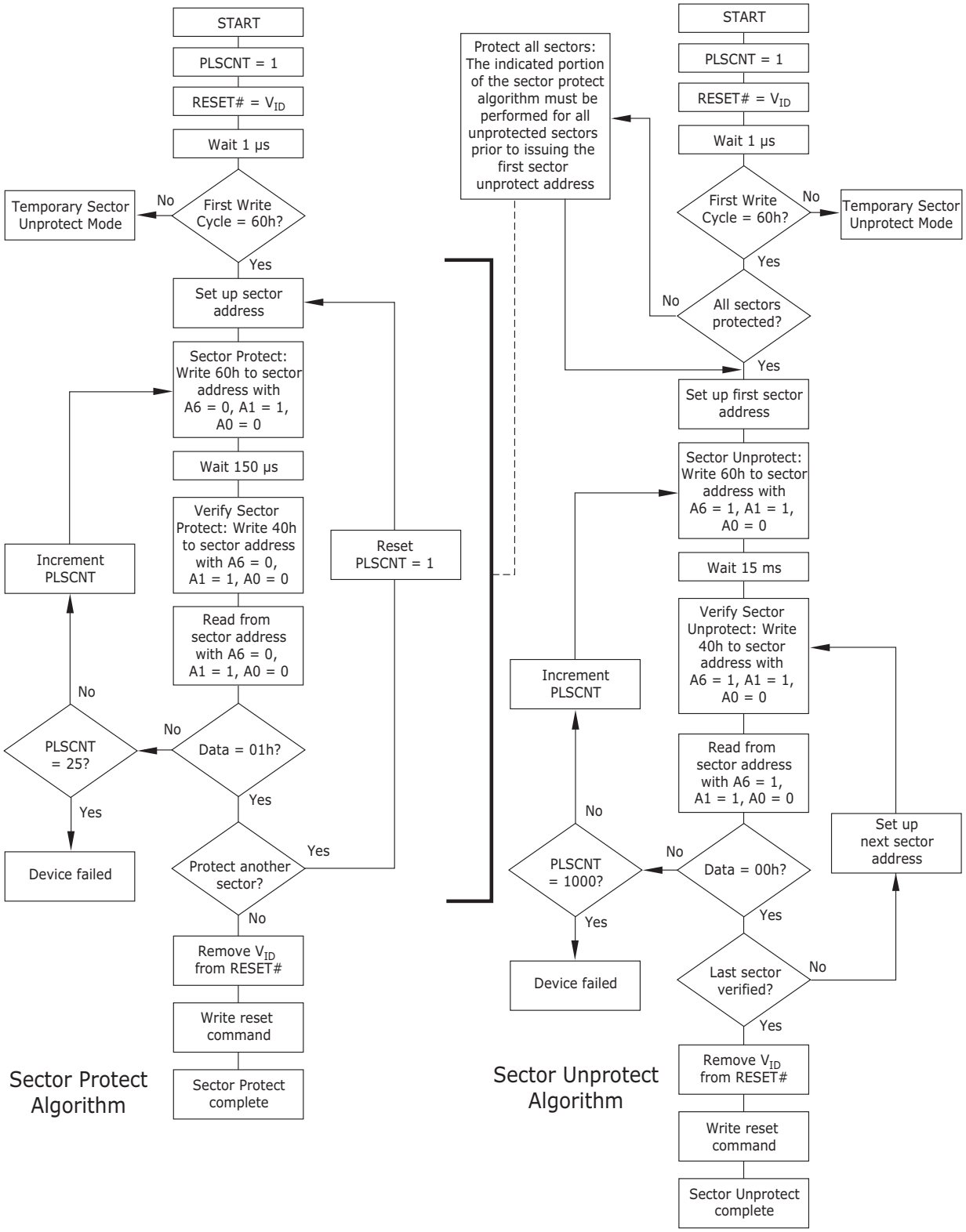
Figure 8.1 Temporary Sector Unprotect Operation



Notes:

1. *All protected sectors unprotected (If WP#/ACC = V_{IL}, sectors 0, 1, 140, and 141 will remain protected).*
2. *All previously protected sectors are protected once again.*

Figure 8.2 In-System Sector Protect/Unprotect Algorithms



8.13 Secured Silicon Region

The Secured Silicon Region feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Region is 256 bytes in length, and may shipped unprotected, allowing customers to utilize that sector in any manner they choose, or may shipped locked at the factory (upon customer request). The Secured Silicon Indicator Bit data will be 81h if factory locked, 41h if customer locked, or 01h if neither. Refer to Table on page 16 for more details.

The system accesses the Secured Silicon Region through a command sequence (see *Enter Secured Silicon Region/Exit Secured Silicon Region Command Sequence* on page 27). After the system has written the Enter Secured Silicon Region command sequence, it may read the Secured Silicon Region by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit Secured Silicon Region command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to the first 256 bytes of Sector 0. *Note that the ACC function and unlock bypass modes are not available when the Secured Silicon Region is enabled.*

8.13.1 Factory Locked: Secured Silicon Region Programmed and Protected At the Factory

In a factory locked device, the Secured Silicon Region is protected when the device is shipped from the factory. The Secured Silicon Region cannot be modified in any way. The device is preprogrammed with both a random number and a secure ESN. The 8-word random number is at addresses 000000h–000007h in word mode (or 000000h–00000Fh in byte mode). The secure ESN is programmed in the next 8 words at addresses 000008h–00000Fh (or 000010h–00001Fh in byte mode). The device is available preprogrammed with one of the following:

- A random, secure ESN only
- Customer code through Spansion programming services
- Both a random, secure ESN and customer code through Spansion programming services

Contact an your local sales office for details on using Spansion programming services.

8.13.2 Customer Lockable: Secured Silicon Region NOT Programmed or Protected At the Factory

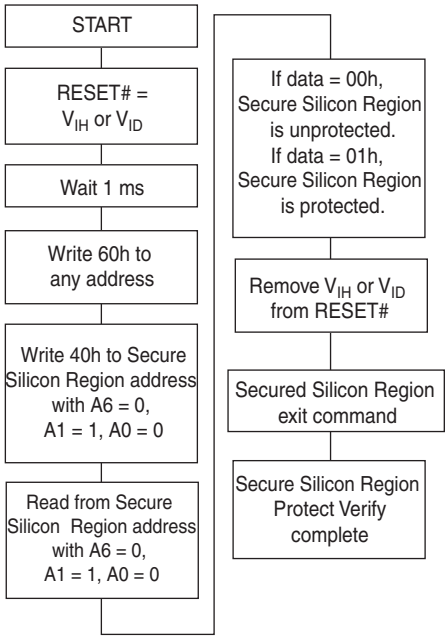
If the security feature is not required, the Secured Silicon Region can be treated as an additional Flash memory space. The Secured Silicon Region can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the Secured Silicon Region.

- Write the three-cycle Enter Secured Silicon Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 8.2 on page 20, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the Secured Silicon Region without raising any device pin to a high voltage. Note that this method is only applicable to the Secured Silicon Region.
- To verify the protect/unprotect status of the Secured Silicon Region, follow the algorithm shown in Figure 8.3 on page 22.

Once the Secured Silicon Region is locked and verified, the system must write the Exit Secured Silicon Region command sequence to return to reading and writing the remainder of the array.

The Secured Silicon Region lock must be used with caution since, once locked, there is no procedure available for unlocking the Secured Silicon Region and none of the bits in the Secured Silicon Region memory space can be modified in any way.

Figure 8.3 Secured Silicon Region Protect Verify



8.14 Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table on page 31 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

8.14.1 Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

8.14.2 Write Pulse Glitch Protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

8.14.3 Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

8.14.4 Power-Up Write Inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

9. Common Flash Memory Interface (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Table on page 23 to Table on page 25. To terminate reading CFI data, the system must write the reset command.The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode via the command register only (high voltage method does not apply). The device enters the CFI query mode, and the system can read CFI data at the addresses given in Table on page 23 to Table on page 25. The system must write the reset command to return to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100. Contact your local sales office for copies of these documents.

CFI Query Identification String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

System Interface String

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0003h	Typical timeout per single byte/word write 2^N µs
20h	40h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	0009h	Typical timeout per individual block erase 2^N ms
22h	44h	000Fh	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0004h	Max. timeout for byte/word write 2^N times typical
24h	48h	0000h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Device Geometry Definition

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
27h	4Eh	0017h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (refer to the CFI publication 100)
2Ah 2Bh	54h 56h	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	62h 64h 66h 68h	007Dh 0000h 0000h 0001h	Erase Block Region 2 Information (refer to the CFI specification or CFI publication 100)
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0007h 0000h 0020h 0000h	Erase Block Region 3 Information (refer to the CFI specification or CFI publication 100)
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to the CFI specification or CFI publication 100)

Primary Vendor-Specific Extended Query

Addresses (Word Mode)	Addresses (Byte Mode)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII (reflects modifications to the silicon)
44h	88h	0033h	Minor version number, ASCII (reflects modifications to the CFI table)
45h	8Ah	000Ch	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Process Technology (Bits 7-2) 0011 = 0.11 µm Floating Gate
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0004h	Sector Protect/Unprotect scheme 01 =29F040 mode, 02 = 29F016 mode, 03 = 29F400, 04 = 29LV800 mode
4Ah	94h	0077h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors (excluding Bank 1)
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	0085h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	0095h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	0001h	Top/Bottom Boot Sector Flag 00h = Uniform device, 01h = 8 x 8 kbyte Sectors, Top And Bottom Boot with Write Protect, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h= Both Top and Bottom
50h	A0h	0000h	Program Suspend 0 = Not supported, 1 = Supported
57h	AEh	0004h	Bank Organization 00 = Data at 4Ah is zero, X = Number of Banks
58h	B0h	0017h	Bank 1 Region Information X = Number of Sectors in Bank 1
59h	B2h	0030h	Bank 2 Region Information X = Number of Sectors in Bank 2